



**DEFENSE LOGISTICS AGENCY**  
DEFENSE SUPPLY CENTER, COLUMBUS  
POST OFFICE BOX 3990  
COLUMBUS, OH 43218-3990

IN REPLY  
REFER TO

DSCC-VAC (Mr. Barone/DSN 850-0510/(614) 692-0510)

July 21, 2004

MEMORANDUM FOR VSS (Mr. Bill Heckman)

SUBJECT: Dated Engineering Practices (EP) Study to Address: (Problems In The Standardization Of Current And Power Ratings, Derating, And Maximum Operating Temperature); Project Number: 5961- 2675

Findings and recommendations Engineering Practices (EP) Study, dated 23 July 2004, and attachments are enclosed.

It is requested that your office take the necessary electronic action to reflect completion of this project.

/signed/  
THOMAS M. HESS  
Chief  
Active Devices Team

Encl 1



**ENGINEERING PRACTICES STUDY**

**TITLE: Problems In The Standardization Of Current And Power Ratings, Derating,  
And Maximum Operating Temperature**

**23 July 2004**

**STUDY PROJECT 5961-2675**

**FINAL REPORT**

**Prepared by**

**Alan Barone**

- I. **OBJECTIVE:** The objective of this project was to create guidance on how to develop accurate and consistent power ratings, current ratings, maximum operating temperature ratings and a device derating formula.
- II. **BACKGROUND:** This study applies to all silicon semiconductor diodes, rectifiers and transistors and involves the cooperation of vendors with engineering support.

While the technology ratings are related we have found one or more of these ratings to lack correlation. Significant debate over these ratings has occurred and is on-going. Our reference parameters are measured and from these measurements we derive power, current, and derating. Thermal resistance, junction temperature and leakage current are to be measured.

Some assumptions and poor characterization practices have resulted in a gray area as to what the real capabilities of these devices are. For example, some rectifiers while having half the thermal resistance have the same current ratings. This is done by starting the derating at elevated temperatures like 55°C and even 110°C rather than at 25°C. What concerns the Government space community most about this practice is that the derating slope changes affect their failures-in-time (FIT) calculations. The power and current ratings appear to be significantly underrated by starting the derating at evaluated temperatures. One vendor explained that limitations such as wire bond might explain the flat portion of the derating curve but it seems that the whole system is not clear. Burn-ins done in accordance with power and current rating are flawed. A minimum junction temperature must be specified when the power and current ratings are not developed using the same conditions and techniques.

$T_{OP}$  and  $T_{STG}$  ratings are not specified consistently particularly when evaluating lead finish limitations.  $T_{OP}$  and  $T_{STG}$  ratings for silicon devices should all be treated the same except for barrier (Schottky, etc) and altered junction devices (altered refers to special processing like gold doping, etc.). For example, one document calls  $T_{OP(max)}$  the maximum junction temperature while another refers to it as the maximum ambient temperature.

### Temperature Limits of Semiconductors

All semiconductor devices have temperature limits and those limits are:

- 1)  $T_J(max)$ : The highest temperature the junction is allowed to reach (°C).
- 2)  $T_C(max)$ : The highest temperature the case can reach (°C).
- 3)  $T_L(max)$ : The highest temperature the lead can reach for axial parts (°C).

All semiconductor devices have power dissipation limits and those limits are determined by thermal resistance and are:

- 1)  $\theta_{JC}(\text{max})$ : Maximum thermal resistance junction-to-case ( $^{\circ}\text{C}/\text{W}$ ).
- 2)  $\theta_{JL}(\text{max})$ : Maximum axial thermal resistance junction-to-lead ( $^{\circ}\text{C}/\text{W}$ ).
- 3)  $\theta_{JX}(\text{max})$ : Maximum apparent thermal impedance as a function of time ( $^{\circ}\text{C}/\text{W}$ ).

$T_J(\text{max})$  for normal silicon PN junctions is based on years of experience and tradition. Values higher or lower result in specific technology-dependant variations. For instance, gold and platinum doped products have  $T_J(\text{max})$  of  $175^{\circ}\text{C}$  or  $150^{\circ}\text{C}$  depending on whether the lifetime is 150ns or 15ns. Schottky barrier devices have  $T_J(\text{max})$  dictated by the barrier metal chosen and the barrier reverse leakage. Schottky devices will have of  $T_J(\text{max})$  range from  $150^{\circ}\text{C}$  to  $175^{\circ}\text{C}$  with exceptions running from  $125^{\circ}\text{C}$  to  $200^{\circ}\text{C}$ .

$T_C(\text{max})$  or  $T_L(\text{max})$  must never be higher than  $T_J(\text{max})$  and is limited by package construction and terminal/lead finish. Where Pb63Sn solder dipped terminals and leads are concerned (very common), the solidus point of  $183^{\circ}\text{C}$  for PbSn solders becomes the limiting factor. Since we must be safely below the solidus, that makes  $T_C(\text{max})$  or  $T_L(\text{max})$   $175^{\circ}\text{C}$  for short exposures (temperature cycle) and  $150^{\circ}\text{C}$  for storage conditions.

It is entirely possible that a  $T_J(\text{max})$  of  $200^{\circ}\text{C}$  is possible due to the silicon technology, but the  $T_C(\text{max})$  of  $150^{\circ}\text{C}$  is indicated by lead finish limitations. If the  $\theta_{JC}(\text{max})$  thermal resistance is low enough, the  $T_J(\text{max})$  of  $200^{\circ}\text{C}$  can never be achieved without exceeding  $T_C(\text{max})$ . The slash sheet specification could still specify  $T_J(\text{max})$  of  $200^{\circ}\text{C}$  but that would only be reachable under pulse conditions and can never be used as a burn-in specification.

All semiconductor devices employ power derating curves which are derived from the above considerations. These derating curves do not need to all look the same because the limitations of thermal resistance, lead finish temperature, current and power density plus specific issues such as gold doping or metal barrier construction will all be combined together to produce the derating curve. However, the derating curve should reflect actual physical properties and not out-dated curves from long-since obsolete technologies.

Appropriate limits for  $T_J$ ,  $T_C$ ,  $T_L$  can and should be derived for each product series much as the  $\theta_{JC}$ ,  $\theta_{JL}$  and  $\theta_{JX}$  limits have already be reviewed and updated or are in the process of being updated. There are specific engineering rules that can easily be followed but there are no clear-cut "clerical" rules that can be imposed (always this temperature, always that way).

III. RESULTS: DSCC needed resolution to the following questions:

- a. Should Max  $T_J$  (junction temperature) be specified at 200°C for all silicon devices except barrier and altered junction devices?
- b. Should Max  $T_{STG}$  be specified as an ambient condition only and reflect all package limitations including lead finish? For example, lead-tin solder melts at 183°C and should never be exposed to temperatures above 175°C (150°C to avoid discoloring the finish).
- c. Should Max  $T_{OP}$  be specified as max temperature achieved by device power only and reflect all package limitations including lead finish? In this definition,  $T_{OP}$  takes on the definition as the external operation temperature of the semiconductor device (ambient, case or lead temperature).
- d. Should all silicon devices except barrier and altered junction devices be derated from  $T_A/T_{OP} = X^\circ\text{C}$  (a reference temperature to be determined, normally 25°C) to the maximum  $T_{OP}$  consistent with a maximum junction of 200°C?
- e. Should lead finish impact the current or power rating of any device?

Max  $T_J$  (junction temperature) is expected be specified at 200°C for all silicon devices except barrier and altered junction devices.  $T_J$  is replacing  $T_{OP}$  on all specifications and lead finish is not part of the device rating and will not be used to derate a device. Normally derating would start at 25°C, however, package or die limitations may require this reference temperature to start at some high temperature. When this occurs applicable notes will be added to the specification.

Industry has developed a math model for ratings correlation. DSCC intends to use this program to check the accuracy of specification ratings.

At the September JEDEC meeting, Industry and Government representatives met and focused on transient thermal impedance curves, conformance inspection, ratings, derating and maximum operating temperatures. Mr. Ray Dibugnara gave a technical presentation on his program, which illustrated the appropriate ratings correlation when inputting the applicable measured parameters. This program is available to anyone who wishes to use it. Copies may be obtain from Ray Dibugnara at [rdibugnara@microsemi.com](mailto:rdibugnara@microsemi.com).

- IV. CONCLUSION: Some corrective actions involving power ratings, thermal resistance and junction temperature have occurred. However, debate and confusion on the reference temperature for derating is an on-going issue. The power-derating program for transistors has been completed and has had several modifications. More modifications may occur as this program evolves. This program will generate the applicable power and temperature ratings. A family of curves as well as the thermal runaway temperature will be generated and specified on all specifications. A current derating program for diodes is also complete, however, this program cannot generate applicable current or temperature, it simply plots the historical ratings we provide. DSCC and the industry must study each technology to determine if the present ratings make sense.
- V. RECOMMENDATIONS: DSCC recommends incorporating the ongoing results into our military specifications. DSCC recommend that we continue to coordinate rating issues with JC-13.1, G-12, JC-22 and JC-25.

# Thermal Ratings

Reconciling Device SOA/Deratings  
from...

Electrical Specification Ratings

by

Ray DiBugnara, Microsemi

JC-13/G-12 September 9-12, 2002

# Issues That Have Been Raised

- 1) Why don't all silicon semiconductors have the same maximum temperature ( 200C)?
- 2) Are all the slash sheet temperature and power ratings realistic?
- 3) Do maximum ratings apply to DC, Squarewave or to Sinewave operation?
- 4) Is there any way to reconcile derating curves with the maximum ratings tables?

In order to assist DSCC with these issues, a simple model was devised to help make some of these discernments. This model, “Thermal Ratings”, will be distributed to anyone requesting a copy. Just email full contact information to [rdibugnara@microsemi.com](mailto:rdibugnara@microsemi.com) and a copy will be emailed shortly. This presentation will be distributed by as part of the JC-13 minutes.

Thermal Ratings allows the user to keyin maximum ratings from a slash sheet (or any specification for that matter), keyin a few key parameters, and then derive a operating temperature derating curve which is also a Safe Operating Area (SOA) curve.

## Answers So Far (To Above Issues)

- 1) Some are gold doped (altered junction) and some are Schottky (barrier device)
- 2) This is left to the user. So far the ones I checked seem to be satisfactory.
- 3) HTRB specifies waveform but apparently maximum ratings do not. What to do?
- 4) The “Thermal Ratings” model does a reasonable job but interpretation may be needed.

# Maximum Operating Temperature Calculator

Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision K

## Input

Title (Appears in the Plots) = Analysis of JAN2N2222A (/255)

Thermal Resistance = 325 °C/W

Rate Ir Doubles = 10.50 °C to Double

Hot Ir = 0.01 mA

Hot Vr = 60 V

Waveform = 1 1=DC, 2=Squarewave 50% D/C

Hot Temp = 150.0 °C

Maximum Rating (Numeric value) = 500 mA, A, mW, W or %

Units for Maximum Rating (Text value) = mW mA, A, mW, W or %

Temp for the Maximum Rating = 37.5 °C

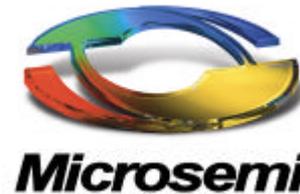
Silicon Runaway Temp = 275.0 °C

Maximum Lead/Case Finish Temp = 180.0 °C

Maximum Internal Package Temp = 300.0 °C

Maximum Die Metalization or Bond Temp = 456.0 °C

Temperature Guardband (0=None) = 5.0 °C



## Results

Ideal Maximum "Sink" Temp = 196.0 °C (Package limitations may lower this)

**Maximum Junction Temp [Top(max)] = 202.1 °C (DC Operation)**

**Maximum Sink Temp [Tsink(max)] = 175.0 °C (DC Operation)**

This is the main input/output interface for the model. You will find that there is a pop-up window for each element to guide you through the operation of the model.

Solver

## Use to Calculate the "Rate Ir Doubles"

This calculator allows one to determine the Ir doubling rate when it has not been previously supplied. You need 2 Ir readings at 2 temperatures (stay above 100C to avoid surface effect errors).

Temp 1 =  °C  
Ir 1 =  mA

Temp 2 =  °C  
Ir 2 =  mA

Input  
Values

Rate Ir Doubles =  °C to Double

Results

## Use to Project Ir at a New Temperature

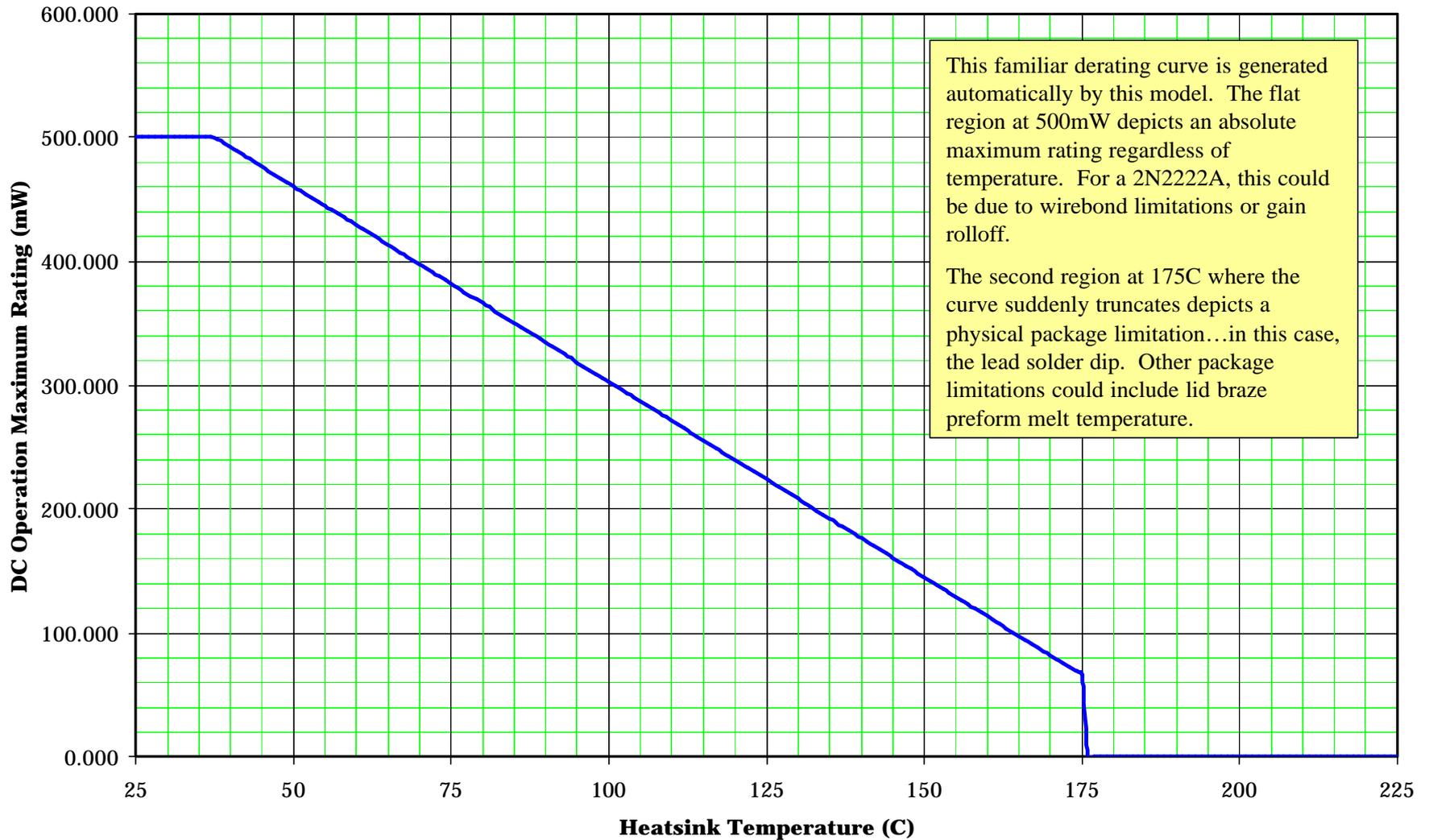
Temp =  °C  
Ir =  mA

Project  
Values

Calculator

## Safe Operating Derating Curve (Safe = Below the Curve)

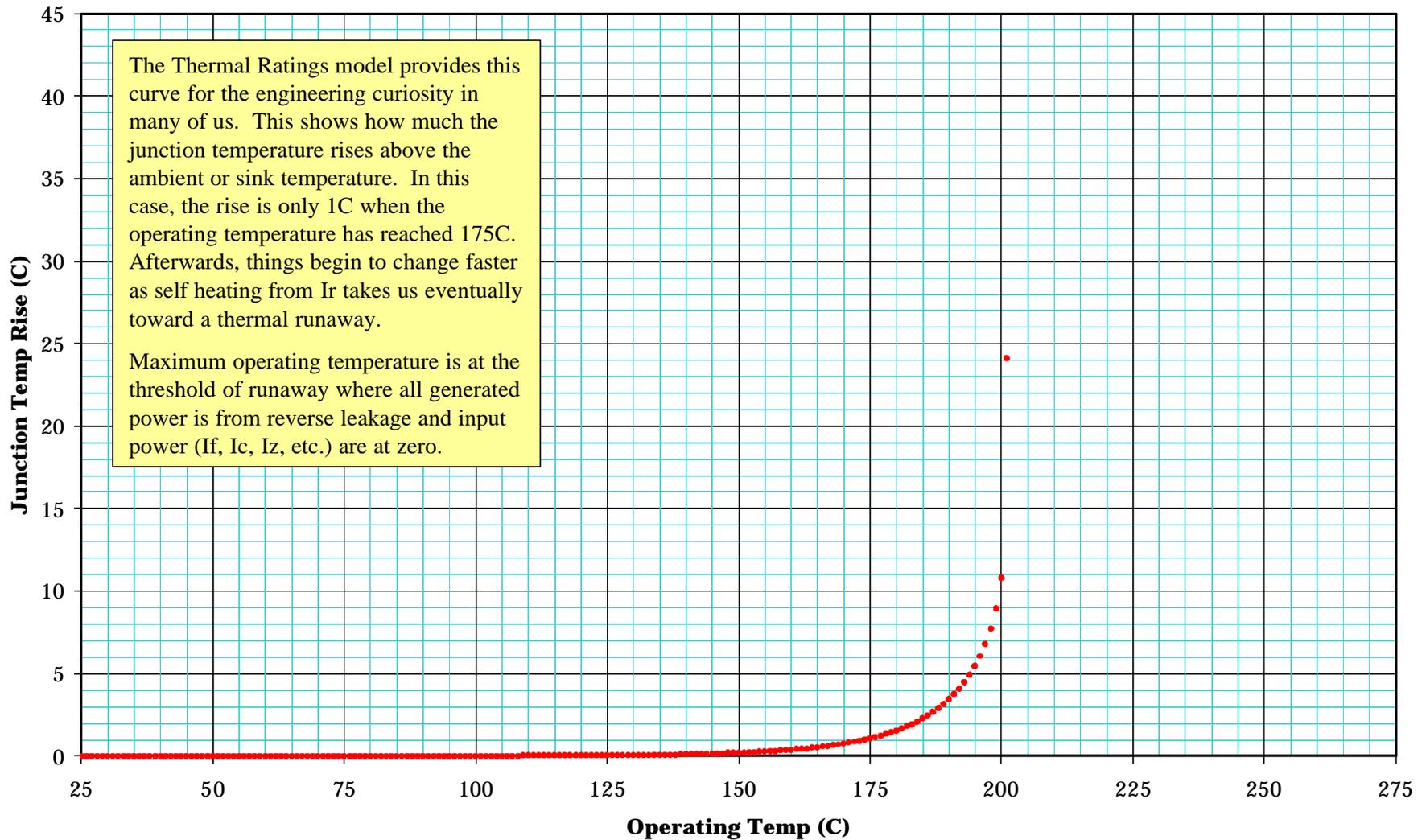
Analysis of JAN2N2222A (/255)



Derating

# Junction Temperature Rise Above Operating Temp Due to Ir Self-Heating

Analysis of JAN2N2222A (/255)



Tj Plot

# Thermal Ratings Model Introduction and Help

## NOTE:

Please save a copy of this model before you begin to use it just in case you accidentally damage it by an inadvertant deletion or the overwrite of some of the calculation cells.

## INTRODUCTION:

All semiconductor devices have temperature limits and those limits are:

- 1)  $T_j(\text{max})$ : The highest temperature the junction is allowed to reach ( $^{\circ}\text{C}$ ).
- 2)  $T_c(\text{max})$ : The highest temperature the case can reach ( $^{\circ}\text{C}$ ).
- 3)  $T_l(\text{max})$ : The highest temperature the lead can reach at a specified distance from the body ( $^{\circ}\text{C}$ ).
- 4)  $T_{ec}(\text{max})$ : The highest temperature the endcap can reach for surface mount parts ( $^{\circ}\text{C}$ ).
- 5)  $T_{op}(\text{max})$ : The maximum junction operating temperature ( $^{\circ}\text{C}$ ) which in the past has typically been  $T_j(\text{max})$ .

All semiconductor devices have power dissipation limits and those limits are determined by thermal resistance and are:

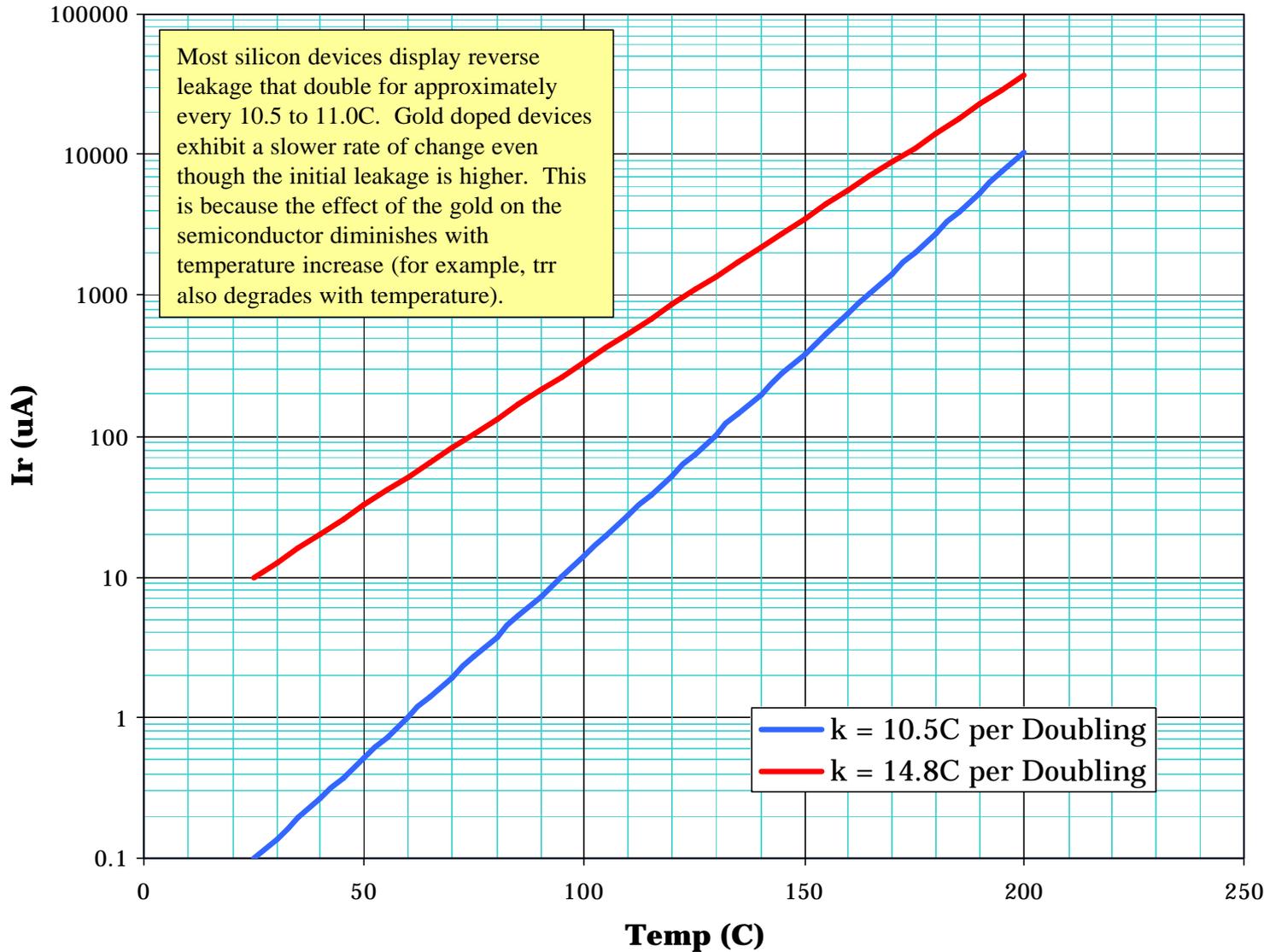
- 6)  $\theta_{jc}(\text{max})$ : Maximum thermal resistance junction-to-case ( $^{\circ}\text{C}/\text{W}$ ) or ...
- 7)  $\theta_{jl}(\text{max})$ : Maximum axial thermal resistance junction-to-lead ( $^{\circ}\text{C}/\text{W}$ ).
- 8)  $\theta_{jecd}(\text{max})$ : Maximum surface mount thermal resistance junction-to-endcap ( $^{\circ}\text{C}/\text{W}$ ).

$T_j(\text{max})$  for normal silicon PN junctions ( $^{\circ}\text{C}$ ) is based on years of experience and tradition. Values higher or lower result in specific technology-dependant variations. For instance, gold and platinum doped product have  $T_j(\text{max})$  of  $150^{\circ}\text{C}$  to  $200^{\circ}\text{C}$  depending on the switching speed. Schottky barrier devices have  $T_j(\text{max})$  dictated by the barrier metal chosen and the barrier reverse leakage. Schottky devices will have of  $T_j(\text{max})$  range from  $150^{\circ}\text{C}$  to  $175^{\circ}\text{C}$  with exceptions running from  $125^{\circ}\text{C}$  to  $200^{\circ}\text{C}$ .

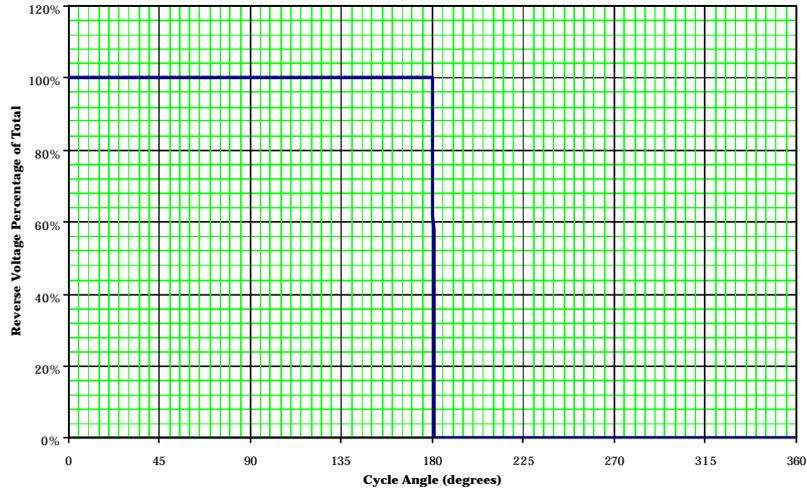
$T_c(\text{max})$ ,  $T_l(\text{max})$  or  $T_{ec}(\text{max})$  must never be higher than  $T_j(\text{max})$  and is limited by package construction and terminal/lead finish. Where Pb63Sn solder dipped terminals and leads are concerned (very common), the solidus point of  $183^{\circ}\text{C}$  for PbSn solders becomes the limiting factor. Since we must be safely below the solidus, that makes  $T_c(\text{max})$ ,  $T_l(\text{max})$  or  $T_{ec}(\text{max})$   $175^{\circ}\text{C}$  for short exposures (temperature cycle) and  $150^{\circ}\text{C}$  for longer storage and operating conditions.

Etc, etc.....

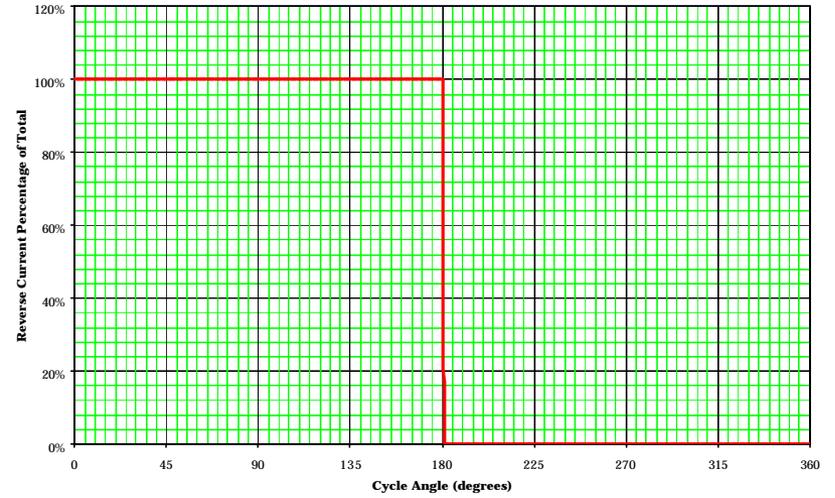
# Ir vs Temp vs Doubling Factor



### Squarewave Voltage Bias Waveform

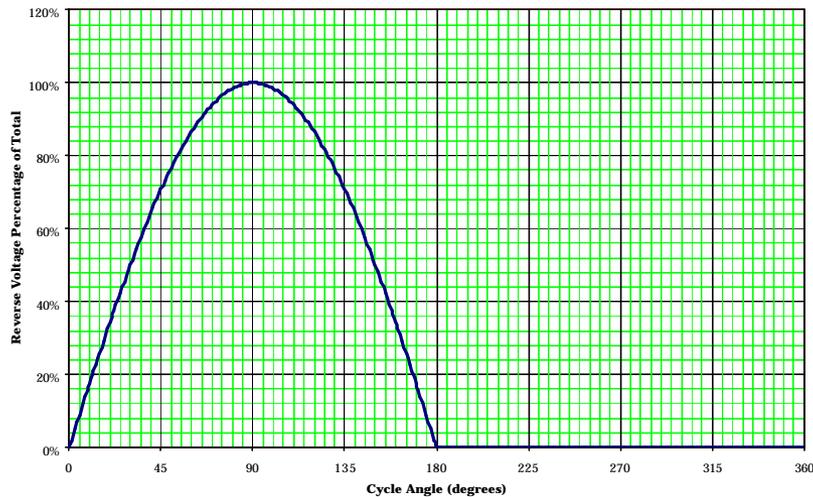


### Squarewave Reverse Current Waveform

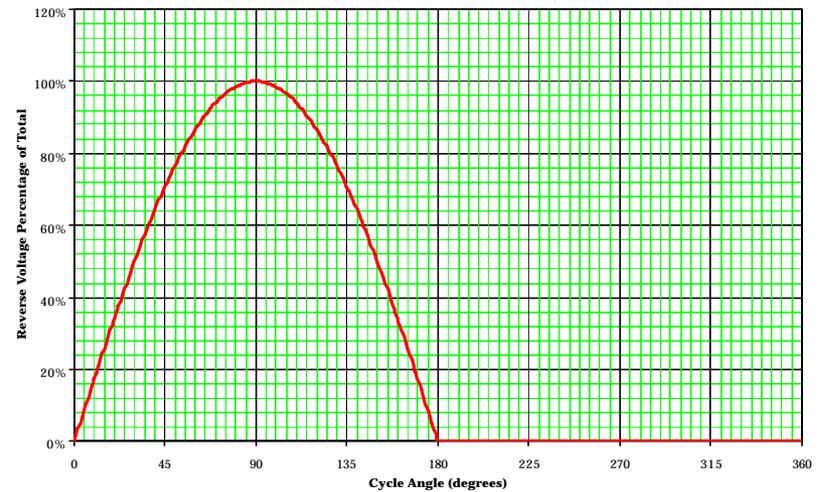


For DC operation, reverse power is easy to calculate, namely  $V_r \times I_r$ . For squarewave operation it becomes  $V_f \times I_r \times \text{Duty Cycle}$ . However, for sinewave operation, things are trickier. If the load were purely resistive, power would be peak values of  $V_f \times I_r \times 0.318$  assuming 50% Duty Cycle. However, you are not likely to encounter a semiconductor with a purely resistive load property.

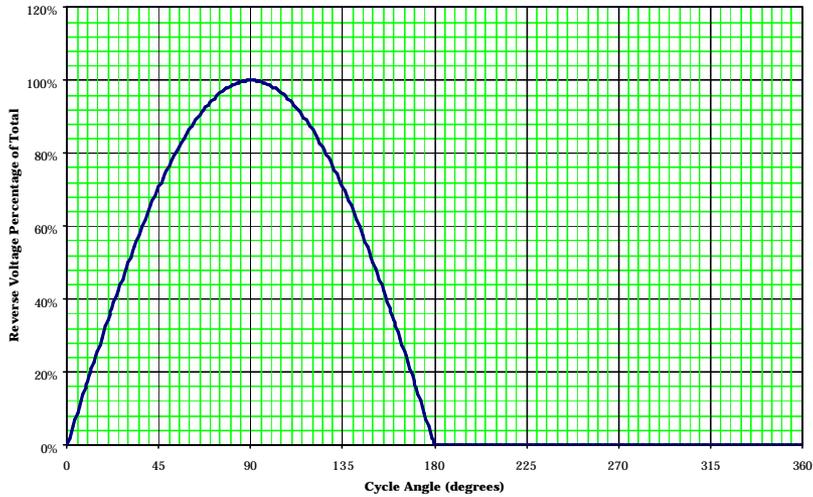
### Half-Sine Voltage Bias Waveform



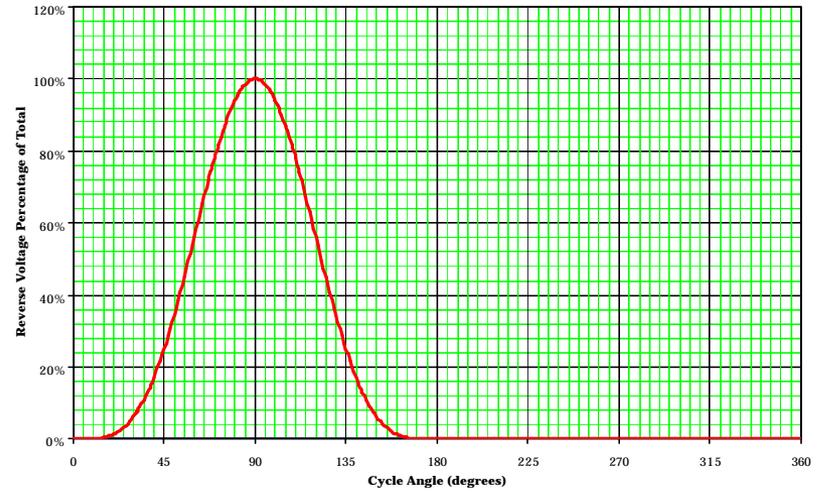
### Half-Sine Reverse Current - Resistive Load



**Half-Sine Voltage Bias Waveform**

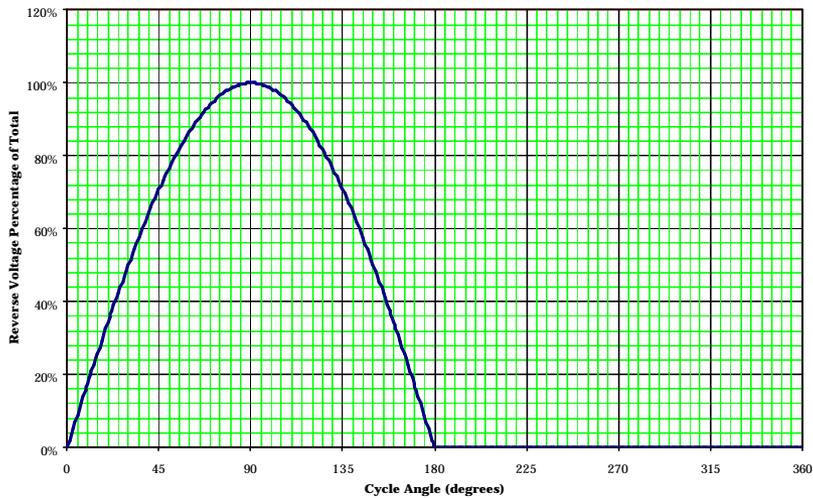


**Half-Sine Reverse Current - Schottky Rectifier**

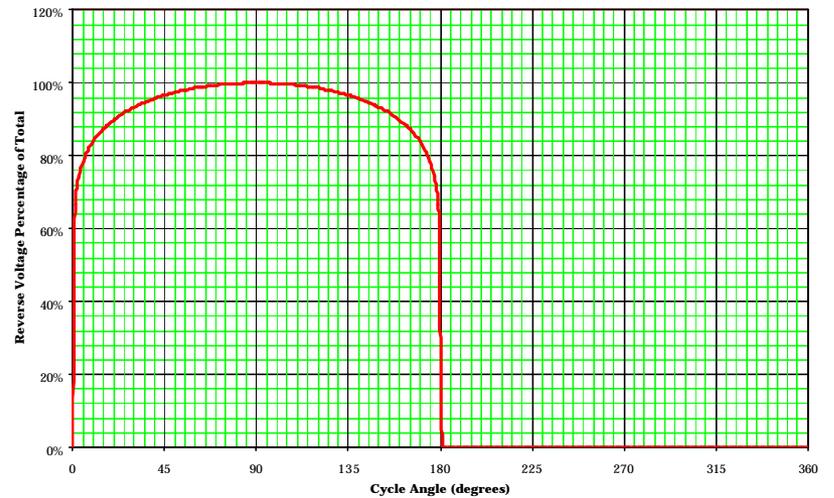


AC operation reverse power predictions are thwarted by the fact that different types of semiconductors have different responses for  $I_r$  when  $V_r$  varies. For Schottkys, the  $I_r$  increases significantly with  $V_r$  so the  $I_r$  curve does not resemble a sinewave. For this reason, Schottkys benefit immensely from AC operation over squarewave. Bipolar transistors are nearly constant current with variations in  $V_r$  so reverse power is somewhere in between.

**Half-Sine Voltage Bias Waveform**



**Half-Sine Reverse Current - Bipolar Transistor**



# Maximum Operating Temperature Calculator

Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision K

## Input

Title (Appears in the Plots) = JAN1N5811, Lead=3/8" (/477)

Thermal Resistance = 22 °C/W

Rate Ir Doubles = 14.81 °C to Double

## 1N5811 - SQUARE

Most likely these high performance rectifiers will operating under squarewave conditions though duty cycle may vary from the 50% figure used here.

Hot Ir = 0.15 mA

Hot Vr = 150 V

Waveform = 2 1=DC, 2=Squarewave 50% D/C

Hot Temp = 100.0 °C

Maximum Rating (Numeric value) = 6 mA, A, mW, W or %

Units for Maximum Rating (Text value) = A mA, A, mW, W or %

Temp for the Maximum Rating = 75.0 °C

Silicon Runaway Temp = 275.0 °C

Maximum Lead/Case Finish Temp = 175.0 °C

Maximum Internal Package Temp = 400.0 °C

Maximum Die Metalization or Bond Temp = 790.0 °C

Temperature Guardband (0=None) = 5.0 °C



## Results

Ideal Maximum "Sink" Temp = 169.0 °C

**Maximum Junction Temp [Top(max)] = 179.0 °C (Squarewave Operation)**

**Maximum Sink Temp [Tsink(max)] = 169.0 °C (Squarewave Operation)**

# Maximum Operating Temperature Calculator

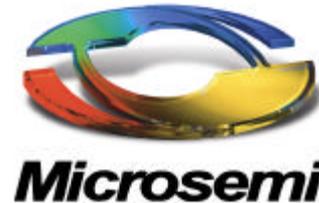
Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision L-Engineering

## Input

**1N5811 - SINE**

Sinewave operation is the easiest condition for gold doped rectifiers and Schottky rectifiers. It permits reaching higher temperatures than with DC or squarewave operation.

Title (Appears in the Plots) =	JAN1N5811, Lead=3/8" (/477)
Thermal Resistance =	22 °C/W
Rate Ir Doubles =	14.81 °C to Double
Hot Ir =	0.15 mA
Hot Vr =	150 V
Waveform =	3 1=DC, 2=Squarewave, 3=Sine
Hot Temp =	100.0 °C
Maximum Rating (Numeric value) =	6 mA, A, mW, W or %
Units for Maximum Rating (Text value) =	A mA, A, mW, W or %
Temp for the Maximum Rating =	75.0 °C
Silicon Runaway Temp =	275.0 °C
Maximum Lead/Case Finish Temp =	180.0 °C
Maximum Internal Package Temp =	400.0 °C
Maximum Die Metalization or Bond Temp =	790.0 °C
Temperature Guardband (0=None) =	5.0 °C



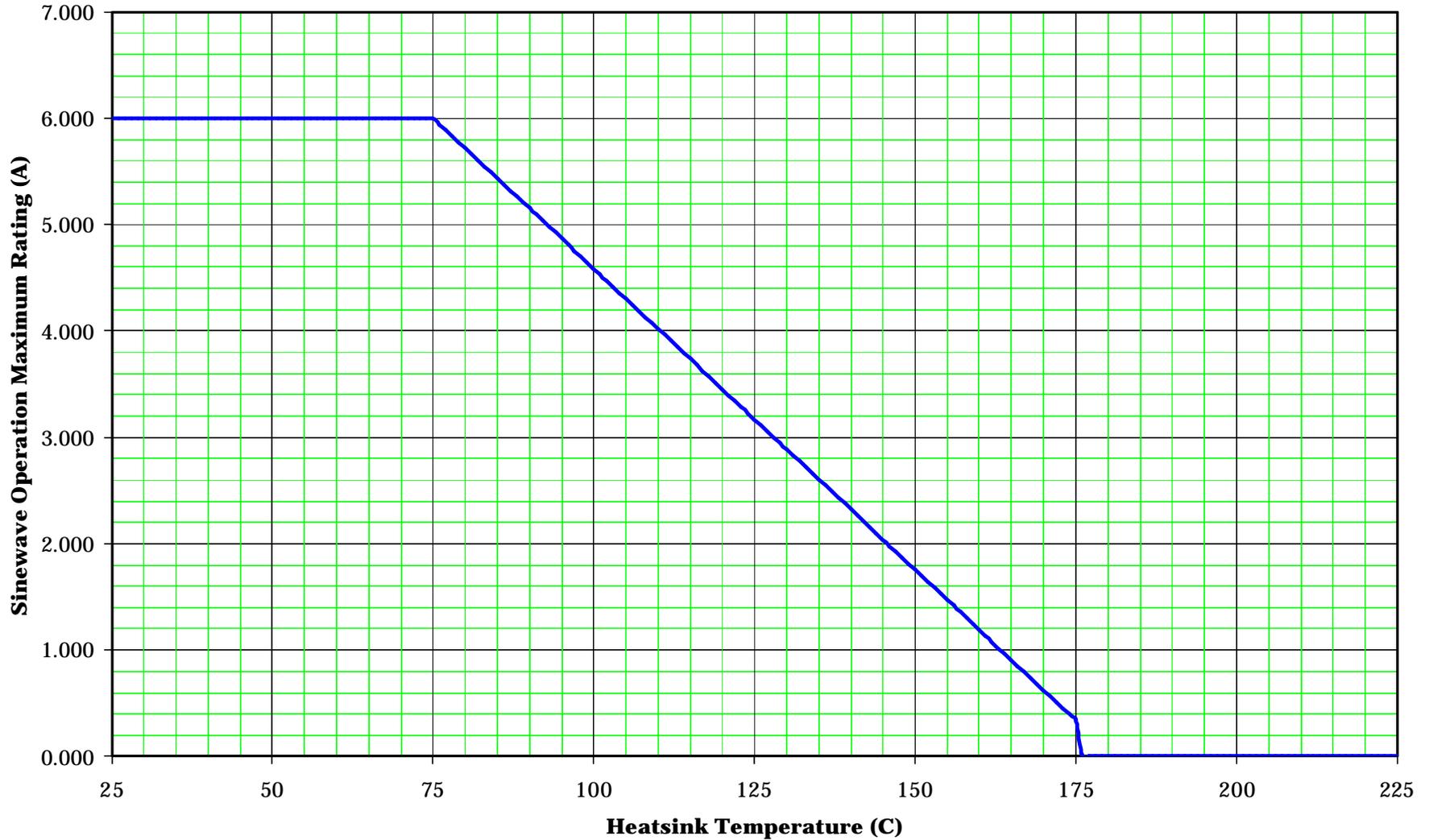
## Results

Ideal Maximum "Sink" Temp =	181.0 °C	(Package limitations may lower this)
<b>Maximum Junction Temp [Top(max)] =</b>	<b>191.1 °C</b>	<b>(Sinewave Operation)</b>
<b>Maximum Sink Temp [Tsink(max)] =</b>	<b>175.0 °C</b>	<b>(Sinewave Operation)</b>

# 1N5811 - SINE

**Safe Operating Derating Curve (Safe = Below the Curve)**

JAN1N5811, Lead=3/8" (/477)



# Maximum Operating Temperature Calculator

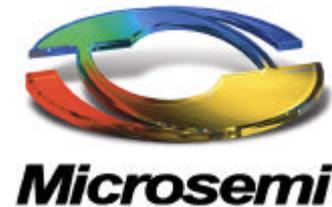
Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision K

## Input

### 1N5811 - DC

High temperature DC operation is especially challenging for gold doped rectifiers and Schottky rectifiers.

Title (Appears in the Plots) =	JAN1N5811, Lead=3/8" (/477)
Thermal Resistance =	22 °C/W
Rate Ir Doubles =	14.81 °C to Double
Hot Ir =	0.15 mA
Hot Vr =	150 V
Waveform =	1 1=DC, 2=Squarewave 50% D/C
Hot Temp =	100.0 °C
Maximum Rating (Numeric value) =	6 mA, A, mW, W or %
Units for Maximum Rating (Text value) =	A mA, A, mW, W or %
Temp for the Maximum Rating =	75.0 °C
Silicon Runaway Temp =	275.0 °C
Maximum Lead/Case Finish Temp =	180.0 °C
Maximum Internal Package Temp =	400.0 °C
Maximum Die Metalization or Bond Temp =	790.0 °C
Temperature Guardband (0=None) =	5.0 °C



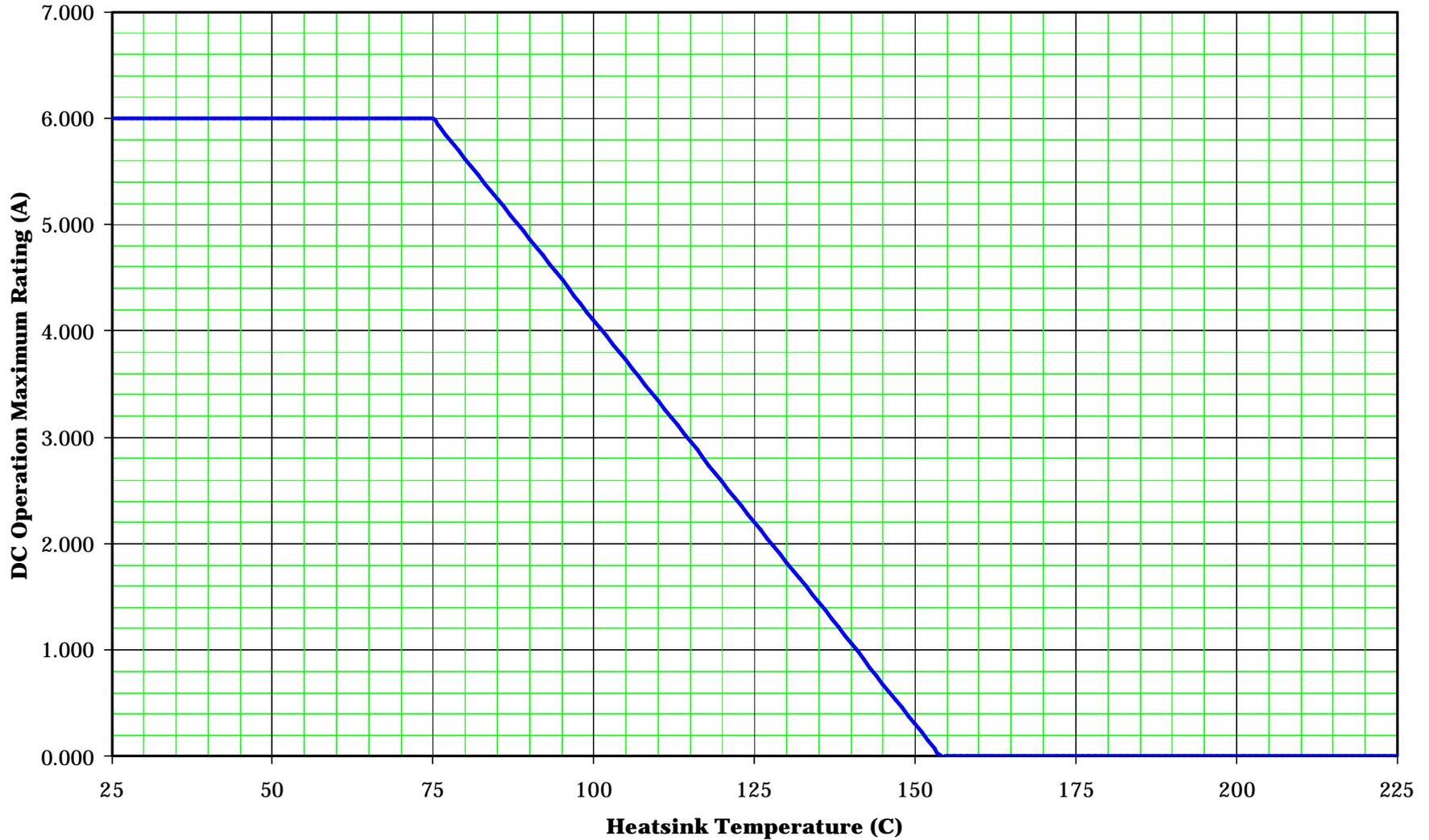
## Results

Ideal Maximum "Sink" Temp =	154.0 °C
<b>Maximum Junction Temp [Top(max)] =</b>	<b>163.8 °C (DC Operation)</b>
<b>Maximum Sink Temp [Tsink(max)] =</b>	<b>154.0 °C (DC Operation)</b>

# 1N5811 - DC

**Safe Operating Derating Curve (Safe = Below the Curve)**

JAN1N5811, Lead=3/8" (/477)



# Maximum Operating Temperature Calculator

Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision L-Engineering

## Input

1N6638 - SQUARE

Title (Appears in the Plots) = 1N6638 Mil-Prf-19500/578

Thermal Resistance = 160 °C/W

Rate Ir Doubles = 14.40 °C to Double

Hot Ir = 0.1 mA

Hot Vr = 125 V

Waveform = 2 1=DC, 2=Squarewave, 3=Sine

Hot Temp = 150.0 °C

Maximum Rating (Numeric value) = 300 mA, A, mW, W or %

Units for Maximum Rating (Text value) = mA mA, A, mW, W or %

Temp for the Maximum Rating = 75.0 °C

Silicon Runaway Temp = 275.0 °C

Maximum Lead/Case Finish Temp = 180.0 °C

Maximum Internal Package Temp = 400.0 °C

Maximum Die Metalization or Bond Temp = 760.0 °C

Temperature Guardband (0=None) = 5.0 °C



**Microsemi**

## Results

Ideal Maximum "Sink" Temp = 187.0 °C (Package limitations may lower this)

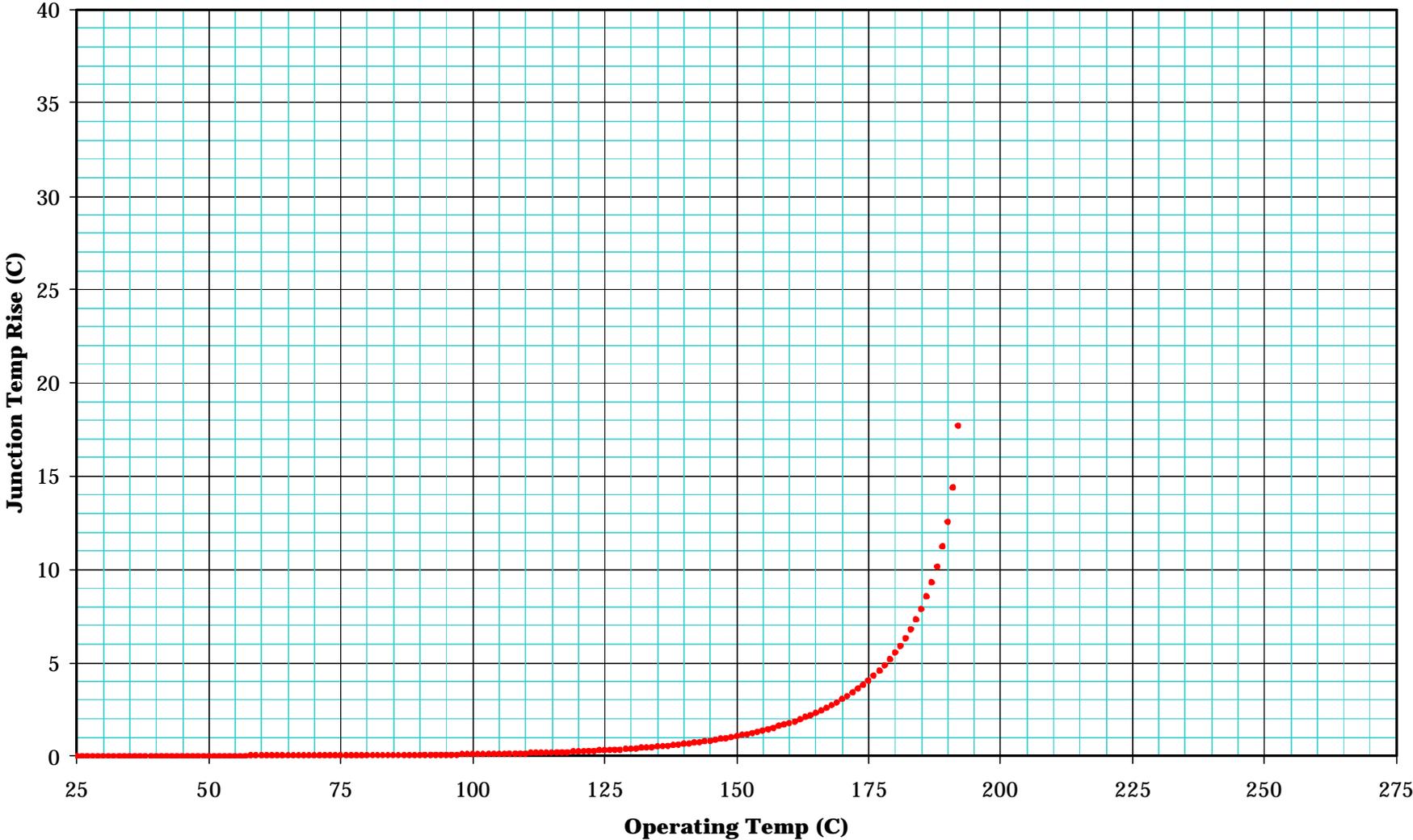
**Maximum Junction Temp [Top(max)] = 196.3 °C (Squarewave Operation)**

**Maximum Sink Temp [Tsink(max)] = 175.0 °C (Squarewave Operation)**

# 1N6638 - SQUARE

## Junction Temperature Rise Above Operating Temp Due to Ir Self-Heating

1N6638 Mil-Prf-19500/578



# Maximum Operating Temperature Calculator

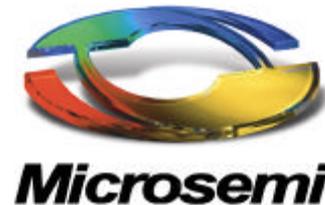
Ray DiBugnara, Microsemi Lawrence, "Thermal Ratings" Revision K

## Input

### TVS – DC

Due to transient nature of operation, max junction temp here applies to DC operation even though during transient clamp, junction can exceed 200C momentarily.

Title (Appears in the Plots) =	1N6152A /516	
Thermal Resistance =	20	°C/W
Rate Ir Doubles =	10.50	°C to Double
Hot Ir =	0.4	mA
Hot Vr =	20.6	V
Waveform =	1	1=DC, 2=Squarewave 50% D/C
Hot Temp =	150.0	°C
Maximum Rating (Numeric value) =	100	mA, A, mW, W or %
Units for Maximum Rating (Text value) =	%	mA, A, mW, W or %
Temp for the Maximum Rating =	75.0	°C
Silicon Runaway Temp =	275.0	°C
Maximum Lead/Case Finish Temp =	180.0	°C
Maximum Internal Package Temp =	400.0	°C
Maximum Die Metalization or Bond Temp =	760.0	°C
Temperature Guardband (0=None) =	5.0	°C



## Results

Ideal Maximum "Sink" Temp =	198.0	°C (Package limitations may lower this)
<b>Maximum Junction Temp [Top(max)] =</b>	<b>203.7</b>	<b>°C (DC Operation)</b>
<b>Maximum Sink Temp [Tsink(max)] =</b>	<b>175.0</b>	<b>°C (DC Operation)</b>

## EXAMPLE SUMMARIES

Part Number	Description	Rating Bias	T <sub>j</sub> (max) <u>1/</u>	T <sub>sink</sub> (max) <u>3/</u>
2N2222A /255 TO-5	Bipolar Transistor	Not Specified	200°C	Not Rated
“	“	DC Bias	202°C <u>2/</u>	196°C
“	“	Squarewave Bias	212°C <u>2/</u>	206°C
1N5811 /477 Axial	Ultrafast Rectifier	Not Specified	175°C	Not Rated
“	“	Sinewave Bias	191°C <u>2/</u>	181°C
“	“	Squarewave Bias	179°C <u>2/</u>	169°C
“	“	DC Bias	164°C <u>2/</u>	154°C
1N6638 /578 Axial	125V Switching	Not Specified	175°C	Not Rated
“	“	Squarewave Bias	196°C <u>2/</u>	187°C
“	“	DC Bias	183°C <u>2/</u>	173°C
1N6152A /516 Axial	20V TVS	Assume DC Bias	175°C	Not Rated
“	“	DC Bias	204°C <u>2/</u>	198°C

1/ Assuming no other physical limitations, part will “runaway” above this temperature.

2/ Other voltages in the series may have higher or lower ratings.

3/ T<sub>sink</sub>(max) here is ignoring any package limitations such as lead finish (solder coat).

## Conclusions on “Thermal Ratings”

- 1) The “Thermal Ratings” can be a useful tool. Accuracy depends upon correct inputs.
- 2) Circuit designers can use “Thermal Ratings” to test for potential runaway conditions.
- 3) The  $I_r$ -C/Doubling constant is most critical to make the model the most accurate.
- 4) Hot  $I_r/V_r$  input data produces the most accurate results when at the highest temperature.
- 5) Users can use suggested settings from “Pop Up” windows but call vendor for specifics.
- 6) Introduction of  $T_{sink}$  concept may assist circuit designers and may be more realistic

## Conclusions on Study

- 1) Definition of  $T_{op}$  and  $T_{op(max)}$  is unclear and needs to be redefined.
- 2) The derating curves on transistors are probably OK due to low  $I_r$  and known DC operation.
- 3) Derating curves on gold doped devices are probably OK because was derived from data.
- 4) Hot  $I_r$  ratings seem practical. Not all room temp ratings, however, are so blessed.
- 5) Schottkys will vary the most due to broad variation of barrier heights. Model will help.
- 6) Question: Should the “ $I_r$ -C/Doubling” rate be part of the specification to aid designers?