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IN REPLY
REFER TO DSCC-VAS **DATE 25 August 2004**

MEMORANDUM FOR MILITARY/INDUSTRY DISTRIBUTION

SUBJECT: Initial Draft of MIL-M-38510/133; Project Number 5962-2046

The initial draft for this subject document, dated 25 August 2004, is now available for viewing and downloading from the DSCC-VA Web site:

http://www.dscc.dla.mil/Programs/MilSpec/DocSearch.asp

Major changes to this document include references to MIL-M-38510 have been changed to MIL-PRF-38535. Paragraphs have been changed to meet current requirements of MIL-STD-961. Burn-in circuits have been deleted and replaced by a statement requiring the circuits to be maintained by the manufacturer under document control. The slash sheet is being updated to reflect current requirements.

Concurrence or comments are required at this Center within 45 days from the date of this letter. Late comments will be held for the next coordination of the document. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply.

The point of contact for this document is Mr. Raj Pithadia, Defense Supply Center Columbus, DSCC-VAS, Post Office Box 3990, Columbus, OH 43216-5000. Mr. Pithadia can also be reached at 614-692-0527/850-0527, or by facsimile 614-692-6939/850-6939, or by e-mail to: rajesh.pithadia@dla.mil

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NOTE: This draft, dated 25 August, 2004 prepared by Defense Supply Center Columbus (DSCC-VAS) has not been approved and is subject to modification.

DO NOT USE PRIOR TO APPROVAL.
(Project 5962-2046)

INCH-POUND
MIL-M-38510/133B
DRAFT
SUPERSEDING
MIL-M-38510/133A
18 August 1982

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, 10-BIT DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

Inactive for new design as of 10 July 1995

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, 10-bit binary digital-to-analog converters containing deposited thin film resistor networks. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3)

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	10-bit binary, internal reference, 2 mA full scale, D/A converter

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+16.5 V
Supply voltage (V_{EE})	-16.5 V
Digital input voltage (V_{IN})	V_{CC} to ground
Output voltage compliance(V_{OUT})	-2 V to +10 V
10 V span resistor to ground	V_{CC} to V_{EE}
Bipolar offset resistor to ground	V_{CC} to V_{EE}
Lead temperature (soldering, 60 seconds)	300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	175°C
Maximum power dissipation	500 mW

1.4 Recommended operating conditions.

Supply voltage range		V_{CC} = 4.5 V to 16.5 V V_{EE} = -10.8 V to -16.5 V
Output compliance voltage range		V_{OUT} = -2 V to +10 V
Logic thresholds:	TTL logic “0”	0.8 V (max)
	logic “1”	2.2 V (min)
	CMOS logic “0”	30% V_{CC} (max)
	logic “1”	70% V_{CC} (min)
Ambient operating temeperature range (T_A)		-55°C to +125°C

1.5 Power and thermal characteristics.

Case outline	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
E	500 mW @ T_A = 125°C	35°C/W	100°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Case outline. The case outline shall be as specified in 1.2.3.

3.3.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VA) upon request.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.8 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 56 (see MIL-PRF-38535, appendix A).

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer’s Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Monotonicity		Guaranteed by the bit linearity and Major carry error tests	01		10	Bits
Supply current from V_{CC}	I_{CC}	All digital inputs at 15.0 V	01	+2	+10	mA
Supply current from V_{EE}	I_{EE}	All digital inputs at 0 V	01	-16	-2	mA
Reference voltage output	V_{REF}	I_{REF} = 2 mA	01	2.45	2.55	V
Digital input leakage	I_{IL}	All digital inputs at 15 V	01	-100	+1	µA
	I_{IH}			-1	+100	
Zero scale current: TTL	I_{ZS1}	V_{CC} = +5 V, All digital inputs at 0.8 V, T_A = 25°C	01	-0.5	+0.5	LSB
CMOS	I_{ZS2}	All digital inputs at 4.5 V, T_A = 25°C		-0.5	+0.5	
Zero scale current drift	d_{IZST}/dt	All digital inputs at 0.8 V	01	-10.0	+10.0	mLSB/°C
Full-scale current: TTL	I_{FS1}	All inputs logic "1", V_O = 0 V, V_{CC} = +5 V	01	+1.5	+2.5	mA
CMOS	I_{FS2}	All inputs logic "1", V_O = 0 V, V_{CC} = +15 V		+1.5	+2.5	
Full-scale current at +10 V compliance	I_{FS+}	All digital inputs logic "1", V_O = +10 V, V_{CC} = +5 V	01	+1.5	+2.5	mA
Full-scale current at -2 V compliance	I_{FS-}	All digital inputs logic "1", V_O = -2 V, V_{CC} = +5 V	01	+1.5	+2.5	mA
Full-scale current change	d_{IFS+}	All digital inputs logic "1", V_O = 0 V to +10 V	01	-5.0	+5.0	µA
Full-scale current change	d_{IFS-}	All digital inputs logic "1", V_O = 0 V to -2 V	01	-5.0	+5.0	µA
Bipolar offset error	B_{POE}	All inputs logic "0", T_A = 25°C 2/	01	-5.0	+5.0	LSB
Bipolar offset drift	d_{BPOE}/dt	All inputs logic "0", measure V_O	01	-60.0	+60.0	mLSB/°C
Bipolar zero error (TTL)	B_{ZE}	Inputs bits = 512 (binary), T_A = 25°C	01	-2.5	+2.5	LSB
Bipolar zero drift	d_{BZ}/dt	Input bits = 512 (binary)	01	-20.0	+20.0	mLSB/°C
Gain error (full scale): TTL	A_{E1}	From 0 to full-scale, V_{CC} = +5 V, $A_{E1} = 10 (V_{FS} – 9.99023 - V_{OS})$, T_A = 25°C 3/	01	-0.5	+0.5	%FS
CMOS	A_{E2}	From 0 to full-scale, $A_{E2} = 10 (V_{FS} – 9.99023 - V_{OS})$, T_A = 25°C 3/		-0.5	+0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Gain error drift	d_{AE2}/dt	Change in V_{FS} from -55°C to +125°C	01	-0.006	+0.006	%/°C
Power supply sensitivity at full-scale from V_{CC}: TTL	$+P_{SS1}$	All digital inputs at V_{CC}; V_{CC} = +5 ±0.5 V, T_A = 25°C 4/	01	-0.01	+0.01	LSB/%PS
		V_{CC} = +5±0.5 V, -55°C < T_A < 125°C		-0.02	+0.02	
CMOS	$+P_{SS2}$	V_{CC} = +15±1.5 V, T_A = 25°C 4/		-0.01	+0.01	
		V_{CC} = +15±1.5 V, -55°C < T_A < 125°C		-0.02	+0.02	
Power supply sensitivity at full-scale from V_{EE}: CMOS	$-P_{SS1}$	V_{EE} = -15±1.5 V, T_A = 25°C 4/	01	-0.025	+0.025	LSB/%PS
		V_{EE} = -15±1.5 V, -55°C < T_A < 125°C		-0.05	+0.05	
TTL	$-P_{SS2}$	V_{EE} = -12±1.2 V, V_{CC} = +5.0 V, T_A = 25°C 4/		-0.025	+0.025	
		V_{EE} = -12±1.2 V, V_{CC} = +5.0 V, -55°C < T_A < 125°C		-0.05	+0.05	
Linearity error (end point)	LE	All combinations of bits 1 to 4, bits 5 to 10 are turned off. Measure V_O relative to REF DAC output. Record the code words for the worst case positive bit error; and for the worst case negative bit error. 5/	01	-0.5	+0.5	LSB
		Turn on bits 5 to 10, one bit at a time, and measure relative to REF DAC output. Bits 1 to 4 are turned off. Record the measured bit error sign. 5/		-0.5	+0.5	
Linearity error (end point)	LE	(All codes test) See table III	01	-0.5	+0.5	LSB
Major carry errors	MCE1 – MCE10	The difference between adjacent codes at all major transitions (i.e. from 01111111 to 10000000) 4/	01	-1.0	+1.0	LSB
Output current settling time (to ½ LSB) 0 V to FS	t_{SLH}	V_{CC} = +5 V. All inputs switched simultaneously. Measure the time to settle to within ½ LSB of the final value. T_A = 25°C. (see figures 3 and 4)	01		500	ns
Output current settling time (to ½ LSB) FS to 0 V	t_{SLH}	V_{CC} = +5 V. All inputs switched simultaneously. Measure the time to settle to within ½ LSB of the final value. T_A = 25°C. (see figures 3 and 4)	01		500	ns
Noise	N_O	VCC = +5.0 V; VEE = -15 V, 0 V, All digital inputs at +2.2 V, see figure 5. T_A = 25°C, BW =100 kHz, 5/ 6/	01		160	µV rms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ V_{CC} = +15 V, V_{EE} = -15 V, Logic "0" = 4.5 V (max), Logic "1" = 10.5 V (min), unipolar and bipolar application, see figure 2, unless otherwise specified. See 6.5 for symbols and definitions.

2/ B_{POE} is the error in the –5 V DUT output voltage when the device is operated in the bipolar mode with all digital bits off.

3/ The gain error of a 10-bit D/A converter corresponds to a zero-scale to full-scale range error in LSB units (i.e. ±0.5% x 1024 LSB/100% = ±5.12 LSB).

4/ This test is performed in the unipolar mode over a 0 to 10 V range. The unipolar scale factor is 1024 LSB/10 V = 102.4 LSB/V.

5/ The manufacturer has the option of testing devices at all digital input codes or an abbreviated series of codes. The abbreviated test should have a sufficient number of codes with or without limit guard banding such that an "all-codes" test will not fail a device which passed the abbreviated test.

6/ The limit 160 µV rms over a 100 kHz bandwidth will result in less than ¼ LSB peak noise over a 4 MHz noise bandwidth.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3	1*, 2, 3
Group A test requirements	1,2,3,7,8,12	1,2,3,7,8,12
Group B electrical test parameters when using the method 5005 QCI option	1,2,3 and table IV delta limits	N/A
Group C end-point electrical parameters	1,2,3 and table IV delta limits	1 and table IV delta limits
Additional electrical subgroups for group C periodic inspections	N/A	----
Group D end-point electrical parameters	1,2,3,	1

* PDA applies to subgroup 1.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 9, 10, and 11 shall be omitted.

c. Subgroup 12 shall be added to group A inspection for all classes and it shall consist of the conditions and limits as specified in table III. The sample size series number shall be 15 for all classes (accept on 0).

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

Device types	01
Case outlines	E
Terminal number	Terminal symbol
1	GROUND
2	BIPOLAR OFFSET
3	$V_{EE(-)}$
4	LSB BIT 10
5	BIT 9
6	BIT 8
7	BIT 7
8	BIT 6
9	BIT 5
10	BIT 4
11	BIT 3
12	BIT 2
13	BIT 1 MSB
14	$V_{CC(+)}$
15	OUTPUT
16	10 V SPAN RESISTOR

Figure 1. Terminal connections.

CIRCUIT HAS BEEN DELETED

Figure X. Functional schematic circuits.

CIRCUIT HAS BEEN DELETED

Figure X. Functional schematic with application notes (unipolar mode).

CIRCUIT HAS BEEN DELETED

Figure X. Functional schematic with application notes (bipolar mode) – Continued.

CIRCUIT HAS BEEN DELETED

Figure X. Test circuit, burn-in and steady state life test.

CIRCUIT HAS BEEN DELETED

Figure X. Test circuit, burn-in, steady state power and reverse bias, steady state life test, and accelerated burn-in.

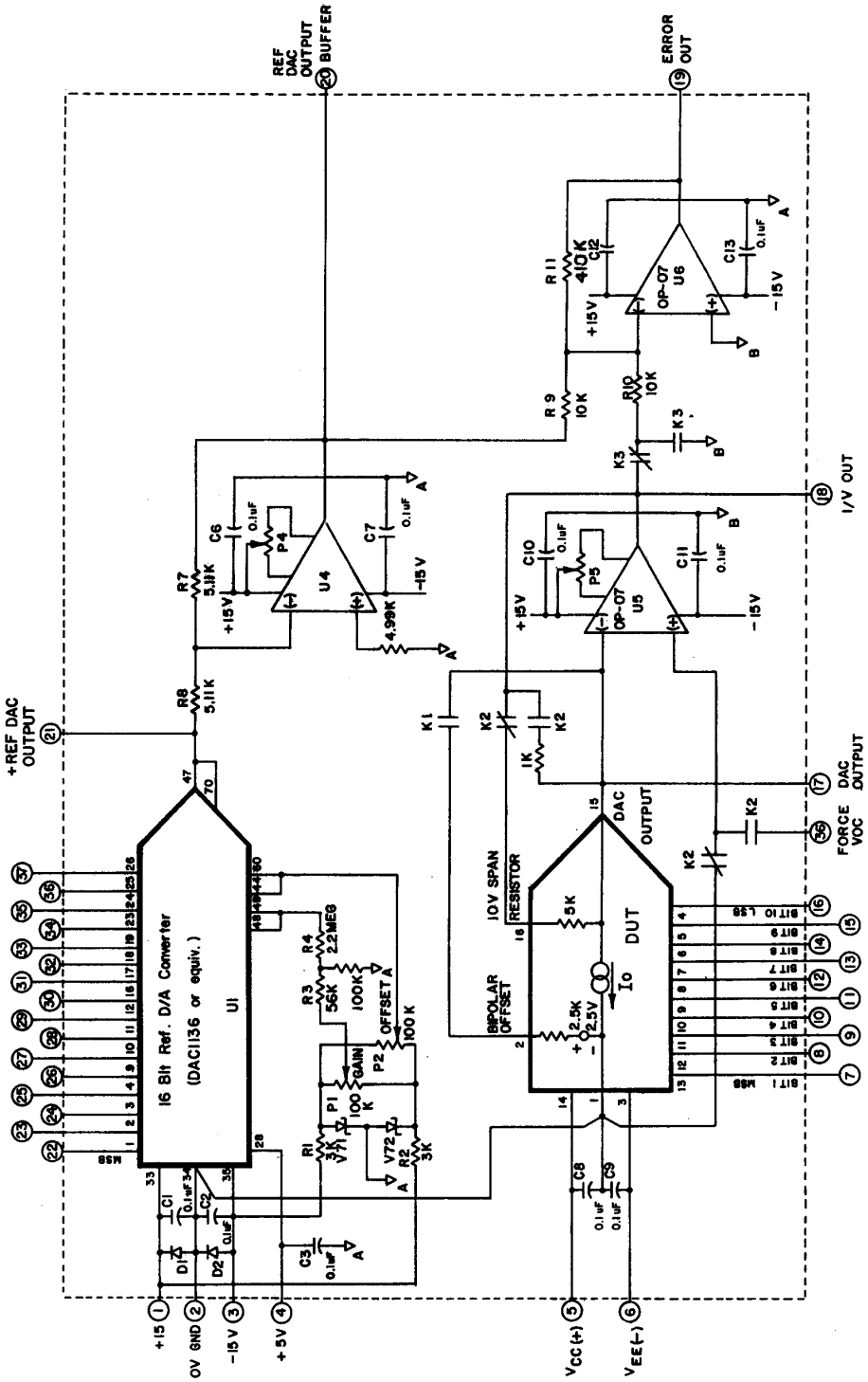
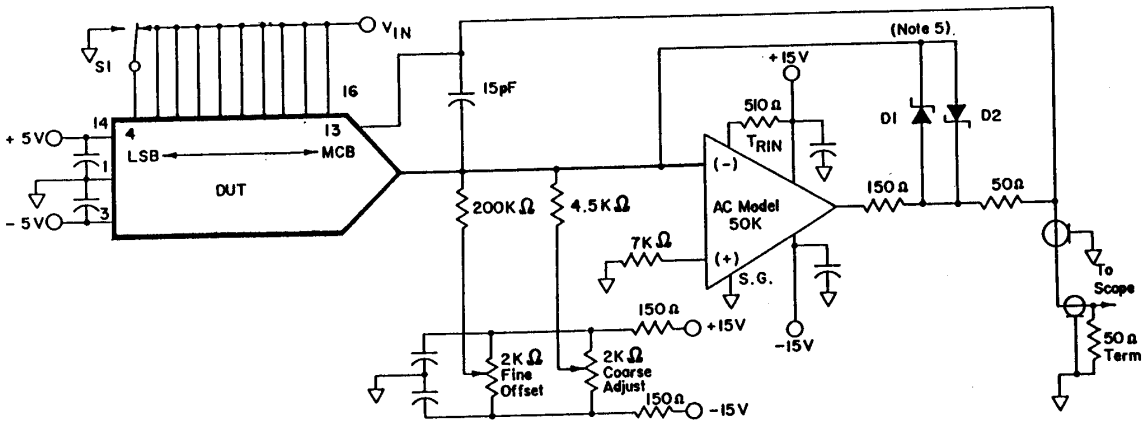
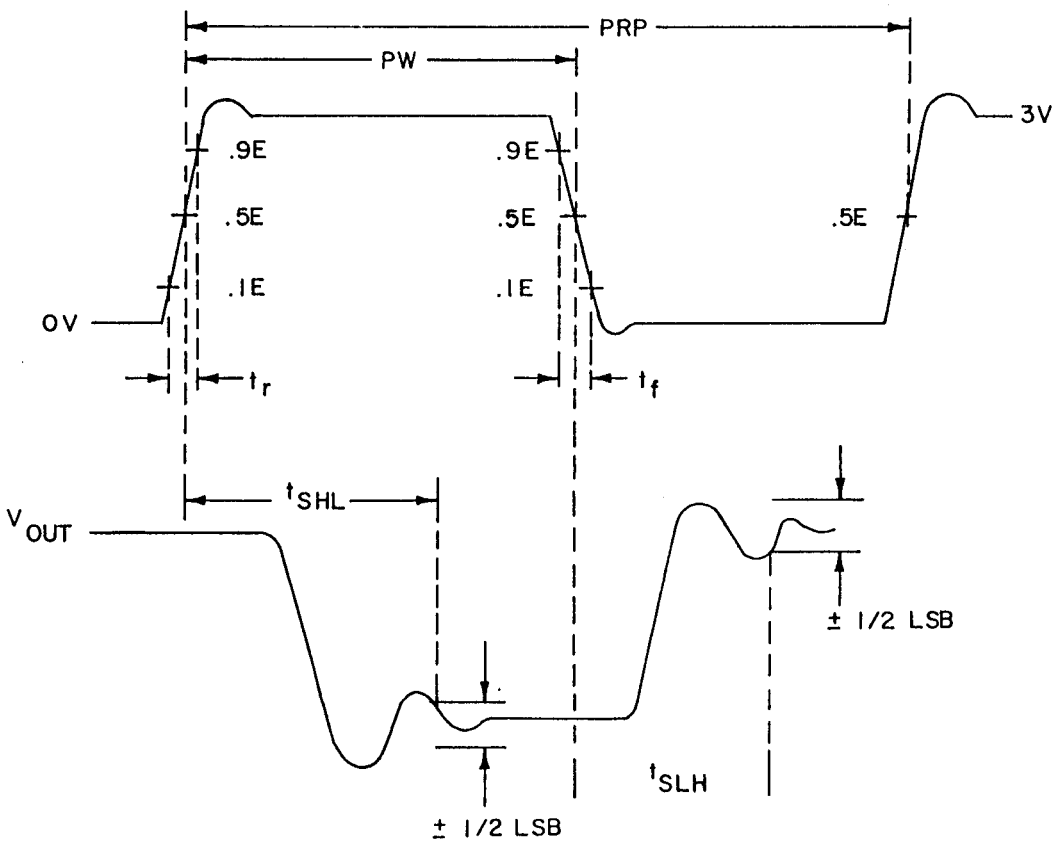


Figure 2. Table III test circuit for static tests.



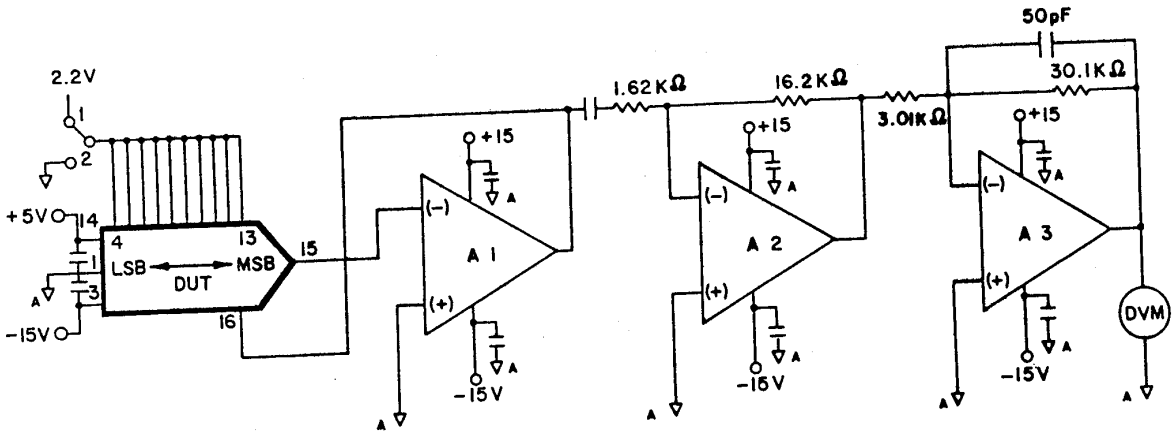
NOTES:
1. Unless otherwise defined, all capacitors are 47 μF tantalum paralleled with 0.1 μF ceramic.
2. Bandwidth of the oscilloscope shall be 50 MHz minimum; saturation of the preamp must be avoided. Use a voltage comparator preamp.
3. Adjust the coarse and fine offset controls to position the waveform final value on the oscilloscope center horizontal graticule.
4. While operating switch S-1, adjust the oscilloscope vertical gain for ½ LSB per cm.
5. D1 = D2 = MP 5082-2835 or equivalent.
6. All grounds must be separately connected to unipoint ground at device pin 1.

Figure 3. Test circuit for settling time.



NOTE: PRP = 1.2 µs (min); PW = 600 ns (min)
$t_r = t_f \leq 10$ ns

Figure 4. Waveforms for settling time tests (device type 01).



NOTES:
1. Unless otherwise stated, all capacitors are 47 μF tantalum paralleled with 0.1 μF ceramic.
2. The meter shall be true rms reading with a bandwidth greater than 100 kHz.
3. A1, A2, and A3 shall have a gain-bandwidth product greater than 5 MHz and input noise density less than 10 nV/$\sqrt{\text{Hz}}$.
4. All "A" point ground connections shall return to a single unipoint ground at device pin 1.
5. With S-1 in position 2, the measured rms noise voltage shall be less than 1.0 mV rms. (N_O for all bits off.)
6. With S-1 in position 1, the measured rms noise voltage shall be:

$$N_O \text{ for DUT} = \frac{\sqrt{(N_O)^2 \text{ for all bits on} - (N_O)^2 \text{ for all bits off}}}{100}$$

Figure 5. Test circuit for noise tests.

TABLE III. Group A inspection.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
Calibration		1	Adjust P6 with all bits at 0 V				None	18	E1	µV	ECA1 = E1		450	µV
1 T_A = 25°C	I_{CC}	2	+15 V	-15 V	0000 0000 00	1111 1111 1111 1111	“ “	5	I1	mA	I_{CC} = I1 (Digital 0 = 0 V)	+2	+10	mA
	I_{EE}	3	“	“	“	“	“	6	I2	mA	I_{EE} = I2 (Digital 0 = 0 V)	-16	-2	mA
	V_{REF}	4	“	“	“	“	“	2	E2	V	V_{REF} = E2 I_{REF} = 2 mA	2.45	2.55	V
	I_{IL}	5	“	“	“	“	“	7	I3	µA	I_{IL} = I3 (Digital 0 = 0 V)	-100	+1	µA
		6	“	“	“	“	“	8	I4	“	I_{IL} = I4	“	“	“
		7	“	“	“	“	“	9	I5	“	I_{IL} = I5	“	“	“
		8	“	“	“	“	“	10	I6	“	I_{IL} = I6	“	“	“
		9	“	“	“	“	“	11	I7	“	I_{IL} = I7	“	“	“
		10	“	“	“	“	“	12	I8	“	I_{IL} = I8	“	“	“
		11	“	“	“	“	“	13	I9	“	I_{IL} = I9	“	“	“
		12	“	“	“	“	“	14	I10	“	I_{IL} = I10	“	“	“
		13	“	“	“	“	“	15	I11	“	I_{IL} = I11	“	“	“
		14	“	“	“	“	“	16	I12	“	I_{IL} = I12	“	“	“
	I_{IH}	15	“	“	1111 1111 11	“	“	7	I13	“	I_{IH} = I13 (Digital 1 = 15 V)	-1	100	“
		16	“	“	“	“	“	8	I14	“	I_{IH} = I14	“	“	“
		17	“	“	“	“	“	9	I15	“	I_{IH} = I15	“	“	“
		18	“	“	“	“	“	10	I16	“	I_{IH} = I16	“	“	“
		19	“	“	“	“	“	11	I17	“	I_{IH} = I17	“	“	“
		20	“	“	“	“	“	12	I18	“	I_{IH} = I18	“	“	“
		21	“	“	“	“	“	13	I19	“	I_{IH} = I19	“	“	“
		22	“	“	“	“	“	14	I20	“	I_{IH} = I20	“	“	“
		23	“	“	“	“	“	15	I21	“	I_{IH} = I21	“	“	“
		24	“	“	“	“	“	16	I22	“	I_{IH} = I22	“	“	“
	I_{FS1}	25	+5 V	“	“		“	18	E3	V	I_{FS1} = E3/1000	+1.5	+2.5	mA
	I_{FS2}	26	+15 V	“	“		“	“	E4	“	I_{FS2} = E4/1000	“	“	“
	G1	27	“	“	0000 0000 00	1111 1111 1111 1111	“	19	E5	“	G_1 = (E6-E5)(4096)/(14)(10)	-41.5	-40.5	V/V
		28	“	“	“	1111 1111 0001 1111	“	“	E6	“	G_1 is the error amplifier gain			
	I_{FS+}	29	+5 V	“	1111 1111 11	0000 0000 0000 0000	K1	18	E7	“	I_{FS+} = E7/1000	+1.5	+2.5	mA
	I_{FS-}	30	“	“	“	“	K1	“	E8	“	I_{FS-} = E8/1000	“	“	“
	$d_{IFS(+)}$	31	“	“	“		None	“	E9	“	V_{OC} = 0 V	-5	+5	µA
		32	“	“	“		“	“	E10	“	V_{OC} = +10 V, dIFS(+) = (E10-E9)/1000			
	$d_{IFS(-)}$	33	“	“	“		“	“	E11	“	V_{OC} = 0 V	“	“	“
		34	“	“	“		“	“	E12	“	V_{OC} = -2 V, dIFS(-) = (E12-E11)/1000			
	I_{ZS1}	35	“	“	0000 0000 00	1111 1111 1111 1111	K1	“	E13	“	I_{ZS1} = E13(1024)/E3	-0.5	+0.5	LSB
	I_{ZS2}	36	+15 V	“	“	“	“	“	E14	“	I_{ZS2} = E14(1024)/E4	“	“	“
	B_{POE}	37	“	“	“	“	“	19	E15	“	B_{POE} = E15/(G1)(9.7656E-3)	-5	+5	“

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
1 T_A = 25°C	B_{ZE}	38	+15 V	-15 V	1000 000 00	1111 1111 1111 1111	None	19	E16	v	B_{ZE} = E16/(G1)(9.7656E-3)	-2.5	+2.5	LSB
	A_{E1}	39	+5 V	"	1111 1111 11 0000 0000 00	0000 0000 0011 1111 1111 1111 1111 1111	" "	21	E17 E18	" "	A_{E1} = 10((E17-E18)/(G1))	-0.5	+0.5	%FS
	A_{E2}	40	+15 V	"	1111 1111 11 0000 0000 00	0000 0000 0011 1111 1111 1111 1111 1111	" "	21	E19 E20	" "	A_{E2} = 10((E19-E20)/(G1))	"	"	"
	$+P_{SS1}$	41	+4.5 V	"	1111 1111 11	0000 0000 0011 1111	"	19	E21	"	$+P_{SS1}$ = ((E21-E22)/G1)(9.7656E-3)(10)	-0.01	+0.01	LSB
		42	+5.0 V	"	"	"	"	"	E22	"		"	"	/%PS
	$-P_{SS1}$	43	+5.5 V	"	"	"	"	"	E23	"	$-P_{SS1}$ = ((E23-E22)/G1)(9.7656E-3)(10)	"	"	"
	$+P_{SS2}$	44	+13.5 V	"	"	"	"	"	E24	"	$+P_{SS2}$ = ((E24-E25)/G1)(9.7656E-3)(10)	"	"	"
		45	+15 V	"	"	"	"	"	E25	"		"	"	"
	$-P_{SS2}$	46	+16.5 V	"	"	"	"	"	E26	"	$+P_{SS2}$ = ((E26-E25)/G1)(9.7656E-3)(10)	"	"	"
	$-P_{SS1}$	47	+5 V	-13.5 V	"	"	"	"	E27	"	$-P_{SS1}$ = ((E27-E28)/G1)(9.7656E-3)(10)	-0.025	+0.025	"
		48	"	-15 V	"	"	"	"	E28	"		"	"	"
		49	"	-16.5 V	"	"	"	"	E29	"	$-P_{SS1}$ = ((E29-E28)/G1)(9.7656E-3)(10)	"	"	"
	$-P_{SS2}$	50	+15 V	-10.8 V	"	"	"	"	E30	"	$-P_{SS2}$ = ((E30-E31)/G1)(9.7656E-3)(10)	"	"	"
		51	"	-12 V	"	"	"	"	E31	"		"	"	"
		52	"	-13.2 V	"	"	"	"	E32	"	$-P_{SS2}$ = ((E32-E31)/G1)(9.7656E-3)(10)	"	"	"
	L_E	53	"	-15 V	0001 0000 00	1110 1111 1111 1111	"	"	E33	"	For each input code N calculate the	-0.5	+0.5	LSB
	"	54	"	"	0010 0000 00	1101 1111 1111 1111	"	"	E34	"	corresponding linearity error in LSB.	"	"	"
	"	55	"	"	0011 0000 00	1100 1111 1111 1111	"	"	E35	"		"	"	"
	"	56	"	"	0100 0000 00	1011 1111 1111 1111	"	"	E36	"		"	"	"
	"	57	"	"	0101 0000 00	1010 1111 1111 1111	"	"	E37	"	L_E = ((EA/G1)+(N)(K)-(V_{OS}))/(9.7656E-3)	"	"	"
	"	58	"	"	0110 0000 00	1001 1111 1111 1111	"	"	E38	"		"	"	"
	"	59	"	"	0111 0000 00	1000 1111 1111 1111	"	"	E39	"	where	"	"	"
	"	60	"	"	1000 0000 00	0111 1111 1111 1111	"	"	E40	"	EA = measured value E33 through E53	"	"	"
	"	61	"	"	1001 0000 00	0110 1111 1111 1111	"	"	E41	"	G1 = error amplifier gain from step 28	"	"	"
	"	62	"	"	1010 0000 00	0101 1111 1111 1111	"	"	E42	"	N = DUT input digital code word in	"	"	"
	"	63	"	"	1011 0000 00	0100 1111 1111 1111	"	"	E43	"	decimal form. Thus for 10 bits	"	"	"
	"	64	"	"	1100 0000 00	0011 1111 1111 1111	"	"	E44	"	N = (A1)(2exp7)+(A2)(2exp6)+…	"	"	"
	"	65	"	"	1101 0000 00	0010 1111 1111 1111	"	"	E45	"	+(A10)(2exp0)	"	"	"
	"	66	"	"	1110 0000 00	0001 1111 1111 1111	"	"	E46	"	A1,A2, … A10 are 0 or 1.	"	"	"
	"	67	"	"	1111 0000 00	0000 1111 1111 1111	"	"	E47	"	K = actual volts/count scale factor.	"	"	"
	"	68	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E48	"	K = (V_{FS} – V_{OS})/1023	"	"	"
	"	69	"	"	0000 0000 10	1111 1111 0111 1111	"	"	E49	"	where V_{FS} = Value at E19	"	"	"
	"	70	"	"	0000 0001 00	1111 1110 1111 1111	"	"	E50	"	V_{OS} = Value at E20	"	"	"
	"	71	"	"	0000 0010 00	1111 1101 1111 1111	"	"	E51	"		"	"	"
	"	72	"	"	0000 0100 00	1111 1011 1111 1111	"	"	E52	"		"	"	"
	"	73	"	"	0000 1000 00	1111 0111 1111 1111	"	"	E53	"		"	"	"

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			4	5	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
1 T_A = 25°C	MCE1	74	+15 V	-15 V	0111 1111 11	1000 0000 0011 1111	None	19	E54	V	For each set of major carry codes N and N+1 calculate the associated error in LSB's as follows: MCE = ((EB-EA)/G1)(9.7656E-3) where EB = Measured value from E54, E56, E58, etc. EA = Measured value from E55, E57, E59, etc.	-1	+1	LSB
			"	"	1000 0000 00	0111 1111 1111 1111	"	"	E55	"		"	"	"
	MCE2	75	"	"	0011 1111 11	1100 0000 0011 1111	"	"	E56	"		"	"	"
			"	"	0100 0000 00	1011 1111 1111 1111	"	"	E57	"		"	"	"
	MCE3	76	"	"	0001 1111 11	1110 0000 0011 1111	"	"	E58	"		"	"	"
			"	"	0010 0000 00	1101 1111 1111 1111	"	"	E59	"		"	"	"
	MCE4	77	"	"	0000 1111 11	1111 0000 0011 1111	"	"	E60	"		"	"	"
			"	"	0001 0000 00	1110 1111 1111 1111	"	"	E61	"		"	"	"
	MCE5	78	"	"	0000 0111 11	1111 1000 0011 1111	"	"	E62	"		"	"	"
			"	"	0000 1000 00	1111 0111 1111 1111	"	"	E63	"		"	"	"
	MCE6	79	"	"	0000 0011 11	1111 1100 0011 1111	"	"	E64	"		"	"	"
			"	"	0000 0100 00	1111 1011 1111 1111	"	"	E65	"		"	"	"
	MCE7	80	"	"	0000 0001 11	1111 1110 0011 1111	"	"	E66	"		"	"	"
			"	"	0000 0010 00	1111 1101 1111 1111	"	"	E67	"		"	"	"
	MCE8	81	"	"	0000 0000 11	1111 1111 1111 1111	"	"	E68	"		"	"	"
			"	"	0000 0001 00	1111 1110 1111 1111	"	"	E69	"		"	"	"
	MCE9	82	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E70	"		"	"	"
			"	"	0000 0000 10	1111 1111 0111 1111	"	"	E71	"		"	"	"
	MCE10	83	"	"	0000 0000 00	1111 1111 1111 1111	"	"	E72	"		"	"	"
			"	"	0000 0000 01	1111 1111 1011 1111	"	"	E73	"		"	"	"
Calibration		84	Adjust P6 with all bits at 0 V				"	18	E74	µV	Ecal = E74		450	µV

Subgroup	Symbol	Test No.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
2 T_A = 125°C	I_{CC}	85	+15 V	-15	0000 0000 00	1111 1111 1111 1111	None	5	I23	mA	I_{CC} = I23 (Digital 0 = 0 V)	+2	+10	mA
	I_{EE}	86	"	"	"	"	"	6	I24	mA	I_{EE} = I24 (Digital 0 = 0 V)	-16	-2	mA
	V_{REF}	87	"	"	"	"	"	2	E75	V	V_{REF} = E75 I_{REF} = 2 mA	2.45	2.55	V
	I_{IL}	88	"	"	"	"	"	7	I25	µA	I_{IL} = I25 (Digital 0 = 0 V)	-100	+1	µA
		89	"	"	"	"	"	8	I26	"	I_{IL} = I26	"	"	"
		90	"	"	"	"	"	9	I27	"	I_{IL} = I27	"	"	"
		91	"	"	"	"	"	10	I28	"	I_{IL} = I28	"	"	"
		92	"	"	"	"	"	11	I29	"	I_{IL} = I29	"	"	"
		93	"	"	"	"	"	12	I30	"	I_{IL} = I30	"	"	"
		94	"	"	"	"	"	13	I31	"	I_{IL} = I31	"	"	"
		95	"	"	"	"	"	14	I32	"	I_{IL} = I32	"	"	"
		96	"	"	"	"	"	15	I33	"	I_{IL} = I33	"	"	"
		97	"	"	"	"	"	16	I34	"	I_{IL} = I34	"	"	"
	I_{IH}	98	"	"	1111 1111 11	"	"	7	I35	"	I_{IH} = I35 (Digital 1 = 15 V)	-1	100	"
		99	"	"	"	"	"	8	I36	"	I_{IH} = I36	"	"	"
		100	"	"	"	"	"	9	I37	"	I_{IH} = I37	"	"	"
		101	"	"	"	"	"	10	I38	"	I_{IH} = I38	"	"	"
		102	"	"	"	"	"	11	I39	"	I_{IH} = I39	"	"	"
		103	"	"	"	"	"	12	I40	"	I_{IH} = I40	"	"	"
		104	"	"	"	"	"	13	I41	"	I_{IH} = I41	"	"	"
		105	"	"	"	"	"	14	I42	"	I_{IH} = I42	"	"	"
		106	"	"	"	"	"	15	I43	"	I_{IH} = I43	"	"	"
		107	"	"	"	"	"	16	I44	"	I_{IH} = I44			"

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
2 T_A = 125°C	I_{FS1} I_{FS2}	108 109	+5 V +15 V	-15 V “	1111 1111 11 “		None “	18 “	E76 E77	V “	I_{FS1} = E76/1000 I_{FS2} = E77/1000	+1.5 “	+2.5 “	mA “
	G1	110 111	“ “	“ “	0000 0000 00 “	1111 1111 1111 1111 1111 1111 0001 1111	“ “	19 “	E78 E79	“ “	G_1 = (E79-E78)(4096)/(14)(10) G_1 is the error amplifier gain	-41.5	-40.5	V/V
	I_{FS+}	112	+5 V	“	1111 1111 11	0000 0000 0000 0000	K1	18	E80	“	I_{FS+} = E80/1000	+1.5	+2.5	mA
	I_{FS-}	113	“	“	“	“	K1	“	E81	“	I_{FS-} = E81/1000	“	“	“
	$d_{IFS(+)}$	114 115	“ “	“ “	“ “		None “	“ “	E82 E83	“ “	V_{OC} = 0 V V_{OC} = +10 V $d_{IFS(+)}$ = (E83-E82)/1000	-5 “	+5 “	µA “
	$d_{IFS(-)}$	116 117	“ “	“ “	“ “		“ “	“ “	E84 E85	“ “	V_{OC} = 0 V V_{OC} = -2 V $d_{IFS(-)}$ = (E85-E84)/1000	-5 “	+5 “	“ “
	d_{IZS2}/dt	118	+15 V	“	0000 0000 00	1111 1111 1111 1111	K1	“	E86	“	d_{IZS2}/dt = (E86-E14)(1024)/(E77-E4)(100)	-10	+10	mLSB /°C
	d_{BPOE}/dt	119	“	“	0000 0000 00	1111 1111 1111 1111	K1	19	E87	“	d_{BPOE}/dt = (E87-E15)/(G1)(9.7656E-1)	-60	+60	“
	d_{BZE}/dt	120	“	“	1000 0000 00	1111 1111 1111 1111	None	19	E88	“	d_{BZE}/dt = (E88-E16)/(G1)(9.7656E-1)	-20	+20	“
	d_{AE2}/dt	121	“	“	1111 1111 11 0000 0000 00	0000 0000 0011 1111 1111 1111 1111 1111	“	21	E89 E90	“	d_{AE2}/dt = 0.1((E89-E90)-(E19-E20))/(G1)	-0.006	+0.006	%/°C
	$+P_{SS1}$ $-P_{SS1}$	122 123 124	+4.5 V +5.0 V +5.5 V	“ “ “	1111 1111 11 “ “	0000 0000 0011 1111 “ “	“ “ “	19 “ “	E91 E92 E93	“ “ “	$+P_{SS1}$ = ((E91-E92)/G1)(9.7656E-3)(10) $-P_{SS1}$ = ((E93-E92)/G1)(9.7656E-3)(10)	-0.02 “ “	+0.02 “ “	LSB /%PS “
	$+P_{SS2}$ $-P_{SS2}$	125 126 127	+13.5 V +15 V +16.5 V	“ “ “	“ “ “	“ “ “	“ “ “	“ “ “	E94 E95 E96	“ “ “	$+P_{SS2}$ = ((E94-E95)/G1)(9.7656E-3)(10) $+P_{SS2}$ = ((E96-E95)/G1)(9.7656E-3)(10)	“ “ “	“ “ “	“ “ “
	$-P_{SS1}$	128 129 130	+5 V “ “	-13.5 V -15 V -16.5 V	“ “ “	“ “ “	“ “ “	“ “ “	E97 E98 E99	“ “ “	$-P_{SS1}$ = ((E97-E98)/G1)(9.7656E-3)(10) $-P_{SS1}$ = ((E99-E98)/G1)(9.7656E-3)(10)	-0.05 “ “	+0.05 “ “	“ “ “
	$-P_{SS2}$	131 132 133	+15 V “ “	-10.8 V -12 V -13.2 V	“ “ “	“ “ “	“ “ “	“ “ “	E100 E101 E102	“ “ “	$-P_{SS2}$ = ((E100-E101)/G1)(9.7656E-3)(10) $-P_{SS2}$ = ((E102-E101)/G1)(9.7656E-3)(10)	“ “ “	“ “ “	“ “ “

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
2	L_E	134	+15 V	-15 V	0001 0000 00	1110 1111 1111 1111	None	19	E103	V	For each input code N calculate the	-0.5	+0.5	LSB
T_A =	"	135	"	"	0010 0000 00	1101 1111 1111 1111	"	"	E104	"	corresponding linearity error in LSB.	"	"	"
+125°C	"	136	"	"	0011 0000 00	1100 1111 1111 1111	"	"	E105	"		"	"	"
	"	137	"	"	0100 0000 00	1011 1111 1111 1111	"	"	E106	"		"	"	"
	"	138	"	"	0101 0000 00	1010 1111 1111 1111	"	"	E107	"	$L_E = ((EA/G1)+(N)(K)-(V_{OS}))/(9.7656E-3)$	"	"	"
	"	139	"	"	0110 0000 00	1001 1111 1111 1111	"	"	E108	"		"	"	"
	"	140	"	"	0111 0000 00	1000 1111 1111 1111	"	"	E109	"	where	"	"	"
	"	141	"	"	1000 0000 00	0111 1111 1111 1111	"	"	E110	"	EA = measured value E103 through E123	"	"	"
	"	142	"	"	1001 0000 00	0110 1111 1111 1111	"	"	E111	"	G1 = error amplifier gain from step 111	"	"	"
	"	143	"	"	1010 0000 00	0101 1111 1111 1111	"	"	E112	"	N = DUT input digital code word in	"	"	"
	"	144	"	"	1011 0000 00	0100 1111 1111 1111	"	"	E113	"	decimal form. Thus for 10 bits	"	"	"
	"	145	"	"	1100 0000 00	0011 1111 1111 1111	"	"	E114	"	N = (A1)(2exp7)+(A2)(2exp6)+…	"	"	"
	"	146	"	"	1101 0000 00	0010 1111 1111 1111	"	"	E115	"	+(A10)(2exp0)	"	"	"
	"	147	"	"	1110 0000 00	0001 1111 1111 1111	"	"	E116	"	A1,A2, … A10 are 0 or 1.	"	"	"
	"	148	"	"	1111 0000 00	0000 1111 1111 1111	"	"	E117	"	K = actual volts/count scale factor.	"	"	"
	"	149	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E118	"	$K = (V_{FS} - V_{OS})/1023$	"	"	"
	"	150	"	"	0000 0000 10	1111 1111 0111 1111	"	"	E119	"	where V_{FS} = Value at E89	"	"	"
	"	151	"	"	0000 0001 00	1111 1110 1111 1111	"	"	E120	"	V_{OS} = Value at E90	"	"	"
	"	152	"	"	0000 0010 00	1111 1101 1111 1111	"	"	E121	"		"	"	"
	"	153	"	"	0000 0100 00	1111 1011 1111 1111	"	"	E122	"		"	"	"
	"	154	"	"	0000 1000 00	1111 0111 1111 1111	"	"	E123	"		"	"	"

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			4	5	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
1	MCE1	155	+15 V	-15 V	0111 1111 11	1000 0000 0011 1111	None	19	E124	V	For each set of major carry codes N and	-1	+1	LSB
T_A =			"	"	1000 0000 00	0111 1111 1111 1111	"	"	E125	"	N+1 calculate the associated error in	"	"	"
125°C	MCE2	156	"	"	0011 1111 11	1100 0000 0011 1111	"	"	E126	"	LSB's as follows:	"	"	"
			"	"	0100 0000 00	1011 1111 1111 1111	"	"	E127	"		"	"	"
	MCE3	157	"	"	0001 1111 11	1110 0000 0011 1111	"	"	E128	"	MCE = ((EB-EA)/G1)(9.7656E-3)	"	"	"
			"	"	0010 0000 00	1101 1111 1111 1111	"	"	E129	"		"	"	"
	MCE4	158	"	"	0000 1111 11	1111 0000 0011 1111	"	"	E130	"	where	"	"	"
			"	"	0001 0000 00	1110 1111 1111 1111	"	"	E131	"	EB = Measured value from E124, E126,	"	"	"
	MCE5	159	"	"	0000 0111 11	1111 1000 0011 1111	"	"	E132	"	E128, etc.	"	"	"
			"	"	0000 1000 00	1111 0111 1111 1111	"	"	E133	"	EA = Measured value from E125, E127,	"	"	"
	MCE6	160	"	"	0000 0011 11	1111 1100 0011 1111	"	"	E134	"	E129, etc.	"	"	"
			"	"	0000 0100 00	1111 1011 1111 1111	"	"	E135	"		"	"	"
	MCE7	161	"	"	0000 0001 11	1111 1110 0011 1111	"	"	E136	"		"	"	"
			"	"	0000 0010 00	1111 1101 1111 1111	"	"	E137	"		"	"	"
	MCE8	162	"	"	0000 0000 11	1111 1111 1111 1111	"	"	E138	"		"	"	"
			"	"	0000 0001 00	1111 1110 1111 1111	"	"	E139	"		"	"	"
	MCE9	163	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E140	"		"	"	"
			"	"	0000 0000 10	1111 1111 0111 1111	"	"	E141	"		"	"	"
	MCE10	164	"	"	0000 0000 00	1111 1111 1111 1111	"	"	E142	"		"	"	"
			"	"	0000 0000 01	1111 1111 1011 1111	"	"	E143	"		"	"	"
Calibration		165	Adjust P6 with all bits at 0 V				"	18	E144	µV	Ecal = E144		450	µV

Subgroup	Symbol	Test No.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
3	I_{CC}	166	+15 V	-15	0000 0000 00	1111 1111 1111 1111	None	5	I45	mA	I_{CC} = I45 (Digital 0 = 0 V)	+2	+10	mA
T_A =	I_{EE}	167	"	"	"	"	"	6	I46	mA	I_{EE} = I46 (Digital 0 = 0 V)	-16	-2	mA
-55°C	V_{REF}	168	"	"	"	"	"	2	E145	V	V_{REF} = E145 I_{REF} = 2 mA	2.45	2.55	V

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
3	I_{IL}	169	+15 V	-15 V	0000 0000 00	1111 1111 1111 1111	None	7	I47	µA	I_{IL} = I47 (Digital 0 = 0 V)	-100	+1	µA
T_A =		170	"	"	"	"	"	8	I48	"	I_{IL} = I48	"	"	"
-55°C		171	"	"	"	"	"	9	I49	"	I_{IL} = I49	"	"	"
		172	"	"	"	"	"	10	I50	"	I_{IL} = I50	"	"	"
		173	"	"	"	"	"	11	I51	"	I_{IL} = I51	"	"	"
		174	"	"	"	"	"	12	I52	"	I_{IL} = I52	"	"	"
		175	"	"	"	"	"	13	I53	"	I_{IL} = I53	"	"	"
		176	"	"	"	"	"	14	I54	"	I_{IL} = I54	"	"	"
		177	"	"	"	"	"	15	I55	"	I_{IL} = I55	"	"	"
		178	"	"	"	"	"	16	I56	"	I_{IL} = I56	"	"	"
	I_{IH}	179	"	"	1111 1111 11	"	"	7	I57	"	I_{IH} = I57 (Digital 1 = 15 V)	-1	100	"
		180	"	"	"	"	"	8	I58	"	I_{IH} = I58	"	"	"
		181	"	"	"	"	"	9	I59	"	I_{IH} = I59	"	"	"
		182	"	"	"	"	"	10	I60	"	I_{IH} = I60	"	"	"
		183	"	"	"	"	"	11	I61	"	I_{IH} = I61	"	"	"
		184	"	"	"	"	"	12	I62	"	I_{IH} = I62	"	"	"
		185	"	"	"	"	"	13	I63	"	I_{IH} = I63	"	"	"
		186	"	"	"	"	"	14	I64	"	I_{IH} = I64	"	"	"
		187	"	"	"	"	"	15	I65	"	I_{IH} = I65	"	"	"
		188	"	"	"	"	"	16	I66	"	I_{IH} = I66	"	"	"
	I_{FS1}	189	+5 V	"	"		"	18	E146	V	I_{FS1} = E146/1000	+1.5	+2.5	mA
	I_{FS2}	190	+15 V	"	"		"	"	E147	"	I_{FS2} = E147/1000	"	"	
	G1	191	"	"	0000 0000 00	1111 1111 1111 1111	"	21	E148	"	G_1 = (E149-E148)(4096)/(14)(10)	-41.5	-40.5	V/V
		192	"	"	"	1111 1111 0001 1111	"	"	E149	"	G_1 is the error amplifier gain			
	I_{FS+}	193	"	"	1111 1111 11	0000 0000 0000 0000	K1	18	E150	"	I_{FS+} = E150/1000	+1.5	+2.5	mA
	I_{FS-}	194	"	"	"	"	"	"	E151	"	I_{FS-} = E151/1000	"	"	"
	$d_{IFS(+)}$	195	"	"	"		None	"	E152	"	V_{OC} = 0 V	-5	+5	µA
		196	"	"	"		"	"	E153	"	V_{OC} = +10 V $d_{IFS(+)}$ = (E153-E152)/1000	"	"	"
	$d_{IFS(-)}$	197	"	"	"		"	"	E154	"	V_{OC} = 0 V	"	"	"
		198	"	"	"		"	"	E155	"	V_{OC} = -2 V $d_{IFS(-)}$ = (E155-E154)/1000	"	"	"
	d_{IZS2}/dt	199	+15 V	"	0000 0000 00	1111 1111 1111 1111	K1	"	E156	"	d_{IZS2}/dt = (E156-E14)(1024)/(E147-E4)(80)	-10	+10	mLSB /°C
	d_{BPOE}/dt	200	"	"	"	"	"	19	E157	"	d_{BPOE}/dt =(E157-E15)/(G1)(9.7656E-3)(80)	-60	+60	"
	d_{BZE}/dt	201	"	"	1000 0000 00	1111 1111 1111 1111	K1	19	E158	"	d_{BZE}/dt = (E158-E16)/(G1)(9.7656E-3)(80)	-20	+20	"
	d_{AE2}/dt	202	"	"	1111 1111 11 0000 0000 00	0000 0000 0011 1111 1111 1111 1111 1111	None	21	E159 E160	"	d_{AE2}/dt=0.125(E159-E160)-(E19-E20)/(G1)	-0.006	+0.006	%/°C

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			5	6	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
3	$+P_{SS1}$	203	+4.5 V	-15 V	1111 1111 11	0000 0000 0011 1111	None	19	E161	V	$+P_{SS1}$ = ((E161-E162)/G1)(9.7656E-3)(10)	-0.02	+0.02	LSB
T_A =		204	+5.0 V	"	"	"	"	"	E162	"		"	"	/%PS
-55°C	$-P_{SS1}$	205	+5.5 V	"	"	"	"	"	E163	"	$-P_{SS1}$ = ((E163-E162)/G1)(9.7656E-3)(10)	"	"	"
	$+P_{SS2}$	206	+13.5 V	"	"	"	"	"	E164	"	$+P_{SS2}$ = ((E164-E165)/G1)(9.7656E-3)(10)	"	"	"
		207	+15 V	"	"	"	"	"	E165	"		"	"	"
	$-P_{SS2}$	208	+16.5 V	"	"	"	"	"	E166	"	$+P_{SS2}$ = ((E166-E165)/G1)(9.7656E-3)(10)	"	"	"
	$-P_{SS1}$	209	+5 V	-13.5 V	"	"	"	"	E167	"	$-P_{SS1}$ = ((E167-E168)/G1)(9.7656E-3)(10)	-0.05	+0.05	"
		210	"	-15 V	"	"	"	"	E168	"		"	"	"
		211	"	-16.5 V	"	"	"	"	E169	"	$-P_{SS1}$ = ((E169-E168)/G1)(9.7656E-3)(10)	"	"	"
	$-P_{SS2}$	212	+15 V	-10.8 V	"	"	"	"	E170	"	$-P_{SS2}$ = ((E170-E171)/G1)(9.7656E-3)(10)	"	"	"
		213	"	-12 V	"	"	"	"	E171	"		"	"	"
		214	"	-13.2 V	"	"	"	"	E172	"	$-P_{SS2}$ = ((E172-E171)/G1)(9.7656E-3)(10)	"	"	"
	L_E	215	"	-15 V	0001 0000 00	1110 1111 1111 1111	"	"	E173	"	For each input code N calculate the	-0.5	+0.5	LSB
	"	216	"	"	0010 0000 00	1101 1111 1111 1111	"	"	E174	"	corresponding linearity error in LSB.	"	"	"
	"	217	"	"	0011 0000 00	1100 1111 1111 1111	"	"	E175	"		"	"	"
	"	218	"	"	0100 0000 00	1011 1111 1111 1111	"	"	E176	"		"	"	"
	"	219	"	"	0101 0000 00	1010 1111 1111 1111	"	"	E177	"	L_E = ((EA/G1)+(N)(K)-(V_{OS}))/(9.7656E-3)	"	"	"
	"	220	"	"	0110 0000 00	1001 1111 1111 1111	"	"	E178	"		"	"	"
	"	221	"	"	0111 0000 00	1000 1111 1111 1111	"	"	E179	"	where	"	"	"
	"	222	"	"	1000 0000 00	0111 1111 1111 1111	"	"	E180	"	EA = measured value E173 through E193	"	"	"
	"	223	"	"	1001 0000 00	0110 1111 1111 1111	"	"	E181	"	G1 = error amplifier gain from step 192	"	"	"
	"	224	"	"	1010 0000 00	0101 1111 1111 1111	"	"	E182	"	N = DUT input digital code word in	"	"	"
	"	225	"	"	1011 0000 00	0100 1111 1111 1111	"	"	E183	"	decimal form. Thus for 10 bits	"	"	"
	"	226	"	"	1100 0000 00	0011 1111 1111 1111	"	"	E184	"	N = (A1)(2exp7)+(A2)(2exp6)+…	"	"	"
	"	227	"	"	1101 0000 00	0010 1111 1111 1111	"	"	E185	"	+(A10)(2exp0)	"	"	"
	"	228	"	"	1110 0000 00	0001 1111 1111 1111	"	"	E186	"	A1,A2, … A10 are 0 or 1.	"	"	"
	"	229	"	"	1111 0000 00	0000 1111 1111 1111	"	"	E187	"	K = actual volts/count scale factor.	"	"	"
	"	230	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E188	"	K = (V_{FS} – V_{OS})/1023	"	"	"
	"	231	"	"	0000 0000 10	1111 1111 0111 1111	"	"	E189	"	where V_{FS} = Value at E159	"	"	"
	"	232	"	"	0000 0001 00	1111 1110 1111 1111	"	"	E190	"	V_{OS} = Value at E160	"	"	"
	"	233	"	"	0000 0010 00	1111 1101 1111 1111	"	"	E191	"		"	"	"
	"	234	"	"	0000 0100 00	1111 1011 1111 1111	"	"	E192	"		"	"	"
	"	235	"	"	0000 1000 00	1111 0111 1111 1111	"	"	E193	"		"	"	"

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			4	5	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
3	MCE1	236	+15 V	-15 V	0111 1111 11	1000 0000 0011 1111	None	19	E194	V	For each set of major carry codes N and	-1	+1	LSB
T_A= -55°C			"	"	1000 0000 00	0111 1111 1111 1111	"	"	E195	"	N+1 calculate the associated error in	"	"	"
	MCE2	237	"	"	0011 1111 11	1100 0000 0011 1111	"	"	E196	"	LSB's as follows:	"	"	"
			"	"	0100 0000 00	1011 1111 1111 1111	"	"	E197	"		"	"	"
	MCE3	238	"	"	0001 1111 11	1110 0000 0011 1111	"	"	E198	"	MCE = ((EB-EA)/G1)(9.7656E-3)	"	"	"
			"	"	0010 0000 00	1101 1111 1111 1111	"	"	E199	"		"	"	"
	MCE4	239	"	"	0000 1111 11	1111 0000 0011 1111	"	"	E200	"	where	"	"	"
			"	"	0001 0000 00	1110 1111 1111 1111	"	"	E201	"	EB = Measured value from E194, E196,	"	"	"
	MCE5	240	"	"	0000 0111 11	1111 1000 0011 1111	"	"	E202	"	E198, etc.	"	"	"
			"	"	0000 1000 00	1111 0111 1111 1111	"	"	E203	"	EA = Measured value from E195, E197,	"	"	"
	MCE6	241	"	"	0000 0011 11	1111 1100 0011 1111	"	"	E204	"	E199, etc.	"	"	"
			"	"	0000 0100 00	1111 1011 1111 1111	"	"	E205	"		"	"	"
	MCE7	242	"	"	0000 0001 11	1111 1110 0011 1111	"	"	E206	"		"	"	"
			"	"	0000 0010 00	1111 1101 1111 1111	"	"	E207	"		"	"	"
	MCE8	243	"	"	0000 0000 11	1111 1111 1111 1111	"	"	E208	"		"	"	"
			"	"	0000 0001 00	1111 1110 1111 1111	"	"	E209	"		"	"	"
	MCE9	244	"	"	0000 0000 01	1111 1111 1011 1111	"	"	E210	"		"	"	"
			"	"	0000 0000 10	1111 1111 0111 1111	"	"	E211	"		"	"	"
	MCE10	245	"	"	0000 0000 00	1111 1111 1111 1111	"	"	E212	"		"	"	"
			"	"	0000 0000 01	1111 1111 1011 1111	"	"	E213	"		"	"	"

TABLE III. Group A inspection – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers				Relays energized	Measured pin			Equation	Limits		Unit
			4	5	7 thru 16	22 thru 37		No.	Value	Unit		Min	Max	
7	L_E	246	+15 V	-15 V	0000 0000 01	1111 1111 1011 1111	None	19	E414	V	For each input code N calculate the			
T_A= 25°C	"	247	"	"	0010 0000 10	1111 1111 0111 1111	"	"	E415	"	corresponding linearity error in LSB.			
	"		"	"	0000 0001 00	1111 1110 1111 1111								
	"		"	"	---- ---- --	---- ---- ---- ----								
	"		"	"	---- ---- --	---- ---- ---- ----					$L_E = 10((EA/G1)+(N)(K)-(V_{OS}))$			
	"		"	"	1111 1111 00	0000 0000 1111 1111								
	"		"	"	1111 1111 01	0000 0000 1011 1111					where			
	"		"	"	1111 1111 10	0000 0000 0111 1111					EA = measured value E414 through E1429			
					This subgroup checks all digital input codes, except zero code (V_{OS}) and full-scale code (V_{FS}) which were Determined in test no. 40.						G1 = error amplifier gain from step 27, 28			
											N = DUT input digital code word in decimal form. Thus for 10 bits N = (A1)(2exp7)+(A2)(2exp6)+… +(A10)(2exp0)			
					V_{OS} = E20						A1,A2, … A10 are 0 or 1.			
					V_{FS} = E19						K = actual volts/count scale factor.			
											K = (E20-E19)/1023			
											Worst positive error		0.5	LSB
											Worst positive code			OCT
											Worst negative error	-0.5		LSB
											Worst negative code			OCT
8 T_A= 125°C	L_E	248 249	Same tests, terminal conditions, and limits as for subgroup 7, tests 246 thru 247 except T_A = 125°C. V_{OS} and V_{FS} are the values determined in subgroup 2.									-0.5	+0.5	LSB OCT LSB OCT
8 T_A= -55°C	L_E	250 251	Same tests, terminal conditions, and limits as for subgroup 7, tests 246 thru 247 except T_A = -55°C. V_{OS} and V_{FS} are the values determined in subgroup 3.									-0.5	+0.5	LSB OCT LSB OCT
12 T_A= 25°C	t_{SLH}	252	All digital inputs switched simultaneously from logic low to logic high. For each device type output settling is to within ½ LSB of the rated accuracy. See figures 3 and 4.					6	t1	ns	t_{SLH} = t1		500	ns
	t_{SHL}	253	All digital inputs switched simultaneously from logic high to logic low. For each device type output settling is to within ½ LSB of the rated accuracy. See figures 3 and 4.					6	t2	ns	t_{SHL} = t2		500	ns
	N_O	254	V_{CC} = +5 V; V_{EE} = -15 V All digital inputs = +2.2 V See figure 5.					6	E416	µV rms	N_O = E416/100		160	µV rms

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

Table IV. Group C end-point electrical parameters. T_A = 25°C

Parameter	Min	Max	Unit
I_{ZS2}	-0.1	+0.1	LSB
A_{E2}	-0.1	+0.1	%
B_{POE}	-1.0	+1.0	LSB

4.5 Methods of inspection. Methods of inspection shall be as specified and as follows:

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminals. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for “JAN” marking.

j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:.

DLE	Differential linearity error is the difference between the actual separation of two adjacent output levels and the ideal separation of two adjacent output levels. It is generally expressed in LSB (i.e. 1 LSB).
MCE	The major carry error is the differential linearity error between the output levels corresponding to the digital code word defined by turning one bit on and all other bits off and the preceding adjacent digital code word. It is expressed in LSB.
CMOS	Complementary metal oxide semiconductor.
V_{CC}	Positive supply voltage (usually +15 V).
V_{EE}	Negative supply voltage (usually –15 V).
GND	Ground zero growth potential.
V_{IL}	Digital low state input voltage.
V_{IH}	Digital high state input voltage.
MSB	Most significant digital input bit.
BIT1	Same as MSB = full-scale/2.
BIT2	Second most significant bit = full-scale/4.
LSB	Least significant bit = full-scale/2 expN.
BITN	Same as LSB for an N-bit converter.
I_{OUT}	Sum of all R-2R ladder currents going through VIH command switches.
RF	Feedback resistor for an external op amp.
I_{CC}	Current supplied to the V_{CC} terminal of the DUT for a given supply voltage (usually +15 V).
I_{EE}	Current supplied to the V_{EE} terminal of the DUT for a given supply voltage (usually -15 V).

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	561

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army – CR
Navy - EC
Air Force - 11
NASA – NA
DLA – CC

Preparing activity:
DLA - CC

Project 5962-2046

Review activities:
Army – MI, SM
Navy – AS, CG, MC, SH, TD
Air Force – 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at www.dodssp.daps.mil.