

INCH-POUND
MIL-M-38510/109B
28 May 2004
SUPERSEDING
MIL-M-38510/109A
18 September 1980

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, PRECISION TIMERS, MONOLITHIC SILICON

Reactivated after 28 May 2004 and may be used for either new or existing design acquisitions.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, precision timers. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3)

1.2 Part or identifying number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are internally compensated and are as follows:

<u>Device type</u>	<u>Circuit</u>
01 ^{1/}	Precision timer
02	Precision timer, dual
03	Precision timer (I _{SOURCE} = -60 mA)

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

^{1/} Warning: Device type 01 in the glass frit sealed C and P packages does not pass the requirement of glassivation layer integrity test, MIL-STD-883, test method 2021, as specified in MIL-PRF-38535. Therefore, the glassivation layer integrity test is waived for device type 01 in the glass frit sealed C and P packages only. Operation of the 01 device in these packages types in the high level output voltage mode, may result in device reliability problems.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43216-5000, or emailed to linear@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

1.3 Absolute maximum ratings.

Positive supply voltage.....	+18 V dc
Discharge current	+200 mA
Output sink current	+200 mA
Output source current:	
Device types 01 and 02	-200 mA
Device type 03	-60 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60 seconds)	+300°C.
Junction temperature (T _J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range:	
Device types 01 and 03	+4.5 V dc to +16.5 V dc
Device type 02	+5.0 V dc to +15.0 V dc ^{2/}
Case operating temperature range	-55°C to +125°C

1.5 Power and thermal characteristics.

Case outlines	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
C	400 mW at T _A = +125°C	45°C/W	120°C/W
G	300 mW at T _A = +125°C	40°C/W	150°C/W
P	370 mW at T _A = +125°C	45°C/W	135°C/W
2	330 mW at T _A = +125°C	55°C/W	121°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

^{2/} Supply voltage upper limit due to excessive junction temperature at T_A = +125°C.

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

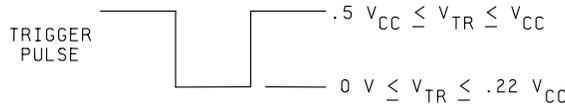
3.3.3 Block diagram and circuit operation table. The block diagram and circuit operation table shall be as specified on figure 2.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The following electrical performance characteristics apply over the full operating ambient temperature range of -55°C to $+125^{\circ}\text{C}$ and for supply voltages of +4.5 V dc to +16.5 V dc for device types 01 and 03, and +5.0 V dc to +15.0 V dc for device type 02, unless otherwise specified (see table I). See figure 2 for circuit operation table.

3.5.1 Triggering. In the monostable mode, the device is triggered on the negative slope of a trigger pulse. The trigger pulse must be of shorter duration than the "RC" time interval. The minimum pulse width is 1 microsecond (s).



3.5.2 Reset. In the monostable mode, the device may be reset (from V_{OH} to V_{OL}) on the negative slope of a reset pulse. Once the reset is returned high, the output will remain low only if the trigger is high. If the trigger is low when reset is returned high, the output will go high. The minimum reset pulse width is 2 μs .

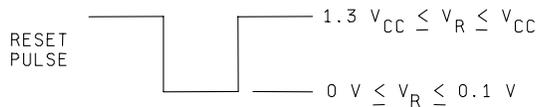


TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits <u>1/</u>		Unit
				Min	Max	
Power supply current	I _{CC}	V _{CC} = 4.5 V dc, R _L = ∞	01, 03		5.0	mA
		V _{CC} = 5.0 V dc, R _L = ∞	02		10.0	
		V _{CC} = 16.5 V dc, R _L = ∞	01, 03		20.0	
		V _{CC} = 15.0 V dc, R _L = ∞	02		30.0	
Trigger voltage	V _{TR}	V _{CC} = 4.5 V dc, T _A = +25°C	01,03	1.30	1.80	V
		V _{CC} = 5.0 V dc, T _A = +25°C	02	1.45	1.95	
		V _{CC} = 4.5 V dc, T _A = +125°C	01,03	1.30	2.10	
		V _{CC} = 5.0 V dc, T _A = +125°C	02	1.45	2.25	
		V _{CC} = 4.5 V dc, T _A = -55°C	01,03	1.15	1.80	
		V _{CC} = 5.0 V dc, T _A = -55°C	02	1.30	1.95	
		V _{CC} = 16.5 V dc, T _A = +25°C	01,03	5.20	5.80	
		V _{CC} = 15.0 V dc, T _A = +25°C	02	4.70	5.30	
		V _{CC} = 16.5 V dc, T _A = +125°C	01,03	5.20	6.10	
		V _{CC} = 15.0 V dc, T _A = +125°C	02	4.70	5.60	
		V _{CC} = 16.5 V dc, T _A = -55°C	01,03	5.00	5.80	
		V _{CC} = 15.0 V dc, T _A = -55°C	02	4.50	5.30	
Trigger current	I _{TR}	V _{CC} = 16.5 V dc for V _{TR} = 5.0 V	01,03	-5.0		μA
		V _{CC} = 15.0 V dc for V _{TR} = 4.5 V	02	-5.0		
Threshold voltage	V _{TH}	V _{CC} = 4.5 V dc, T _A = +25°C	01,03	2.70	3.30	V
		V _{CC} = 5.0 V dc, T _A = +25°C	02	3.05	3.65	
		V _{CC} = 4.5 V dc, -55°C ≤ T _A ≤ +125°C	01,03	2.60	3.40	
		V _{CC} = 5.0 V dc, -55°C ≤ T _A ≤ +125°C	02	2.95	3.75	
		V _{CC} = 16.5 V dc, T _A = +25°C	01,03	10.70	11.30	
		V _{CC} = 15.0 V dc, T _A = +25°C	02	9.70	10.30	
		V _{CC} = 16.5 V dc, -55°C ≤ T _A ≤ +125°C	01,03	10.60	11.40	
		V _{CC} = 15.0 V dc, -55°C ≤ T _A ≤ +125°C	02	9.60	10.40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits ^{1/}		Unit
				Min	Max	
Threshold current	I _{TH}	V _{CC} = 16.5 V dc, +25°C ≤ T _A ≤ +125°C	01,03		250	nA
		V _{CC} = 15.0 V dc, +25°C ≤ T _A ≤ +125°C	02		250	
		V _{CC} = 16.5 V dc, T _A = -55°C	01,03		2.5	μA
		V _{CC} = 15.0 V dc, T _A = -55°C	02		2.5	
Low level output voltage	V _{OL}	V _{CC} = 4.5 V dc, I _{SINK} = 5 mA, T _A = +25°C	01,03		.250	V
		V _{CC} = 5.0 V dc, I _{SINK} = 5 mA, T _A = +25°C	02		.250	
		V _{CC} = 4.5 V dc, I _{SINK} = 5 mA, T _A = -55°C, T _A = +125°C	01,03		.350	
		V _{CC} = 5.0 V dc, I _{SINK} = 5 mA, T _A = -55°C, T _A = +125°C	02		.350	
		V _{CC} = 4.5 V dc, I _{SINK} = 50 mA, +25°C ≤ T _A ≤ +125°C	01,03		2.20	
		V _{CC} = 5.0 V dc, I _{SINK} = 50 mA, +25°C ≤ T _A ≤ +125°C	02		2.20	
		V _{CC} = 4.5 V dc, I _{SINK} = 50 mA, T _A = -55°C	01,03		2.60	
		V _{CC} = 5.0 V dc, I _{SINK} = 50 mA, T _A = -55°C	02		2.60	
		V _{CC} = 16.5 V dc, I _{SINK} = 10 mA, -55°C ≤ T _A ≤ +25°C	01,03		.150	
		V _{CC} = 15.0 V dc, I _{SINK} = 10 mA, -55°C ≤ T _A ≤ +25°C	02		.150	
		V _{CC} = 16.5 V dc, I _{SINK} = 10 mA, T _A = +125°C	01,03		.250	
		V _{CC} = 15.0 V dc, I _{SINK} = 10 mA, T _A = +125°C	02		.250	
		V _{CC} = 16.5 V dc, I _{SINK} = 50 mA, -55°C ≤ T _A ≤ +25°C	01,03		.500	
		V _{CC} = 15.0 V dc, I _{SINK} = 50 mA, -55°C ≤ T _A ≤ +25°C	02		.500	
		V _{CC} = 16.5 V dc, I _{SINK} = 50 mA, T _A = +125°C	01,03		.700	
		V _{CC} = 15.0 V dc, I _{SINK} = 50 mA, T _A = +125°C	02		.700	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits <u>1/</u>		Unit
				Min	Max	
Low level output voltage	V _{OL}	V _{CC} = 16.5 V dc, T _A = +25°C I _{SINK} = 100 mA	01,03		2.20	V
		V _{CC} = 15.0 V dc, T _A = +25°C I _{SINK} = 100 mA	02		2.20	
		V _{CC} = 16.5 V dc, I _{SINK} = 100 mA, T _A = -55°C, T _A = +125°C	01,03		2.80	
		V _{CC} = 15.0 V dc, I _{SINK} = 100 mA, T _A = -55°C, T _A = +125°C	02		2.80	
High level output voltage	V _{OH}	V _{CC} = 4.5 V dc, I _{SOURCE} = -100 mA, <u>6/</u> +25°C ≤ T _A ≤ +125°C	01,03	2.60		V
		V _{CC} = 5.0 V dc, I _{SOURCE} = -100 mA, <u>6/</u> +25°C ≤ T _A ≤ +125°C	02	3.10		
		V _{CC} = 4.5 V dc, T _A = -55°C, <u>6/</u> I _{SOURCE} = -100 mA	01,03	2.20		
		V _{CC} = 5.0 V dc, T _A = -55°C, <u>6/</u> I _{SOURCE} = -100 mA	02	2.70		
		V _{CC} = 16.5 V dc, I _{SOURCE} = -100 mA, <u>6/</u> +25°C ≤ T _A ≤ +125°C	01,03	14.6		
		V _{CC} = 15.0 V dc, I _{SOURCE} = -100 mA, <u>6/</u> +25°C ≤ T _A ≤ +125°C	02	13.1		
		V _{CC} = 16.5 V dc, T _A = -55°C, <u>6/</u> I _{SOURCE} = -100 mA	01,03	14.0		
		V _{CC} = 15.0 V dc, T _A = -55°C, <u>6/</u> I _{SOURCE} = -100 mA	02	12.5		
Discharge transistor leakage current	I _{C_{EX}}	V _{CC} = 16.5 V dc, -55°C ≤ T _A ≤ +25°C	01,03		100	nA
		V _{CC} = 15.0 V dc, -55°C ≤ T _A ≤ +25°C	02		100	
		V _{CC} = 16.5 V dc, T _A = +125°C	01,03		3.0	μA
		V _{CC} = 15.0 V dc, T _A = +125°C	02		3.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits <u>1/</u>		Unit
				Min	Max	
Discharge transistor saturation voltage	V _{SAT}	V _{CC} = 16.5 V dc, I _D = 50 mA, -55°C ≤ T _A ≤ +25°C	01,03		0.80	V
		V _{CC} = 15.0 V dc, I _D = 50 mA, -55°C ≤ T _A ≤ +25°C	02		0.80	
		V _{CC} = 16.5 V dc, I _D = 50 mA, T _A = +125°C	01,03		1.00	
		V _{CC} = 15.0 V dc, I _D = 50 mA, T _A = +125°C	02		1.00	
Reset voltage	V _R	V _{CC} = 16.5 V dc, see figure 7	01,03	0.1	1.3	V
		V _{CC} = 15.0 V dc, see figure 7	02	0.1	1.3	
Reset current	I _R	V _{CC} = 16.5 V dc, V _R = 0 V dc	01,03	-1.60	0	mA
		V _{CC} = 15.0 V dc, V _R = 0 V dc	02	-1.60	0	
Propagation delay time, low to high level output (monostable)	t _{PLH}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4, -55°C ≤ T _A ≤ +25°C	01,03		800	ns
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4, -55°C ≤ T _A ≤ +25°C	02		800	
		4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4, T _A = +125°C	01,03		900	
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4, T _A = +125°C	02		900	
Transition time, low to high level output (monostable)	t _{TLH}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	01,03		300	ns
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	02		300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits ^{1/}		Unit
				Min	Max	
Transition time, high to low level output (monostable)	t _{THL}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	01,03		300	ns
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	02		300	
Time delay, output high (monostable)	t _{D(OH)}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	01,03	106.7	113.3	μs
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	02	106.7	113.3	
		4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 100 kΩ, C _T = 0.1 μF, see figure 4	01,03	10.67	11.33	ms
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 100 kΩ, C _T = 0.1 μF, see figure 4	02	10.67	11.33	
Drift in time delay versus change in supply voltage (monostable)	Δt _{D(OH)} / ΔV _{CC}	ΔV _{CC} = 12 V dc, R _T = 1 kΩ, C _T = 0.1 μF, T _A = +25°C, see figure 4	01,03	-220	220	ns/V
		ΔV _{CC} = 10 V dc, R _T = 1 kΩ, C _T = 0.1 μF, T _A = +25°C, see figure 4	02	-220	220	
Propagation delay time, threshold to output	t _{PHL}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _T = 1 kΩ, see figure 5	01,03		12.0	μs
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _T = 1 kΩ, see figure 5	02		12.0	
Temperature coefficient of time delay (monostable)	Δt _{D(OH)} / ΔT	V _{CC} = 16.5 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	01,03	-11	11	ns/°C
		V _{CC} = 15.0 V dc, R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	02	-11	11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits <u>1/</u>		Unit
				Min	Max	
Capacitor charge time (astable)	t _{ch}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	01,03	120	156	μs
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	02	120	156	
		4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _{TA} = R _{TB} = 100 kΩ, C _T = 0.1 μF, see figure 6	01,03	11.3	15.0	ms
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _{TA} = R _{TB} = 100 kΩ, C _T = 0.1 μF, see figure 6	02	11.3	15.0	
Capacitor discharge time (astable)	t _{dis}	4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	01,03	57.5	80	μs
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	02	57.5	80	
		4.5 V dc ≤ V _{CC} ≤ 16.5 V dc, R _{TA} = R _{TB} = 100 kΩ, C _T = 0.1 μF, see figure 6	01,03	5.4	7.7	ms
		5.0 V dc ≤ V _{CC} ≤ 15.0 V dc, R _{TA} = R _{TB} = 100 kΩ, C _T = 0.1 μF, see figure 6	02	5.4	7.7	
Drift in capacitor charge time versus change in supply voltage (astable)	Δt _{ch} / ΔV _{CC}	ΔV _{CC} = 12 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6, T _A = +25°C	01,03	-820	820	ns/V
		ΔV _{CC} = 10 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6, T _A = +25°C	02	-820	820	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified see figure 3	Device type	Limits <u>1/</u>		Unit
				Min	Max	
Temperature coefficient of capacitor charge time (astable)	t _{ch} / ΔT	V _{CC} = 16.5 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	01,03	-68	68	ns / °C
		V _{CC} = 15.0 V dc, R _{TA} = R _{TB} = 1 kΩ, C _T = 0.1 μF, see figure 6	02	-68	68	
Reset time	t _{res}	V _{CC} = 16.5 V dc, see figure 7, -55°C ≤ T _A ≤ +25°C	01,03		1.5	μs
		V _{CC} = 15.0 V dc, see figure 7, -55°C ≤ T _A ≤ +25°C	02		1.5	
		V _{CC} = 16.5 V dc, see figure 7, T _A = +125°C	01,03		2	
		V _{CC} = 15.0 V dc, see figure 7, T _A = +125°C	02		2	
Matching, time delay, output high (monostable)	Δt _{D(OH)M} <u>3/</u>	5 V dc ≤ V _{CC} ≤ 15 V dc, <u>2/</u> R _T = 1 kΩ, C _T = 0.1 μF, T _A = +25°C, see figure 4	02	-1.1	+1.1	μs
Matching, temperature coefficient of time delay (monostable)	Δt _{D(OH)M} / ΔT <u>4/</u>	V _{CC} = 15 V dc, <u>2/</u> R _T = 1 kΩ, C _T = 0.1 μF, see figure 4	02	-20	+20	ns/°C
Matching, drift in time delay versus supply voltage (monostable)	Δt _{D(OH)M} / ΔV _{CC} <u>5/</u>	ΔV _{CC} = 10 V dc, <u>2/</u> R _T = 1 kΩ, C _T = 0.1 μF, T _A = +25°C, see figure 4	02	-110	+110	ns/V

1/ Limits apply to both device types unless otherwise specified. Each side of device type 02 shall be tested separately.

2/ Device type 02 only – matching between side “A” and side “B”.

3/ Δt_{D(OH)M} = Δt_{D(OH)} side “A” - Δt_{D(OH)} side “B”.

4/ Δt_{D(OH)M} / ΔT = Δt_{D(OH)} / ΔT side “A” - Δt_{D(OH)} / ΔT side “B”.

5/ Δt_{D(OH)M} / ΔV_{CC} = Δt_{D(OH)} / ΔV_{CC} side “A” - Δt_{D(OH)} / ΔV_{CC} side “B”.

6/ I_{SOURCE} for device type 03 = -60 mA.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 9	1*, 2, 3, (9 <u>1/</u>)
Group A test requirements	1, 2, 3, 9, 10, 11	1, 2, 3, 9, (10, 11 <u>2/</u>)
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3 and table IV delta limits <u>4/</u>	N/A
Group C end-point electrical parameters	1, 2, 3 and table IV delta limits <u>4/</u>	1 and table IV delta limits
Additional electrical subgroups for Group C periodic inspections	N/A	(10, 11 <u>3/</u>)
Group D end-point electrical parameters	1, 2, 3	1

* PDA applies to subgroup 1.

1/ For subgroup 9, the following tests are not required: 58 through 65, and 83.

2/ For subgroups 10 and 11, the following tests are not required: 96, 105, 106, 120, 129, and 130.

3/ For subgroups 10 and 11, tests 96, 105, 106, 120, 129, and 130 shall be performed.

4/ At the manufacturer's option and with sufficient data and TRB approval, Table IV delta limits may be omitted for class S devices.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 54 (see MIL-PRF-38535, appendix A).

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. Special subgroups shall be added to the group C inspection and shall consist of group A, subgroups 10 and 11 as specified in table III herein.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test cooldown procedure. When devices are measured at +25°C following application of the operating life or burn-in test condition, they shall be cooled within +10°C of their power stable condition (at room temperature) prior to removal of the bias.

Device types	01, 03	02 (See note)	01, 03	01, 03	01
Case outlines	C	C	G	P	2
Terminal number	Terminal symbol				
1	GND	DISCHARGE A	GROUND	GND	NC
2	NC	THRESHOLD A	TRIGGER	TRIGGER	GND
3	TRIGGER	CONTROL VOLTAGE A	OUTPUT	OUTPUT	NC
4	OUTPUT	RESET A	RESET	RESET	NC
5	NC	OUTPUT A	CONTROL VOLTAGE	CONTROL VOLTAGE	TRIGGER
6	RESET	TRIGGER A	THRESHOLD	THRESHOLD	NC
7	NC	GROUND	DISCHARGE	DISCHARGE	OUTPUT
8	CONTROL VOLTAGE	TRIGGER B	V _{CC}	V _{CC}	NC
9	NC	OUTPUT B	---	---	NC
10	THRESHOLD	RESET B	---	---	RESET
11	NC	CONTROL VOLTAGE B	---	---	NC
12	DISCHARGE	THRESHOLD B	---	---	CONTROL VOLTAGE
13	NC	DISCHARGE B	---	---	NC
14	V _{CC}	V _{CC}	---	---	NC
15	---	---	---	---	THRESHOLD
16	---	---	---	---	NC
17	---	---	---	---	DISCHARGE
18	---	---	---	---	NC
19	---	---	---	---	NC
20	---	---	---	---	V _{CC}

NOTE : V_{CC} and GROUND are common to both sides.

Figure 1. Terminal connections.

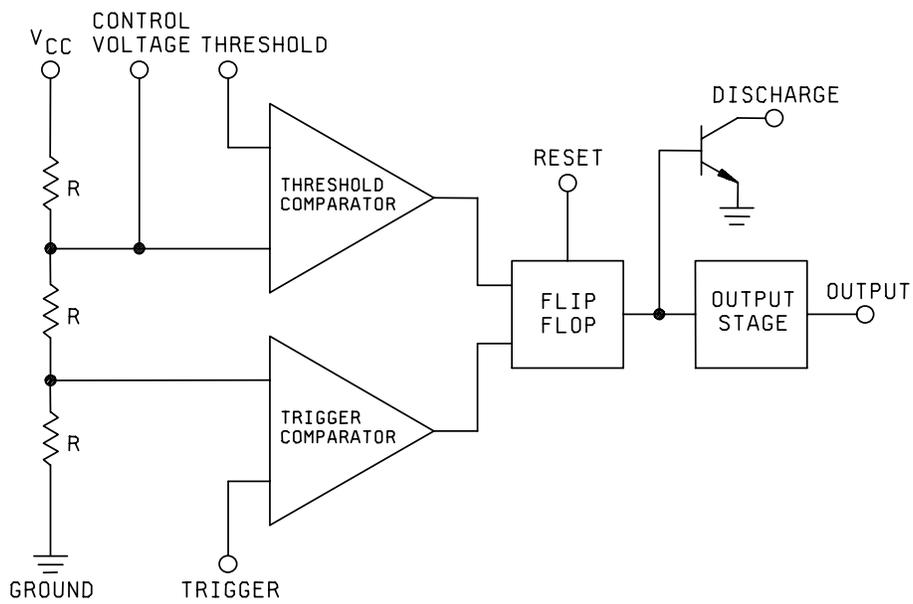


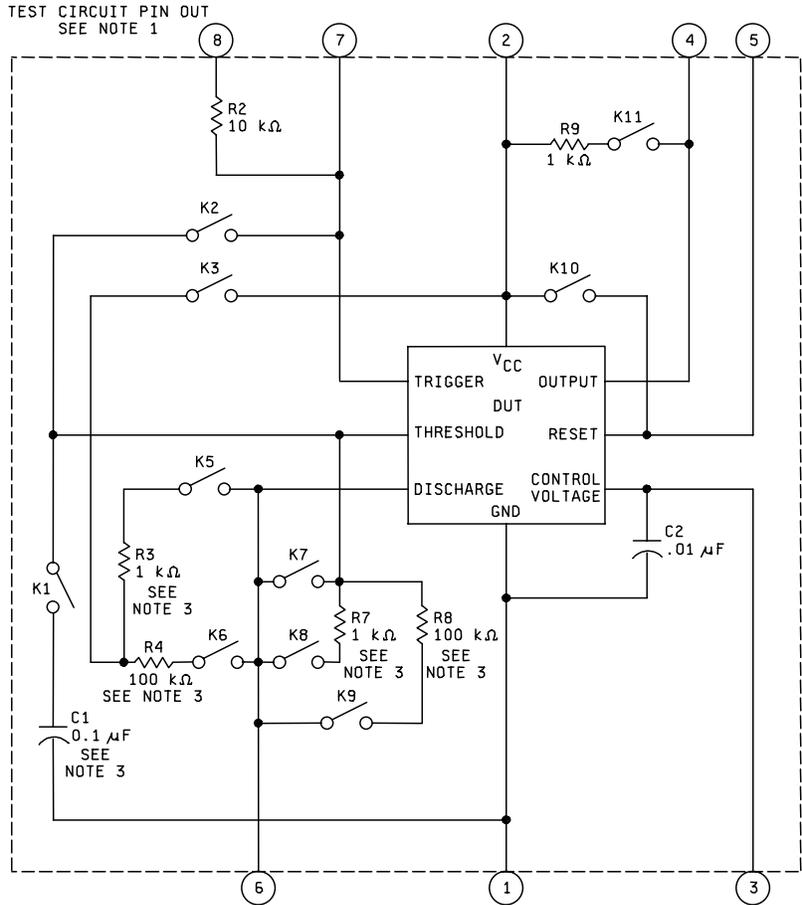
FIGURE 2. Block diagram and circuit operation table.

INPUTS			OUTPUT
RESET	THRESHOLD	TRIGGER	
	0	1	RESETS ()
	1	1	0
	0	0	
	1	0	
1		1	RESETS
1		0	1
0		1	0
0		0	0
1	0		SETS ()
1	1		(SEE NOTE 1)
0	0		0
0	1		0

NOTES:

1. Some devices latch high for $V_{CC} < 10$ V dc.
2. Discharge transistor follows the output as follows:
 Output high = Discharge transistor OFF
 Output low = Discharge transistor ON

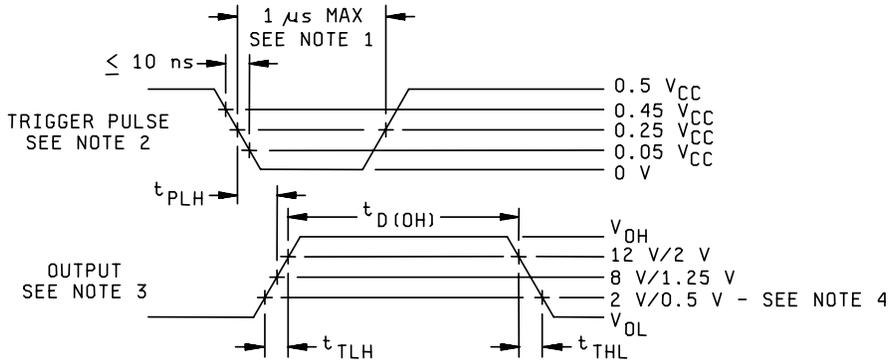
FIGURE 2. Block diagram and circuit operation table – Continued.



NOTES:

1. Test circuit pin conditions and test temperatures shall be as specified in table III.
2. Precautions shall be taken to prevent damage to the device under test during insertion into the socket and during changing of relay switching positions (example: disable voltage/current supplies, current limit, $\pm V_{CC}$, etc...).
3. These resistors and capacitor are 0.1% tolerance. The remainder of resistors and capacitors are 10% tolerance.

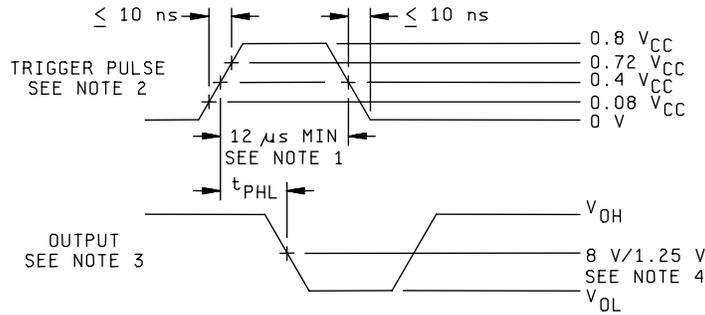
FIGURE 3. Test circuit pin out.



Notes:

1. This limit applies only during tests for t_{PLH} , t_{TLH} , and t_{THL} .
2. The pulse is applied to pin 7 of the test adapter.
3. This measurement shall be made on pin 4 of the test adapter.
4. A/B means value "A" for $V_{CC} = 15 \text{ V}$ or 16.5 V and "B" for $V_{CC} = 4.5 \text{ V}$ or 5 V .

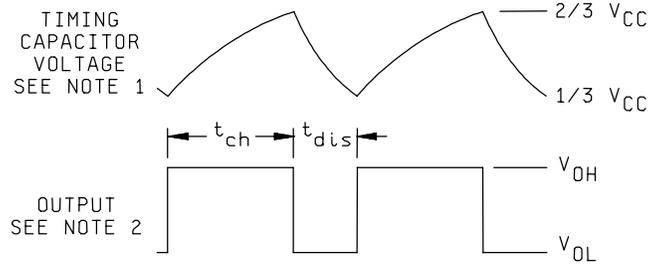
FIGURE 4. Waveforms for switching and timing parameters (monostable).



Notes:

1. This limit applies only during tests for t_{PHL} .
2. The pulse is applied to pin 7 of the test adapter.
3. This measurement shall be made on pin 4 of the test adapter.
4. A/B means value "A" for $V_{CC} = 15 \text{ V}$ or 16.5 V and "B" for $V_{CC} = 4.5 \text{ V}$ or 5 V .

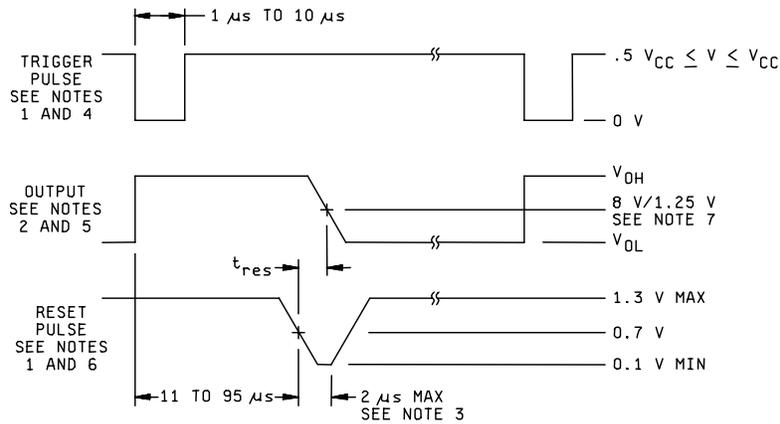
FIGURE 5. Waveforms for switching and timing parameters (monostable).



NOTES:

1. The timing capacitor voltage measurement (threshold) shall be made on pin 7 of the test adapter.
2. The timing measurement (output) shall be made at pin 4 of the test adapter.

FIGURE 6. Waveforms for timing parameters (astable).



NOTES:

1. Reset pulse rise and fall times shall be ≤ 10 ns.
2. Reset threshold are checked by applying the specified reset levels and verifying
 - a. Output high after trigger pulse and before reset goes low and
 - b. Output goes low stays low 2 μ seconds minimum after rest is returned high.
3. This limit only applies during test for t_{RES} .
4. This pulse shall be applied to pin 7 of the test adapter.
5. This measurement shall be made on pin 4 of the test adapter.
6. This pulse shall be applied to pin 5 of the test adapter.
7. A/B means value "A" for $V_{CC} = 15$ V or 16.5 V and "B" for $V_{CC} = 4.5$ V or 5 V.

FIGURE 7. Waveforms for reset tests.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Adapter pin number 14/								Relays closed	Pin measured			Devices 01, 03 limits			Device 02 limits 1/			
				1	2		3	4	6		7		8	No.	Value	Unit	Min	Max	Unit	Min	Max	Unit
					01,03	02			01,03	02												
9 T _A = +25°C	t _{dis}		75	GND	4.5	5		See		See	14/	t _{dis}	μs	57.5	80.0	μs	57.5	80.0	μs			
			76	"	16.5	15		fig. 6		fig. 6	1,2,3,5, 8,10	"	μs	57.5	80.0	μs	57.5	80.0	μs			
			77	"	4.5	5		"		"	1,2,3,6, 9,10	"	ms	5.40	7.70	ms	5.40	7.70	ms			
			78	"	16.5	15		"		"	"	"	ms	5.40	7.70	ms	5.40	7.70	ms			
		Δt _{ch} / ΔV _{CC}		79	"	ΔV _{CC} = 12	ΔV _{CC} = 10		For devices 01 and 03, V _{CC} = 4.5 V to 16.5 V Z/ see fig. 6		For device 02, V _{CC} = 5.0 V to 15.0 V g/ see fig. 6	4	Δt _{ch} / ΔV _{CC}	ns / V	-820	820	ns / V	-820	820	ns / V		
		Δt _{b(OH)M}		80	"	---	5		For device 02 only 11/ see fig. 4		1,3,5,7, 10,11	4	Δt _{b(OH)M}	μs	---	---	μs	---	---	μs		
		Δt _{b(OH)M} / ΔV _{CC}		81	"	---	15		For device 02 only 11/ see fig. 4		"	"	μs / V	---	---	μs / V	---	---	μs / V			
		t _{res}		82	GND	16.5	15		See		1,3,5,7, 10,11	4	t _{res}	μs	---	1.5	μs	---	1.5	μs		
		t _{pLH}		83	"	4.5	5		fig. 7		1,3,5,7, 10,11	"	t _{pLH}	ns	---	900	ns	---	900	ns		
	10 T _A = +125°C	t _{pLH}		84	"	16.5	15		See		1,3,5,7, 10,11	"	t _{pLH}	ns	---	900	ns	---	900	ns		
t _{pLH}			85	"	4.5	5		fig. 4		"	"	t _{pLH}	ns	---	300	ns	---	300	ns			
t _{pLH}			86	"	16.5	15		See		1,3,5,7, 10,11	"	t _{pLH}	ns	---	---	ns	---	---	ns			
t _{pLH}			87	"	4.5	5		fig. 4		"	"	t _{pLH}	ns	---	---	ns	---	---	ns			
t _{pHL}			88	"	16.5	15		See		1,3,5,7, 10,11	"	t _{pHL}	ns	---	---	ns	---	---	ns			
t _{pHL}			89	"	4.5	5		fig. 4		"	"	t _{pHL}	ns	---	---	ns	---	---	ns			
t _{pHL}			90	"	16.5	15		See		2,3,5,7, 10,11	"	t _{pHL}	μs	---	12.0	μs	---	12.0	μs			
t _{pHL}			91	"	4.5	5		fig. 5		"	"	t _{pHL}	μs	---	12.0	μs	---	12.0	μs			
t _{b(OH)}			92	GND	4.5 V	5 V		See		1,3,5,7, 10,11	"	t _{b(OH)}	μs	106.7	113.3	μs	106.7	113.3	μs			
t _{b(OH)}			93	"	16.5 V	15 V		fig. 4		"	"	t _{b(OH)}	μs	"	"	μs	"	"	μs			
		94	"	4.5 V	5 V		"		1,3,6,7, 10,11	"	t _{b(OH)}	ms	10.67	11.33	ms	10.67	11.33	ms				
		95	"	16.5 V	15 V		"		"	"	t _{b(OH)}	ms	"	"	ms	"	"	ms				
	Δt _{b(OH)} / ΔT		96	"	16.5	15		"		1,3,5,7, 10,11	4	Δt _{b(OH)} / ΔT	ns / °C	-11	11	ns / °C	-11	11	ns / °C			
	t _{ch}		97	"	4.5	5		See		1,2,3,5, 8,10	4	t _{ch}	μs	120	156	μs	120	156	μs			
			98	"	16.5	15		fig. 6		"	"	t _{ch}	μs	120	156	μs	120	156	μs			
			99	"	4.5	5		"		1,2,3,6, 9,10	"	t _{ch}	ms	11.3	15.0	ms	11.3	15.0	ms			
			100	"	16.5	15		"		"	"	t _{ch}	ms	11.3	15.0	ms	11.3	15.0	ms			

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Adapter pin number 14/								Relays closed	Pin measured			Devices 01, 03 limits			Device 02 limits 1/										
			Test no.	2		3	4		5			6	7	8		No.	Value	Unit	Min	Max	Unit	Min	Max	Unit				
				01,03	02		01,03	02	01,03	02				01,03	02													
10 T _A = +125°C	t _{dis}		GND	4.5	5		See fig. 6				See fig. 6		1,2,3,5, 8,10	4	t _{dis}	μs	57.5	80.0	μs	57.5	80.0	μs						
			"	16.5	15		"				"		"	"	"	"	μs	57.5	80.0	μs	57.5	80.0	μs					
			"	4.5	5		"				"		1,2,3,6, 9,10	"	"	ms	5.40	7.70	ms	5.40	7.70	ms	5.40	7.70	ms			
			"	16.5	15		"				"		"	"	"	"	ms	5.40	7.70	ms	5.40	7.70	ms	5.40	7.70	ms		
		Δt _{ch} / ΔT		"	16.5	15							See fig. 6 10/	1,2,3,5, 8,10	4	Δt _{ch} / ΔT	ns / °C	-68	68	ns / °C	-68	68	ns / °C	-68	68	ns / °C		
11 T _A = -55°C	Δt _{D(OH)M} / ΔV _{CC}		GND	---	15		For device 02 only 13/ see fig. 4						1,3,5,7, 10,11	4	Δt _{D(OH)M} / ΔV _{CC}	ns / °C	---	---	ns / °C	---	---	ns / °C	---	---	ns / °C	---	---	ns / °C
	t _{res}		"	16.5	15			See fig. 7					1,3,5,7, 11	4	t _{res}	μs	---	2.0	μs	---	2.0	μs	---	2.0	μs	---	2.0	μs
	t _{PLH}		"	4.5	5		See fig. 4				See fig. 7		1,3,5,7, 10,11	"	t _{PLH}	ns	---	800	ns	---	800	ns	---	800	ns	---	800	ns
	t _{TLH}		"	16.5	15		See fig. 4				See fig. 4		"	"	t _{PLH}	ns	---	800	ns	---	800	ns	---	800	ns	---	800	ns
	t _{TLH}		"	4.5	5		See fig. 4				See fig. 4		1,3,5,7, 10,11	"	t _{TLH}	ns	---	300	ns	---	300	ns	---	300	ns	---	300	ns
	t _{THL}		"	16.5	15		See fig. 4				See fig. 4		"	"	t _{THL}	ns	---	"	ns	---	"	ns	---	"	ns	---	"	ns
	t _{THL}		"	4.5	5		See fig. 4				See fig. 4		1,3,5,7, 10,11	"	t _{THL}	ns	---	"	ns	---	"	ns	---	"	ns	---	"	ns
	t _{PHL}		"	16.5	15		See fig. 4				See fig. 4		"	"	t _{PHL}	ns	---	"	ns	---	"	ns	---	"	ns	---	"	ns
	t _{PHL}		"	4.5	5		See fig. 5				See fig. 5		2,3,5, 10,11	"	t _{PHL}	μs	---	12.0	μs	---	12.0	μs	---	12.0	μs	---	12.0	μs
	t _{PHL}		"	16.5	15		See fig. 5				See fig. 5		"	"	t _{PHL}	"	---	12.0	"	---	12.0	"	---	12.0	"	---	12.0	"
	t _{D(OH)}		GND	4.5V	5V		See fig. 4				See fig. 4		1,3,5,7, 10,11	"	t _{D(OH)}	μs	106.7	113.3	μs	106.7	113.3	μs	106.7	113.3	μs	106.7	113.3	μs
	t _{D(OH)}		"	16.5V	15V		"				"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
t _{D(OH)}		"	4.5V	5V		"				"		1,3,6,7, 10,11	"	"	ms	10.67	11.33	ms	10.67	11.33	ms	10.67	11.33	ms	10.67	11.33	ms	
t _{D(OH)}		"	16.5V	15V		"				"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
t _{D(OH)}		"	16.5	15		"				"		1,3,5,7, 10,11	4	Δt _{D(OH)}	ns / °C	-11	11	ns / °C	-11	11	ns / °C	-11	11	ns / °C	-11	11	ns / °C	
t _{ch}		"	4.5	5		See fig. 6				See fig. 6		1,2,3,5, 8,10	4	t _{ch}	μs	120	156	μs	120	156	μs	120	156	μs	120	156	μs	
t _{ch}		"	16.5	15		"				"		1,2,3,6, 9,10	"	"	μs	120	156	μs	120	156	μs	120	156	μs	120	156	μs	
t _{ch}		"	4.5	5		"				"		"	"	"	ms	11.3	15.0	ms	11.3	15.0	ms	11.3	15.0	ms	11.3	15.0	ms	
t _{ch}		"	16.5	15		"				"		"	"	"	ms	11.3	15.0	ms	11.3	15.0	ms	11.3	15.0	ms	11.3	15.0	ms	

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Adapter pin numbers 14/								Relays closed	Pin measured			Devices 01, 03 limits			Device 02 limits 1/					
				2		3		4		5			6		7		8		No.	Value	Unit	Min	Max	Unit
				01,03	02	01,03	02	01,03	02	01,03	02		01,03	02	01,03	02	Min	Max						
11	t_{dis}		125	GND	4.5	5	See fig. 6	See fig. 6	See fig. 6	See fig. 6	See fig. 6	1,2,3,5, 8,10	4	t_{dis}	μs	57.5	80.0	μs	57.5	80.0	μs			
			126	"	16.5	15	"	"	"	"	"	"	"	"	"	μs	57.5	80.0	μs	57.5	80.0	μs		
			127	"	4.5	5	"	"	"	"	"	"	1,2,3,6, 9,10	"	"	ms	5.40	7.70	ms	5.40	7.70	ms		
			128	"	16.5	15	"	"	"	"	"	"	"	"	"	ms	5.40	7.70	ms	5.40	7.70	ms		
T _A = -55°C	$\Delta t_{ch} / \Delta T$		129	"	16.5	15	See fig. 6 10/	1,2,3,5, 8,10	4	$\Delta t_{ch} / \Delta T$	ns / °C	-68	68	ns / °C	-68	68	ns / °C							
	$\Delta t_D(OH)M / \Delta T$		130	GND	---	15	For device 02 only 13/ see fig. 4	For device 02 only 13/ see fig. 4	For device 02 only 13/ see fig. 4	For device 02 only 13/ see fig. 4	1,3,5,7, 10,11	4	$\Delta t_D(OH)M / \Delta T$	ns / °C	---	---	ns / °C	---	---	ns / °C				
	t_{res}		131	"	16.5	15	See fig. 7	See fig. 7	See fig. 7	See fig. 7	1,3,5,7, 11	4	t_{res}	μs	---	1.5	μs	---	1.5	μs				

- 1/ Limits apply to both halves of device type 02 independently.
- 2/ The voltage at adapter pin 8 is swept downward from a voltage > 2/3 V_{CC}. V_{TR} is measured when the output switches to the "high" state.
- 3/ The voltage at adapter pin 8 is swept upward from a voltage < 1/3 V_{CC}. V_{TH} is measured when the output switches to the "low" state.
- 4/ The application of GND to test circuit pin 5 causes the output to be reset (latched low). Measure I_R into adapter pin 5.
- 5/ $\Delta t_D(OH) / \Delta V_{CC} = (t_D(OH) \text{ at } V_{CC} = 16.5 \text{ V} - t_D(OH) \text{ at } V_{CC} = 4.5 \text{ V}) / (16.5 \text{ V} - 4.5 \text{ V})$.
- 6/ For 02, $\Delta t_D(OH) / \Delta V_{CC} = (t_D(OH) \text{ at } V_{CC} = 15 \text{ V} - t_D(OH) \text{ at } V_{CC} = 5 \text{ V}) / (15 \text{ V} - 5 \text{ V})$.
- 7/ $\Delta t_{ch} / \Delta V_{CC} = (t_{ch} \text{ at } V_{CC} = 16.5 \text{ V} - t_{ch} \text{ at } 4.5 \text{ V}) / (16.5 \text{ V} - 4.5 \text{ V})$.
- 8/ For 02, $\Delta t_{ch} / \Delta V_{CC} = (t_{ch} \text{ at } V_{CC} = 15 \text{ V} - t_{ch} \text{ at } 5 \text{ V}) / (15 \text{ V} - 5 \text{ V})$.
- 9/ $\Delta t_D(OH) / \Delta T = (t_D(OH) \text{ at } 125^\circ\text{C} - t_D(OH) \text{ at } 25^\circ\text{C}) / (125^\circ\text{C} - 25^\circ\text{C})$ and $(t_D(OH) \text{ at } 25^\circ\text{C} - t_D(OH) \text{ at } -55^\circ\text{C}) / (25^\circ\text{C} - (-55^\circ\text{C}))$.
- 10/ $\Delta t_{ch} / \Delta T = (t_{ch} \text{ at } 125^\circ\text{C} - t_{ch} \text{ at } 25^\circ\text{C}) / (125^\circ\text{C} - 25^\circ\text{C})$ and $(t_{ch} \text{ at } 25^\circ\text{C} - t_{ch} \text{ at } -55^\circ\text{C}) / (25^\circ\text{C} - (-55^\circ\text{C}))$.
- 11/ $\Delta t_D(OH)M = t_D(OH) \text{ side "A"} - t_D(OH) \text{ side "B"}$.
- 12/ $\Delta t_D(OH)M / \Delta V_{CC} = (\Delta t_D(OH) / \Delta V_{CC}) \text{ side "A"} - (\Delta t_D(OH) / \Delta V_{CC}) \text{ side "B"}$.
- 13/ $\Delta t_D(OH)M / \Delta T = (\Delta t_D(OH) / \Delta T) \text{ side "A"} - (\Delta t_D(OH) / \Delta T) \text{ side "B"}$.
- 14/ Test circuit pin numbers and relays refer to those shown on figure 3.
- 15/ V_{OL} shall be measured after the output has been low for 100 μs (minimum).
- 16/ I_{SOURCE} for device type 03 = -60 mA.

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TABLE IV. Group C end point electrical parameters.

($T_A = 25^\circ\text{C}$, $V_{CC} = 16.5\text{ V dc}$ for device types 01 and 03, $V_{CC} = 15.0\text{ V dc}$ for all device type 02)

Test	Limits for device types 01 and 03		Limits for device type 02		Delta limits ^{1/}
	Min	Max	Min	Max	
V_{TR}	5.20 V	5.80 V	4.70 V	5.30 V	$\pm 50\text{ mV}$
V_{TH}	10.70 V	11.30 V	9.70 V	10.30 V	$\pm 50\text{ mV}$
V_{OL} at 10 mA	---	0.150 V	---	0.150 V	$\pm 50\text{ mV}$
I_{CEX}	---	100 nA	---	100 nA	$\pm 50\text{ nA}$

^{1/} Delta limits apply to the measured value (see delta limit definition in MIL-PRF-38535).

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

Symbol	Description
V_{TR}	Trigger voltage. The voltage at which the output latches from the "low" state to the "high" state. This voltage is nominally $1/3 V_{CC}$.
I_{TR}	Trigger current. The current flowing out of the trigger terminal while the output is in the "high" state.
V_{TH}	Threshold voltage. The voltage at which the output latches from the "high" state to the "low" state. This voltage is nominally $2/3 V_{CC}$.
I_{TH}	Threshold current. The current flowing into the threshold terminal while the output is in the "low" state.
V_{CL}	Control voltage. The control voltage is the reference voltage for the threshold comparator. It is internally generated by a voltage divider (from V_{CC} to ground) tapped at $2/3 V_{CC}$. NOTE: The divider is also tapped at $1/3 V_{CC}$, which is the reference voltage for the trigger comparator.
V_R	Reset voltage. The reset acts as an inhibit. If $1.3 \leq V_R \leq V_{CC}$, the device is free to function. If $0 V \leq V_R \leq 0.1 V$, the output is forced to the "low" state. The output will remain low after the reset voltage goes high only if the trigger voltage is high. If the trigger voltage is low, the output will go high when the reset voltage goes high. The reset voltage going low also causes the discharge transistor to turn on, thus preventing the timing capacitor (C_T) from charging.
I_R	Reset current. The current out of the reset terminal after the reset voltage has been applied and the output is latched low.
V_{SAT}	Discharge transistor saturation voltage. When the output is low, the discharge terminal is sinking current. V_{SAT} is defined as the collector-emitter voltage of the discharge transistor when sinking the specified current.
$t_{D(OH)}$	Time delay, output high. In the monostable mode of operation, the interval of time the output remains high once triggered. This delay is given by the following equation: $t_{D(OH)} = 1.1 R_T C_T$ (see figure 5).
t_{ch}	Capacitor charge time. In the astable mode of operation, the time interval during which the external timing capacitor (C_T) is charging from $1/3 V_{CC}$ to $2/3 V_{CC}$. This interval is ideally given by the equation: $t_{ch} = 0.693 (R_{TA} + R_{TB}) C_T$ (see figure 6).
t_{dis}	Capacitor discharge time. In the astable mode of operation, the time interval during which the external timing capacitor (C_T) is discharging from $2/3 V_{CC}$ to $1/3 V_{CC}$. This interval is ideally given by the equation: $t_{dis} = 0.693 R_{TB} C_T$ (see figure 6).

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

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6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Military device type</u>	<u>Generic-industry type</u>
01	555
02	556
03	555 (ISOURCE = -60 mA)

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army – CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA – CC

Preparing activity:

DLA - CC
 Project 5962-2025

Review activities:

Army - MI, SM
 Navy - AS, CG, MC, SH, TD
 Air Force – 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at www.dodssp.daps.mil.