

MILITARY SPECIFICATION  
 MICROCIRCUITS, DIGITAL TTL, COUNTERS,  
 MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, binary and decode counters. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	Divide-by-12 Counter
02	4-Bit Binary Counter
03	Synchronous 4-Bit Decade Counter (Asynchronous Clear)
04	Synchronous 4-Bit Binary Counter (Synchronous Clear)
05	Synchronous 4-Bit Decade Counter (Synchronous Clear)
06	Synchronous 4-Bit Binary Counter (Asynchronous Clear)
07	High-speed Decade Counter
08	Synchronous 4-Bit Up/Down Decade Counter
09	Synchronous 4-Bit Up/Down Binary Counter

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline, (see MIL-M-38510, appendix C)</u>
A	F-1 (14-lead, 1/4" x 1/4" flat package)
B	F-3 (14-lead, 1/8" x 1/4" flat package)
C	D-1 (14-lead, 1/4" x 3/4" dual-in-line package)
D	F-2 (14-lead, 1/4" x 3/8" flat package)
E	D-2 (16-lead, 1/4" x 7/8" dual-in-line package)
F	F-5 (16-lead, 1/4" x 3/8" flat package)

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 Vdc to 7.0 Vdc
Input voltage range- - - - -	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range- - - - -	-65° to +150°C
Maximum power dissipation (P <sub>D</sub> ) <sup>1/</sup>	
Device types 01, 02, 07- - - - -	268 mW
Device types 03 through 06 - - - - -	500 mW
Device types 08 and 09 - - - - -	490 mW
Lead temperature (soldering 10 seconds)- -	300°C
Thermal resistance, junction to case (θ <sub>JC</sub> )	0.09°C/mW for flat package;
0.08°C/mW for dual-in-line package	
Junction temperature (T <sub>J</sub> )- - - - -	175°C

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage - - - - -	2.0 Vdc
Maximum low level input voltage- - - - -	0.8 Vdc
Normalized fanout (each output)	
Device types 01, 02, 07, 08, 09- - - - -	10 maximum
Device types 03, 04, 05, 06	
Low-level- - - - -	10 maximum
High level - - - - -	20 maximum
Width of input count pulse, t <sub>p</sub> (in)	
Device types 01, 02, 07- - - - -	50 ns minimum
Device types 08, 09- - - - -	25 ns minimum
Width of reset pulse, t <sub>p</sub> (reset)	
Device types 01, 02, 07- - - - -	50 ns minimum
Input clock frequency, f <sub>CLOCK</sub>	
Device types 01, 02, 07- - - - -	0 to 10 MHz
Device types 03, 04, 05, 06, 08, 09- - -	0 to 20 MHz
Width of clock pulse, t <sub>w</sub> (CLOCK)	
Device types 03, 04, 05, 06- - - - -	30 ns minimum
Width of clear pulse, t <sub>w</sub> (CLEAR)	
Device types 03, 04, 05, 06, 08, 09- - -	25 ns minimum
Setup time, t(SETUP),	
Device types 03, 04, 05, 06	
Data inputs- - - - -	20 ns minimum
Enable P - - - - -	25 ns minimum
Load - - - - -	30 ns minimum
Clear (04 and 05 only) - - - - -	25 ns minimum
Setup time, t(SETUP),	
Device types 08, 09	
Data inputs- - - - -	25 ns minimum
Hold time at any input, t <sub>HOLD</sub>	
Device types 03, 04, 05, 06, 08, 09- - -	0 ns minimum
Case operating temperature range - - - - -	-55° to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

<sup>1/</sup> Must withstand the added P<sub>D</sub> due to short circuit test (e.g., I<sub>OS</sub>).

## STANDARD

## MILITARY

## MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

## 3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and logic diagram. The terminal connections and logic diagrams shall be as specified on figures 1 and 2 respectively.

3.2.2 Truth tables and timing diagrams. The truth tables and timing diagrams shall be as specified on figures 3 and 4 respectively.

3.2.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All manufacturers' schematics shall be maintained and available upon request.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. (Subgroups 7 and 8 testing requires only a summary of attributes data.)

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 5 (see MIL-M-38510, appendix E).

## 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
High-level output voltage	$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $V_{IN} = 0.8 \text{ V}$ $I_{OH} = -400 \text{ } \mu\text{A}$	01,02,07, 08,09	2.4		V
High-level output voltage	$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $V_{IN} = 0.8 \text{ V}$ $I_{OH} = -800 \text{ } \mu\text{A}$	03,04, 05,06	2.4		V
Low-level output voltage	$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 16 \text{ mA}$	$V_{IN} = 2.0 \text{ V}$		0.4	V
			$V_{IN} = 0.8 \text{ V}$	01,02,03, 04,05,06, 07 08,09		0.4
Input clamp voltage	$V_{IC}$	$V_{CC} = 4.5 \text{ V}$ , $I_{IN} = -12 \text{ mA}$ $T_C = 25^\circ\text{C}$	01,02,03, 04,05,06, 07,08,09		-1.5	V
High-level input current at reset inputs	$I_{IH1}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	01,02,07		40	$\mu\text{A}$
High-level input current at reset inputs	$I_{IH2}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	01,02,07		100	$\mu\text{A}$
High-level input current at input A	$I_{IH3}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	01,07		80	$\mu\text{A}$
High-level input current at input A	$I_{IH4}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	01,07		200	$\mu\text{A}$
High-level input current at input BC or BD	$I_{IH5}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	01,07		160	$\mu\text{A}$
High-level input current at input BC or BD	$I_{IH6}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	01,07		400	$\mu\text{A}$
High-level input current at input A or B	$I_{IH7}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	02		80	$\mu\text{A}$
High-level input current at input A or B	$I_{IH8}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	02		200	$\mu\text{A}$
High-level input current at clock or enable T	$I_{IH9}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	03,04, 05,06		80	$\mu\text{A}$
High-level input current at clock or enable T	$I_{IH10}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	03,04, 05,06		200	$\mu\text{A}$
High-level input current at other inputs	$I_{IH11}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.4 \text{ V}$	03,04,05, 06,08,09		40	$\mu\text{A}$
High-level input current at other inputs	$I_{IH12}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 5.5 \text{ V}$	03,04,05, 06,08,09		100	$\mu\text{A}$
Low-level input current at reset inputs	$I_{IL1}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	01,02,07	-0.4	-1.6	mA
Low-level input current at input A	$I_{IL2}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	01	-0.4	-3.2	mA
			08,09	-0.7	-1.6	mA
Low-level input current at input BC or BD	$I_{IL3}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	01	-0.4	-6.4	mA
			07	-1.4	-6.4	mA
Low-level input current at input A or E	$I_{IL4}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	02	-0.4	-3.2	mA
Low-level input current at clock, count up or count down	$I_{IL5}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	03,04 05,06	-1.0	-2.3	mA
			08,09	-0.7	-1.6	mA
Low-level input current at data inputs	$I_{IL6}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	03,04,05, 06	-0.4	-1.3	mA
			08,09	-0.7	-1.6	mA
Low-level input current at clear, enable, and load	$I_{IL7}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	03,04,05, 06,08,09	-0.5	-1.6	mA
Low-level input current at count enable T	$I_{IL8}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.4 \text{ V}$	03,04,05, 06	-1.0	-3.2	mA
Short-circuit supply current	$I_{OS}$	$V_{CC} = 5.5 \text{ V } \underline{1/}$	01,02,03, 04,05,06, 07	-20	-57	mA
			08,09	-20	-65	mA
Supply current	$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 4.5 \text{ V}$	01,02,07		44	mA
			08,09		89	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
High-level supply current	$I_{CCH}$	$V_{CC} = 5.5 \text{ V } \underline{2/}$	03,04, 05,06		85	mA
Low-level supply current	$I_{CCL}$	$V_{CC} = 5.5 \text{ V } \underline{3/}$	03,04, 05,06		91	mA
Maximum frequency of input count pulses	$F_{MAX}$	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF } \pm 10\%$ $R_L = 390\Omega \pm 5\%$	01,02,07	10		MHz
Maximum input clock frequency	$F_{MAX}$		03,04,05, 06,08,09	20		MHz
Propagation delay time to logical H level from input count pulse to output D	$t_{PLH1}$		01,07	20	115	ns
Propagation delay time to logical L level from input count pulse to output D	$t_{PHL1}$		01,07	20	115	ns
Propagation delay time to logical H level from input count pulse to output D	$t_{PLH2}$		02	20	135	ns
Propagation delay time to logical L level from input count pulse to output D	$t_{PHL2}$		02	20	135	ns
Propagation delay time, low-to-high-level carry output from clock	$t_{PLH3}$		03,04, 05,06	3	58	ns
Propagation delay time, high-to-low-level carry output from clock	$t_{PHL3}$		03,04, 05,06	3	58	ns
Propagation delay time, low-to-high-level Q output from clock	$t_{PLH4}$		03,04, 05,06	3	36	ns
Propagation delay time, high-to-low-level Q output from clock	$t_{PHL4}$		03,04, 05,06	3	38	ns
Propagation delay time, low-to-high-level carry output from enable T	$t_{PLH5}$		03,04, 05,06	3	27	ns
Propagation delay time, high-to-low-level carry output from enable T	$t_{PHL5}$		03,04, 05,06	3	27	ns
Propagation delay time, high-to-low-level Q output from clear	$t_{PHL6}$		03,04, 05,06	3	47	ns
Propagation delay time, high-to-low-level Q output from clear	$t_{PHL7}$		08,09	3	57	ns
Propagation delay time, low-to-high-level Q output from load input	$t_{PLH8}$		08,09	3	66	ns
Propagation delay time, high-to-low-level Q output from load input	$t_{PHL8}$		08,09	3	62	ns
Propagation delay time, high-to-low-level carry output from count up input	$t_{PHL9}$		08,09	3	39	ns
Propagation delay time, low-to-high-level carry output from count up input	$t_{PLH9}$		08,09	3	45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Propagation delay time, high-to-low-level borrow output from count down input	$t_{PHL10}$	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 390\Omega \pm 5\%$	08,09	3	39	ns
Propagation delay time, low-to-high-level borrow output from count down input	$t_{PLH10}$		08,09	3	42	ns
Propagation delay time, low-to-high-level, Q output from count up or count down input	$t_{PLH11}$		08,09	3	63	ns
Propagation delay time, high-to-low-level, Q output from count up or count down input	$t_{PHL11}$		08,09	3	71	ns

1/ Not more than one output should be shorted at a time.

2/  $I_{CCH}$  is measured: (a) With the load input high; and (b) Then again with the load input low with all other inputs high and all outputs open.

3/  $I_{CCL}$  is measured: (a) With the clock input high; and (b) Then again with the clock input low with all other inputs low and all outputs open.

TABLE II. Electrical test requirements.

MIL-STD-883 Test requirements	Subgroup (see table III)		
	Class S devices	Class B devices	Class C devices
Interim electrical parameters (Pre Burn-In) (Method 5004)	1	1	None
Final electrical test parameters (Method 5004)	1*,2,3,7, 9,10,11	1*,2,3,7,9	1,7
Group A test requirements (Method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7, 9,10,11	1,2,3,7,9
Group B test requirements (Method 5005)	1,2,3 9,10,11	N/A	N/A
Group C end point electrical parameters (Method 5005)	N/A	1,2,3	1
Additional electrical subgroups for Group C periodic inspections	N/A	None	10,11
Group D end point electrical parameters (Method 5005)	1,2,3	1,2,3	1

\*PDA applies to subgroup 1 (see 4.2c).

- a. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
  - (2)  $T_A = 125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Percent defective allowable (PDA) - The PDA for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Steady state life test (method 1005 of MIL-STD-883) conditions, or equivalent.
  - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent..
  - (2)  $T_A = 125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End point electrical parameters shall be as specified in table II herein.

4.4.5 Inspection of packaging. The sampling and inspection of the preservation, packaging, and container marking shall be in accordance with the requirements of MIL-M-38510.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for the packaging of microcircuits shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

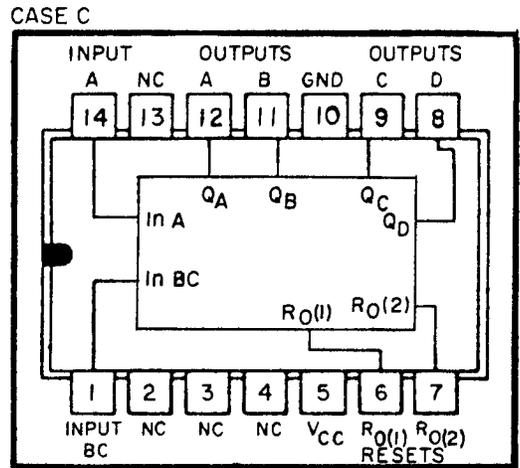
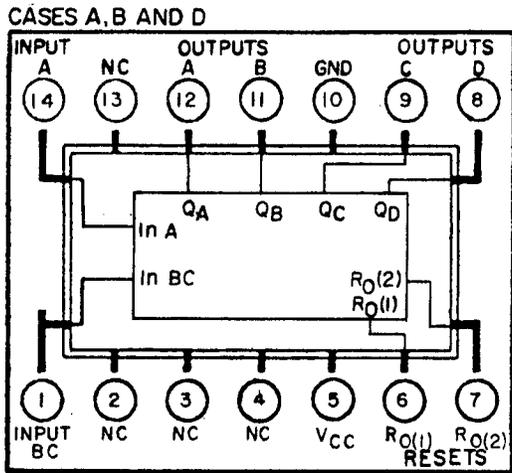
6.3 Ordering data. The contract or purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

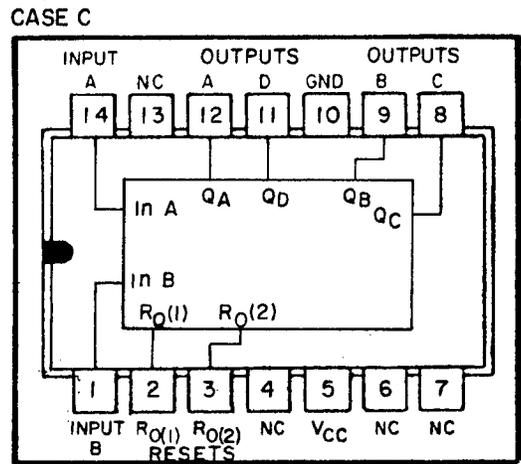
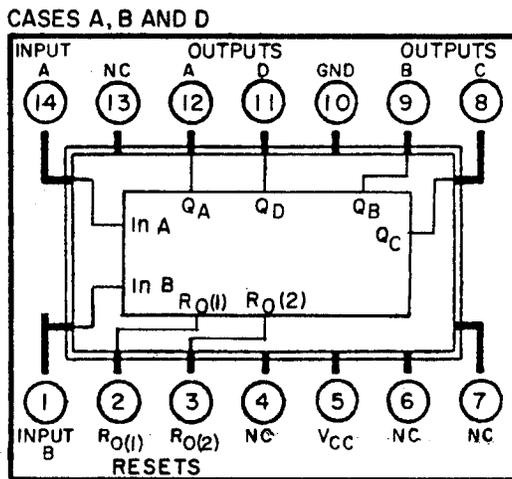
6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - - Electrical ground (common terminal)  
VIN - - - - - Voltage level at an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

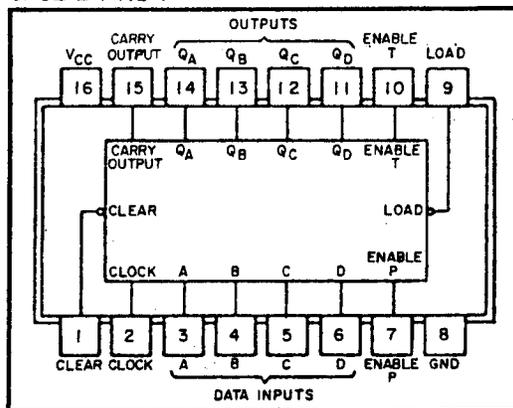


DEVICE TYPE 01



DEVICE TYPE 02

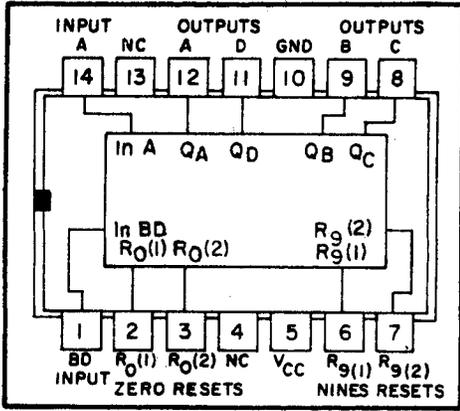
CASE E AND F



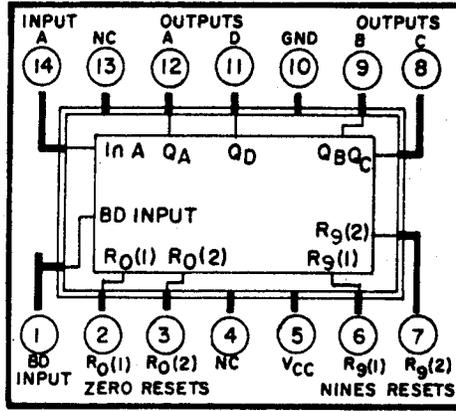
DEVICE TYPES 03, 04, 05, 06

FIGURE 1. Terminal connections (top view).

CASE C

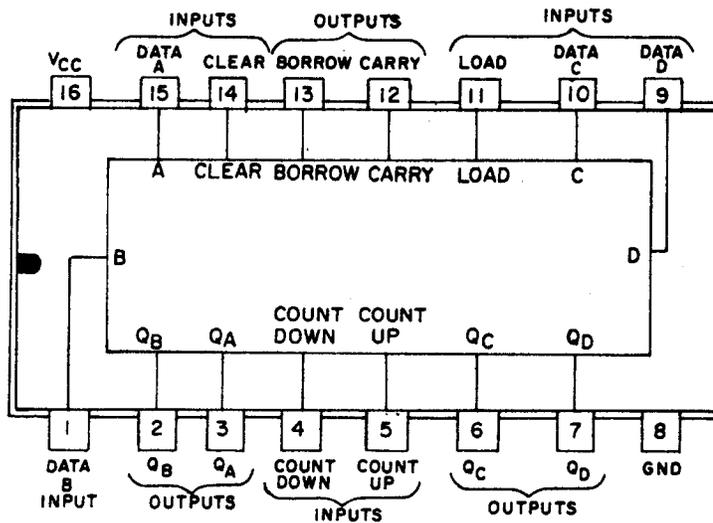


CASES A AND D



DEVICE TYPE 07

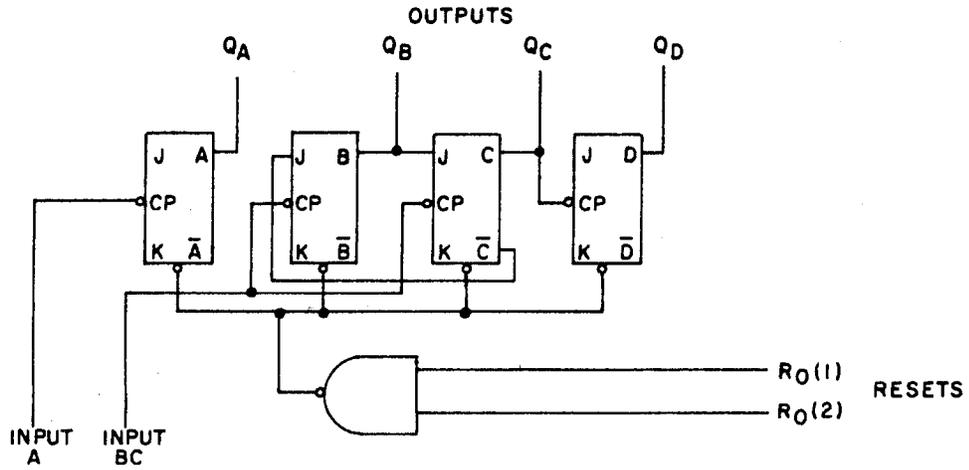
CASES E AND F



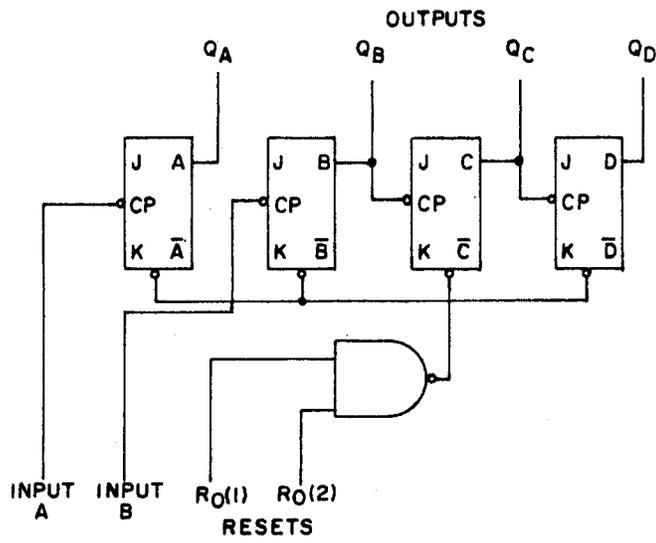
LOGIC: Low input to load sets  $Q_A = A$ ,  
 $Q_B = B$ ,  $Q_C = C$ , and  $Q_D = D$

DEVICE TYPES 08 and 09

FIGURE 1. Terminal connections - Continued.

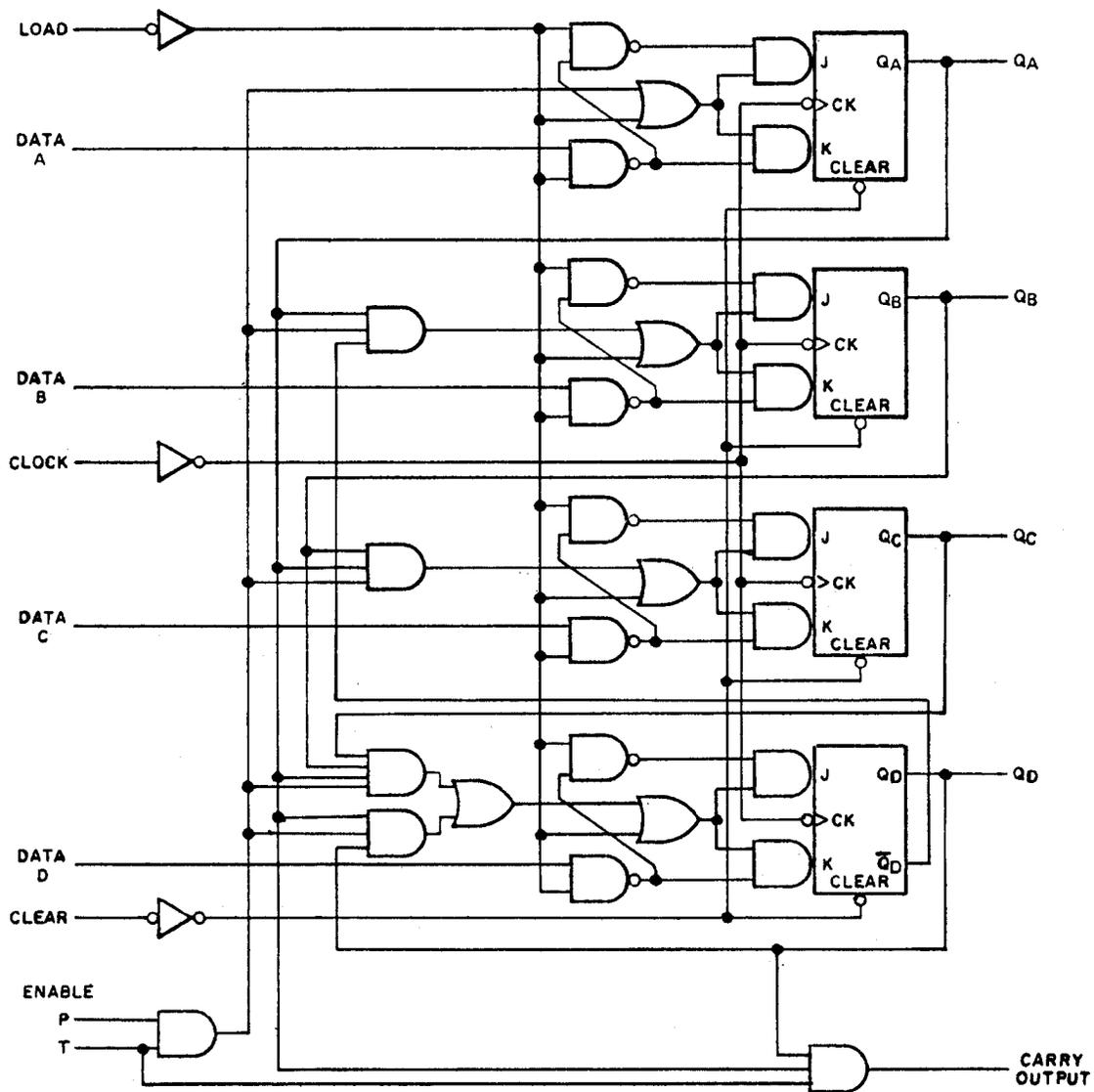


DEVICE TYPE 01



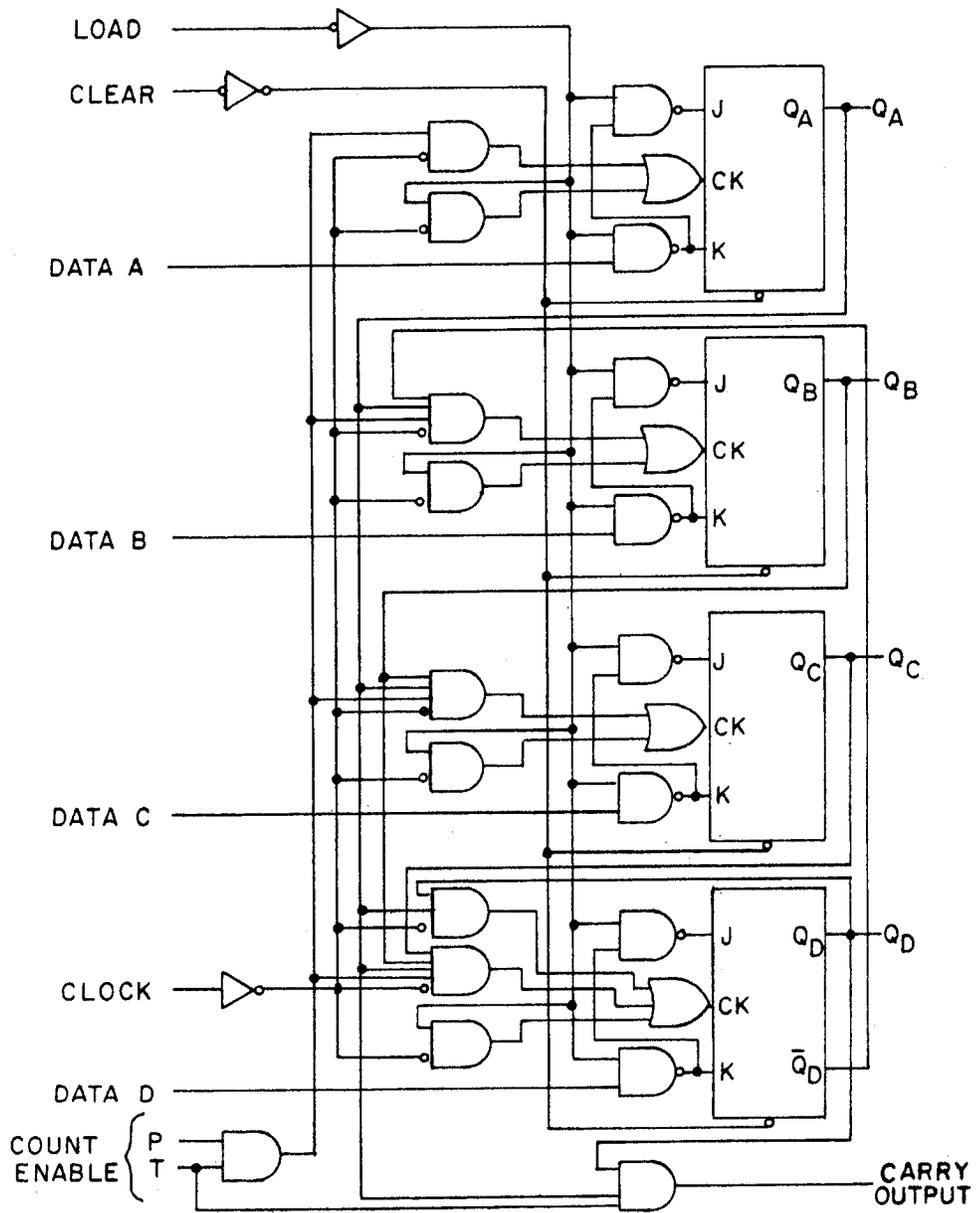
DEVICE TYPE 02

FIGURE 2. Logic diagrams.



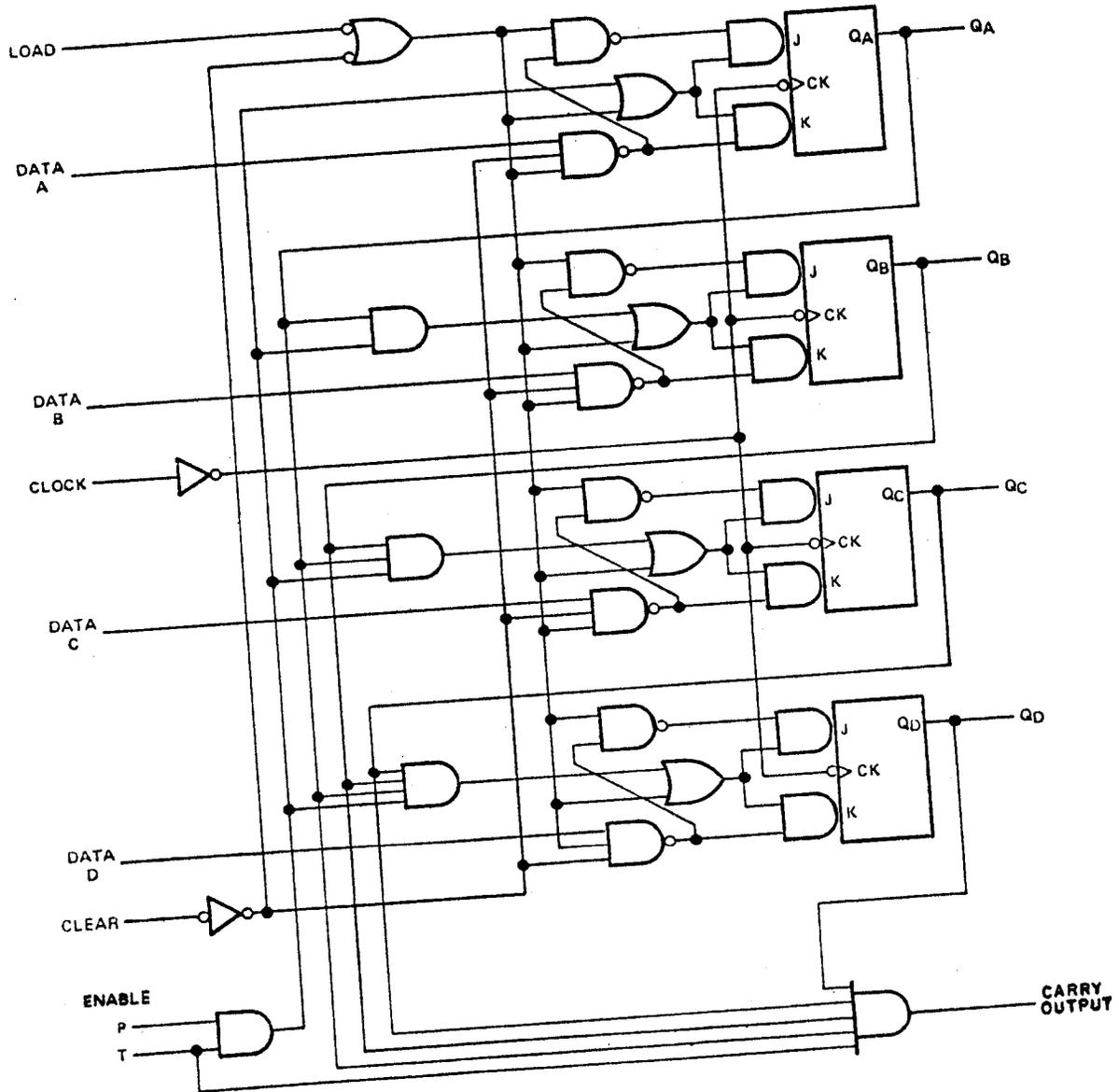
DEVICE TYPE 03

FIGURE 2. Logic diagrams - Continued.



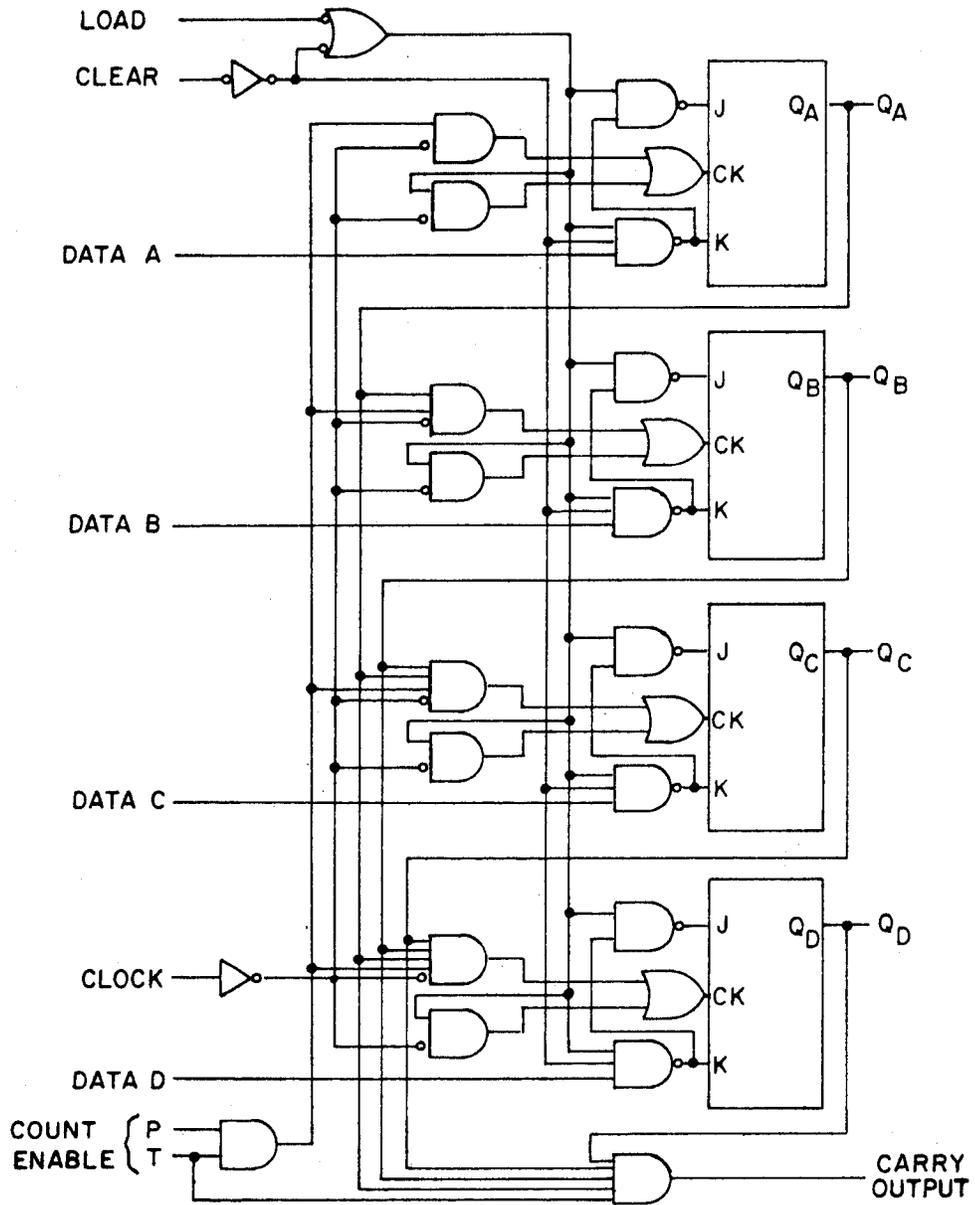
DEVICE TYPE 03

FIGURE 2. Logic diagrams - Continued.



DEVICE TYPE 04

FIGURE 2. Logic diagrams - Continued.



DEVICE TYPE 04

FIGURE 2. Logic diagram - Continued.

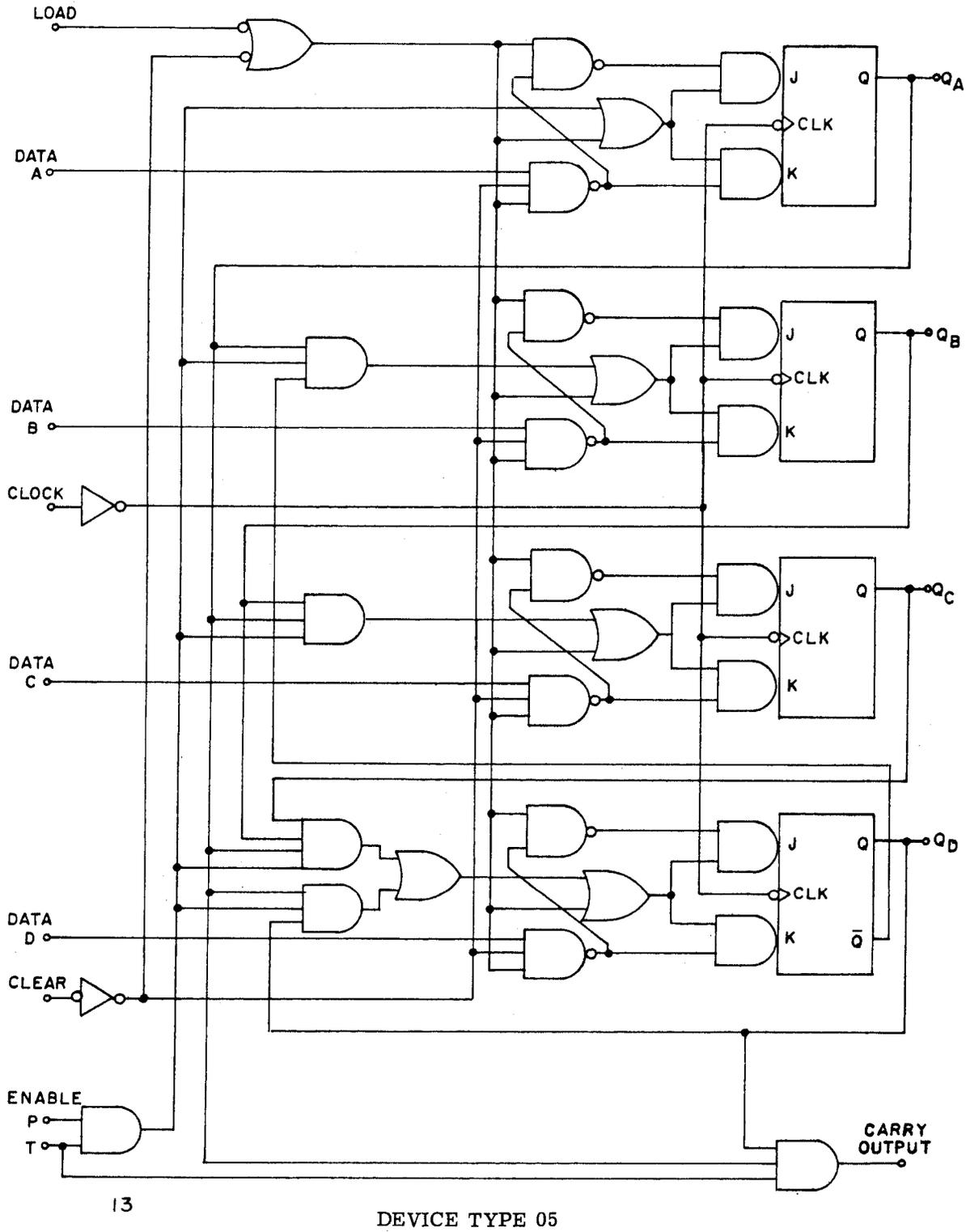
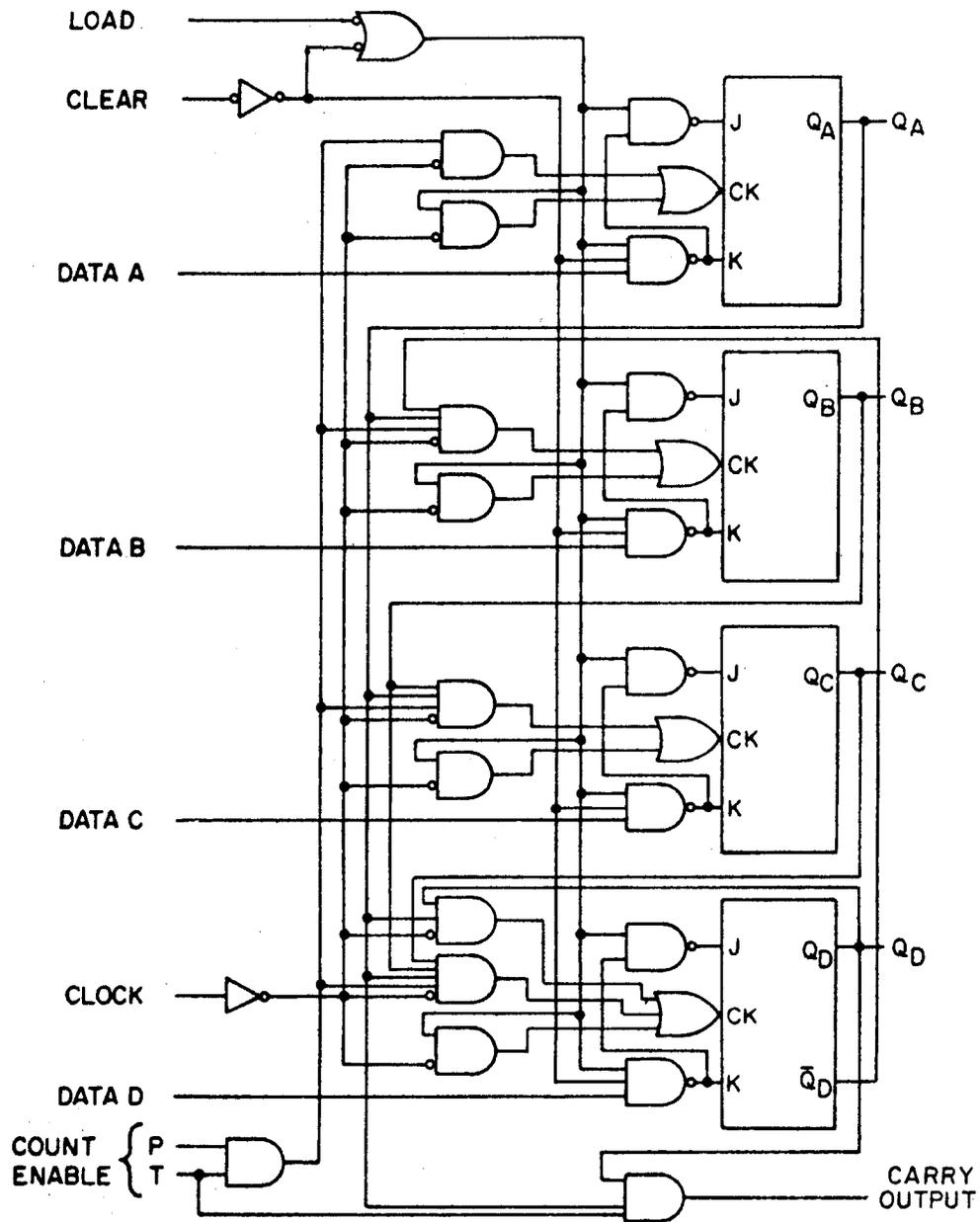
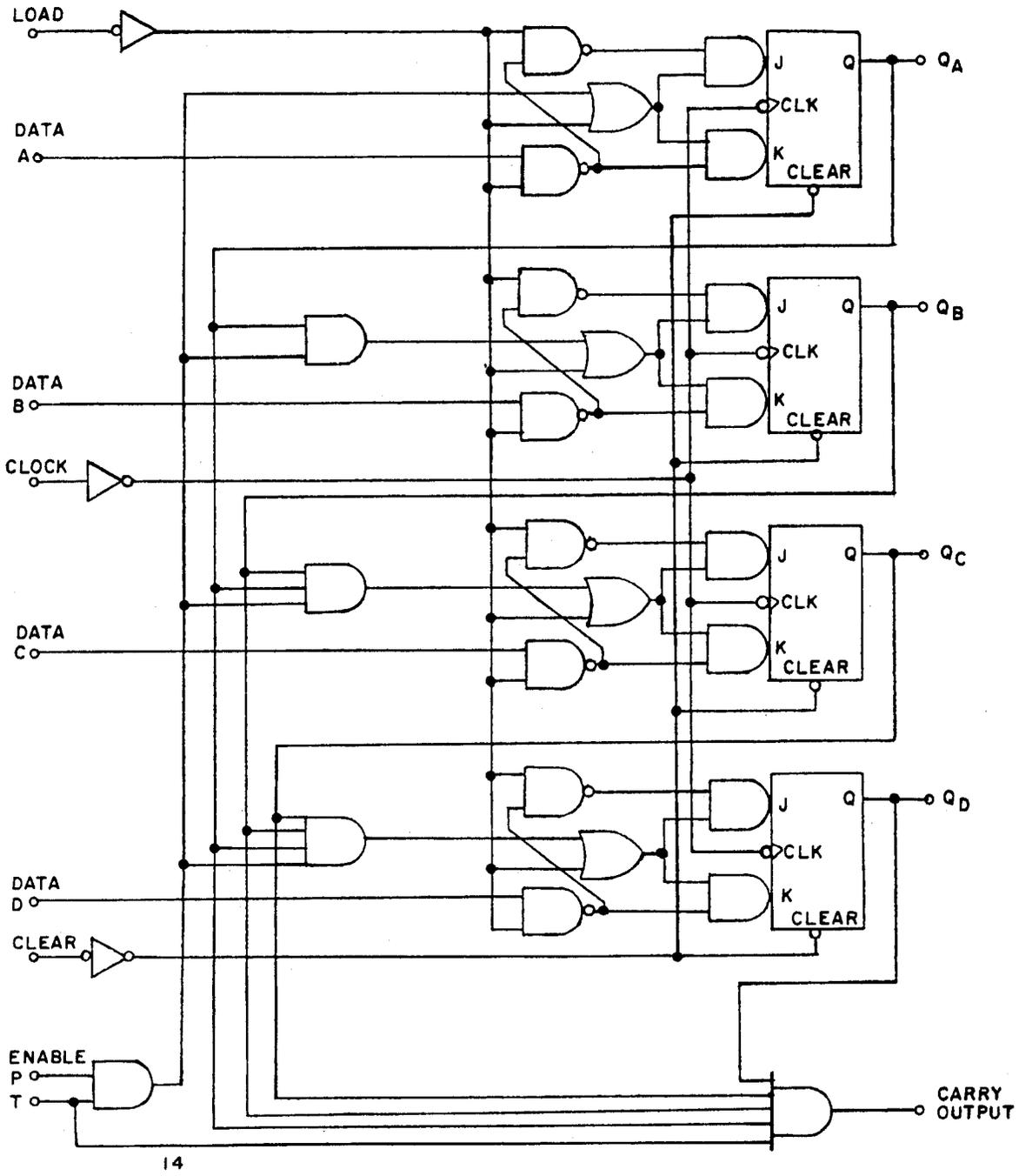


FIGURE 2. Logic diagram - Continued.



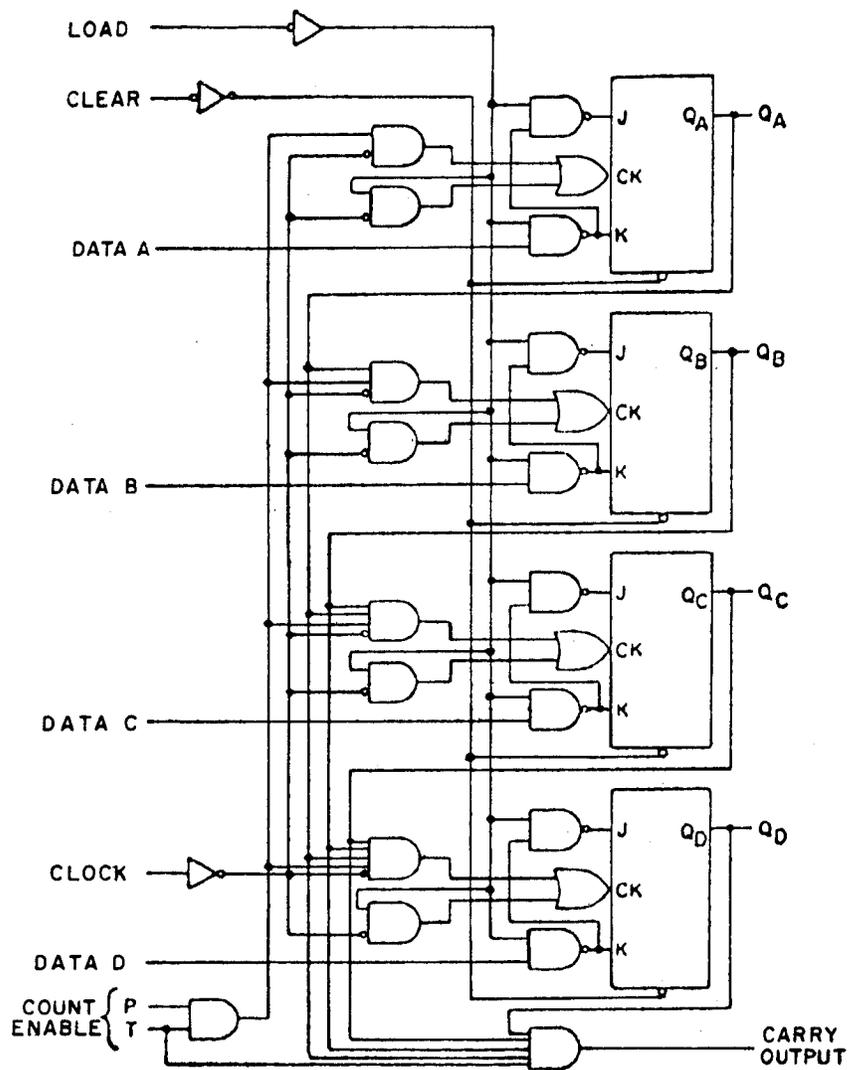
DEVICE TYPE 05

FIGURE 2. Logic diagrams - Continued.



DEVICE TYPE 06

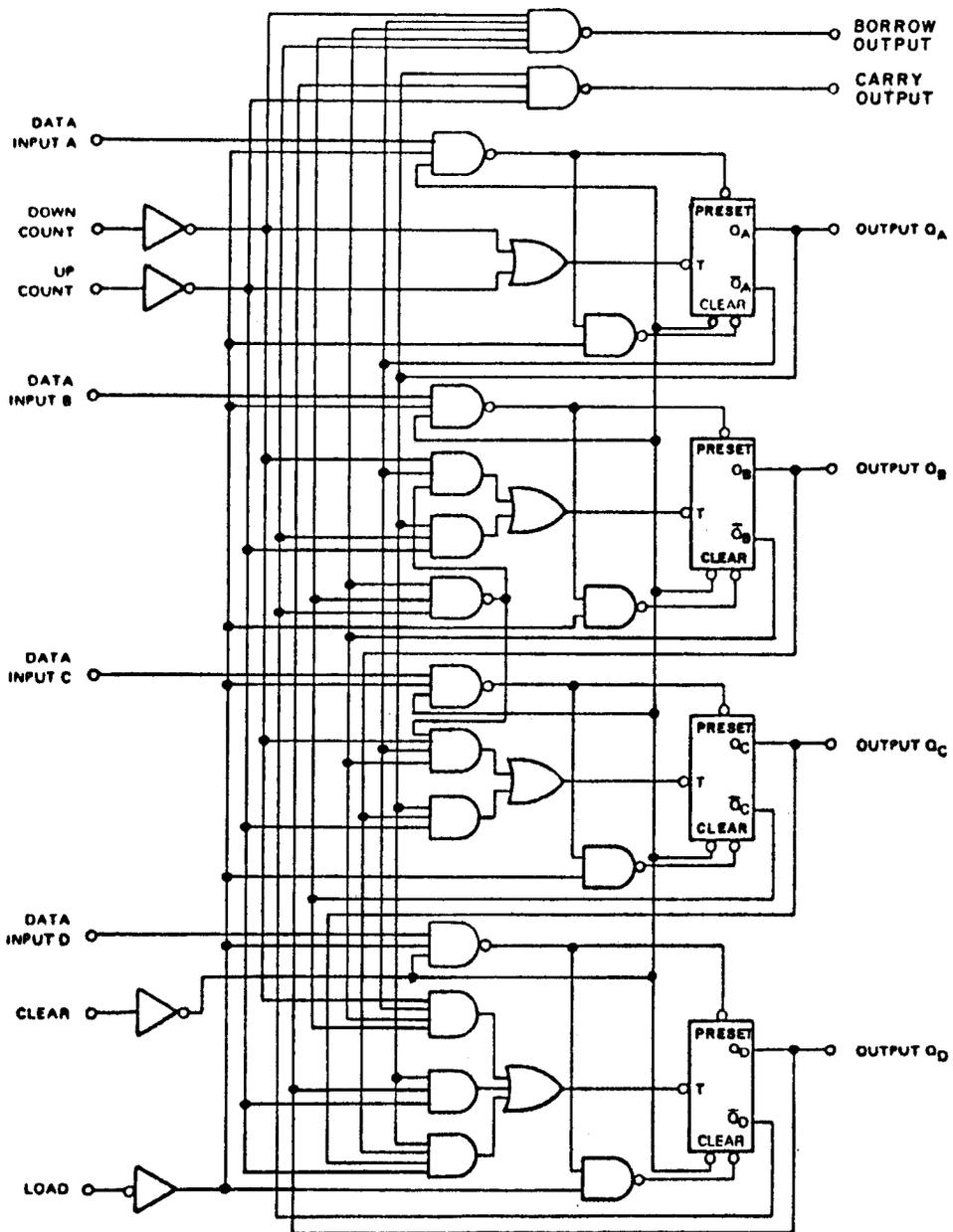
FIGURE 2. Logic diagrams - Continued.



DEVICE TYPE 06

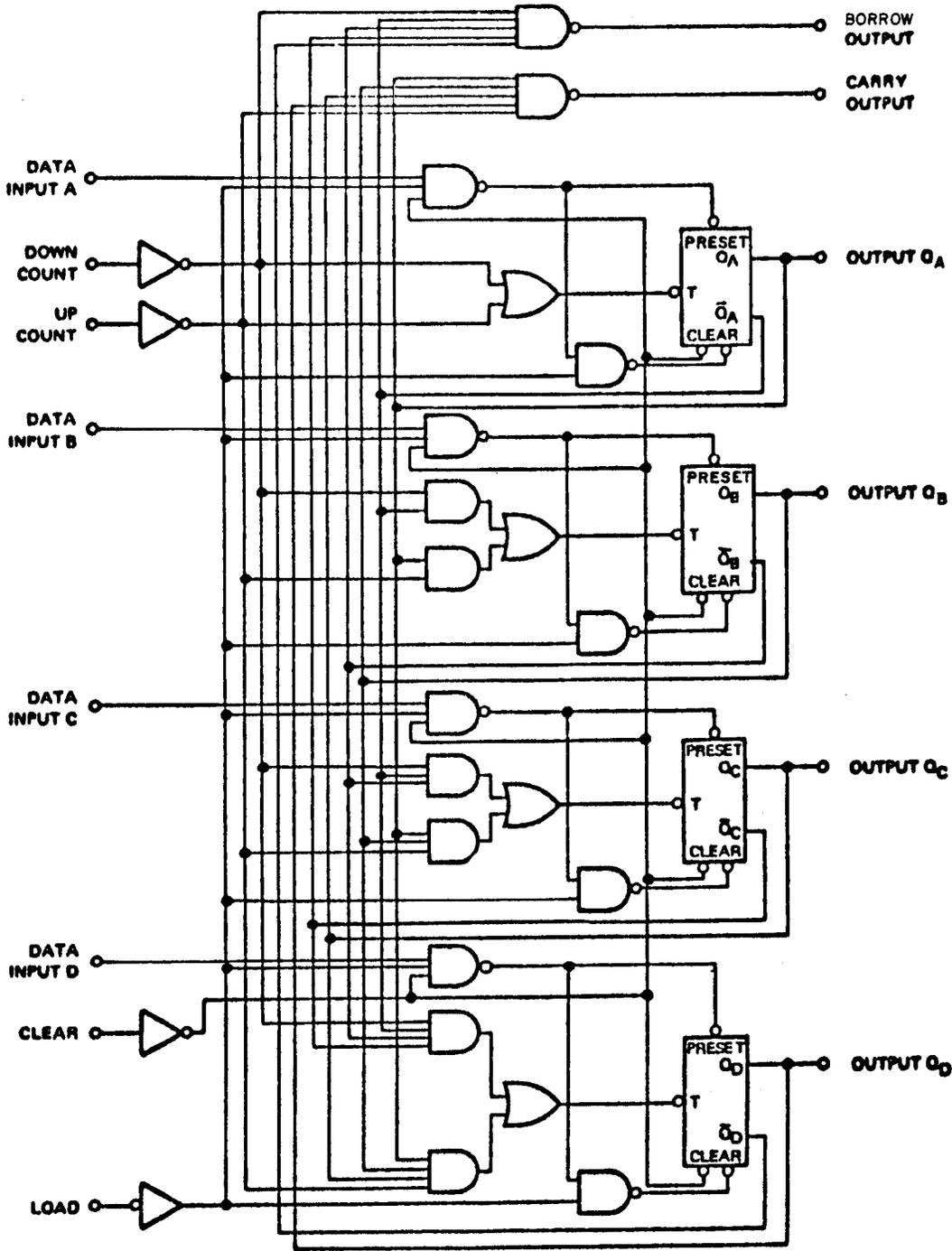
FIGURE 2. Logic diagrams - Continued.





DEVICE TYPE 08

FIGURE 2. Logic diagram - Continued.



DEVICE TYPE 09

FIGURE 2. Logic diagram - Continued.

DEVICE TYPE 01				
Count	Output			
	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

DEVICE TYPE 02				
Count	Output			
	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

## NOTES FOR TYPE 01:

1. Output A connected to input BC.
2. To reset all outputs to logical L, both  $R_0(1)$  and  $R_0(2)$  inputs must be at logical H.
3. Either (or both) reset inputs  $R_0(1)$  and  $R_0(2)$  must be at logical L to count.
4. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.
5. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

## NOTES FOR TYPE 02:

1. Output A connected to input B.
2. To reset all outputs to logical L, both  $R_0(1)$  and  $R_0(2)$  inputs must be at logical H.
3. Either (or both) reset inputs  $R_0(1)$  and  $R_0(2)$  must be at logical L to count.
4. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
5. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

FIGURE 3. Truth tables.

SYNCHRONOUS TRUTH TABLE, DEVICE TYPES 03 AND 05

Inputs at time $t_n$									Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	QA	QB	QC	QD	Carry output
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L
CP	H	H	H	X	X	X	X	H	Previous count plus 1 (note 1)				H if count = 9 L if count < 9
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 9 L if count < 9
CP	X	L	L	X	X	X	X	H	A	B	C	D	L

ASYNCHRONOUS TRUTH TABLE, DEVICE TYPE 03

Inputs at time $t_n$									Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	QA	QB	QC	QD	Carry output
X	X	X	X	X	X	X	X	L	L	L	L	L	L

## NOTES:

1. See UP count sequence table.
2. L =  $V_{IL}$  for inputs,  $V_{OL}$  for outputs.
3. H =  $V_{IH}$  for inputs,  $V_{OH}$  for outputs.
4. X =  $V_{IH}$  or  $V_{IL}$ .
5. CP = clock pulse.
6. NC = no change.

UP Count Sequence Table

QA (LSB)	QB	QC	QD (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H

FIGURE 3. Truth tables - Continued.

SYNCHRONOUS TRUTH TABLE, DEVICE TYPES 04 AND 06

Inputs at time $t_n$									Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	QA	QB	QC	QD	Carry output
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L
CP	H	H	H	X	X	X	X	H	Previous count plus 1 (note 1)				H if count = 15 L if count < 15
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 15 L if count < 15
CP	X	L	L	X	X	X	X	H	A	B	C	D	L

ASYNCHRONOUS TRUTH TABLE, DEVICE TYPE 06

Inputs at time $t_n$									Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	QA	QB	QC	QD	Carry output
X	X	X	X	X	X	X	X	L	L	L	L	L	L

## NOTES:

1. See UP count sequence table.
2. L =  $V_{IL}$  for inputs,  $V_{OL}$  for outputs.
3. H =  $V_{IH}$  for inputs,  $V_{OH}$  for outputs.
4. X =  $V_{IH}$  or  $V_{IL}$ .
5. CP = clock pulse.
6. NC = no change.

UP Count Sequence Table

QA (LSB)	QB	QC	QD (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	H

FIGURE 3. Truth tables - Continued.

## DEVICE TYPE 07

BCD count sequence (see note 1)				
Count	Output			
	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Reset count (see note 2)							
Reset inputs				Output			
R <sub>O</sub> (1)	R <sub>O</sub> (2)	R <sub>9</sub> (1)	R <sub>9</sub> (2)	D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NC - No internal connection.

## NOTES:

1. Output A connected to input BD for BCD count.
2. X indicates that either a logical H or a logical L may be present.
3. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.
4. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
5. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

FIGURE 3. Truth tables - Continued.

DEVICE TYPE 08 TRUTH TABLE

Inputs at time $t_n$										Outputs at time $T_{n+1}$						
Count up	Count down	Load	A	B	C	D	Clear	$Q_A$	$Q_B$	$Q_C$	$Q_D$	Carry	Count down	Count up	Borrow	
H	H	H	X	X	X	X	L	NC	NC	NC	NC	H	NC	NC	H	
H	H	H	X	X	X	X	H	L	L	L	L	H	NC	NC	H	
H	H	L	X	X	X	X	L	A	B	C	D	L if count = 9 H if count > 9	NC	NC	L if count = 0 H if count ≠ 0	
P	H	H	X	X	X	X	L	Previous count plus 1 (note 1)			L if count = 9 H if count > 9	NC	NC	NA		
H	P	H	X	X	X	X	L	Previous count minus 1 (note 2)			NC	NC	NA	L is count = 0 H if count ≠ 0		

## NOTES:

1. See up count sequence table.
2. See down count sequence table.
3. L =  $V_{IL}$  for inputs,  $V_{OL}$  for outputs.
4. H =  $V_{IH}$  for inputs,  $V_{OH}$  for outputs.
5. X =  $V_{IH}$  or  $V_{IL}$ .
6. NC = no change.
7. NA = not applicable.
8. P = Positive going pulse.

FIGURE 3. Truth tables - Continued.

## DEVICE TYPE 08

UP COUNT SEQUENCE TABLE

Q <sub>A</sub> (LSB)	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub> (MSB)	Carry
L	L	L	L	H
H	L	L	L	H
L	H	L	L	H
H	H	L	L	H
L	L	H	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	L	H
L	L	L	H	H
H	L	L	H	L

DOWN COUNT SEQUENCE TABLE

Q <sub>A</sub> (LSB)	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub> (MSB)	Borrow
H	L	L	H	H
L	L	L	H	H
H	H	H	L	H
L	H	H	L	H
H	L	H	L	H
L	L	H	L	H
H	H	L	L	H
L	H	L	L	H
H	L	L	L	H
L	L	L	L	L

FIGURE 3. Truth tables - Continued.

DEVICE TYPE 09 TRUTH TABLE

Inputs at time $t_n$										Outputs at time $T_{n+1}$					
Count up	Count down	Load	A	B	C	D	Clear	$Q_A$	$Q_B$	$Q_C$	$Q_D$	Carry		Borrow	
H	H	H	X	X	X	X	L	NC	NC	NC	NC	H		H	
H	H	H	X	X	X	X	H	L	L	L	L	H		H	
H	H	L	X	X	X	X	L	A	B	C	D	Count up L if count = 15 H if count > 15	Count down NC	Count up NC	Count down L if count = 0 H if count $\neq$ 0
P	H	H	X	X	X	X	L	Previous count plus 1 (note 1)			L if count = 15 H if count > 15		NC	NC	NA
H	P	H	X	X	X	X	L	Previous count minus 1 (note 2)			NA		NC	NC	L is count = 0 H if count $\neq$ 0

## NOTES:

- See up count sequence table.
- See down count sequence table.
- L =  $V_{IL}$  for inputs,  $V_{OL}$  for outputs.
- H =  $V_{IH}$  for inputs,  $V_{OH}$  for outputs.
- X =  $V_{IH}$  or  $V_{IL}$ .
- NC = no change.
- NA = not applicable.
- P = Positive going pulse.

FIGURE 3. Truth tables - Continued.

## DEVICE TYPE 09

UP COUNT SEQUENCE TABLE

QA (LSB)	QB	QC	QD (MSB)	Carry
L	L	L	L	H
H	L	L	L	H
L	H	L	L	H
H	H	L	L	H
L	L	H	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	L	H
L	L	L	H	H
H	L	L	H	H
L	H	L	H	H
H	H	L	H	H
L	L	H	H	H
H	L	H	H	H
L	H	H	H	H
H	H	H	H	L

DOWN COUNT SEQUENCE TABLE

QA (LSB)	QB	QC	QD (MSB)	Borrow
H	H	H	H	H
L	H	H	H	H
H	L	H	H	H
L	L	H	H	H
H	H	L	H	H
L	H	L	H	H
H	L	L	H	H
L	L	L	H	H
H	H	H	L	H
L	H	H	L	H
H	L	H	L	H
L	L	H	L	H
H	H	L	L	H
L	H	L	L	H
H	L	L	L	H
L	L	L	L	L

FIGURE 3. Truth tables - Continued.

DEVICE TYPES 03 AND 05: SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.

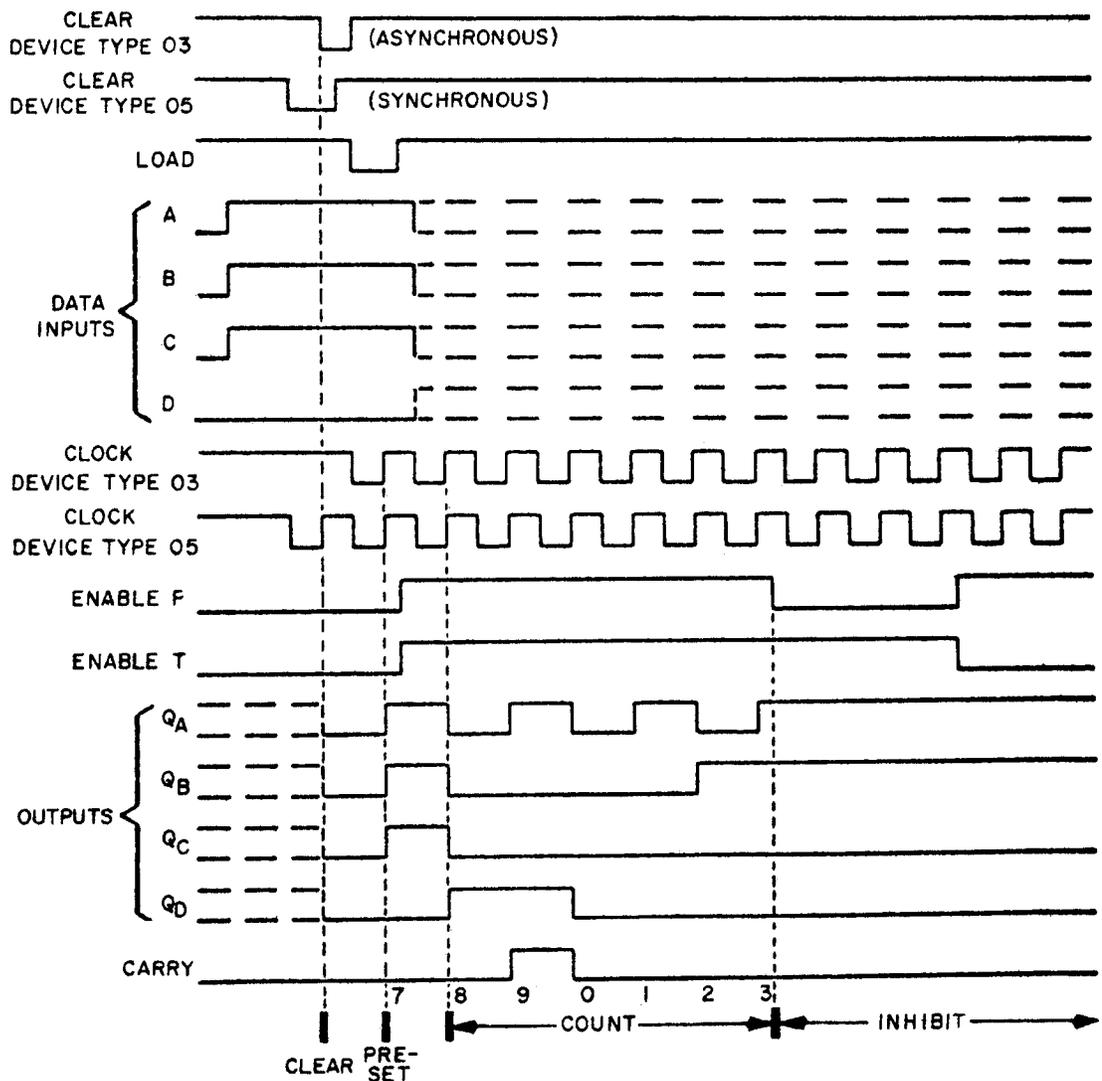


FIGURE 4. Timing diagrams.

DEVICE TYPES 04 AND 06: SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences.

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

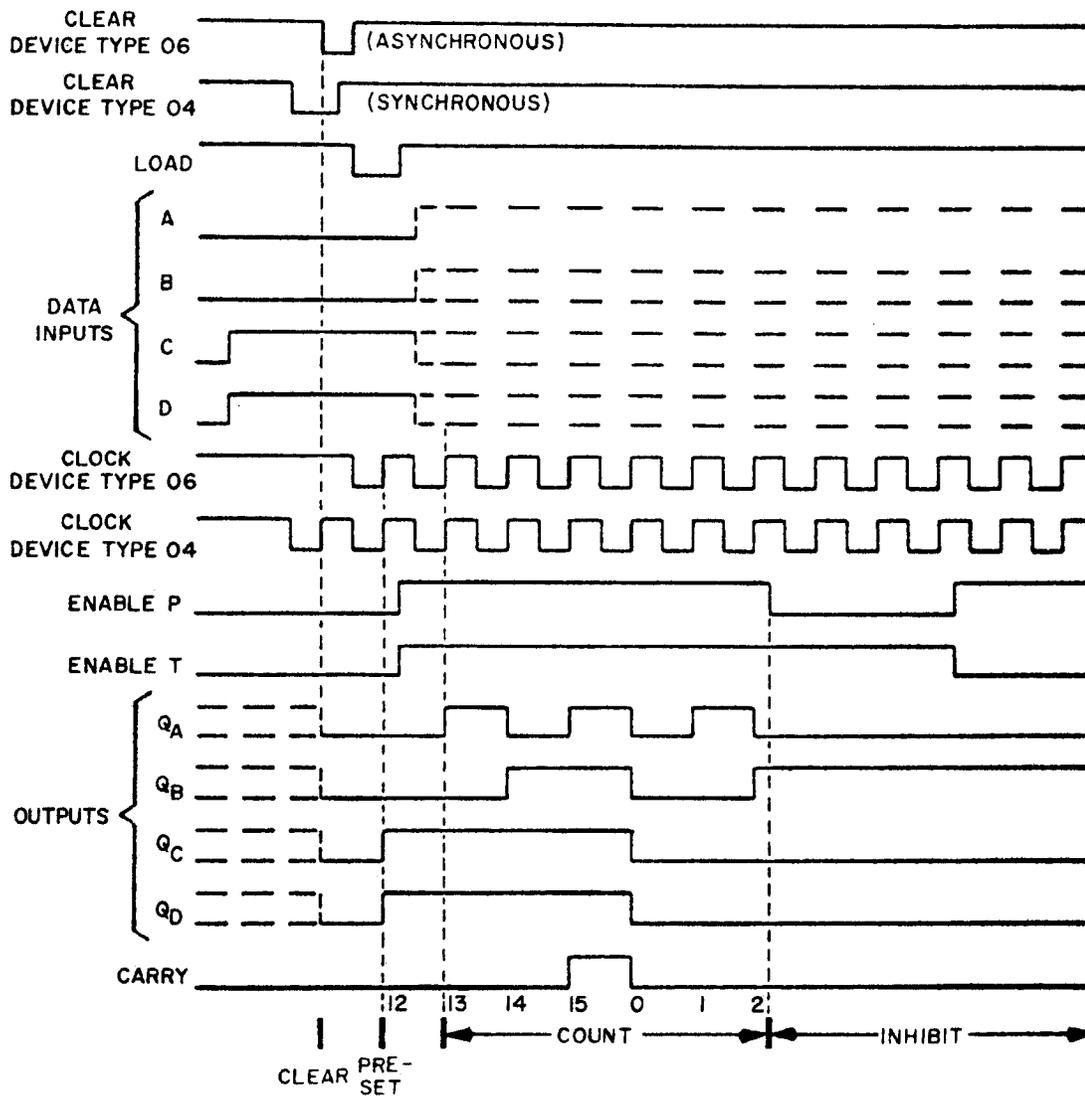
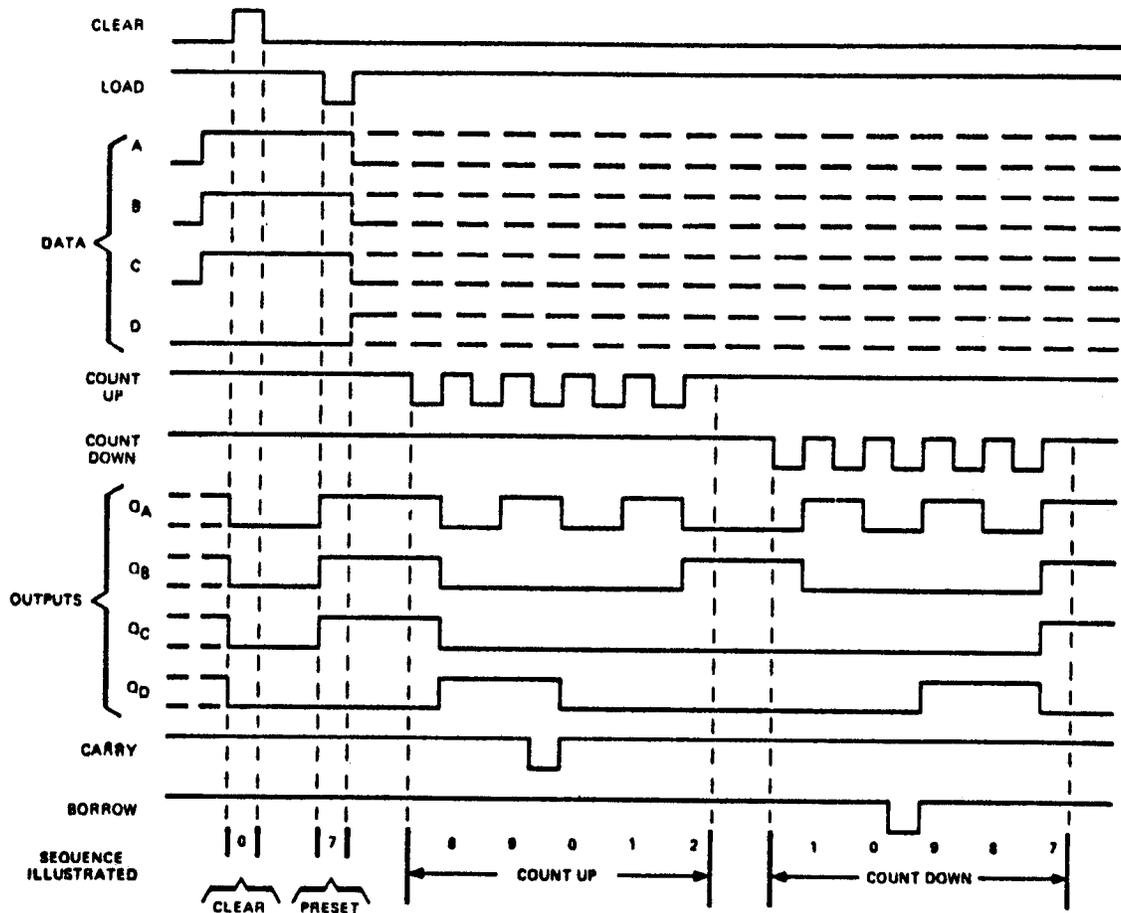


FIGURE 4. Timing diagrams - Continued.

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



DEVICE TYPE 08 SYNCHRONOUS DECADE COUNTER

NOTES:

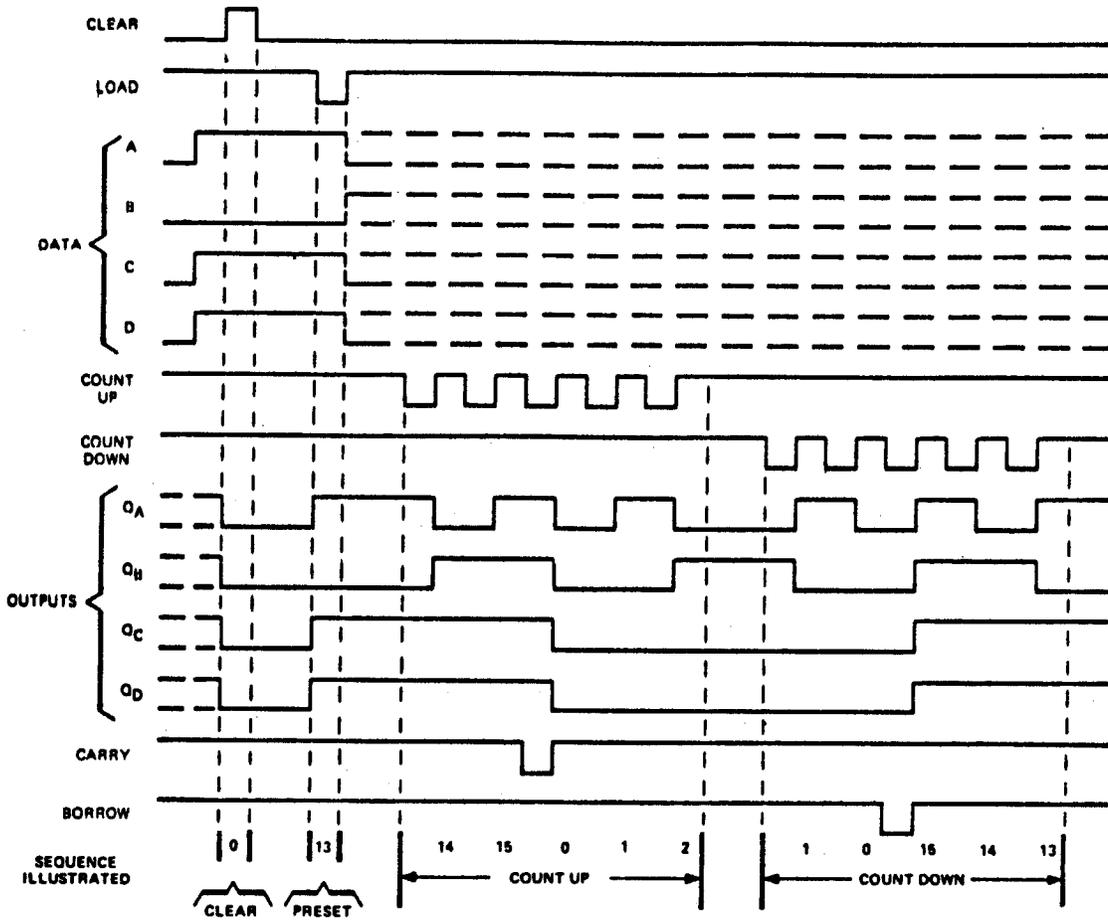
- A. Clear overrides load, data, and count inputs.
- B. When counting up, count down input must be high; when counting down, count-up input must be high.

FIGURE 4. Timing diagrams - Continued.

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



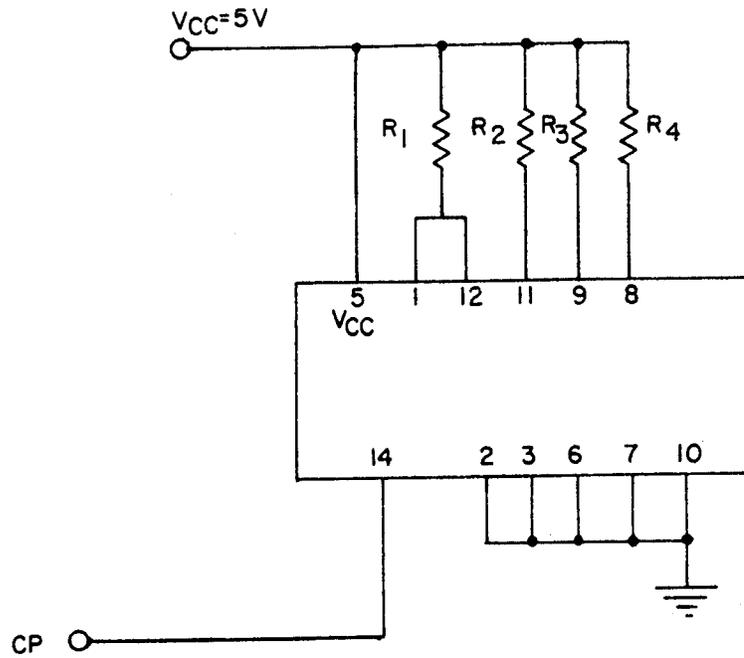
DEVICE TYPE 09: SYNCHRONOUS BINARY COUNTER

NOTES:

- A. Clear overrides load, data, and count inputs.
- B. When counting up, count-down input must be high; when counting down, count-up input must be high.

FIGURE 4. Timing diagrams - Continued.

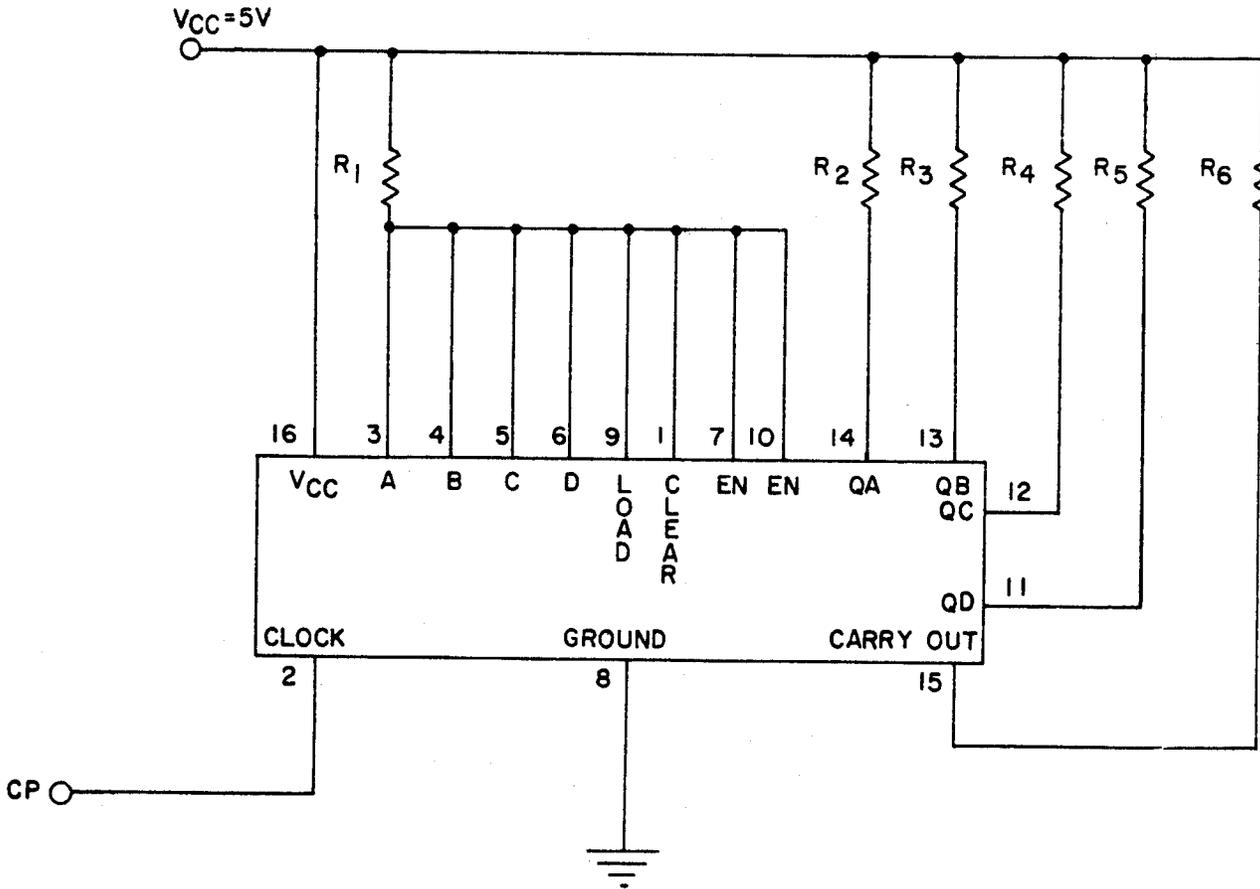
Device types 01, 02, and 07



CP: 100 kHz square wave; 0-3 V  
 $R_1$  thru  $R_4 = 220 \Omega \pm 5\%$

FIGURE 5. Burn-in and life test circuits.

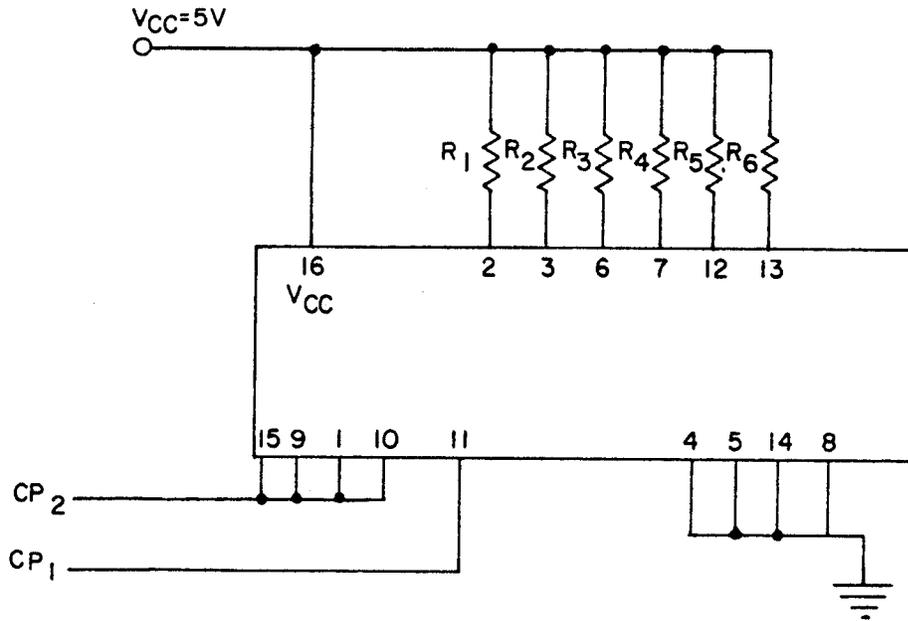
Device types 03, 04, 05, and 06



CP: 100 kHz square wave; 0-3 V  
 R<sub>1</sub> thru R<sub>6</sub> = 270 Ω ± 5%

FIGURE 5. Burn-in and life test circuits - Continued.

Device types 08 and 09



$R_1$  thru  $R_6 = 270 \Omega \pm 5\%$

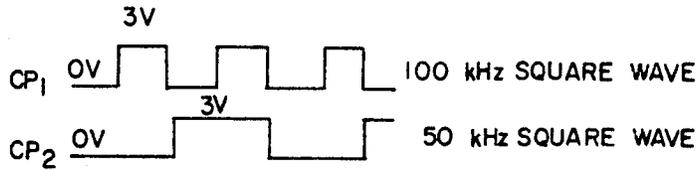
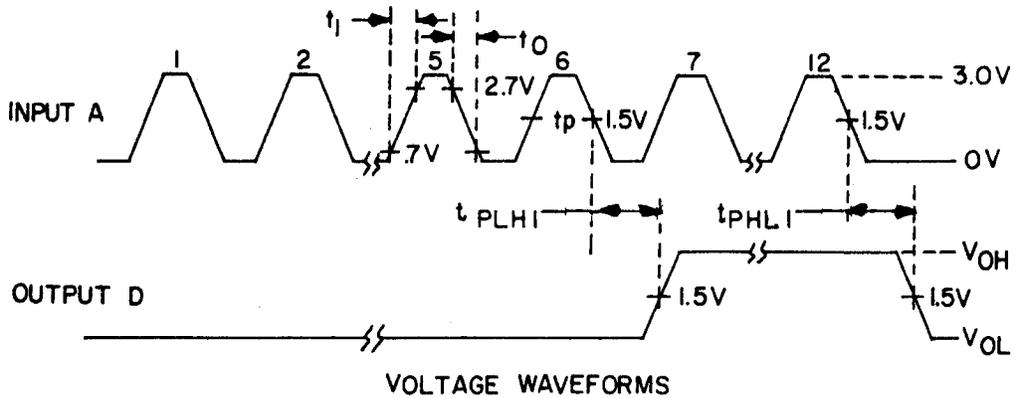
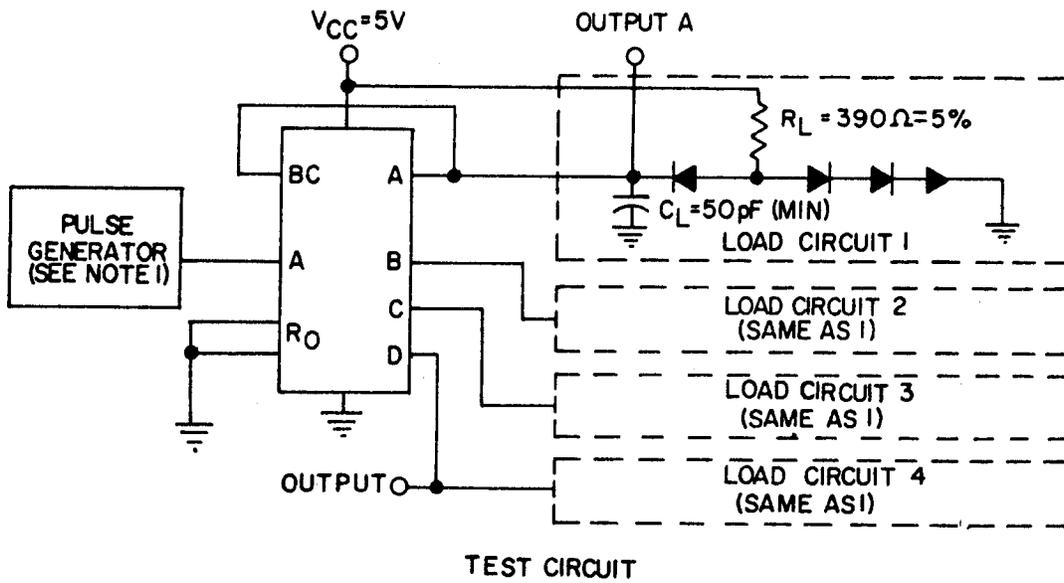


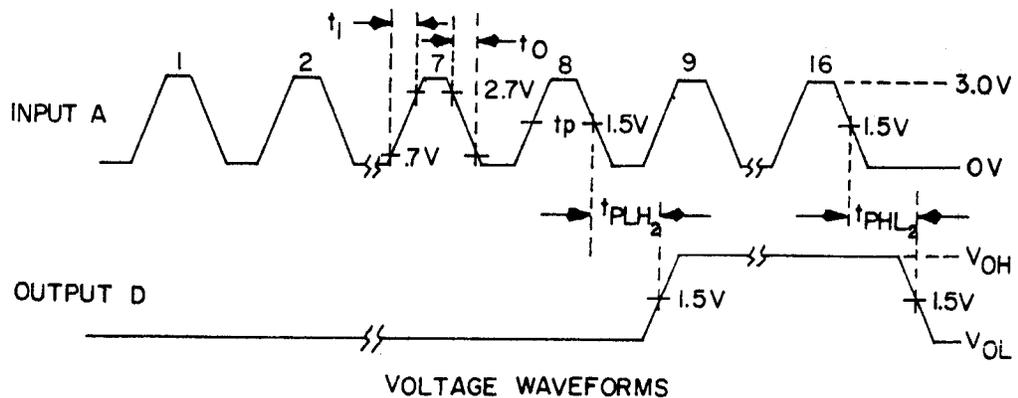
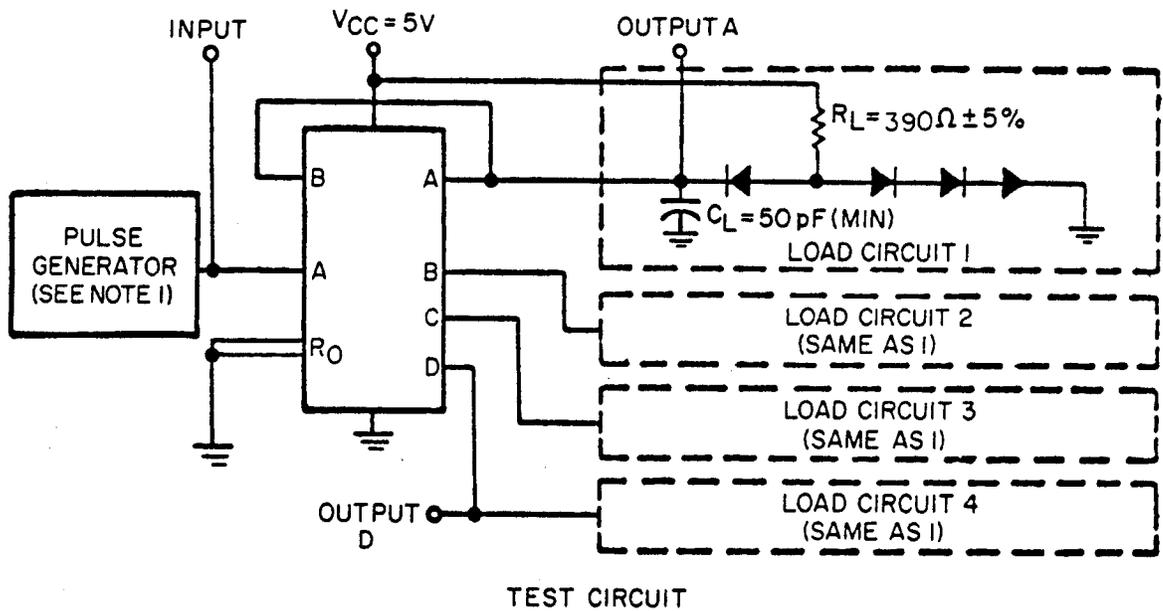
FIGURE 5. Burn-in and life test circuits - Continued.



**NOTES:**

1. The pulse generator has the following characteristics:  $V_{gen} = 3\text{ V}$ ,  $t_0 = t_1 \leq 15\text{ ns}$ ,  
 $t_p = .5\text{ }\mu\text{s}$ ,  $\text{PRR} = 1\text{ MHz}$ ,  $Z_{out} \approx 50\Omega$ .
2. All diodes are 1N3064, or equivalent.
3.  $C_L$  includes probe and jig capacitance.
4. Voltage values are with respect to ground terminal.
5.  $F_{MAX}$  pulse generator has the following characteristics:  $V_{gen} = 3.0\text{ V} \pm 0.2\text{ V}$ ,  $t_0 = t_1 \leq 10\text{ ns}$ ,  
 $t_p = 50\text{ ns}$ ,  $\text{PRR} = 10\text{ MHz}$ .

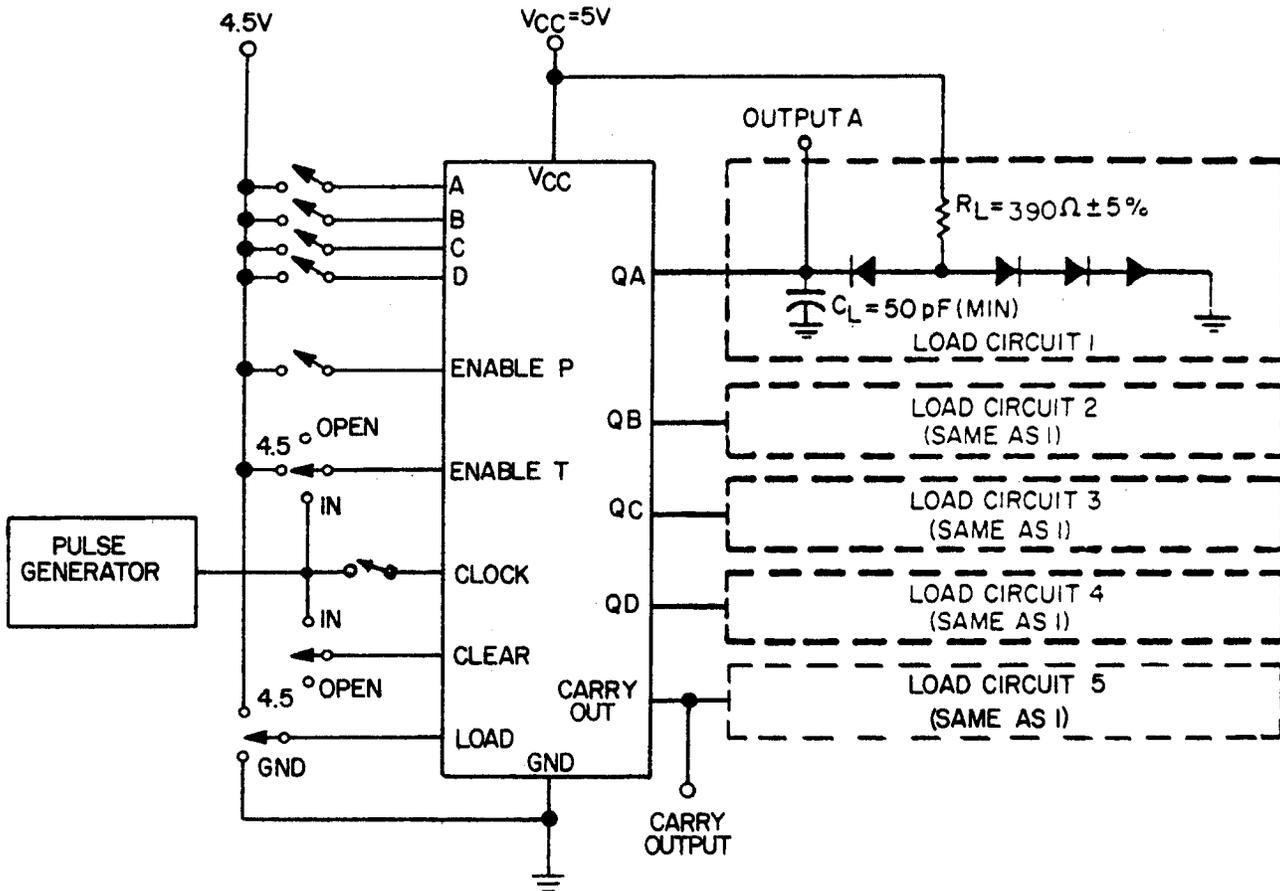
FIGURE 6. Switching time test circuits and waveforms for device type 01.



## NOTES:

1. The pulse generator has the following characteristics:  $V_{gen} = 3\text{ V}$ ,  $t_0 = t_1 < 15\text{ ns}$ ,  $t_p = .5\text{ }\mu\text{s}$ ,  $PRR = 1\text{ MHz}$ ,  $Z_{out} \approx 50\Omega$ .
2. All diodes are 1N3064 or equivalent.
3.  $C_L$  includes probe and jig capacitance.
4. Voltage values are with respect to ground terminal.
5.  $F_{MAX}$  pulse generator has the following characteristics:  $V_{gen} = 3.0\text{ V} \pm 0.2\text{ V}$ ,  $t_0 = t_1 \leq 10\text{ ns}$ ,  $t_p = 50\text{ ns}$ ,  $PRR = 10\text{ MHz}$ .

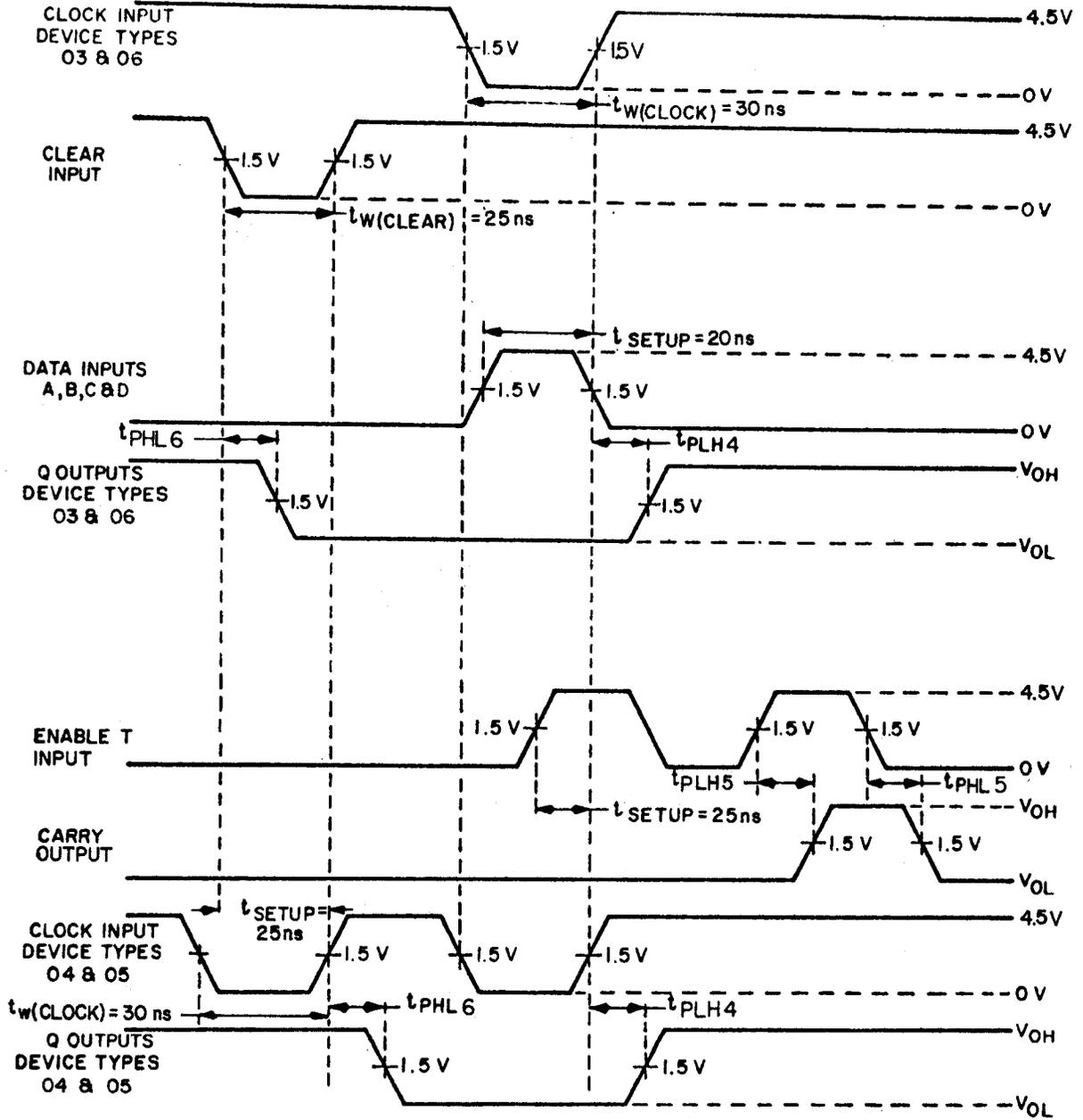
FIGURE 7. Switching time test circuit and waveforms for device type 02.



## NOTES:

1. The pulse generator has the following characteristics:  $t_r < 10$  ns,  $t_f < 10$  ns, PRR  $< 1$  MHz, duty cycle  $< 50\%$ ,  $Z_{out} \approx 50\Omega$ .
2. All diodes are 1N3064, or equivalent.
3.  $C_L$  includes probe and jig capacitance.
4. Voltage values are with respect to ground terminal.
5. Load circuits on a given output are only required where the specific test given in table III indicates "OUT" on that output. Load circuits may otherwise be omitted.

FIGURE 8. Switching time test circuits and waveform for device types 03, 04, 05, and 06.

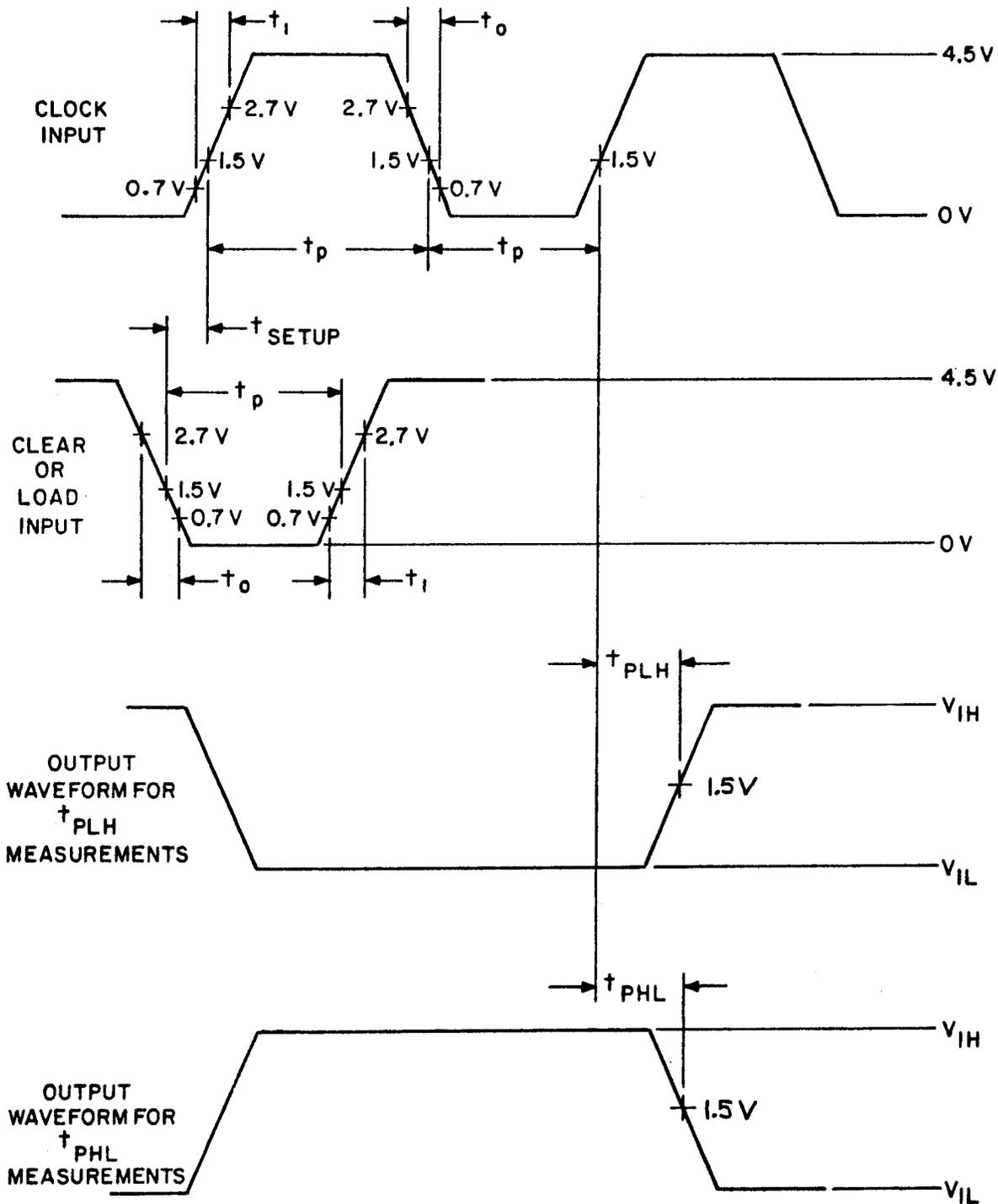


VOLTAGE WAVEFORMS

NOTES:

1. The input pulses are supplied by a generator having the following characteristics:  $t_r < 10 \text{ ns}$ ,  $t_f < 10 \text{ ns}$ ,  $\text{PRR} < 1 \text{ MHz}$ ,  $Z_{\text{out}} \approx 50 \Omega$ .
2. Enable T duty cycle  $\leq 50\%$ ,  $\text{PRR} = 1 \text{ MHz}$ .

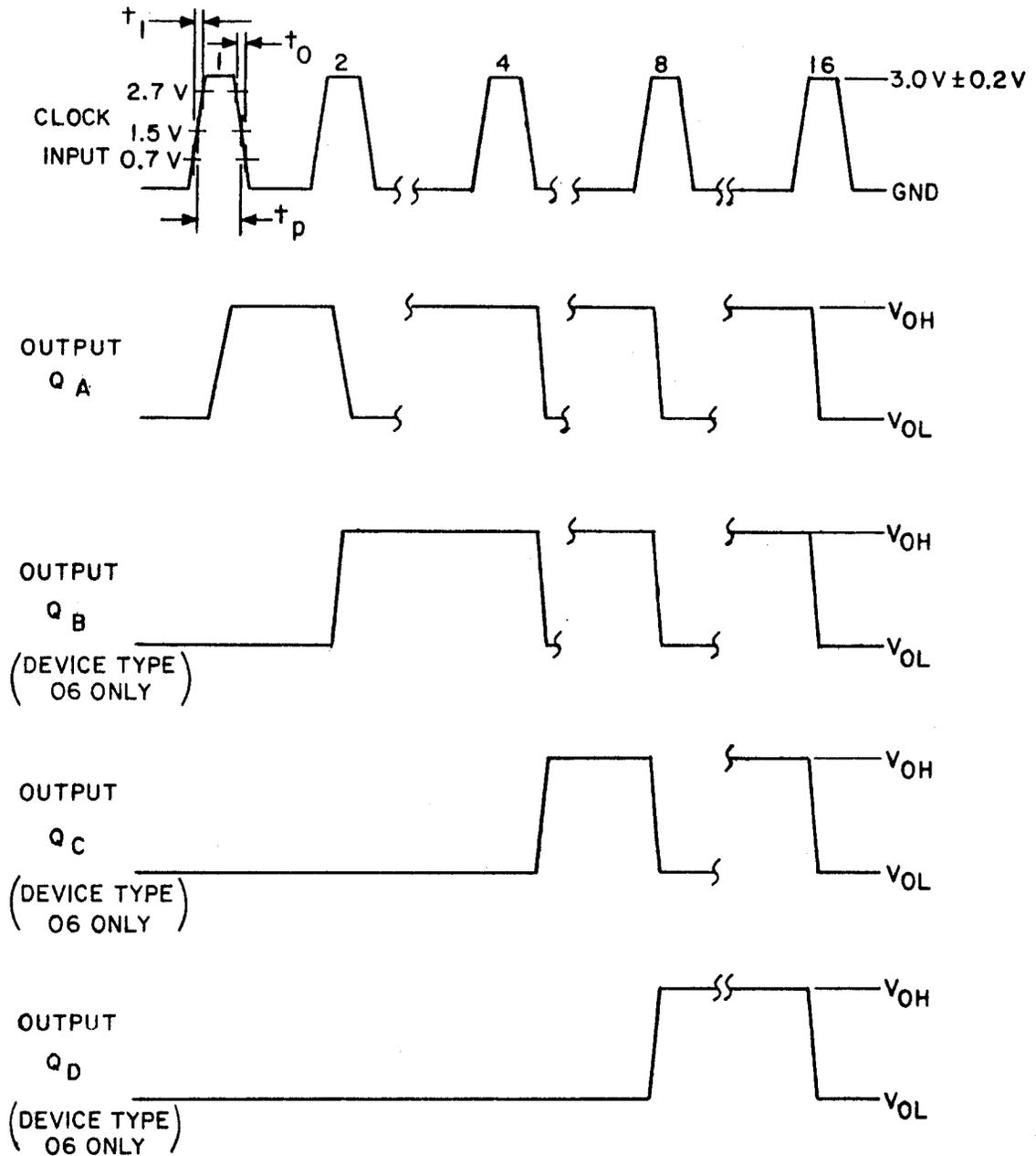
FIGURE 8A. Switching time test circuits and waveforms for device types 03, 04, 05, and 06 - Continued.



## NOTES:

- The input pulses are supplied by generators having the following characteristics:  
 $t_o = t_i \leq 10$  ns,  $PRR \leq 1.0$  MHz,  $t_p \leq 500$  ns,  $Z_{out} \approx 50\Omega$ .
- The  $t_{SETUP}$  for load pulse = 30 ns;  $t_{SETUP}$  for clear pulse = 25 ns.

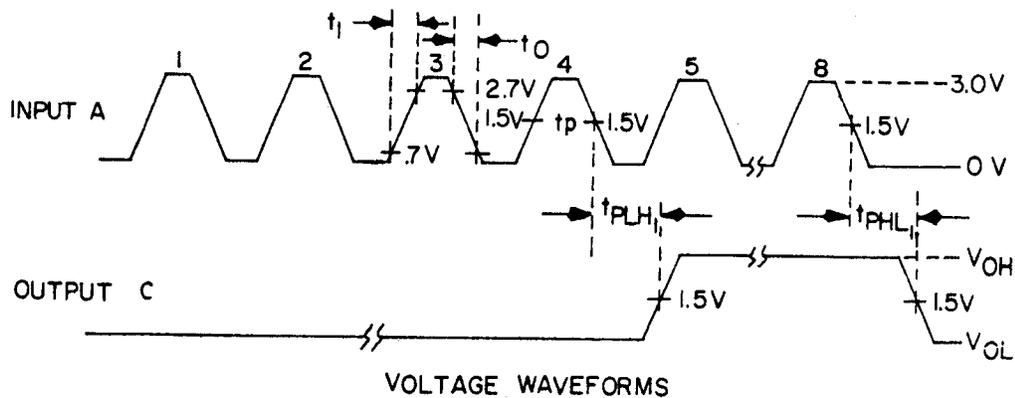
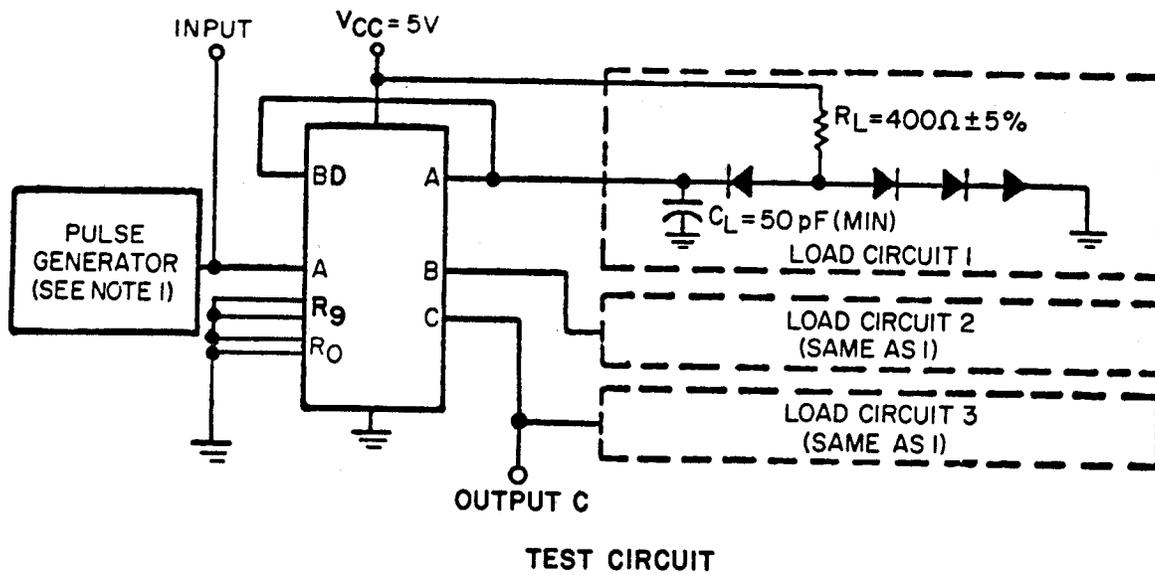
FIGURE 8B. Switching time test circuits and waveforms for device types 03, 04, 05 and 06.



## NOTES:

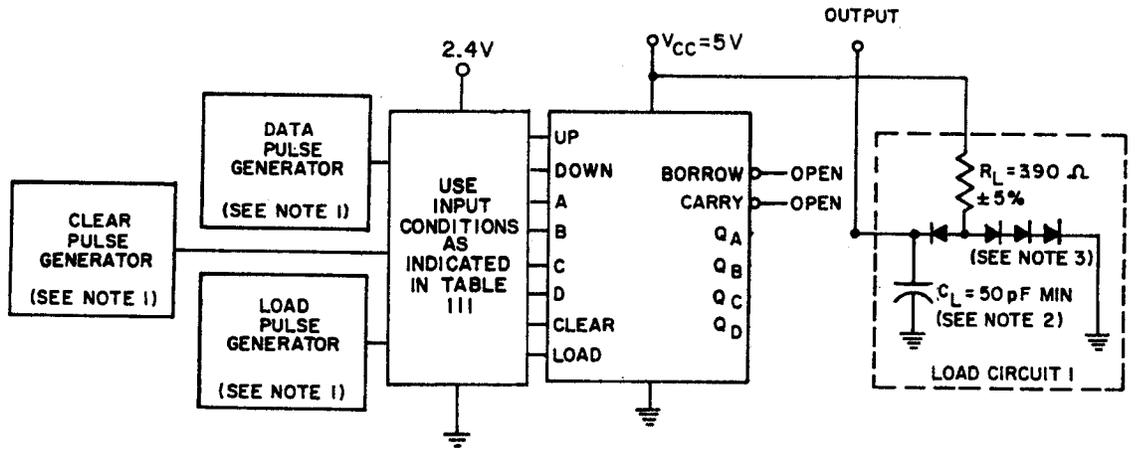
1. The pulse generator has the following characteristics:  $t_0 = t_1 = 5 \pm 1$  nsec,  $t_p = 20$  ns,  $V_{gen} = 4.5$  V,  $Z_{out} \approx 50\Omega$ , PRR = 20 MHz.
2. The output frequency shall be:
  - a. Output Q<sub>A</sub> = one-half the input frequency.
  - b. Output Q<sub>B</sub> = one-quarter the input frequency.
  - c. Output Q<sub>C</sub> = one-eighth the input frequency.
  - d. Output Q<sub>D</sub> = one-sixteenth the input frequency.

FIGURE 8C.  $F_{max}$  waveforms for device types 03, 04, 05 and 06.

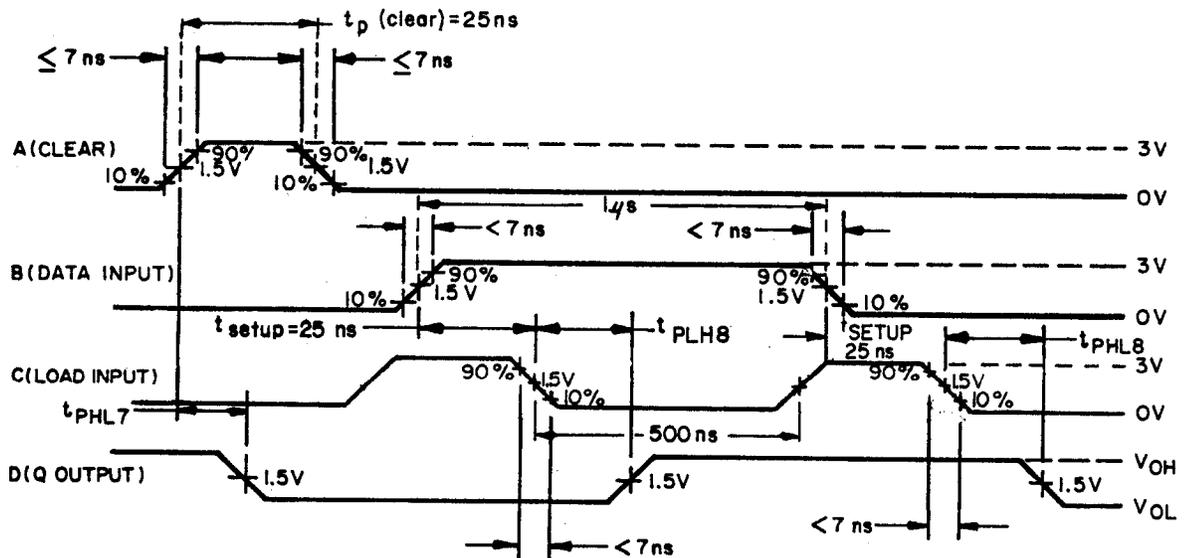
**NOTES:**

1. The pulse generator has the following characteristics:  $V_{gen} = 3\text{ V}$ ,  $t_0 = t_1 \leq 15\text{ ns}$ ,  $t_p = .5\text{ }\mu\text{s}$ ,  $\text{PRR} = 1\text{ MHz}$ ,  $Z_{out} \approx 50\Omega$ .
2. All diodes are 1N3064 or equivalent.
3.  $C_L$  includes probe and jig capacitance.
4. Voltage values are with respect to ground terminal.
5.  $F_{MAX}$  pulse generator has the following characteristics:  $V_{gen} = 3.0\text{ V} \pm 0.2\text{ V}$ ,  $t_0 = t_1 \leq 10\text{ ns}$ ,  $t_p = 50\text{ ns}$ ,  $\text{PRR} = 10\text{ MHz}$ .

FIGURE 9. Switching time test circuit and waveforms for device type 07.



TEST CIRCUIT

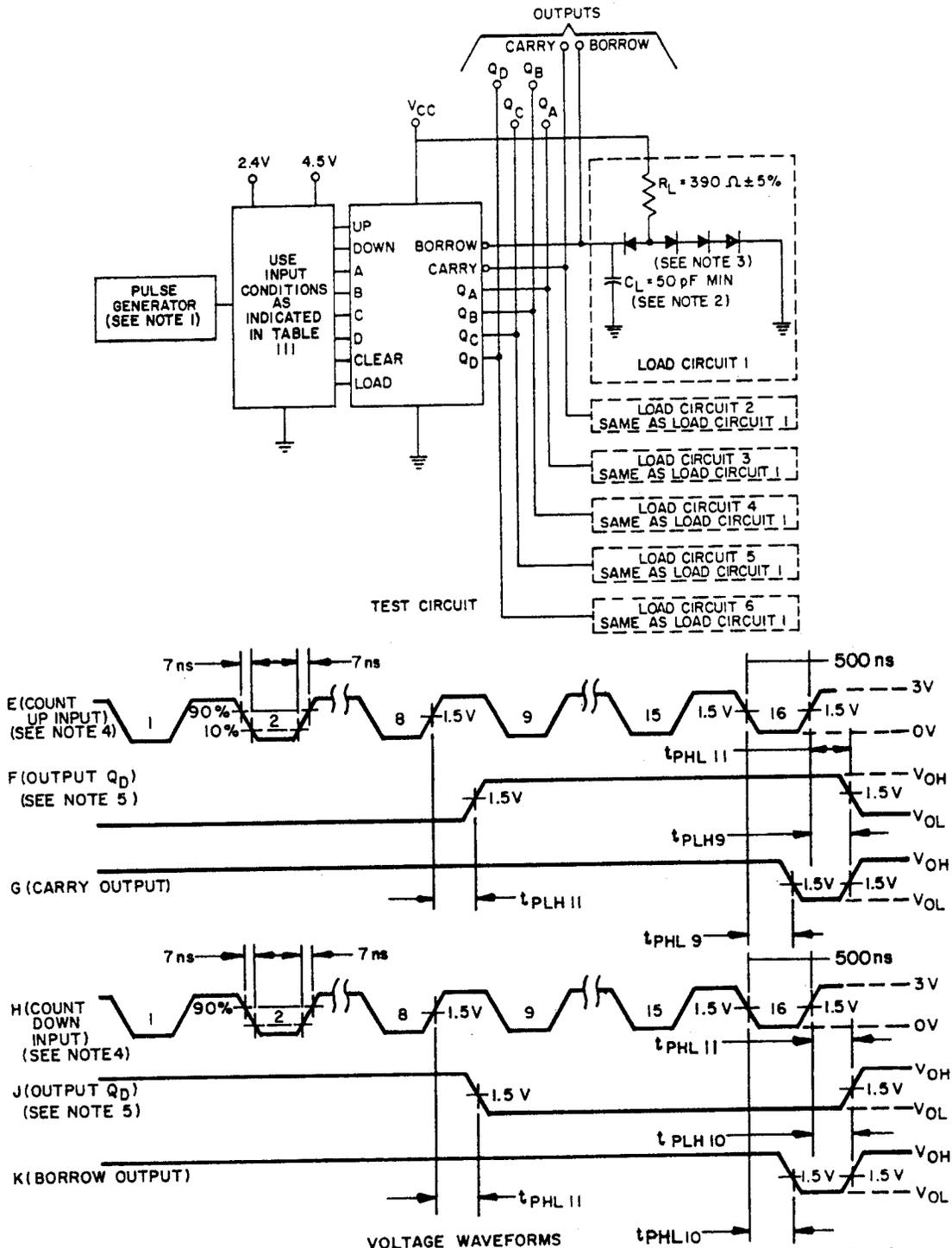


VOLTAGE WAVEFORMS

NOTES:

1. The pulse generators have the following characteristics:  $Z_{out} \approx 50 \Omega$ ; for the data pulse generator,  $PRR = 500 \text{ kHz}$ , duty cycle = 50%; for the load pulse generator,  $PRR = 1 \text{ MHz}$ , duty cycle = 50%.
2.  $C_L$  includes probe and jig capacitance.
3. All diodes are 1N3064, or equivalent.

FIGURE 10. Switching time test circuits and waveforms for device types 08 and 09.



NOTES:

1. The pulse generator has the following characteristics: PRR = 1 MHz, Z<sub>out</sub> ≈ 50 Ω, duty cycle = 50%.
2. C<sub>L</sub> includes probe and jig capacitance.
3. All diodes are 1N3064, or equivalent.
4. Count-up and count-down pulse shown are for device type 09 binary counters. Count cycle for the device type 08 decade counter is 1 through 10.
5. Waveforms for outputs Q<sub>A</sub>, Q<sub>B</sub>, and Q<sub>C</sub> are omitted to simplify the drawing.
6. Load circuits on a given output are only required where the specific test given in table III indicates "OUT" on that output. Load circuits may otherwise be omitted.

FIGURE 10A. Switching time test circuits and waveforms for device types 08 and 09.



TABLE III. Group A inspection for device type 01 - Continued.  
Terminal conditions 13/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits				
				Input BC	NC	NC	NC	VCC	R <sub>0</sub> (1)	R <sub>0</sub> (2)	Output D	Output C	GND	Output B	Output A	NC	Input A	Meas. terminal	Min	Max	Unit	
7 TC = 25°C	Func-tional tests 4/	3014	30	B 3/	NC	NC	NC	4.5 V	A 3/	A 3/	L	L	GND	L	L	NC	B 3/	}	See 5/			
				A	NC	NC	NC	4.5 V	A 3/	A 3/	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				A	NC	NC	NC	4.5 V	A	A	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				A	NC	NC	NC	4.5 V	A	A	L	L	GND	L	L	GND	L				NC	B 3/
				A	NC	NC	NC	4.5 V	A	A	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				A	NC	NC	NC	4.5 V	A	A	L	L	GND	L	L	GND	L				NC	B 3/
				A	NC	NC	NC	4.5 V	A	A	L	L	GND	L	L	GND	L				NC	B 3/
				B	NC	NC	NC	4.5 V	B	B	L	L	GND	L	L	GND	L				NC	B 3/
				8	Repeat subgroup 7 at TC = 125°C and TC = -55°C.																	

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.  
Terminal conditions 13/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D		Case C		1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits		
			Test No.	Input BC	NC	NC	VCC	R <sub>0</sub> (1)	R <sub>0</sub> (2)	Output D	Output C	Output B	Output A	NC	Input	Meas. terminal	Min	Max	Unit				
9 T <sub>C</sub> = 25°C	F <sub>MAX</sub> 9/	Fig 6																					
	t <sub>PLH1</sub>	↓																					
	t <sub>PHL1</sub>	↓																					
10 T <sub>C</sub> = 125°C	F <sub>MAX</sub> 9/	Fig 6																					
	t <sub>PLH1</sub>	↓																					
	t <sub>PHL1</sub>	↓																					
11	Same tests, terminal conditions and limits as for subgroup 10, except T <sub>C</sub> = -55°C.																						

- 1/ Momentarily apply 2.4 V, then ground prior to taking measurements to set the device in desired state. Maintain ground for measurement.
- 2/ Apply 4.5 V pulse then ground prior to taking measurements to set the device in the desired state. Maintain ground for measurement.
- 3/ A ≥ 2.0 V, B ≤ 0.8 V. Input voltages shown are the maximum for VIH and the minimum for VIL.
- 4/ Only a summary of attributes data is required.
- 5/ Output voltages shall be either:
  - (a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or
  - (b) H ≥ 1.5 volts and L ≤ 1.5 volts when using a high speed checker single comparator.
- 6/ Input must be applied 3 times after R<sub>0</sub> pulses.
- 7/ Input must be applied 2 times after R<sub>0</sub> pulses.
- 8/ Input must be applied once after R<sub>0</sub> pulses.
- 9/ F<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- 10/ Connect terminals together during test.
- 11/ See test figure 6 for terminal load.
- 12/ Omit specified loads for this test.
- 13/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
- 14/ The limits shown shall be as follows:

Test	Min/Max limits (ma) for circuit:				
	A	B	C	D	E
I <sub>IL1</sub>	-0.4/-1.3	-0.7/-1.6	-0.3/-1.3	-0.7/-1.6	-0.7/-1.6
I <sub>IL2</sub>	-1.4/-3.2	-0.4/-1.3	-0.7/-3.2	-0.7/-3.2	-0.7/-3.2
I <sub>IL3</sub>	-1.4/-4.8	-0.4/-1.3	-0.7/-4.8	-1.4/-6.4	-1.4/-6.4

TABLE III. Group A inspection for device type 02.  
Terminal conditions 13/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D			Case C			Case A, B, D			Case C			Meas. terminal		Test limits			
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	Min	Max	Unit	
1 T <sub>C</sub> = 25°C	VOL	3007	Input B GND 2.0 V 2.0 V 2.0 V	R <sub>0</sub> (1) 2.0 V	R <sub>0</sub> (2) 2.0 V	NC	V <sub>CC</sub> 4.5 V	NC	Output C 16 mA	Output B 16 mA	GND	Output D 16 mA	Output A 16 mA	NC	Input A 2.0 V GND GND GND	Output A Output B Output C Output D	0.4		V	
	VOH	3006	GND 1/6/ 1/7/ 1/8/	1/	1/				Output C -400 μA			Output D -400 μA			1/6/ GND GND GND	Output A Output B Output C Output D	2.4		V	
	I <sub>OS</sub>	3011	GND 2/6/ 2/7/ 2/8/	2/	2/		5.5 V		GND			GND			2/6/ GND GND GND	Output A Output B Output C Output D	-20	-57	mA	
	I <sub>IH1</sub>	3010	2.4 V	2.4 V	GND											R <sub>0</sub> (1)	40	40	μA	
	I <sub>IH1</sub>		2.4 V	GND	2.4 V												R <sub>0</sub> (2)	40	40	μA
	I <sub>IH2</sub>		5.5 V	5.5 V	GND												R <sub>0</sub> (1)	100	100	μA
	I <sub>IH2</sub>		5.5 V	GND	5.5 V												R <sub>0</sub> (2)	100	100	μA
	I <sub>IH7</sub>		2.4 V	2.4 V													Input A	80	80	μA
	I <sub>IH7</sub>		5.5 V	5.5 V													Input B	80	80	μA
	I <sub>IH8</sub>		2.4 V	2.4 V													Input A	200	200	μA
	I <sub>IH8</sub>		5.5 V	5.5 V													Input B	200	200	μA
	I <sub>IL1</sub>	3009	0.4 V	0.4 V	4.5 V											R <sub>0</sub> (1)	14/	14/	mA	
	I <sub>IL1</sub>		4.5 V	4.5 V	0.4 V												R <sub>0</sub> (2)	14/	14/	mA
	I <sub>IL2</sub>		2/	2/	2/												Input A			
	I <sub>IL3</sub>		2/	2/	2/												Input B			
	I <sub>CC</sub>	3005	GND	2/	2/											V <sub>CC</sub>	44	44	mA	
	V <sub>IC</sub>			-12 mA	-12 mA	-12 mA		4.5 V								Input A Input B R <sub>0</sub> (1) R <sub>0</sub> (2)	-1.5	-1.5	V	
	2	Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = 125°C and V <sub>IC</sub> tests are omitted.																		
	3	Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = -55°C and V <sub>IC</sub> tests are omitted.																		

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.  
Terminal conditions 13/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D Case C	Test No.	Terminal conditions 13/														Test limits								
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit					
					R <sub>0</sub> (1)	R <sub>0</sub> (2)	NC	V <sub>CC</sub>	NC	Output C	Output B	GND	Output D	Output A	NC	Input A											
7 T <sub>C</sub> = 25°C	Func-tional tests 4/	3014	30	B 5/	A 5/	A 5/	NC	V <sub>CC</sub> 4.5 V	NC	L	L	GND	L	L	NC	B 5/											
				A																							
				B																							
				B																							
				B																							
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				B																							
				B																							
				B																							
				B																							
				8	Repeat subgroup 7 at T <sub>C</sub> = 125°C and T <sub>C</sub> = -55°C.																						

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.  
Terminal conditions 13/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D		Case C		Terminal conditions 13/														Test limits	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit		
9 T <sub>C</sub> = 25°C	F <sub>MAX</sub> 9/	Fig 7	Input	R <sub>0</sub> (1)	R <sub>0</sub> (2)	NC	VCC	NC	NC	Output C	Output B	GND	Output D	Output A	NC	Input A	Output A	10		MHz		
	t <sub>PLH2</sub>	↓	10/	GND	GND		5.0 V			12/	11/	↓	OUT 11/	OUT 11/		IN	Output D	20	135	ns		
	t <sub>PHL2</sub>	↓	10/	↓	↓					11/	11/		OUT 11/	OUT 11/		IN	Output D	20	135	ns		
10 T <sub>C</sub> = 125°C	F <sub>MAX</sub> 9/	Fig 7															Output A	10		MHz		
	t <sub>PLH2</sub>	↓	10/	↓	↓					12/	11/	↓	OUT 11/	OUT 11/		IN	Output D	20	135	ns		
11																	Output D	20	135	ns		

- 1/ Momentarily apply 2.4 V, then ground prior to taking measurements to set the device in desired state. Maintain ground for measurement.
- 2/ Apply 4.5 V pulse, then ground prior to taking measurements to set the device in desired state. Maintain ground for measurement.
- 3/ Output voltages shall be either:  
 (a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or  
 (b) H ≥ 1.5 volts and L ≤ 1.5 volts when using a high speed checker single comparator.
- 4/ Only a summary of attributes data is required.
- 5/ A ≥ 2.0 V, B ≈ 0.8 V. Input voltages shown are the maximum for V<sub>IL</sub> and the minimum for V<sub>IH</sub>.
- 6/ Input pulse must be applied 1 time after R<sub>0</sub> pulses.
- 7/ Input pulse must be applied 2 times after R<sub>0</sub> pulses.
- 8/ Input pulse must be applied 4 times after R<sub>0</sub> pulses.
- 9/ F<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency. Connect terminals together during test.
- 10/ See test figure 7 for terminal load.
- 11/ Omit specified loads for this test.
- 12/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
- 13/ The limits shown are as follows:

Test	Min/Max limits (mA) for circuit:				
	A	B	C	D	E
I <sub>IL1</sub>	-0.4/-1.3	-0.7/-1.6	-0.4/-1.3	-0.7/-1.6	-0.7/-1.6
I <sub>IL2</sub>	-0.7/-3.2	-0.4/-1.3	-0.7/-3.2	-0.7/-3.2	-0.7/-3.2
I <sub>IL3</sub>	-0.7/-3.2	-0.4/-1.3	-0.7/-3.2	-0.7/-3.2	-0.7/-3.2

TABLE III. Group A inspection for device type 03.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3			7	8	9	10	11	12	13	14	15	16	Test limits			
						A	B	C											D	Meas. terminal	Min	Max
1 T <sub>C</sub> = 25°C	V <sub>OH</sub>	3006	1	Clear	Clock						GND		-800 μA	Output QD	Output QA	Carry output	4.5 V		2.4	V		
			2		1/		2.0 V															
			3				2.0 V	2.0 V				2.0 V										
			4				2.0 V	0.8 V														
			5				0.8 V	0.8 V														
			6					0.8 V	0.8 V			0.8 V										
			7																			
			8																			
			9																			
			10																			
		11																				
		12																				
		13																				
		14																				
		15																				
		16																				
		17																				
		18																				
		19																				
		20																				
	I <sub>H9</sub>	3010	20																			
	I <sub>H9</sub>		21																			
	I <sub>H10</sub>		22																			
	I <sub>H10</sub>		23																			
	I <sub>H11</sub>		24																			
			25																			
			26																			
			27																			
			28																			
			29																			
			30																			
			31																			
	I <sub>HL12</sub>		32																			
			33																			
			34																			
			35																			
			36																			
			37																			
			38																			
	I <sub>HL5</sub>	3009	39																			
	I <sub>HL6</sub>		40																			
			41																			
			42																			
	I <sub>HL7</sub>		43																			
			44																			
			45																			
	I <sub>HL8</sub>		46																			

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.		1	2	3	DATA INPUTS		4	5	6	7	8	9	10	11	12	13	14	15	16		Test limits											
			Clear	Clock				A	B													C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Meas. terminal	Min
1 TC = 25°C	IOS	3011	47	4.5 V	1/				4.5 V						GND		GND																		
			48	4.5 V	↓				4.5 V								4.5 V																		
			49	4.5 V	↓				4.5 V																										
			50	4.5 V	↓				4.5 V																										
			51	4.5 V	↓				4.5 V																										
2	ICCH ICCH ICCL ICCL	3005	52	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V												
			53	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											
			54	GND	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND						
			55	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND						
3	Same tests, terminal conditions and limits as subgroup 1, except TC = 125°C and VIC tests are omitted.																																		
	Same tests, terminal conditions and limits as subgroup 1, except TC = -55°C and VIC tests are omitted.																																		
7 TC = 25°C	Functional tests 4/	3014	56	B 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/	A 5/								
			57	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
			58	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
			59	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
			60	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
			61	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
			62	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
			63	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
			64	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
			65	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
			66	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			67	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			68	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			69	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			70	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			71	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			72	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			73	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			74	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			75	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			76	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
77	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
78	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
79	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
80	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
81	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
82	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
83	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
84	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
85	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
86	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
87	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
88	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
89	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
90	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
91	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			

See footnotes at end of device type 03.



TABLE III. Group A inspection for device type 03 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
																				Meas. terminal	Min	Max	Unit	
7 T <sub>C</sub> = 25°C	Functional tests 4/	3014	143	A5/	B5/	B5/	B5/	A5/	B5/	A5/	GND	B5/	A5/	L	L	H	H	L	Carry output	V <sub>CC</sub>				
			144		A	A	A													L	4.5 V			
			145		A	A	A														L			
			146		B	A	A														L			
			147		A	A	A														L			
			148		A	A	A														L			
149		B	B	B														L						
150		A	A	B														L						
8	Repeat subgroup 7 at T <sub>C</sub> = 125°C and T <sub>C</sub> = -55°C.																					See 3/		
9 T <sub>C</sub> = 25°C	F <sub>MAX</sub> 6/ t <sub>PLH3</sub> t <sub>PHL3</sub> t <sub>PLH4</sub> t <sub>PHL4</sub> t <sub>PLH4</sub> t <sub>PHL4</sub> t <sub>PLH4</sub> t <sub>PHL4</sub> t <sub>PLH4</sub> t <sub>PHL4</sub> t <sub>PLH4</sub> t <sub>PHL4</sub> t <sub>PLH5</sub> t <sub>PHL5</sub> t <sub>PHL6</sub> t <sub>PHL6</sub> t <sub>PHL6</sub>	Fig 8 & 8C Fig 8 & 8B	151	4.5 V	IN	GND	GND	GND	4.5 V	4.5 V	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V								
			152																					
			153																					
			154																					
			155																					
			156																					
			157																					
			158																					
			159																					
			160																					
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166																								
167																								
168																								
169																								
170																								
171																								

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 Clear	2 Clock	3 A	4 DATA INPUTS			7 Enable P	8 GND	9 Load	10 Enable T	11 Output QD	12 Output QC	13 Output QB	14 Output QA	15 Carry output	16 VCC	Meas. terminal		Test limits	
							B	C	D											Min	Max	Unit	
10 TC = 125°C	FMAX 5/	Fig 8 & 8C	172	4.5 V	IN	GND	GND	4.5 V	4.5 V	GND	4.5 V	4.5 V					OUT	5.0 V	QA	20	58	MHz	
	tpLH3	Fig 8 & 8B	173			4.5 V	4.5 V	4.5 V			IN						OUT		Carry	3	58	ns	
	tpHL3		174			4.5 V	4.5 V	GND									OUT		Carry		38		
	tpHL4		175			4.5 V	4.5 V	4.5 V									OUT		QA				
	tpHL4		176			4.5 V	4.5 V	4.5 V									OUT		QB				
	tpHL4		177			4.5 V	4.5 V	GND									OUT		QC				
	tpHL4		178			4.5 V	4.5 V	GND									OUT		QD				
	tpLH4		179	8/	4.5 V		4.5 V	GND									OUT		QA				
	tpLH4		180		4.5 V		4.5 V	GND									OUT		QB				
	tpLH4		181				4.5 V	4.5 V	4.5 V								OUT		QC				
	tpLH4		182				4.5 V	4.5 V	4.5 V								OUT		QD				
11	tpLH4	Fig 8 and 8A	183	8/		IN	4.5 V	4.5 V			GND					OUT			QA				
	tpLH4		184			4.5 V	4.5 V	4.5 V								OUT			QB				
	tpLH4		185			4.5 V	4.5 V	4.5 V								OUT			QC				
	tpLH4		186			4.5 V	4.5 V	IN								OUT			QD				
	tpLH5		187	4.5 V		4.5 V	4.5 V	IN				IN				OUT		OUT	Carry				
	tpHL5		188	4.5 V		GND	GND	4.5 V				IN				OUT		OUT	Carry				
	tpHL6		189	IN		GND	GND	4.5 V				IN				OUT		OUT	Carry				
	tpHL6		190	IN		4.5 V	4.5 V									OUT		OUT	QA				
	tpHL6		191			4.5 V	4.5 V									OUT		OUT	QB				
	tpHL6		192			4.5 V	4.5 V									OUT		OUT	QC				
							4.5 V	4.5 V								OUT		OUT	QD				

1/ Normal clock pulse: (VIL ≤ 0.8 V, VIH ≥ 2.0 V).

2/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

3/ Output voltages shall be either:  
(a) H = 2.4 volts minimum and I = 0.4 volt maximum when using a high speed checker double comparator, or  
(b) H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.

(c) X = Don't care.

4/ Only a summary of attributes data is required.

5/ A ≥ 2.0 V, B ≤ 0.8 V. Input voltages shown are the maximum for VIL and the minimum for VIH.

6/ FMAX: minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

7/ Apply 1 clock pulse prior to input pulses.

8/ Apply momentary GND, then 4.5 volts prior to input pulses, maintain 4.5 volts during test.

TABLE III. Group A inspection for device type 04.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	DATA INPUTS										Meas. terminal	Test limits																	
				1	2	3	4	5	6	7	8	9	10		11	12	13	14	15	16	Min	Max	Unit									
1 TC=25°C	VOH	3006	1	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QA	Carry output	VCC	QD	2.4	V											
				4.5 V	1/	2.0 V	2.0 V	2.0 V	2.0 V	GND	2.0 V	-800 μA	-800 μA	-800 μA	4.5 V	QC																
						2.0 V	2.0 V	2.0 V	2.0 V	GND	2.0 V	-800 μA	-800 μA	-800 μA	-800 μA	4.5 V	QB															
						0.8 V	0.8 V	0.8 V	0.8 V	GND	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	4.5 V	QA														
						0.8 V	0.8 V	0.8 V	0.8 V	GND	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	4.5 V	Carry output														
	VOL	3007	6																		0.4											
VIC			11																		-1.5											
				IH9	3010	20																			80							
IHL11		24																			40											
IHL12		31																			100											
IIL5	3009	38																														

See footnotes at end of device type 04.



TABLE III. Group A inspection for device type 04 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4		5	6	7	8	9	10	11	12	13	14	15	16	Test limits					
				Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Meas. terminal	Min	Max	Unit			
7 TC = 25°C	Func-tional tests 4/	3014	92	A 5/	A 5/	B 5/	B 5/	B 5/	B 5/	B 5/	A 5/	GND	A 5/	B 5/	H	L	H	L	L	L	4.5 V	See 3/				
			93	A	B	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L			L		
			94	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			95	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			96	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			97	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			98	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			99	A	B	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			100	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			101	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			102	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			103	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			104	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			105	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			106	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			107	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			108	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			109	A	B	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			110	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			111	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
			112	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L			L	L	
113	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
114	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
115	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
116	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
117	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
118	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
119	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
120	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
121	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
122	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
123	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
124	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
125	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
126	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
127	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
128	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
129	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
130	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
131	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
132	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
133	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
134	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
135	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
136	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
137	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
138	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
139	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
140	A	A	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						
141	A	B	A	A	A	A	A	A	A	A	A	A	A	A	L	L	L	L	L	L						

See footnotes at end of device type 04.



TABLE III. Group A inspection for device type 04 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	DATA INPUTS			7	8	9	10	11	12	13	14	15	16	Test limits			
							A	B	C											D	Meas. terminal	Min	Max
10 TC = 125°C	F <sup>6/</sup> MAX	Fig 8 & 8C	188	4.5 V	IN	GND	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QA	20	58	MHz
	tplH3	Fig 8 & 8B	189	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Carry	3	58	ns
	tpHL3		190	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Carry	3	58	ns
	tpHL4		191	4.5 V	IN	GND	GND	GND	GND	GND	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QA	20	38	ns
	tpHL4		192	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QB	20	38	ns
	tpHL4		193	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QC	20	38	ns
	tpHL4		194	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QD	20	38	ns
	tpHL4		195	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QA	20	36	ns
	tpHL4		196	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QB	20	36	ns
	tpHL4		197	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QC	20	36	ns
	tpHL4		198	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QD	20	36	ns
	tpHL4	Fig 8 and 8A		199	8/	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QA	20	36	ns
	tpHL4			200	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QB	20	36	ns
	tpHL4			201	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QC	20	36	ns
tpHL4			202	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QD	20	36	ns	
tpHL5			203	4.5 V	7/	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Carry	27	27	ns	
tpHL5			204	4.5 V	7/	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Carry	27	27	ns	
tpHL6			205	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QA	20	38	ns	
tpHL6			206	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QB	20	38	ns	
tpHL6			207	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QC	20	38	ns	
tpHL6			208	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	5.0 V	QD	20	38	ns	
11	Same tests, terminal conditions and limits as subgroup 10, except TC = -55°C.																						

1/ Normal clock pulse: (VIL < 0.8 V, VIH > 2.0 V).

2/ Terminal conditions (plus not designated may be H > 2.0 V, or L < 0.8 V, or open).

3/ Output voltages shall be either:

(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or

(b) H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.

(c) X = Don't care

4/ Only a summary of attributes data is required.

5/ A > 2.0 V, B < 0.8 V. Input voltages shown are the maximum for VIL and the minimum for VIH.

6/ FMAX: minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

7/ Apply 1 clock pulse prior to input pulses.

8/ Momentarily ground, then apply 4.5 V.

TABLE III. Group A inspection for device type 05.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	DATA INPUTS						Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Test limits																
				1	2	3	4	5	6											7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit			
1 TC = 25°C	VOH	3006	1	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	4.5 V	2.4		V														
			2		1/	2.0 V	2.0 V	2.0 V	2.0 V		GND	GND	2.0 V	-800 μA	4.5 V																					
			3			2.0 V	0.8 V	0.8 V	0.8 V				2.0 V																							
			4			2.0 V	0.8 V	0.8 V	0.8 V				2.0 V																							
			5			2.0 V	0.8 V	0.8 V	0.8 V				2.0 V																							
			6							0.8 V				16 mA	16 mA																					
			7							0.8 V				16 mA																						
			8							0.8 V				16 mA																						
			9							0.8 V				16 mA																						
			10							0.8 V				16 mA																						
		11																																		
		12																																		
		13																																		
		14																																		
		15																																		
		16																																		
		17																																		
		18																																		
		19																																		
		20																																		
	I <sub>IH9</sub>	3010	20	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	5.5 V																	
	I <sub>IH9</sub>		21	1/	2.4 V	GND	GND	GND	GND	GND	GND	GND	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH10</sub>		22	1/	5.5 V	GND	GND	GND	GND	GND	GND	GND	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH10</sub>		23	1/	5.5 V	GND	GND	GND	GND	GND	GND	GND	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		24	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		25	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		26	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		27	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		28	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		29	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH11</sub>		30	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V																	
	I <sub>IH12</sub>		31	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		32	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		33	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		34	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		35	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		36	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IH12</sub>		37	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																	
	I <sub>IL5</sub>	3009	38		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL6</sub>		39		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL6</sub>		40		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		41		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		42		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		43		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		44		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		45		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						
	I <sub>IL7</sub>		46		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V																						

See footnotes at end of device type 05.



TABLE III. Group A inspection for device type 05 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits					
				Clear	Clock	A	A 5/ B	A 5/ C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Meas. terminal	Min	Max	Unit		
7 T <sub>C</sub> =25°C	Func-tional tests 4/	3014	92	A 5/	A 5/ B	A 5/	A 5/ B	A 5/ C	A 5/ D	B 5/ B	GND	A 5/ B	A 5/ A	A 5/ B	L	L	L	L	L	4.5 V					
			93																						
			94																						
			95																						
			96																						
			97																						
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139																									
140																									
141																									

See 3/

See footnotes at end of device type 05.



TABLE III. Group A inspection for device type 05 - Continued.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 Clear	2 Clock	3			7 Enable P	8 GND	9 Load	10 Enable T	11 Output Q <sub>D</sub>	12 Output Q <sub>C</sub>	13 Output Q <sub>B</sub>	14 Output Q <sub>A</sub>	15 Carry output	16 VCC	Meas. Terminal		Test limits	
						A	B	C											D	Min	Max	Unit
10 T <sub>C</sub> = 125°C	F <sub>MAX</sub> <sup>5/</sup>	Fig 8 & 8C	173	4.5 V	IN	GND	GND	4.5 V	GND	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	20	58	MHz
	tp <sub>LH3</sub>	Fig 8 & 8B	174	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN	IN	4.5 V				OUT	OUT	5.0 V	Carry	3	58	ns
	tp <sub>HL3</sub>		175	4.5 V	4.5 V	GND	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	Carry	3	58	ns
	tp <sub>HL4</sub>		176	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	20	38	ns
	tp <sub>HL4</sub>		177	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	20	38	ns
	tp <sub>HL4</sub>		178	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QB	20	36	ns
	tp <sub>HL4</sub>		179	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	20	36	ns
	tp <sub>HL4</sub>		180	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	20	36	ns
	tp <sub>HL4</sub>		181	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	20	36	ns
	tp <sub>HL4</sub>		182	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QB	20	36	ns
	tp <sub>HL4</sub>		183	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	20	36	ns
	tp <sub>HL4</sub>		184	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	20	36	ns
	tp <sub>HL4</sub>		185	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QB	20	36	ns
tp <sub>HL4</sub>		186	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	20	36	ns	
tp <sub>HL4</sub>		187	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	Carry	27	27	ns	
tp <sub>HL4</sub>		188	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	Carry	27	27	ns	
tp <sub>HL5</sub>		189	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	27	27	ns	
tp <sub>HL6</sub>		190	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QA	27	27	ns	
tp <sub>HL6</sub>		191	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QB	27	27	ns	
tp <sub>HL6</sub>		192	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	27	27	ns	
tp <sub>HL6</sub>		193	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V				OUT	OUT	5.0 V	QC	27	27	ns	

11 Same tests, terminal conditions and limits as subgroup 10, except T<sub>C</sub> = -55°C.

- 1/ Normal clock pulse: (V<sub>IL</sub> < 0.8 V, V<sub>IH</sub> > 2.0 V).
- 2/ Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open).
- 3/ Output voltages shall be either:  
(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or  
(b) H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.
- 4/ Only a summary of attributes data is required.
- 5/ A > 2.0 V, B < 0.8 V. Input voltages shown are the maximum for V<sub>IL</sub> and the minimum for V<sub>IH</sub>.
- 6/ F<sub>MAX</sub> minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- 7/ Apply 1 clock pulse prior to input pulses.
- 8/ Momentarily ground, then apply 4.5 V.

TABLE III. Group A inspection for device type 06.  
Terminal conditions 2/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	DATA INPUTS			7	8	9	10	11	12	13	14	15	16	Test limits							
						A	B	C											D	Meas. terminal	Mfn	Max	Unit			
1 TC=25°C	VOH	3006	1 2 3 4 5	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	QD	2.4	V				
				4.5 V	1/	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	0.8 V	GND	GND	2.0 V	-800 μA	-800 μA	-800 μA	-800 μA	4.5 V	QC					
					1/	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	0.8 V	GND	GND	2.0 V	-800 μA	-800 μA	-800 μA	-800 μA	4.5 V	QB					
					1/	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	0.8 V	GND	GND	2.0 V	-800 μA	-800 μA	-800 μA	-800 μA	4.5 V	QA					
					1/	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	0.8 V	GND	GND	2.0 V	-800 μA	-800 μA	-800 μA	-800 μA	4.5 V	Carry output					
	VOL	3007	6 7 8 9 10		1/	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	QD	0.4	V				
					1/	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	QC					
					1/	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	QB					
					1/	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	QA					
					1/	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	Carry output					
	VIC	3010	11 12 13 14 15 16 17 18 19			-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA								Input A	-1.5	V				
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Input B					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Input C					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Input D					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Enable P					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Load					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Enable T					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Clear					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA							Clock					
						-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA								Clock				
	I <sub>HH9</sub> I <sub>HH9</sub> I <sub>HH10</sub> I <sub>HH10</sub> I <sub>HH11</sub>	3010	20 21 22 23 24	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Clock	80	μA				
				4.5 V	1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	Enable T	80			
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	Clock	200		
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	Enable T	200	
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	Clock	40	
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	Clear		
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	A		
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	B		
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	C		
					1/	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	5.5 V	D		
	I <sub>HL5</sub> I <sub>HL6</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL8</sub>	3009	38 39 40 41 42 43 44 45 46	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Clock	100					
				5.5 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Clear				
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	A			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	B			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	C			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	D			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Clear			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Load			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Enable P			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Load			
	I <sub>HL5</sub> I <sub>HL6</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL7</sub> I <sub>HL8</sub>	3009	38 39 40 41 42 43 44 45 46	Clear	Clock	A	B	C	D	Enable P	GND	Load	Enable T	Output QD	Output QC	Output QB	Output QA	Carry output	VCC	Clock	-1.0	-2.3	mA			
				5.5 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Clear	-0.4	-1.3		
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Input A			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Input B			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Input C			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Input D			
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Enable P	-0.7	-1.6	
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Load	-0.5	-1.6	
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Clear	-0.7	-1.6	
					0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.5 V	Enable T	-1.0	-3.2	

See footnotes at end of device type 06.

















TABLE III. Group A inspection for device type 08.  
Terminal conditions Y/

Subgroup	Symbol	MIL-STD-883 method	Case E, F																Test limits						
			Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit		
1 TC = 25°C	IIL2	3010	1																Data A Input	-0.7			mA		
	IIL6		2	0.4 V																Data B Input					
	IIL7		3																	Data C Input					
	IIL8		4					0.4 V												Data D Input					
	IIL5		5																		Load		18/		
			6																		Clear Input		18/		
					7					0.4 V											Count Up Input				
					8																Count Down Input				
	IHL11		9																Data A Input	4.5 V			40	μA	
			10	2.4 V																Data B Input					
			11																	Data C Input					
			12																	Data D Input					
			13																	Load					
			14																	Clear Input					
			15																	Count Up Input					
			16																	Count Down Input					
	IHL12		17																Data A Input	4.5 V				100	μA
			18	5.5 V																Data B Input					
			19																	Data C Input					
			20																	Data D Input					
			21																	Load					
			22																	Clear Input					
			23																	Count Up Input					
			24																	Count Down Input					

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Case E, F, Test No.	Terminal conditions 17/											Test limits														
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit						
1 T <sub>C</sub> = 25°C	V <sub>OH</sub>	3006	25	Data B Input	2.0 V	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	GND	Data D Input	2.0 V	Load	0.8 V	Carry Output	-400 μA	Borrow Output	0.8 V	Clear Input	2.0 V	Data A Input	2.0 V	V <sub>CC</sub>	4.5 V	Output Q <sub>A</sub>	2.4	V <sub>dC</sub>			
			26	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Output Q <sub>C</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Load	0.8 V	Carry Output	-400 μA	Borrow Output	-400 μA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>B</sub>	0.4	
			27	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Output Q <sub>C</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Load	0.8 V	Carry Output	-400 μA	Borrow Output	-400 μA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>C</sub>	0.4	
			28	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Output Q <sub>C</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Load	0.8 V	Carry Output	-400 μA	Borrow Output	-400 μA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>D</sub>	0.4	
			29	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Output Q <sub>C</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Load	0.8 V	Carry Output	-400 μA	Borrow Output	-400 μA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Carry Output	0.4	
			30	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Output Q <sub>C</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	Load	0.8 V	Carry Output	-400 μA	Borrow Output	-400 μA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Borrow Output	0.4	
	2	V <sub>OL</sub>	3007	31	Data B Input	0.8 V	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Data D Input	0.8 V	Load	0.8 V	Carry Output	16 mA	Borrow Output	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V	Output Q <sub>A</sub>	0.4	mAdc		
				32	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Load	0.8 V	Carry Output	16 mA	Borrow Output	16 mA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>B</sub>	0.4
				33	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Load	0.8 V	Carry Output	16 mA	Borrow Output	16 mA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>C</sub>	0.4
				34	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Load	0.8 V	Carry Output	16 mA	Borrow Output	16 mA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Output Q <sub>D</sub>	0.4
				35	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Load	0.8 V	Carry Output	16 mA	Borrow Output	16 mA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Carry Output	0.4
				36	Output Q <sub>B</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Load	0.8 V	Carry Output	16 mA	Borrow Output	16 mA	Output Q <sub>A</sub>	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	4.5 V		Borrow Output	0.4
3	I <sub>OS</sub>	3011	37	Data B Input	2.4 V	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Data D Input	2.4 V	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Clear Input	2.0 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V	Output Q <sub>A</sub>	-20	mAdc			
			38	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>B</sub>	-65	
			39	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>C</sub>	-65	
			40	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>D</sub>	-65	
			41	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Carry Output	-65	
			42	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	2.0 V	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Borrow Output	-65	
2	I <sub>CC</sub>	3010	43	Data B Input	2.4 V	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Data D Input	2.4 V	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Clear Input	GND	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V	Output Q <sub>A</sub>	-20	mAdc			
			44	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>B</sub>	-65	
			45	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>C</sub>	-65	
			46	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Output Q <sub>D</sub>	-65	
			47	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Carry Output	-65	
			48	Output Q <sub>B</sub>	GND	Output Q <sub>D</sub>	GND	Output Q <sub>C</sub>	GND	Output Q <sub>D</sub>	GND	Load	GND	Carry Output	GND	Borrow Output	2.0 V	Output Q <sub>A</sub>	2.4 V	Clear Input	2.4 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V		Borrow Output	-65	
2	V <sub>IC</sub>		49	Data B Input	-12 mA	Output Q <sub>B</sub>		Output Q <sub>D</sub>		Data D Input	-12 mA	Load	-12 mA	Carry Output		Borrow Output	-12 mA	Clear Input	-12 mA	Data A Input	-12 mA	V <sub>CC</sub>	4.5 V	Output Q <sub>A</sub>	-89	V			
			50	Output Q <sub>B</sub>		Output Q <sub>D</sub>		Output Q <sub>C</sub>		Output Q <sub>D</sub>		Load	-12 mA	Carry Output		Borrow Output	-12 mA	Output Q <sub>A</sub>	-12 mA	Clear Input	-12 mA	Data A Input	-12 mA	V <sub>CC</sub>	4.5 V		Output Q <sub>B</sub>	-89	
			51	Output Q <sub>B</sub>		Output Q <sub>D</sub>		Output Q <sub>C</sub>		Output Q <sub>D</sub>		Load	-12 mA	Carry Output		Borrow Output	-12 mA	Output Q <sub>A</sub>	-12 mA	Clear Input	-12 mA	Data A Input	-12 mA	V <sub>CC</sub>	4.5 V		Output Q <sub>C</sub>	-89	
			52	Output Q <sub>B</sub>		Output Q <sub>D</sub>		Output Q <sub>C</sub>		Output Q <sub>D</sub>		Load	-12 mA	Carry Output		Borrow Output	-12 mA	Output Q <sub>A</sub>	-12 mA	Clear Input	-12 mA	Data A Input	-12 mA	V <sub>CC</sub>	4.5 V		Output Q <sub>D</sub>	-89	
2			Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = 125°C, and V <sub>IC</sub> tests are omitted.																										
3			Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = -55°C, and V <sub>IC</sub> tests are omitted.																										

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
				Data B Input A 3/	Output QB	Output QA	Count Down Input A 3/	Count Up Input A 3/	Output QC	Output QD	GND	Data D Input A 3/	Data C Input A 3/	Load A 3/	Carry Output H	Borrow Output H	Clear Input A 3/ B	Data A Input A 3/	VCC 4.5 V	Meas. terminal	Min	Max	Unit	
7 TC = 25°C	Functional tests 2/	3014	53	A 3/	L	L	A 3/	A	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/					
			54	A 3/	L	L	A 3/	A	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/				
			55	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			56	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			57	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			58	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			59	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			60	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			61	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
			62	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/			
63	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
64	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
65	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
66	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
67	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
68	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
69	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
70	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
71	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
72	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
73	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
74	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
75	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
76	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
77	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
78	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
79	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
80	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
81	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
82	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
83	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
84	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
85	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
86	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
87	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
88	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
89	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
90	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
91	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
92	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
93	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
94	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
95	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
96	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
97	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
98	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
99	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
100	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
101	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						
102	A 3/	L	L	A 3/	A	L	L	L	L	L	A 3/	A 3/	A 3/	H	H	A 3/	A 3/	A 3/						

See footnotes at end of device type 08.



TABLE III. Group A inspection for device type 08--Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Cases E, F																Test limits			
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit
10 TC = 125 °C	F <sub>MAX</sub> <sup>14/</sup>	Fig 10A		Output QB	Output QA	Count Down Input	Count Up Input	Output QC	Output QD	GND	Data D Input	Data C Input	Load	Carry Output	Borrow Output	Clear Input	Data A Input	VCC	Output QA	20	57	MHz
	F <sub>MAX</sub> <sup>14/</sup>	Fig 10A				2.4 V	2.4 V			GND			2.4 V			GND	2.4 V	5.0 V	Output QA	20	57	MHz
	t <sub>PHL7</sub>	Fig 10				GND	GND						5/			5/	2.4 V		Output QA	3	66	ns
	t <sub>PLH8</sub>	Fig 10				GND	GND						6/			GND	2.4 V		Output QA	3	66	ns
	t <sub>PHL8</sub>	Fig 10				2.4 V	2.4 V				2.4 V		7/			8/ GND	2.4 V		Output QA	3	62	ns
	t <sub>PHL9</sub>	Fig 10A				2.4 V	2.4 V					2.4 V		8/	OUT	9/	2.4 V		Carry	39	39	ns
	t <sub>PLH9</sub>					2.4 V	2.4 V					2.4 V		9/	OUT	10/	2.4 V		Carry	45	45	ns
	t <sub>PHL10</sub>							10/	2.4 V			GND		10/	OUT	11/	2.4 V		Borrow Output	39	39	ns
	t <sub>PLH10</sub>							11/	2.4 V			GND		11/	OUT		2.4 V		Borrow Output	42	42	ns
	t <sub>PLH11</sub>							2.4 V	15/	OUT		GND		15/		GND	2.4 V		Output QA	63	63	ns
	t <sub>PHL11</sub>							2.4 V	15/	OUT		GND		15/		GND	2.4 V		Output QB	63	63	ns
	t <sub>PLH11</sub>							2.4 V	15/	OUT		GND		15/		GND	2.4 V		Output QC	63	63	ns
	t <sub>PHL11</sub>							2.4 V	16/	OUT		2.4 V		16/		GND	2.4 V		Output QD	71	71	ns
	t <sub>PLH11</sub>							2.4 V	16/	OUT		GND		16/		GND	2.4 V		Output QD	71	71	ns
	t <sub>PHL11</sub>							2.4 V	16/	OUT		GND		16/		GND	2.4 V		Output QC	71	71	ns
t <sub>PLH11</sub>							2.4 V	16/	OUT		GND		16/		GND	2.4 V		Output QC	71	71	ns	

11 Same tests, terminal conditions, and limits as subgroup 10, except TC = -55 °C.

- 1/ Output voltages shall be either:  
(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or  
(b) H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.
- 2/ Only a summary of attributes data is required.
- 3/ A ≥ 2.0 V, B ≤ 0.8 V. Input voltages shown are the maximum for V<sub>IL</sub> and the minimum for V<sub>IH</sub>.
- 4/ See figure 10A. Apply waveform E for tests 117 and 134, and waveform H for tests 118 and 135.
- 5/ See figure 10, waveforms A, B, C, and D. Load A<sub>IN</sub>, then apply waveform A and observe the drop in Q<sub>A</sub> output.
- 6/ See figure 10, waveforms B, C, and D. Load A<sub>IN</sub>, and observe t<sub>PLH</sub> of waveform D at output Q<sub>A</sub>.
- 7/ Repeat steps as in note 6. Observe the pulse delay of the drop in Q<sub>A</sub> when the load pulse is applied.
- 8/ See figures 10 and 10A, waveforms A, B, C, E, F, and G. First use clear pulse, then load pulse, then one count up pulse. Also see figure 10A, note 4.
- 9/ See note 5, add one more count up pulse for t<sub>PLH9</sub> as shown on figure 10A, waveforms F and G.
- 10/ See figures 10 and 10A. First clear pulse, then one count down pulse.
- 11/ See note 7. Clear pulse first, figure 10 waveforms A, B, and C, add one more count down pulse for t<sub>PLH10</sub> as shown on figure 10A, waveforms J and K.
- 12/ See figures 10 and 10A. First a clear pulse, then one count up pulse for Q<sub>A</sub>. On next three tests enter count up pulses to appropriate count to check Q<sub>B</sub>, Q<sub>C</sub>, and Q<sub>D</sub>.
- 13/ See figure 10A waveforms H and J. On next three tests enter count down pulse, waveform H and observe t<sub>PHL11</sub>, waveform J on outputs Q<sub>C</sub>, Q<sub>B</sub>, and Q<sub>A</sub>.
- 14/ F<sub>MAX</sub> minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- 15/ Load pulse before count up input, then 4.5 V.
- 16/ Load pulse before count down input, then 4.5 V.
- 17/ Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open).
- 18/ The limits shall be: -0.5 mA minimum, -1.3 mA maximum for circuit C, and -0.7 mA minimum, -1.6 mA maximum for all other circuits.

TABLE III. Group A inspection for device type 09.  
Terminal conditions 1/

Subgroup	Symbol	MIL-STD-883 method	Case E, F																Test limits				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit	
1 TC = 25°C	I <sub>IL2</sub>	3010	Data B Input															Data A Input	-0.7	-1.6	mA		
	I <sub>IL6</sub>		Data B Input	0.4 V															Data A Input				
	I <sub>IL7</sub> I <sub>IL8</sub>		Data D Input	0.4 V																Data A Input			
			Data D Input	0.4 V																Data A Input			
	I <sub>IL5</sub> I <sub>IL5</sub>		Count Up Input				0.4 V													Count Up Input			
			Count Down Input				0.4 V													Count Down Input			
	I <sub>IH11</sub>		I <sub>IH11</sub>		Data A Input															Data A Input	40		μA
					Data B Input	2.4 V															Data B Input		
Data C Input		2.4 V																		Data C Input			
Data D Input		2.4 V																		Data D Input			
Load																				Load			
Clear																				Clear			
Count Up Input							2.4 V													Count Up Input			
Count Down Input							2.4 V													Count Down Input			
I <sub>IH12</sub>	I <sub>IH12</sub>		Data A Input															Data A Input	100		μA		
			Data B Input	5.5 V															Data B Input				
			Data C Input	5.5 V															Data C Input				
			Data D Input	5.5 V															Data D Input				
			Load																Load				
			Clear																Clear				
			Count Up Input				5.5 V												Count Up Input				
			Count Down Input				5.5 V												Count Down Input				

See footnotes at end of device type 09.

TABLE III. Group A inspection for device type 09 - Continued.  
Terminal conditions 17

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	Terminal conditions 17											Test limits																					
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit													
1 T <sub>C</sub> = 25°C	V <sub>OH</sub>	3006	25	Data B Input	2.0 V	Output Q <sub>B</sub>	-400 μA	Output Q <sub>D</sub>	-400 μA	GND	Data D Input	2.0 V	Data C Input	2.0 V	Load	0.8 V	Carry Output	-400 μA	Borrow Output	0.8 V	Clear Input	0.8 V	Data A Input	2.0 V	V <sub>CC</sub>	4.5 V	Output QA	2.4		Vdc						
			26	Output Q <sub>B</sub>	-400 μA																															
			27	Output Q <sub>B</sub>	-400 μA																															
	V <sub>OL</sub>	3007	28	Output Q <sub>B</sub>	-400 μA																															
			29	Output Q <sub>B</sub>	-400 μA																															
			30	Output Q <sub>B</sub>	-400 μA																															
			31	Output Q <sub>B</sub>	-400 μA																															
	I <sub>OS</sub>	3011	32	Output Q <sub>B</sub>	16 mA	Output Q <sub>A</sub>	16 mA	Output Q <sub>C</sub>	16 mA	Output Q <sub>D</sub>	16 mA	Count Down Input	2.0 V	Count Up Input	2.0 V	Load	0.8 V	Carry Output	16 mA	Borrow Output	0.8 V	Clear Input	0.8 V	Data A Input	0.8 V	V <sub>CC</sub>	5.5 V	Output QA	0.4							
			33	Output Q <sub>B</sub>	16 mA																															
			34	Output Q <sub>B</sub>	16 mA																															
			35	Output Q <sub>B</sub>	16 mA																															
36			Output Q <sub>B</sub>	16 mA																																
I <sub>CC</sub>	3010	37	Data B Input	2.4 V	Output Q <sub>B</sub>	GND	Output Q <sub>A</sub>	GND	Output Q <sub>C</sub>	GND	Count Down Input	2.4 V	Count Up Input	2.4 V	Load	GND	Carry Output	GND	Borrow Output	0.8 V	Clear Input	0.8 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V	Output QA	-20				mAdd				
		38	Output Q <sub>B</sub>	GND																																
		39	Output Q <sub>B</sub>	GND																																
		40	Output Q <sub>B</sub>	GND																																
		41	Output Q <sub>B</sub>	GND																																
		42	Output Q <sub>B</sub>	GND																																
V <sub>IC</sub>	3010	43	Data B Input	2.4 V	Output Q <sub>B</sub>	GND	Output Q <sub>A</sub>	GND	Output Q <sub>C</sub>	GND	Count Down Input	2.4 V	Count Up Input	2.4 V	Load	GND	Carry Output	GND	Borrow Output	0.8 V	Clear Input	0.8 V	Data A Input	2.4 V	V <sub>CC</sub>	5.5 V	Output QA	-20								
		44	Output Q <sub>B</sub>	-12 mA																																
		45	Output Q <sub>B</sub>	-12 mA																																
		46	Output Q <sub>B</sub>	-12 mA																																
		47	Output Q <sub>B</sub>	-12 mA																																

2 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = 125°C and V<sub>IC</sub> tests are omitted.

3 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = -55°C and V<sub>IC</sub> tests are omitted.

TABLE III. Group A inspection for device type 09 - Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Case, E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
				Data B Input	Output QB	Output QA	Count Down Input	Count Up Input	Output QC	Output QD	GND	Data D Input	Data C Input	Load	Carry Output	Borrow Output	Clear Input	Data A Input	VCC	Meas. terminal	Min	Max	Unit	
7 TC = 25 °C	Func-tional tests 2/	3014	52	B 3/	L	L	A 3/	A 3/	L	L	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V					
			53	A	H	H	A	A	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V				
			54	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			55	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			56	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			57	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			58	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			59	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			60	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			61	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			62	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			63	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			64	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			65	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			66	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			67	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			68	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			69	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			70	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			71	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			72	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			73	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			74	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			75	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			76	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			77	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			78	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			79	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			80	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			81	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			82	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			83	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			84	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			85	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			86	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			87	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			88	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			89	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			90	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			91	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			92	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			93	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			94	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			95	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			96	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			97	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			98	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			99	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			100	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			
			101	A	H	H	A	A	H	H	H	H	GND	B 3/	B 3/	B 3/	H	H	B 3/	B 3/	4.5 V			

See 1/

See footnotes at end of device type 09.

TABLE III. Group A inspection for device type 09 - Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	Terminal conditions 17/													Test limits												
				1 Data B Input	2 Output QB	3 Output QA	4 Count Down Input	5 Count Up Input	6 Output QC	7 Output QD	8 GND	9 Data D Input	10 Data C Input	11 Load	12 Carry Output	13 Borrow Output	14 Clear Input	15 Data A Input	16 VCC	Meas. terminal	Min	Max	Unit						
7 TC = 125°C	Func-tional tests 2/	3014	102	A 3/	L	L	L	B 3/	A 3/	L	H	H	GND	A 3/	A 3/	A 3/	H	H	B 3/	A 3/	4.5 V	See 1/							
			103		H	H	A	A 3/	H	L	L	L	L																
			104				H	A	A	A	A	A	A	A															
			105				A	B	B	B	B	B	B	B															
			106				L	L	L	A	A	A	A	A															
			107				L	L	L	A	A	A	A	A															
			108						L	A	A	A	A	A															
			109						L	A	A	A	A	A															
			110						L	A	A	A	A	A															
			111						H	A	A	A	A	A															
			112							A	A	A	A	A															
			113							A	A	A	A	A															
			114							A	A	A	A	A															
			115							A	A	A	A	A															
			116							A	A	A	A	A															
			117							A	A	A	A	A															
			118							A	A	A	A	A															
			119							A	A	A	A	A															
			120							A	A	A	A	A															
			121							A	A	A	A	A															
			122							A	A	A	A	A															
123							A	A	A	A	A																		
124							A	A	A	A	A																		
125							A	A	A	A	A																		
126							A	A	A	A	A																		
127							A	A	A	A	A																		
128							A	A	A	A	A																		
129							A	A	A	A	A																		
130							A	A	A	A	A																		
131							A	A	A	A	A																		
132							A	A	A	A	A																		
133							A	A	A	A	A																		
134							A	A	A	A	A																		
135							A	A	A	A	A																		
136							A	A	A	A	A																		
137							A	A	A	A	A																		
138							A	A	A	A	A																		
139							A	A	A	A	A																		
140							A	A	A	A	A																		
141							A	A	A	A	A																		
142							A	A	A	A	A																		
143							A	A	A	A	A																		
144							A	A	A	A	A																		
145							A	A	A	A	A																		
146							A	A	A	A	A																		
147							A	A	A	A	A																		
148							A	A	A	A	A																		
149							A	A	A	A	A																		
150							A	A	A	A	A																		
151							A	A	A	A	A																		

See footnotes at end of device type 09.



TABLE III. Group A inspection for device type 09 - Continued.  
Terminal conditions 17/

Subgroup	Symbol	MIL-STD-883 method	Case E, F										Test limits									
			Test no.	Data B Input	Output QB	Output QA	Count Down Input	Count Up Input	Output QC	Output QD	GND	Data D Input	Data C Input	Load	Carry Output	Borrow Output	Clear Input	Data A Input	VCC	Meas. terminal	Min	Max
TC = 125 °C	FMAX <sup>14</sup>	Fig 10A	178			OUT	2.4 V	4/	2.4 V	GND									Output QA	20	57	MHz
	FMAX <sup>14</sup>	Fig 10A	179			OUT	2.4 V	4/	2.4 V										Output QA	20	57	MHz
	tPHL7	Fig 10	180				GND	GND	GND										Output QA	3	66	ns
	tPLH8	Fig 10	181				GND	GND	GND										Output QA	3	66	ns
	tPHL8	Fig 10	182	2.4 V				2.4 V	8/	2.4 V	2.4 V								Output QA	3	66	ns
	tPHL9	Fig 10A	183					2.4 V	8/	2.4 V	2.4 V								Output QA	3	66	ns
	tPLH9		184	2.4 V				2.4 V	9/	2.4 V	2.4 V								Carry	39	45	
	tPHL10		185	2.4 V				2.4 V	10/	2.4 V	GND								Output	39	45	
	tPLH10		186	GND				2.4 V	11/	2.4 V	GND								Output	39	45	
	tPLH11		187	GND			OUT	2.4 V	15/	2.4 V	GND								Output QA	42	63	
			188	GND			OUT	2.4 V	15/	2.4 V	GND								Output QB	42	63	
			189	2.4 V				2.4 V	16/	2.4 V	GND								Output QC	42	63	
			190	2.4 V				2.4 V	16/	2.4 V	GND								Output QD	42	63	
			191	GND				2.4 V	16/	2.4 V	GND								Output QD	42	63	
		192	GND				2.4 V	16/	2.4 V	GND								Output QC	42	63		
		193	GND				2.4 V	16/	2.4 V	GND								Output QC	42	63		
		194	GND			OUT	2.4 V	16/	2.4 V	GND								Output QA	42	63		

11 Same tests, terminal conditions, and limits as subgroup 10, except TC = -55 °C.

- 1/ Output voltages shall be either:  
(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or  
(b) H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.
- 2/ Only a summary of attributes data is required.
- 3/ A > 2.0 V, B < 0.8 V. Input voltages shown are the maximum for VIL and the minimum for VIH.
- 4/ See figure 10A. Apply waveform E for tests 162 and 179, and waveform H for tests 163 and 180.
- 5/ See figure 10, waveforms A, B, C, and D. Load AJN, then apply waveform A and observe the drop in QA output.
- 6/ See figure 10, waveform B, C, and D. Load AJN, and observe tPLH of waveform D at output QA.
- 7/ Repeat steps as in note 6. Observe the pulse delay of the drop in QA when the load pulse is applied.
- 8/ See figures 10 and 10A, waveforms A, B, C, E, F, and G. First use clear pulse, then load pulse, then one count up pulse. Also see figure 10B, note 7.
- 9/ See note 8, add one more count up pulse for tPLH9 as shown on figure 10A, waveforms F and G.
- 10/ See figures 10 and 10A. First clear pulse, then one count down pulse.
- 11/ See note 10. Clear pulse first, figure 10, waveforms A, B, and C, add one more count down pulse for tPLH10 as shown on figure 10A, waveforms J and K.
- 12/ See figures 10 and 10A. First a clear pulse, then one count up pulse for QA. On next three tests enter count up pulses to appropriate count to check QB, QC, and QD.
- 13/ See figure 10A, waveforms H and J. On next three tests enter count down pulse, waveform H and observe tPHL11, waveform J on outputs QC, QB, and QA.
- 14/ FMAX, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- 15/ Load pulse before count up input, then 4.5 V.
- 16/ Load pulse before count down input, then 4.5 volts.
- 17/ Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open).
- 18/ The limits shall be: -0.5 mA minimum, -1.3 mA maximum for circuit C, and -0.7 mA minimum, -1.6 mA maximum for all other circuits.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	5492
02	5493
03	54160
04	54163A
05	54162
06	54161
07	5490
08	54192
09	54193

6.7 Manufacturers designation. Manufacturers circuits' included in this specification are designated as shown in table IV herein.

TABLE IV. Manufacturers' designation.

Circuit	A	B	C	D	E	F
Device type	Texas Instruments, Incorporated	National Semiconductor Corporation	Motorola Incorporated	Advanced Micro Devices, Incorporated	Signetics Corporation	Fairchild Semiconductor
01	X	X	X		X	
02	X	X	X		X	
03	X	X	X	X	X	
04	X	X	X	X	X	
05	X	X	X	X	X	X
06	X	X	X	X	X	X
07	X	X	X		X	
08			X		X	
09			X		X	

Custodians:  
 Army - ER  
 Navy - EC  
 Air Force - 17

Preparing activity:  
 Air Force - 17

(Project 5962-0477)

Review activities:  
 Army - AR, MI  
 Navy - SH, OS  
 Air Force - 11, 19, 85, 99  
 DLA - ES

User activities:  
 Army - SM  
 Navy - AS, CG, MC

Agent:  
 DLA - ES