

MIL-M-38510/15A
27 July 1979
SUPERSEDING
MIL-M-38510/15
28 December 1973

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL,
TTL, BISTABLE LATCHES, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, 4-bit bistable latch microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. Device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	4-Bit latch, complementary outputs
02	4-Bit latch
03	Dual, 4-bit latch
04	4-Bit latch, master reset

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Case outline letter</u>	<u>MIL-M-38510, appendix C, case outline</u>
A	F-1 (14-lead, 1/4" x 1/4", flat pack)
B	F-3 (14-lead, 1/4" x 1/8", flat pack)
C	D-1 (14-lead, 1/4" x 3/4", dual-in-line pack)
D	F-2 (14-lead, 1/4" x 3/8", flat pack)
E	D-2 (16-lead, 1/4" x 7/8", dual-in-line pack)
F	F-5 (16-lead, 1/4" x 3/8", flat pack)
J	D-3 (24-lead, 1/2" x 1/4", dual-in-line pack)
K	F-6 (24-lead, 3/8" x 1/2", flat pack)
L	F-7 (24-lead, 3/8" x 1/2", flat pack)
Z	F-8 (24-lead, 1/4" x 3/8", flat pack)

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 to 7.0 Vdc
Input voltage range - - - - -	-1.5 Vdc at 12 mA to 5.5 Vdc
Storage temperature range - - - - -	-65° to 150°C
Maximum power dissipation, P_D ^{1/}	
Device types 01 and 02 - - - - -	280 mW
Device type 03 - - - - -	630 mW
Device type 04 - - - - -	325 mW

^{1/} Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration.

Beneficial comments (recommendations, additions, deletions) any and pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center ATTN: RADC (RBE-2) Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Lead temperature (soldering, 10 seconds)- - - - -	300°C
Thermal resistance, junction to case - - -	$\theta_{JC} = [0.15^\circ\text{C}/\text{mW}$ for flat pack $0.08^\circ\text{C}/\text{mW}$ for dual-in-line pack]
Junction temperature - - - - -	$T_J = 175^\circ\text{C}$

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage - - -	2.0 Vdc
Maximum low level input voltage- - -	0.8 Vdc
Normalized fanout (each output) 1/ - - -	5 maximum
Ambient operating temperature range- - -	-55° to 125°C
Setup time, $t(\text{SETUP})$	
Types 01 and 02- - - - -	25 ns, minimum
Setup time, $t(\text{SETUP})$, type 03	
Data to enable (high)- - - - -	10 ns, minimum
Data to enable (low) - - - - -	16 ns, minimum
Setup time, $t(\text{SETUP})$, type 04	
Data to enable (high)- - - - -	5 ns, minimum
Data to enable (low) - - - - -	25 ns, minimum
Setup time, $t(\text{SETUP})$, type 04	
Data to set (high) - - - - -	8 ns, minimum
Input hold time, $t(\text{HOLD})$,	
types 01 and 02	
Clock to data- - - - -	5 ns, minimum
Data to clock- - - - -	35 ns, minimum
Input hold time, $t(\text{HOLD})$, type 03	
Data to enable (high)- - - - -	0 ns, maximum
Data to enable (low) - - - - -	4 ns, maximum
Input hold time, $t(\text{HOLD})$, type 04	
Data to enable (high)- - - - -	0 ns, maximum
Data to enable (low) - - - - -	7 ns, maximum
Input hold time, $t(\text{HOLD})$, type 04	
Data to set (low)- - - - -	8 ns, maximum

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

1/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline. Case outline shall be as specified in 1.2.3 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.

3.2.4 Schematic circuits and logic diagrams. The schematic circuits and logic diagrams shall be as specified on figure 3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.6).

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container.

a. Country of origin.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 5 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) $T_A = 125^\circ\text{C}$ minimum.

- b. Interim and final electrical test parameters shall be as specified in table II, except the interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Percent defective allowable (PDA) - The PDA for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II.
- b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Operating life-test (method 1005 of MIL-STD-883) conditions, or equivalent:
 - (1) Test conditions D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Device types	Limits		Unit	
				Min	Max		
High-level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V};$ $V_{IN} = 0.8 \text{ V}$	$I_{OH} = -400 \mu\text{A}$	01,02	2.4	Volts	
			$I_{OH} = -800 \mu\text{A}$	03,04	2.4	Volts	
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V};$ $V_{IN} = 2.0 \text{ V}$	$I_{OL} = 16 \text{ mA}$	01,02,04	0.4	Volts	
			$I_{OL} = 14.4 \text{ mA}$	03	0.4	Volts	
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}; V_{IN} = -12 \text{ mA}$	A11		-1.5	Volts	
Low-level input current, data	I_{IL1}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.4 \text{ V}$	01,02	-1.4	-3.2	mA	
			03 4/	-0.5	-2.4	mA	
			04	-0.7	-2.7	mA	
Low-level input current Clock	I_{IL2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.4 \text{ V } 1/$	01,02	-2.8	-6.4	mA	
			03,04	-0.7	-1.6	mA	
			04	-0.7	-1.6	mA	
			01,02		80	μA	
High-level input current, data	I_{IH1}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.4 \text{ V } 1/$	03		40	μA	
			04		60	μA	
			01,02		200	μA	
High-level input current, data	I_{IH2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V } 1/$	03,04		100	μA	
			01,02		160	μA	
			03,04		40	μA	
High-level input current Clock	I_{IH3}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.4 \text{ V } 1/$	04		40	μA	
			01,02		400	μA	
			03,04		100	μA	
			04		100	μA	
High-level input current Master reset and enable Set	I_{IH4}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V } 1/$	01,02		-20	-57	mA
			03,04		-10	-70	mA
			04		-20	-100	mA
			01,02		46	mA	
Short-circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V } 2/ \underline{3/}$	03		106	mA	
			04		55	mA	
			01,02				
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V } 2/;$ $V_{IN} = 4.5 \text{ V}$	03				
			04				
			01,02				
Propagation delay time for types 01 and 02							
To high level, from D input to Q output	t_{PLH1}	$C_L = 50 \text{ pF } \pm 10\%;$ $R_L = 390 \text{ ohms } \pm 5\%$	01,02	2	44	ns	
To high level, from D input to \bar{Q} output	t_{PLH2}		01	2	55	ns	
To low level, from D input to Q output	t_{PHL1}		01,02	2	38	ns	
To low level, from D input to \bar{Q} output	t_{PHL2}		01	2	25	ns	
To low level, from clock input to Q output	t_{PHL3}		01	2	25	ns	
To high level, from clock input to Q output	t_{PLH3}		01,02	2	44	ns	
To low level, from clock input to \bar{Q} output	t_{PHL4}		01	2	25	ns	
To high level from clock input to \bar{Q} output	t_{PLH4}		01	2	44	ns	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions	Device types	Limits		Unit
				Min	Max	
Propagation delay time for types 03 and 04						
To high level, from enable to output	t_{PLH1}	$C_L = 50 \text{ pF} \pm 10\%$, $R_L = 390 \text{ ohms} \pm 5\%$	03,04	3	60	ns
To low level, from enable to output	t_{PHL1}		03,04	3	40	ns
To high level, from data to output	t_{PLH2}		03,04	3	49	ns
To low level, from data to output	t_{PHL2}		03,04	3	37	ns
To low level, from master reset to output	t_{PHL3}		03,04	3	37	ns
To high level, from set to output	t_{PLH4}		04	9	47	ns

- 1/ All unspecified inputs at 5.5 volts.
- 2/ All unspecified inputs grounded.
- 3/ Not more than one output should be shorted at a time.
- 4/ Circuit B limits for I_{IL1} shall be -1.6 mA, maximum.
- 5/ Circuit B and C limits for I_{OS} shall be -20 mA minimum to -57 mA maximum.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)		
	Class S devices	Class B devices	Class C devices
Interim electrical parameters (pre burn-in) (Method 5004)	1	1	None
Final electrical test parameters (Method 5005)	1*, 2, 3, 9, 10, 11	1*, 2, 3, 9	1
Group A test requirements (Method 5005)	1, 2, 3, 9, 10, 11	1, 2, 3, 9	1, 2, 3, 9
Group C end point electrical parameters (Method 5005)	N/A	1, 2, 3	1
Additional electrical subgroups for group C periodic inspection	N/A	10, 11	10, 11
Group D end point electrical parameters (Method 5005)	1, 2, 3	1, 2, 3	1

* PDA applies to subgroup 1 (see 4.3c).

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Life test and burn-in cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of bias. Alternately, the bias may be removed during cooling, if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for the packaging of microcircuits shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic support.

6.3 Ordering data. The contract should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for preservation and packing.
- f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number.
- i. Requirements for JAN marking.

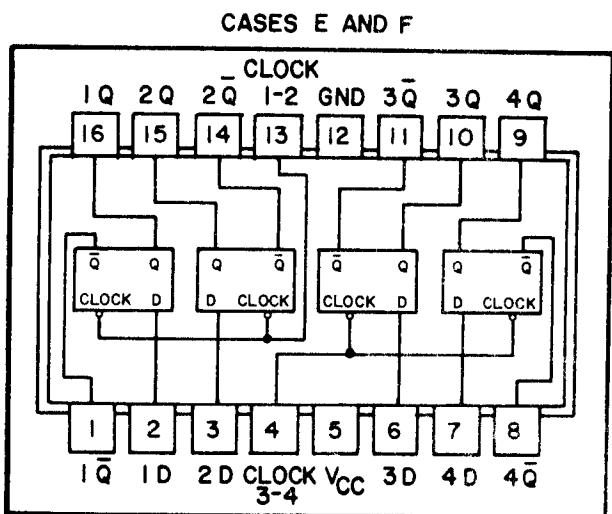
6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1331, and as follows:

GND - - - - - Electrical ground (common terminal)
 VIN - - - - - Voltage level at an input terminal

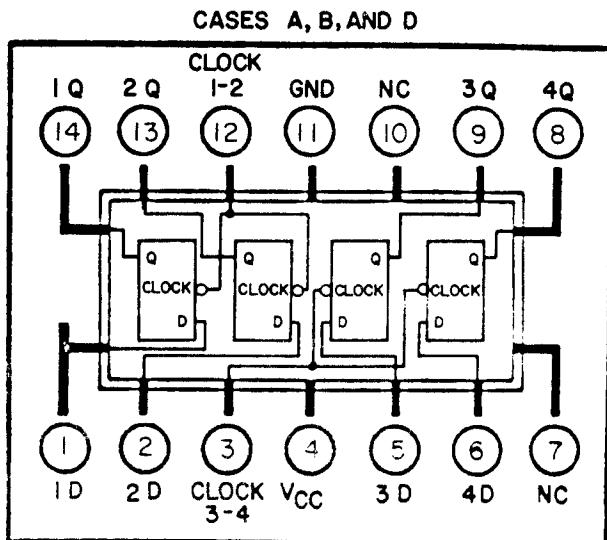
6.5 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

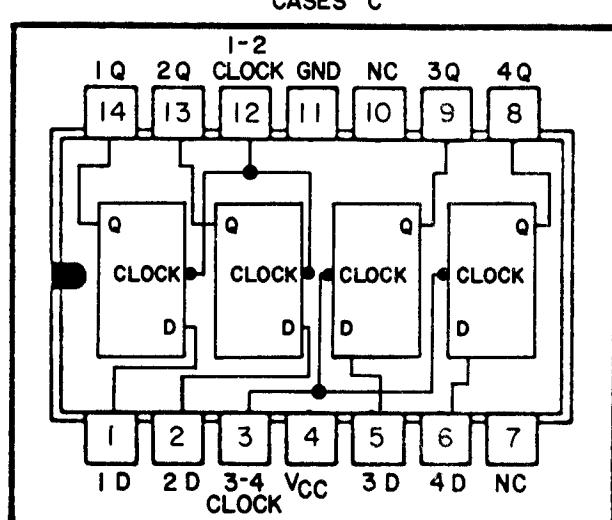
Device type 01



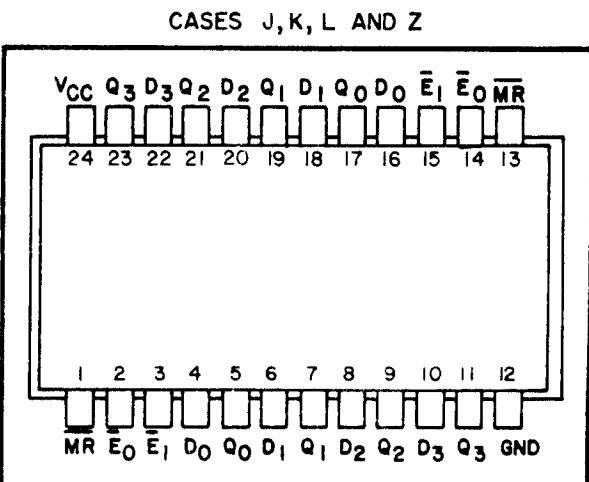
Device type 02



Device type 02



Device type 03



Device type 04

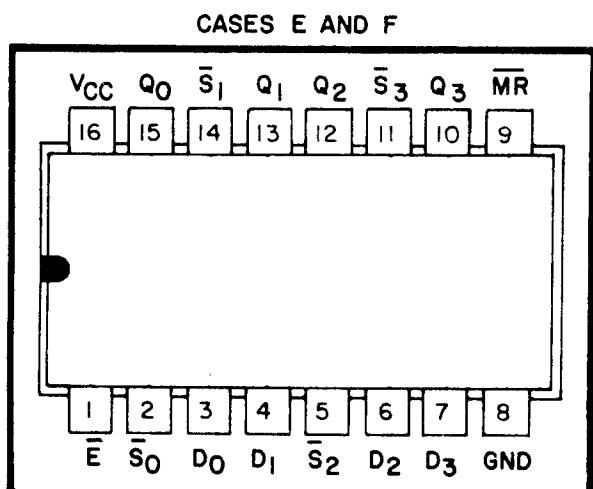


FIGURE 1. Terminal connections.

Device types 01 and 02

Truth table	
t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:

1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

Device type 03

Truth table					
MR	$\overline{E_0}$	$\overline{E_1}$	D	Q_n	Operation
H	L	L	L	L	Data entry
H	L	L	H	H	Data entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

 X = Don't care

L = Low voltage level

H = High voltage level

 Q_{n-1} = Previous output state Q_n = Present output state

Device type 04

Truth table					
MR	\overline{E}	D	\overline{S}	Q_{n-1}	Operation
H	L	L	L	L	D mode
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	Reset

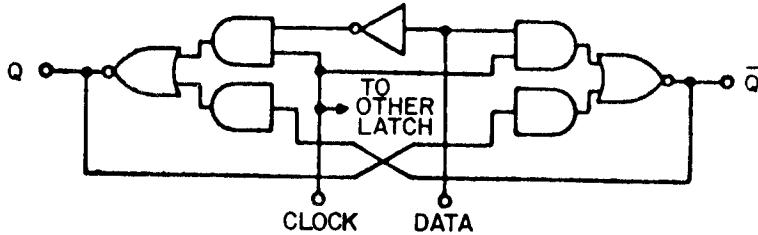
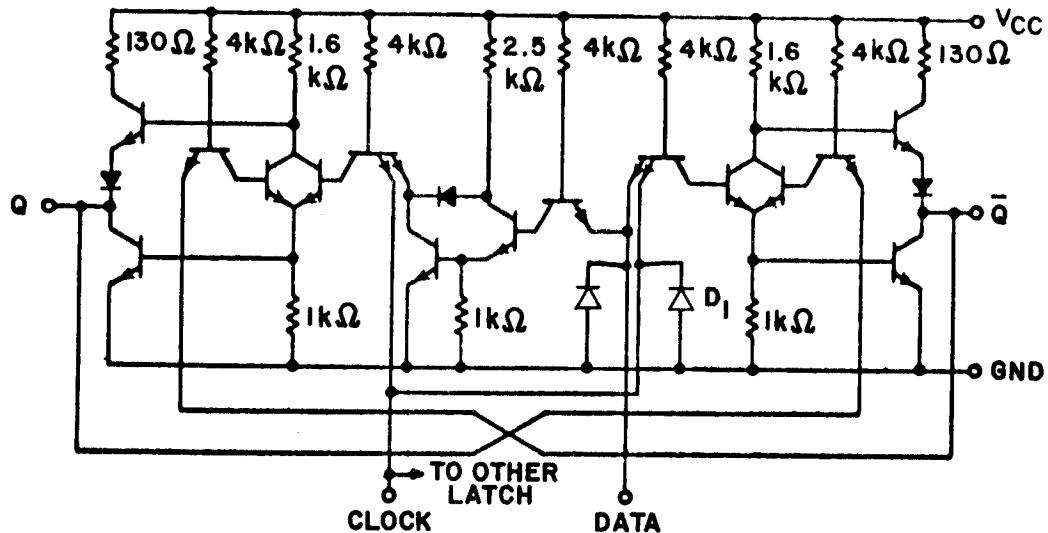
 X = Don't care

L = Low voltage level

H = High voltage level

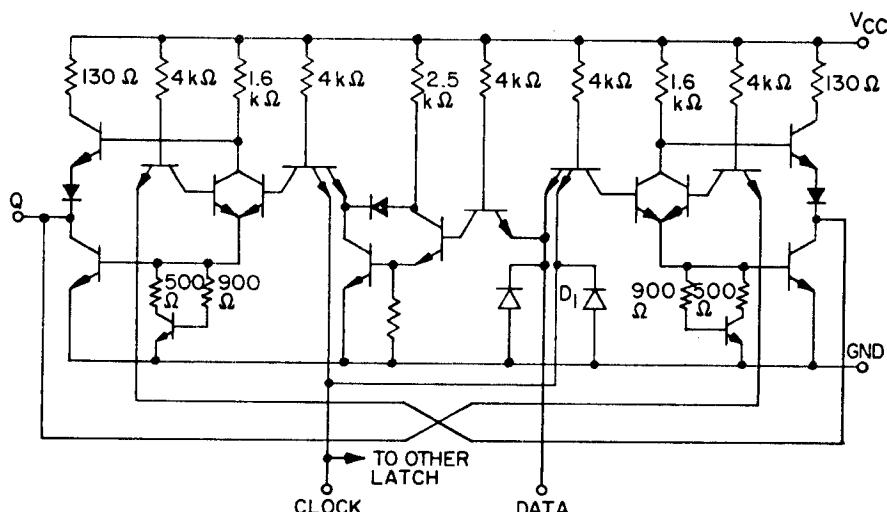
 Q_{n-1} = Previous output state Q_n = Present output state

FIGURE 2. Truth tables.

LOGIC DIAGRAM (EACH LATCH)CIRCUIT A (EACH LATCH)

NOTES:

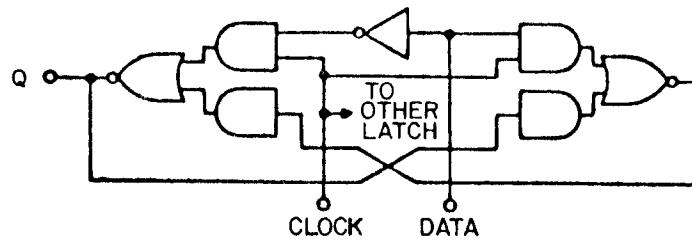
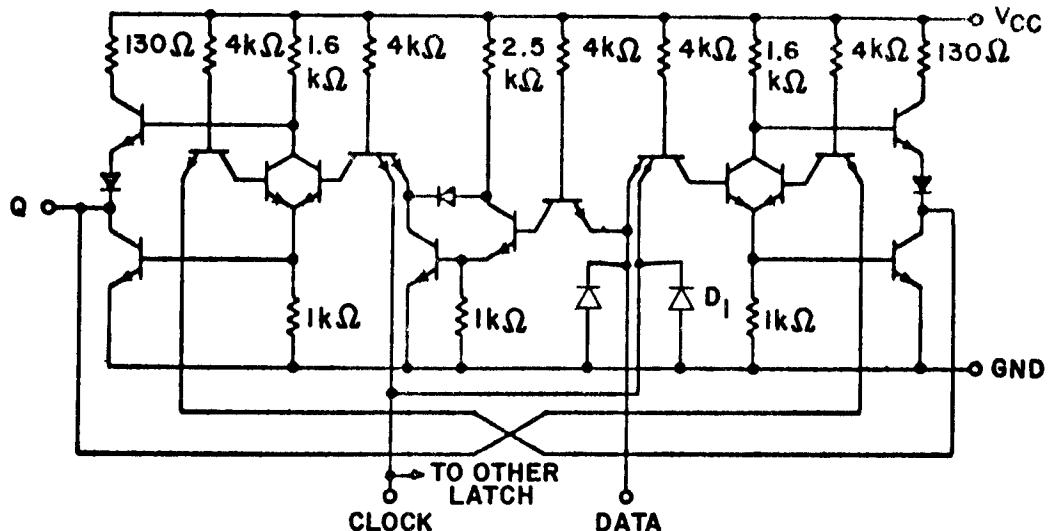
1. All resistance values shown are nominal.
2. D₁ is common to each latch in the pair.

CIRCUIT B (EACH LATCH)

NOTES:

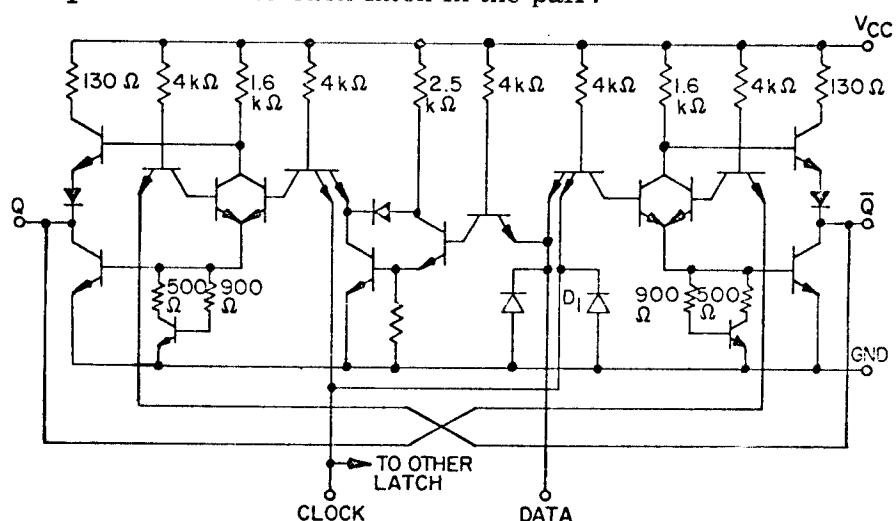
1. All resistance values shown are nominal.
2. D₁ is common to each latch in the pair.

FIGURE 3. Logic diagram and schematic circuits for device type 01.

LOGIC DIAGRAM (EACH LATCH)CIRCUIT A (EACH LATCH)

NOTES:

1. All resistance values shown are nominal.
2. D₁ is common to each latch in the pair.

CIRCUIT B (EACH LATCH)

NOTES:

1. All resistance values shown are nominal.
2. D₁ is common to each latch in the pair.

FIGURE 3. Logic diagram and schematic circuits for device type 02 - Continued.

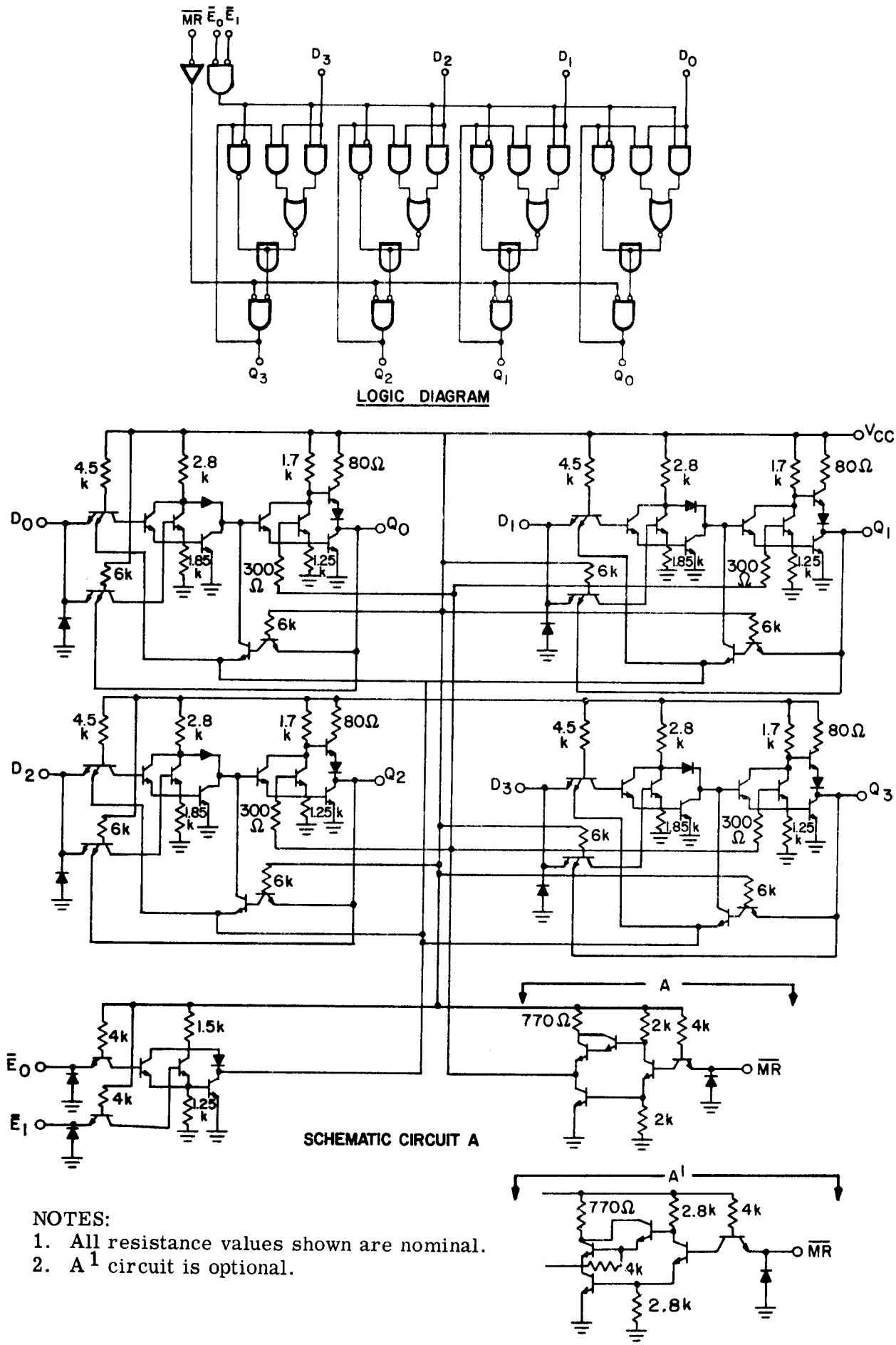


FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

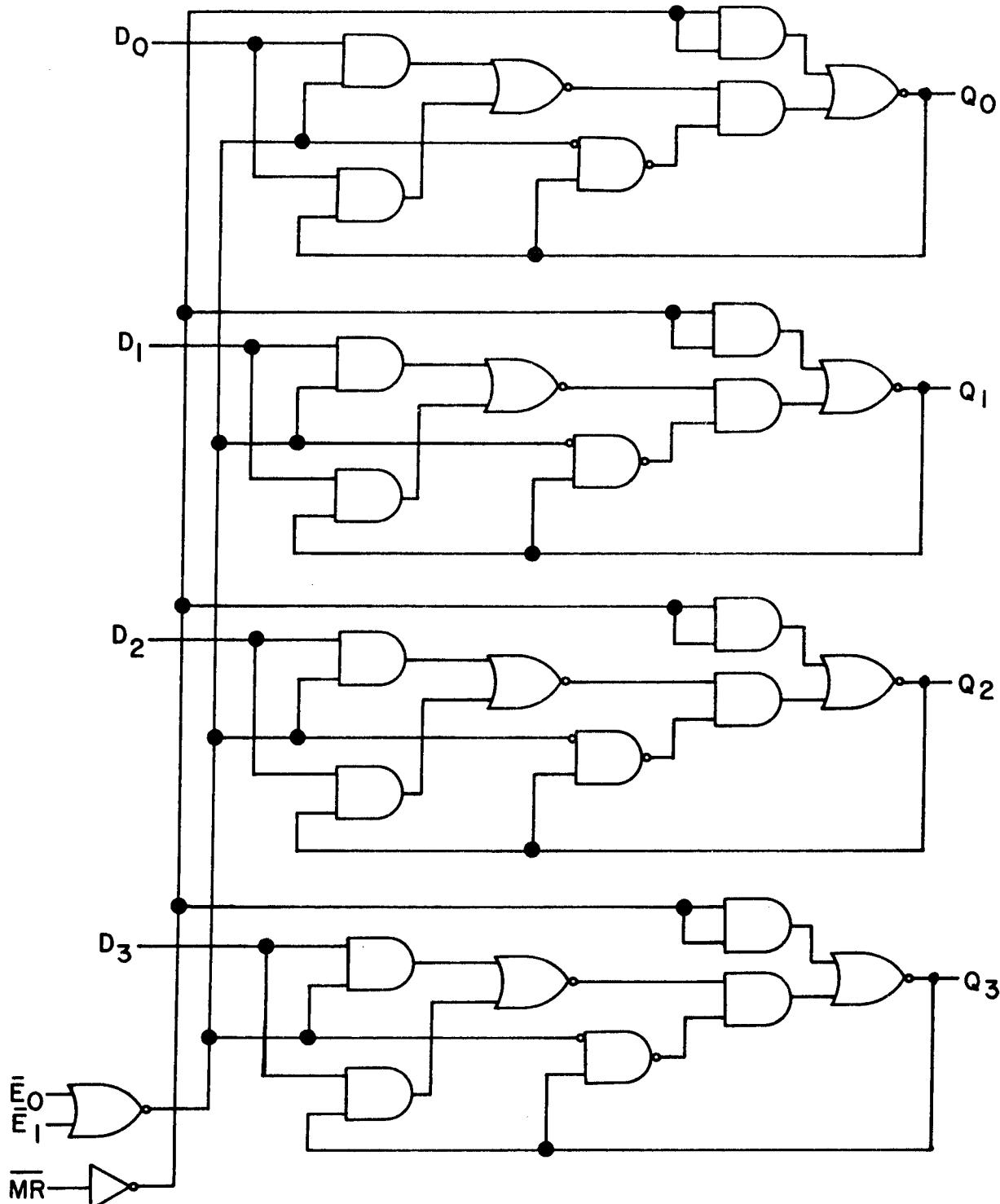
LOGIC DIAGRAM (CIRCUIT B)

FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

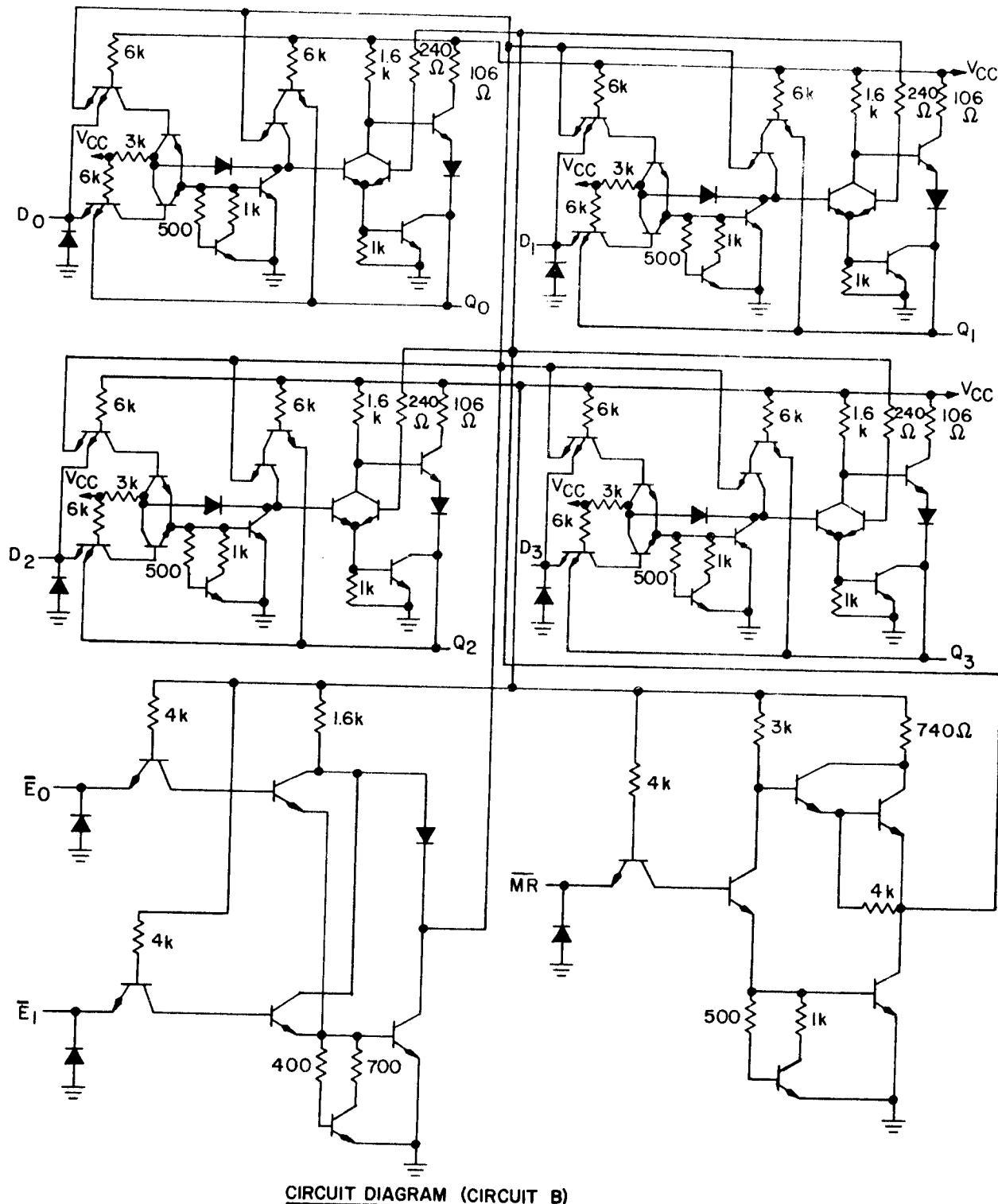


FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

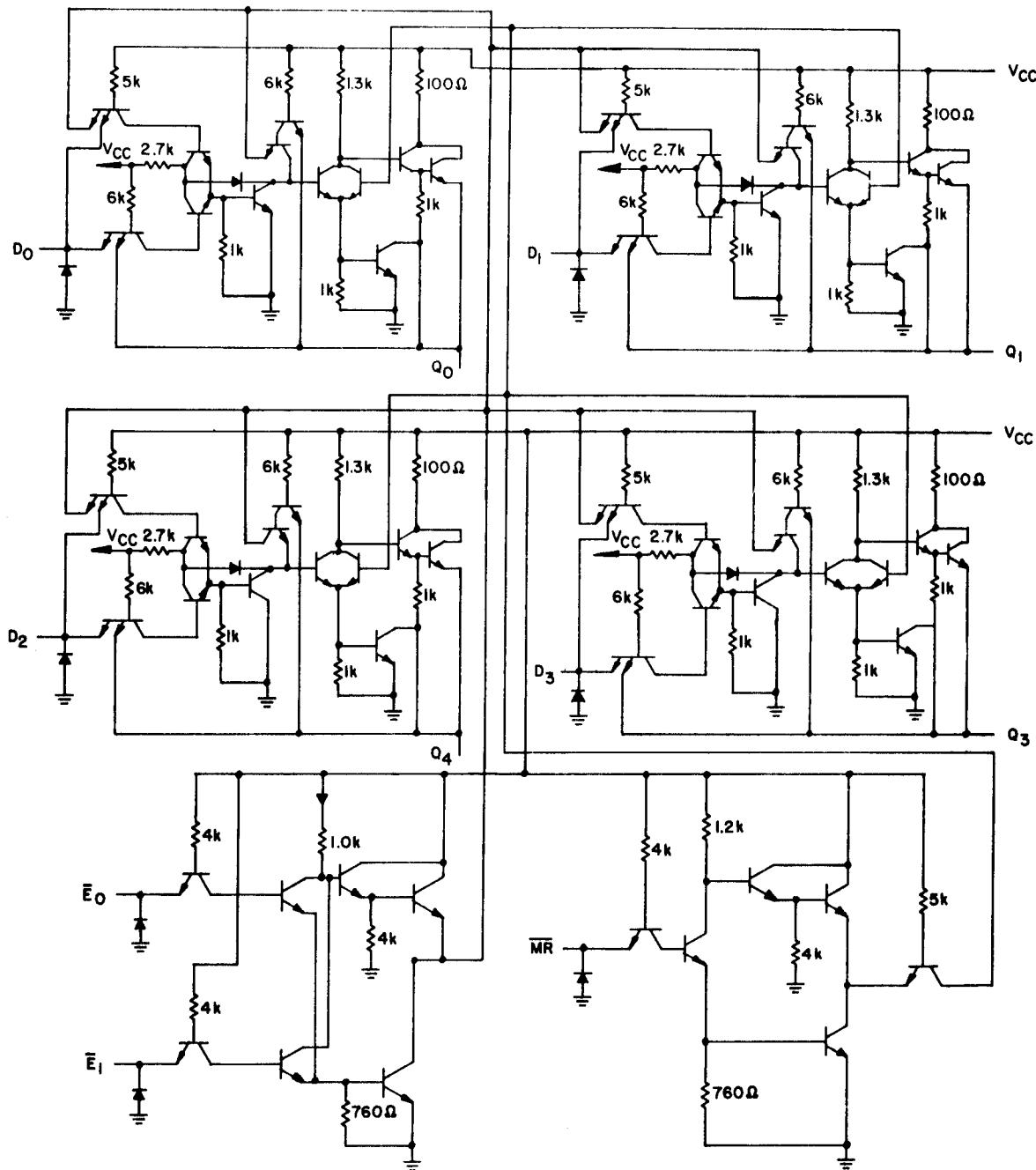
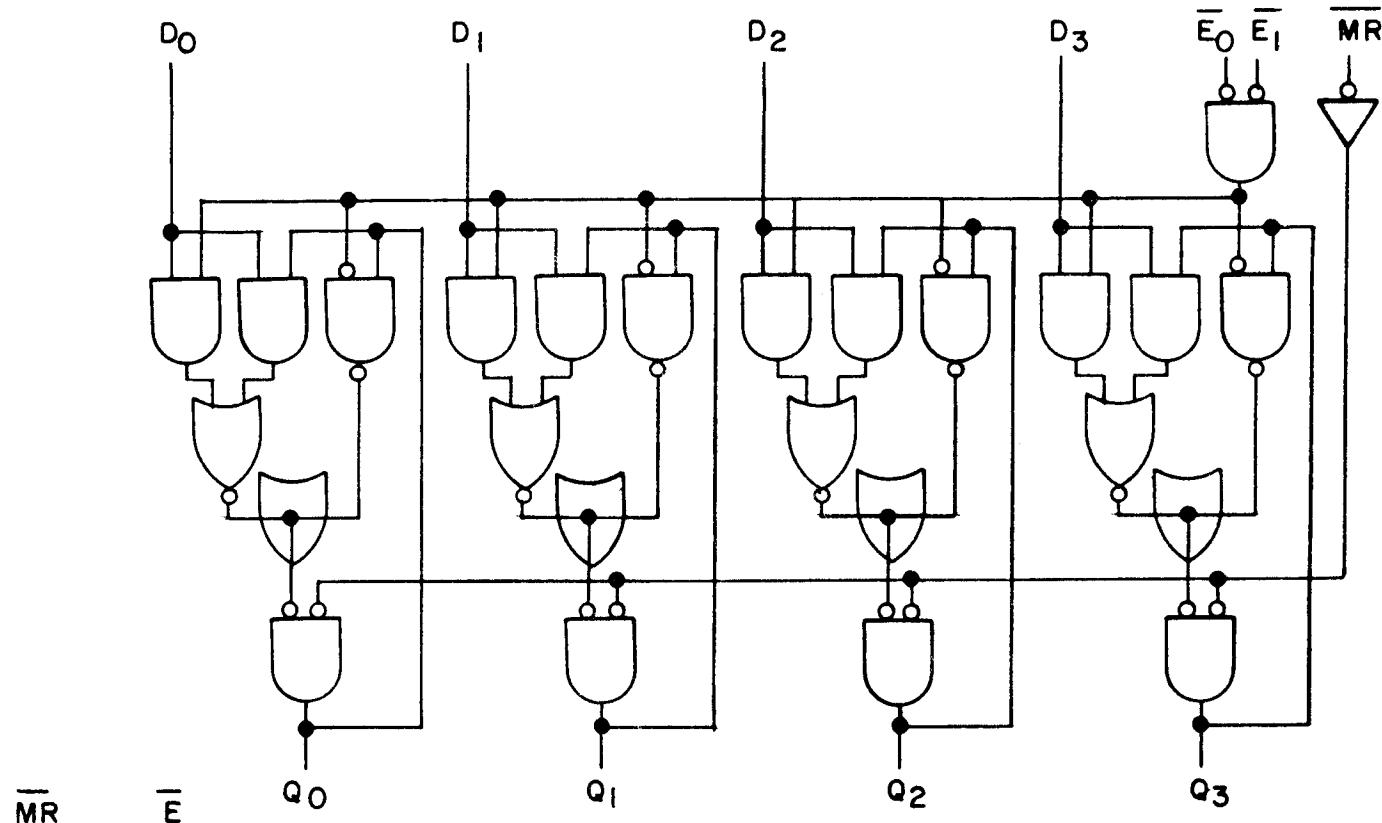
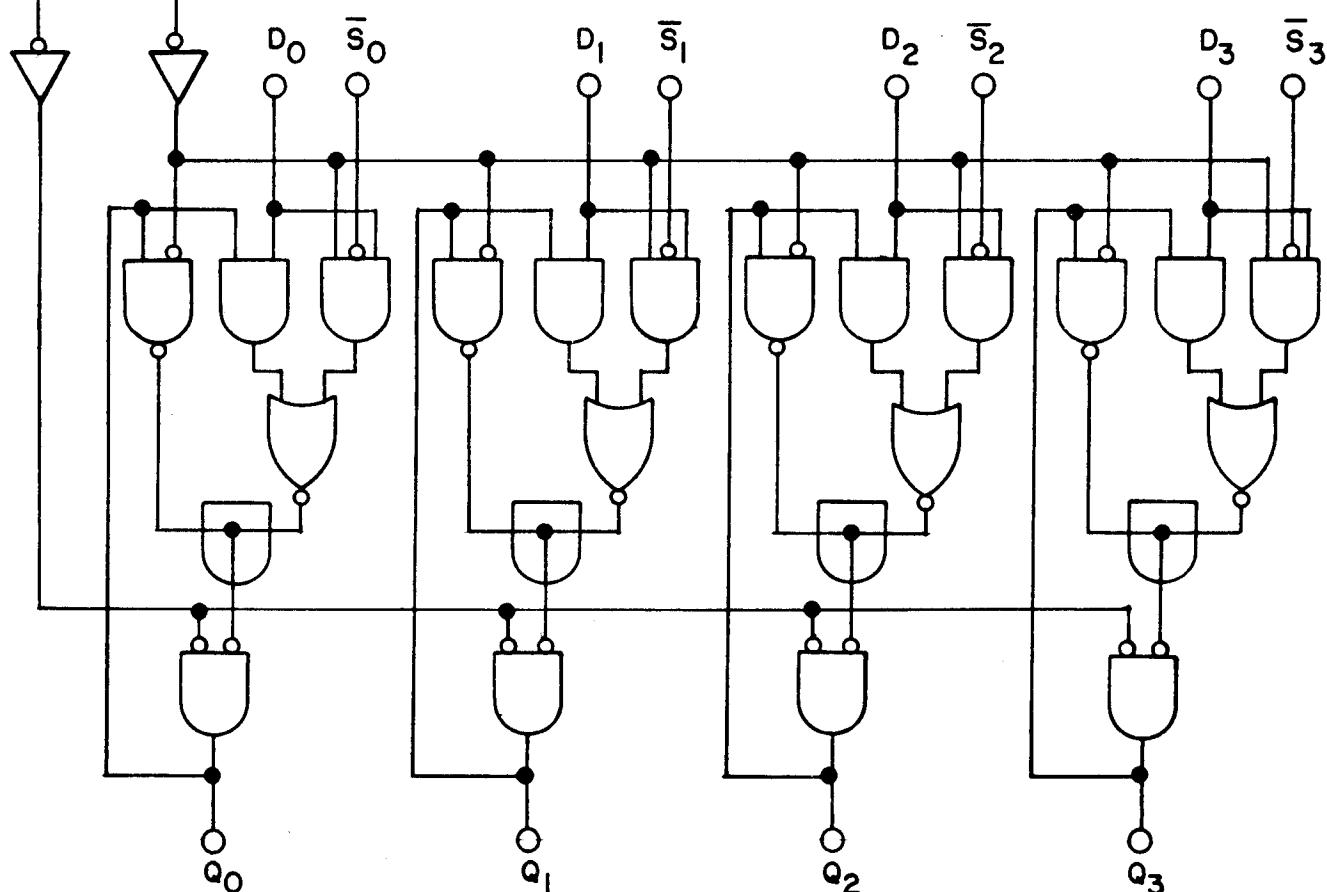
CIRCUIT DIAGRAM (CIRCUIT C)

FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.



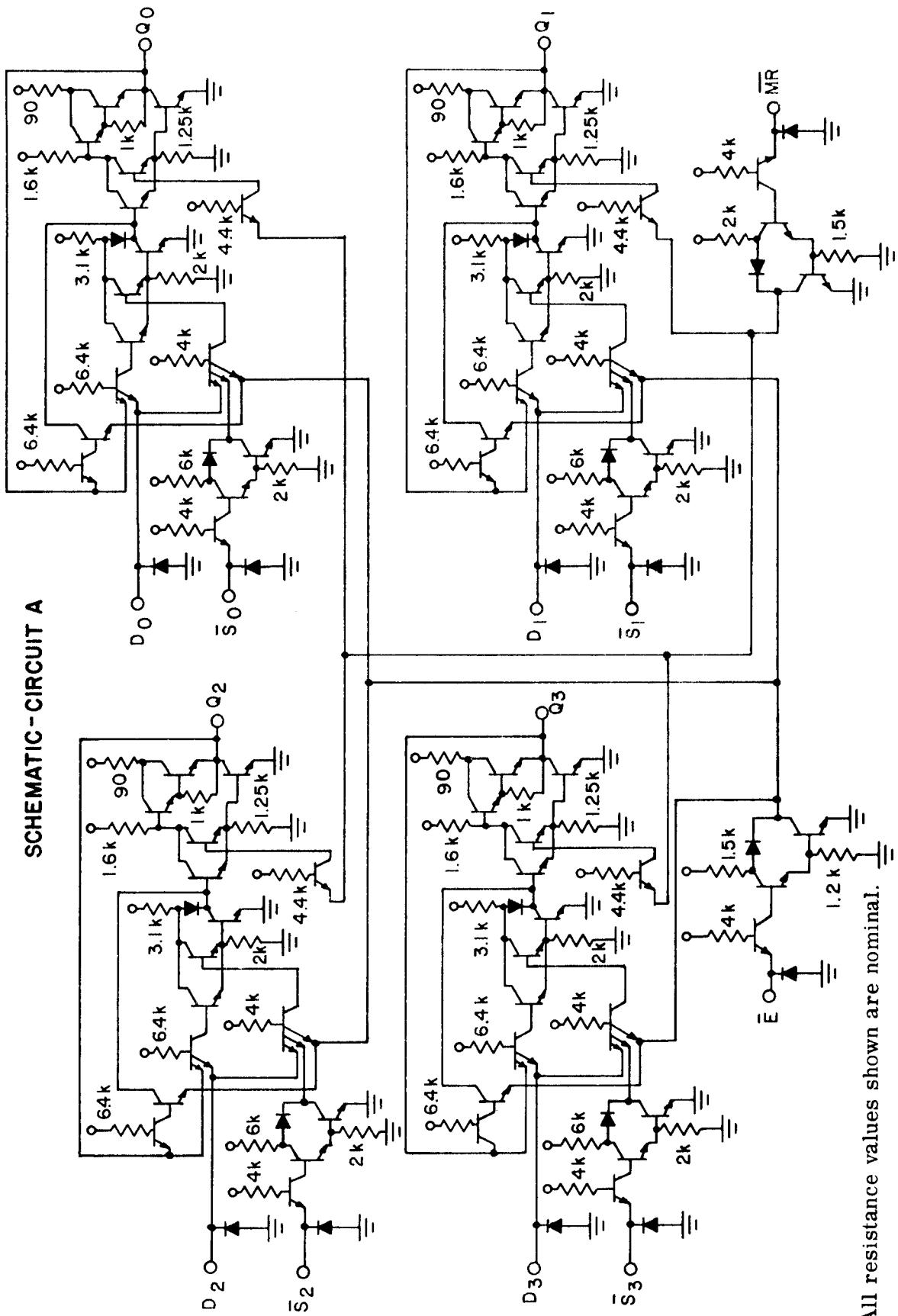
LOGIC DIAGRAM - Device type 03



LOGIC DIAGRAM - Device type 04

FIGURE 3. Logic diagram and schematic circuits - Continued.

SCHEMATIC-CIRCUIT A



NOTE: All resistance values shown are nominal.

FIGURE 3. Logic diagram and schematic circuits for device type 04 - Continued.

SCHEMATIC-CIRCUIT B

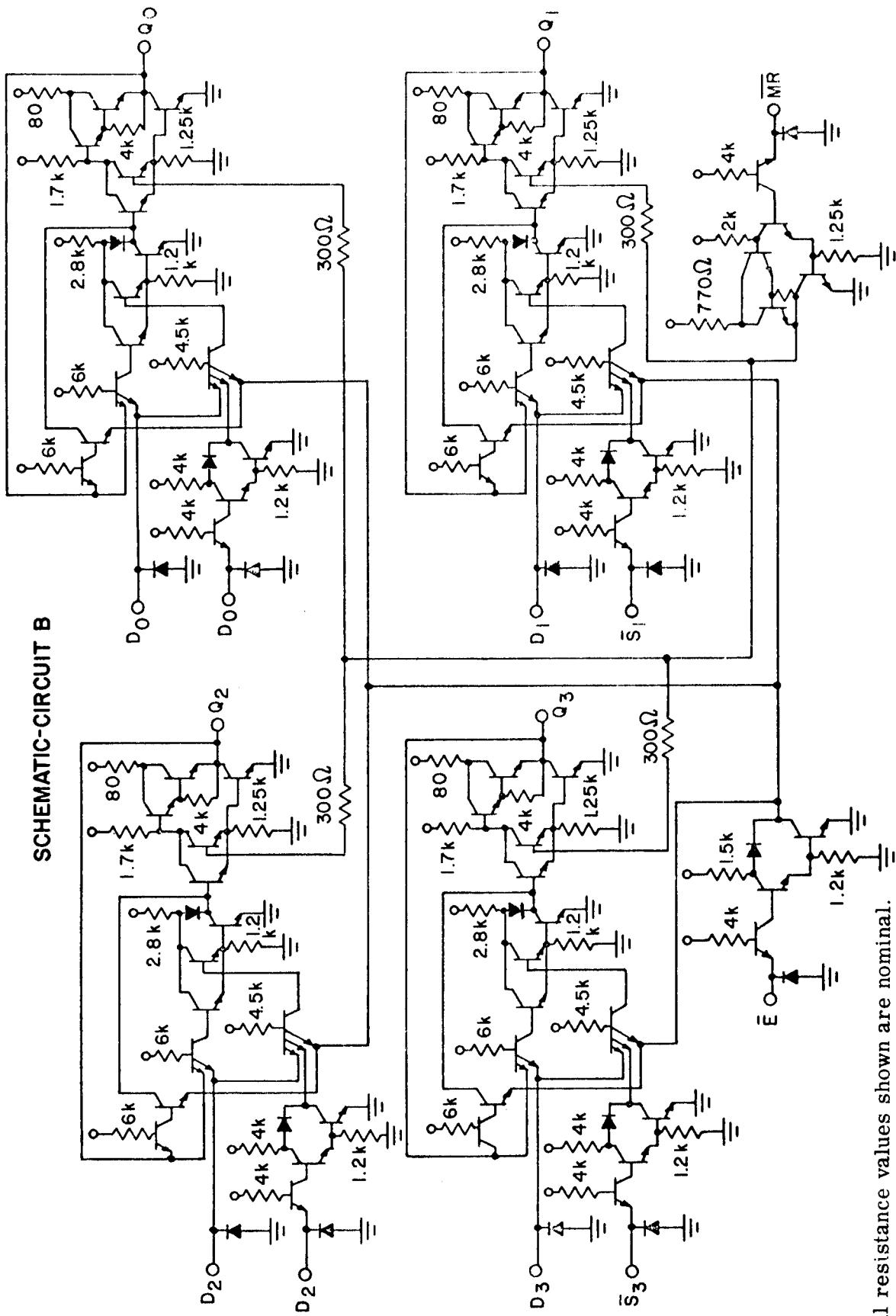
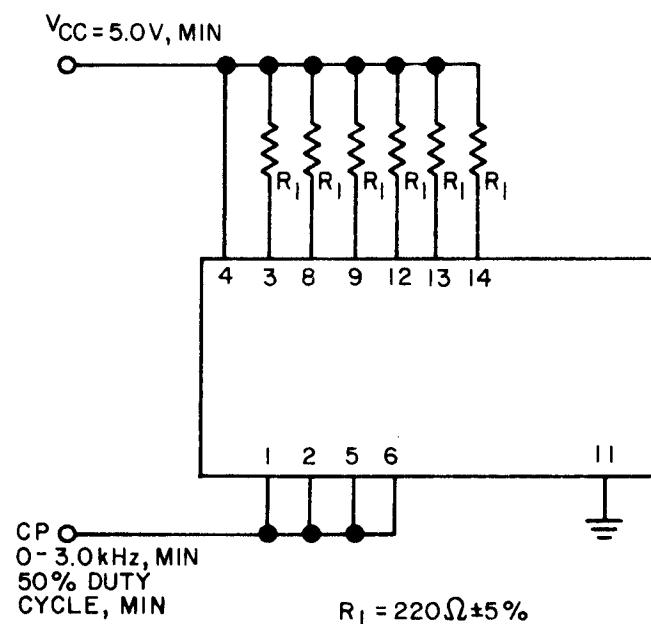
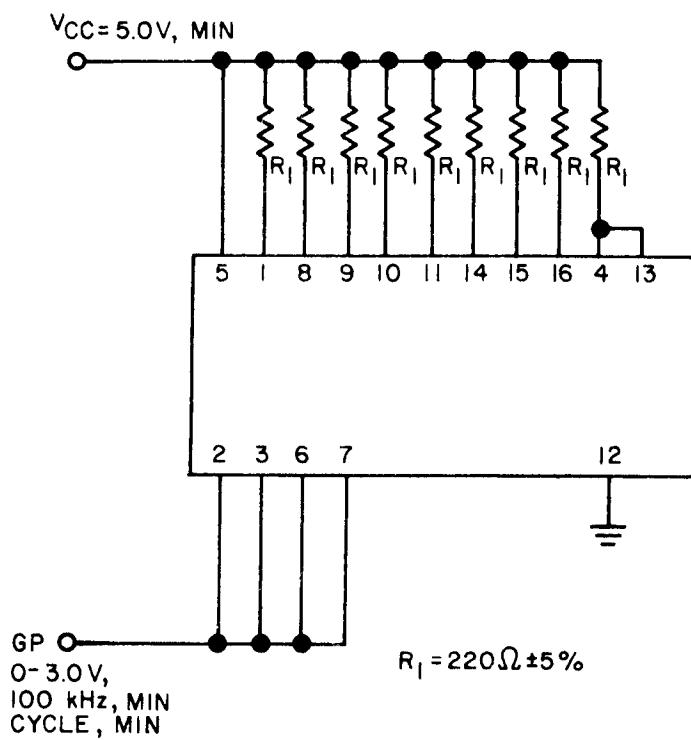


FIGURE 3. Logic diagram and schematic circuits for device type 04 - Continued.

NOTE: All resistance values shown are nominal.

FIGURE 4. Burn-in and life test circuit.

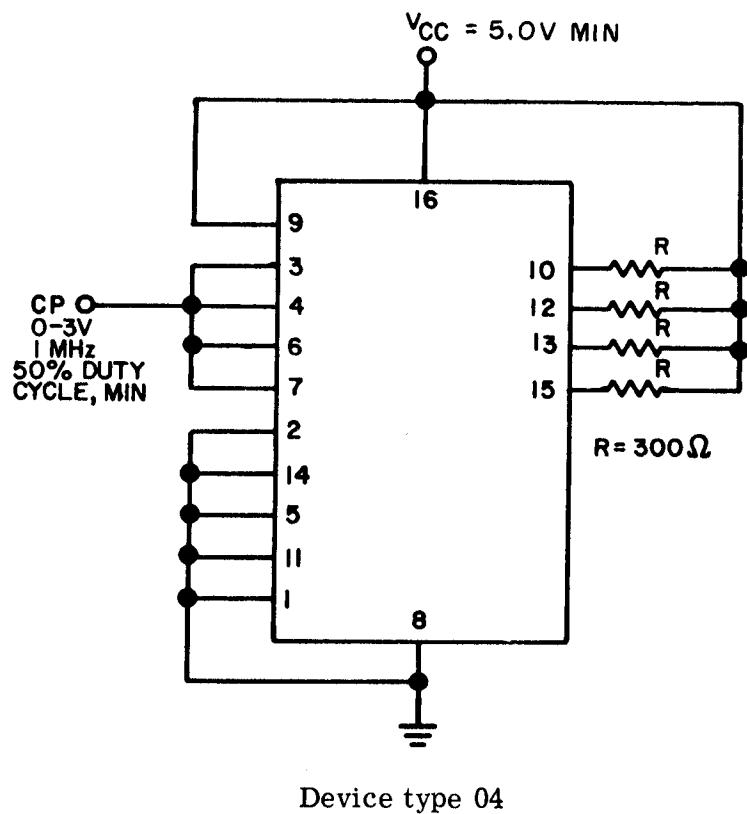
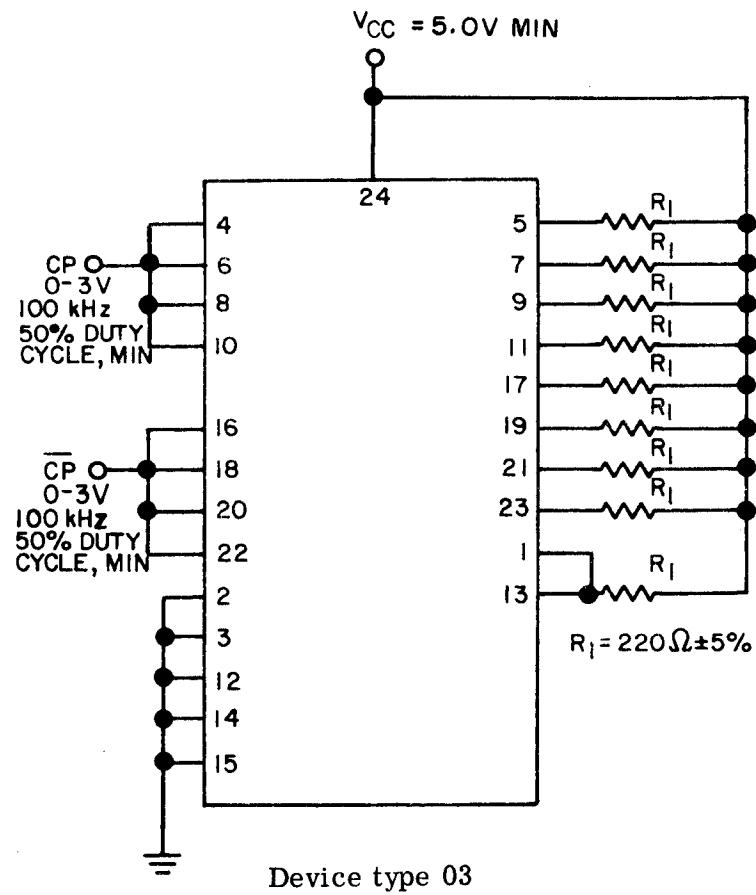
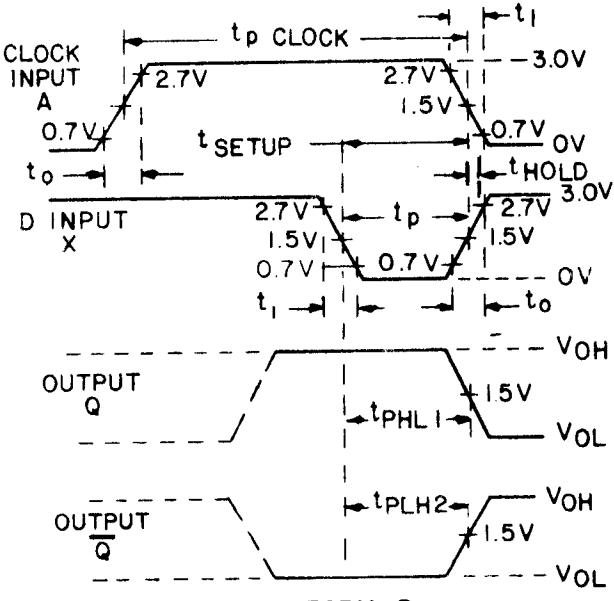
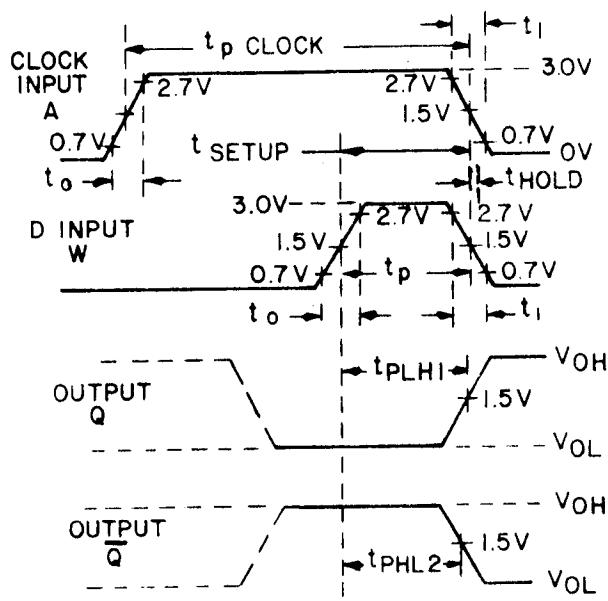
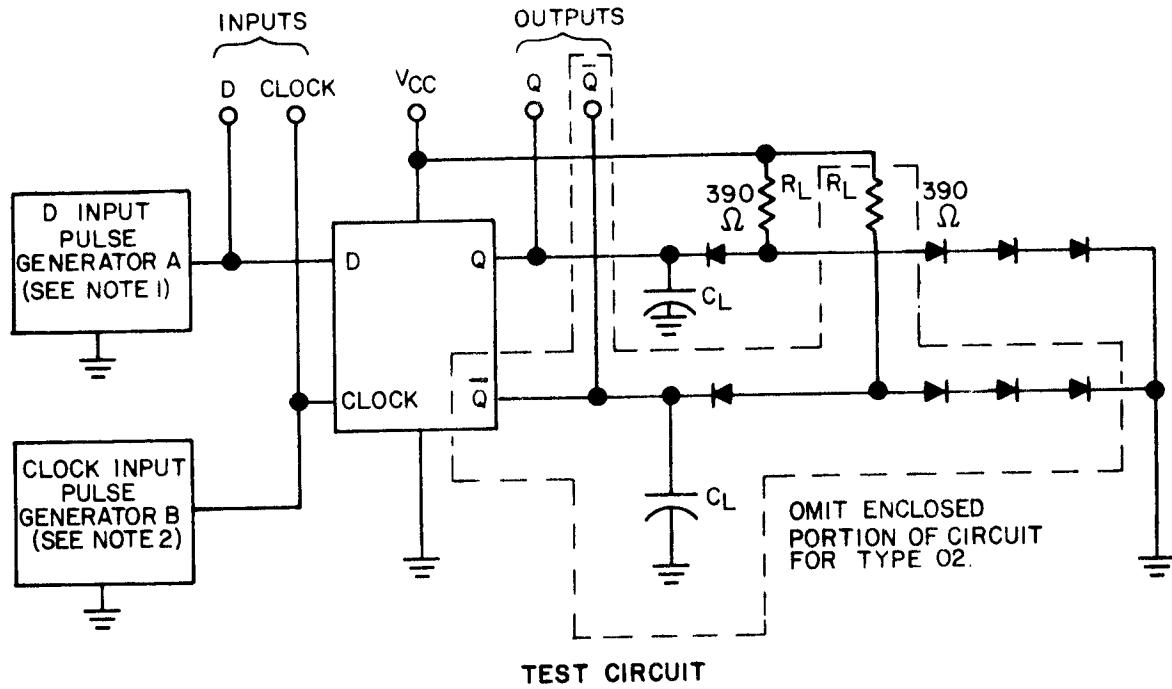
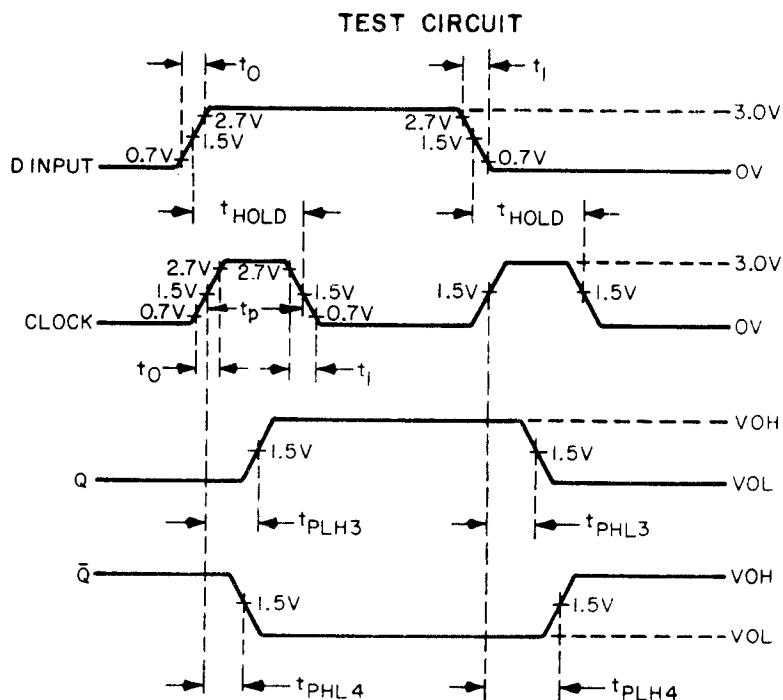
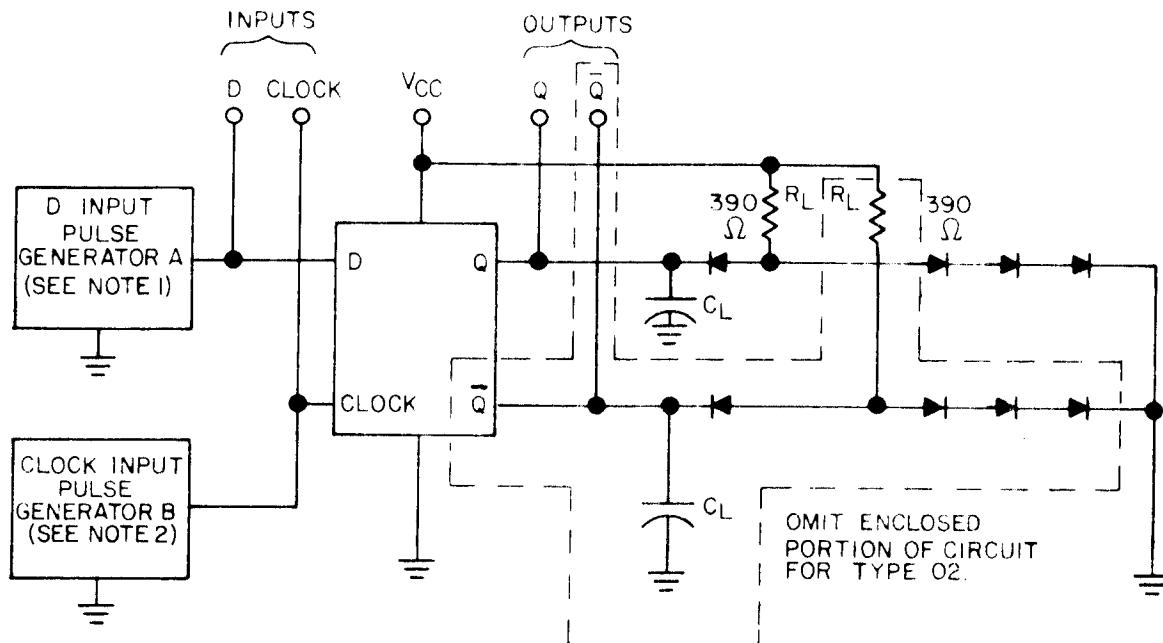


FIGURE 4. Burn-in and life test circuit - Continued.

**NOTES:**

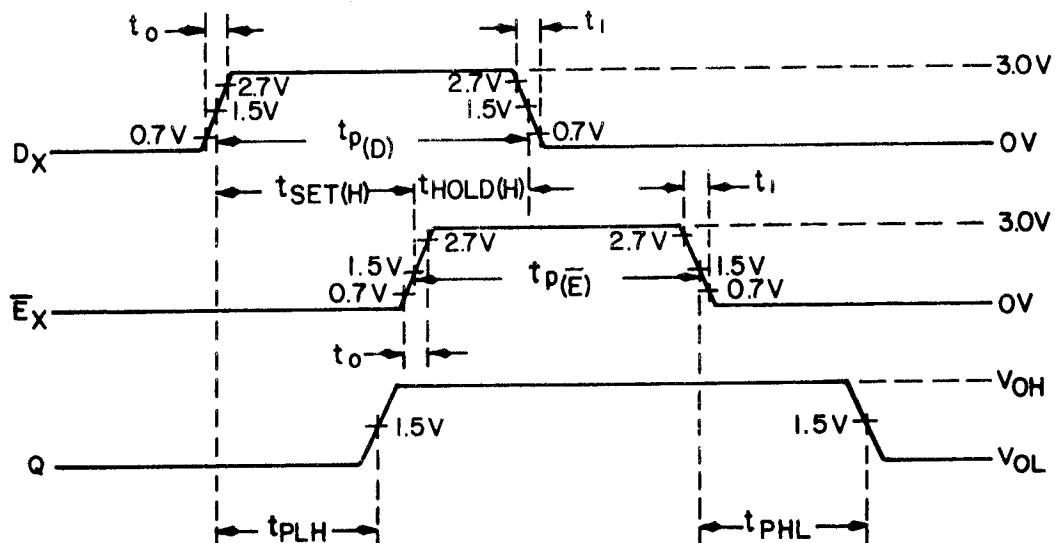
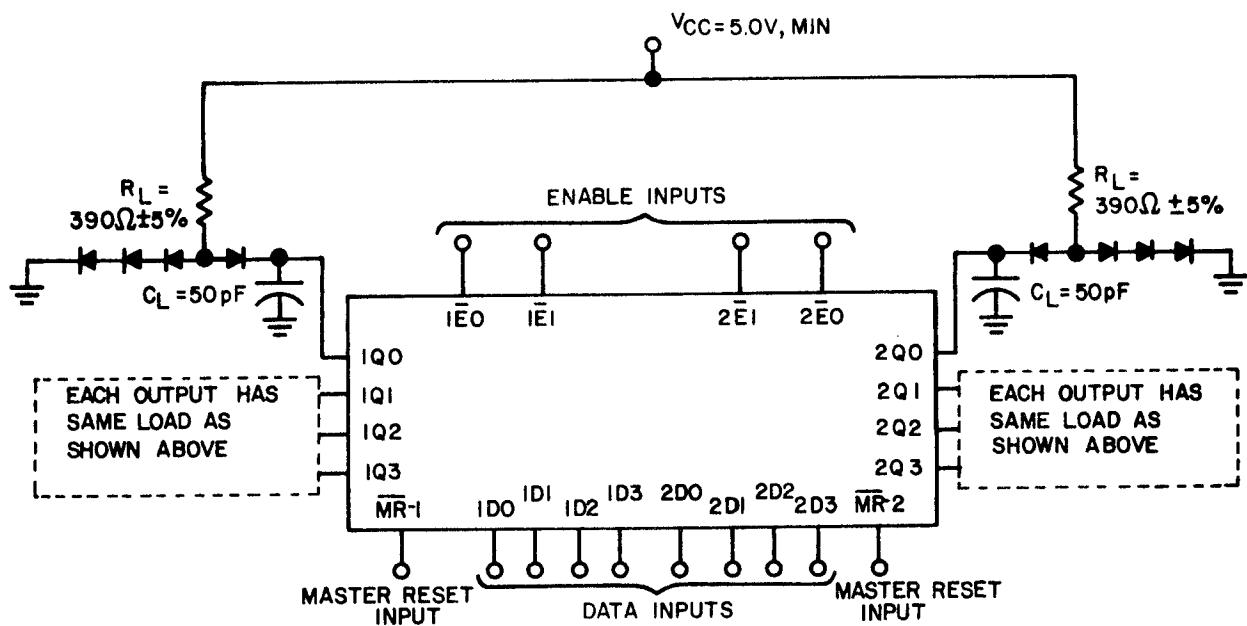
1. The D input pulse generator has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 = t_0 \leq 10 \text{ ns}$, $t_p = 30 \text{ ns}$, $t_{(\text{setup})} = 25 \text{ ns}$, $t_{(\text{HOLD})} = 5 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$ and $Z_{out} \approx 50 \Omega$.
2. The clock pulse generator has the following characteristics: $V_{gen} = 3 \text{ V}$, minimum, $t_1 = t_0 \leq 10 \text{ ns}$, $t_{p(\text{clock})} = 500 \text{ ns}$, and $\text{PRR} = 1 \text{ MHz}$.
3. Prior to testing the device shall be preconditioned to a high logic level for waveform A and to a low logic level for waveform B.
4. Each latch is tested separately.
5. $C_L = 50 \text{ pF}$, which includes probe and jig capacitance.
6. $R_L = 390 \Omega \pm 5\%$.
7. The \bar{Q} waveforms are not applicable to type 02.
8. All diodes are 1N3064 or equivalent.

FIGURE 5. Switching test circuit and waveforms for device types 01 and 02.

**NOTES:**

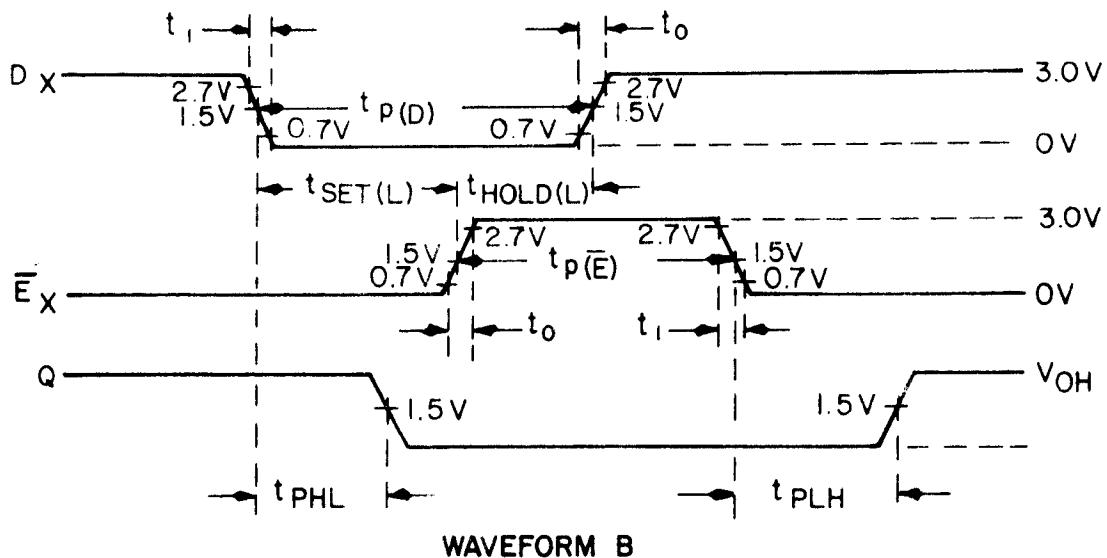
1. D input pulse generator has the following characteristics: $V_{gen} = 3$ V, minimum, $t_0 = t_1 \leq 10$ ns, and PRR = 500 kHz at 50% duty cycle. For subgroups 7 and 8, PRR ≤ 25 kHz at 50% duty cycle and PRR (D input) = 1/2 PRR (clock).
2. Clock input pulse generator has the following characteristics: $V_{gen} = 3$ V, minimum, $t_0 = t_1 \leq 10$ ns, $t_p(\text{clock}) = 35$ ns, $t_{(\text{HOLD})} = 35$ ns and PRR = 1 MHz. For subgroups 7 and 8, PRR ≤ 50 kHz.
3. Each latch is tested separately.
4. $C_L = 50$ pF, which includes probe and jig capacitance.
5. $R_L = 390 \Omega \pm 5\%$.
6. The \bar{Q} waveforms are not applicable to device type 02.
7. All diodes are 1N3064 or equivalent.

FIGURE 6. Switching test circuit and waveforms for device types 01 and 02.

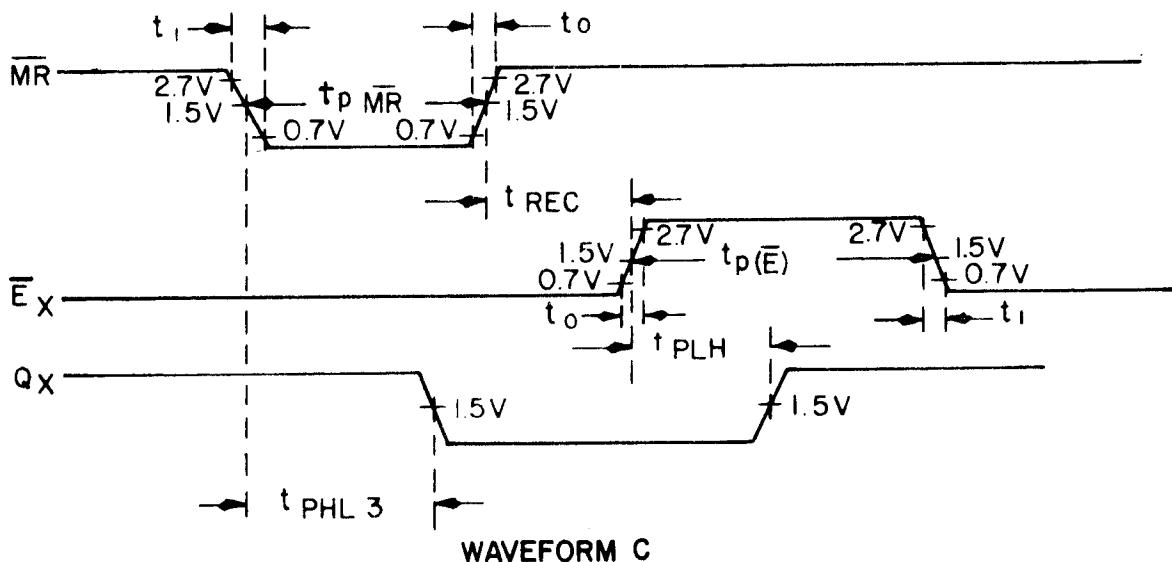
**NOTES:**

1. The data inputs have the following characteristics: $V_{gen} = 3$ V, $t_0 = t_1 \leq 10$ ns, $t_p(D) = 10$ ns, and PRR = 1 MHz.
2. The enable inputs have the following characteristics: $V_{gen} = 3$ V, $t_0 = t_1 \leq 10$ ns, $t_{SET(H)} = 10$ ns, $t_{HOLD(H)} = 0$ ns, $t_p(\bar{E}) = 20$ ns, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.
3. Each latch is tested separately.
4. $C_L = 50 \text{ pF}$, which includes probe and jig capacitance.
5. $R_L = 390\Omega \pm 5\%$.
6. All diodes are 1N3064 or equivalent.

FIGURE 7. Switching time test circuit and waveforms for device type 03.

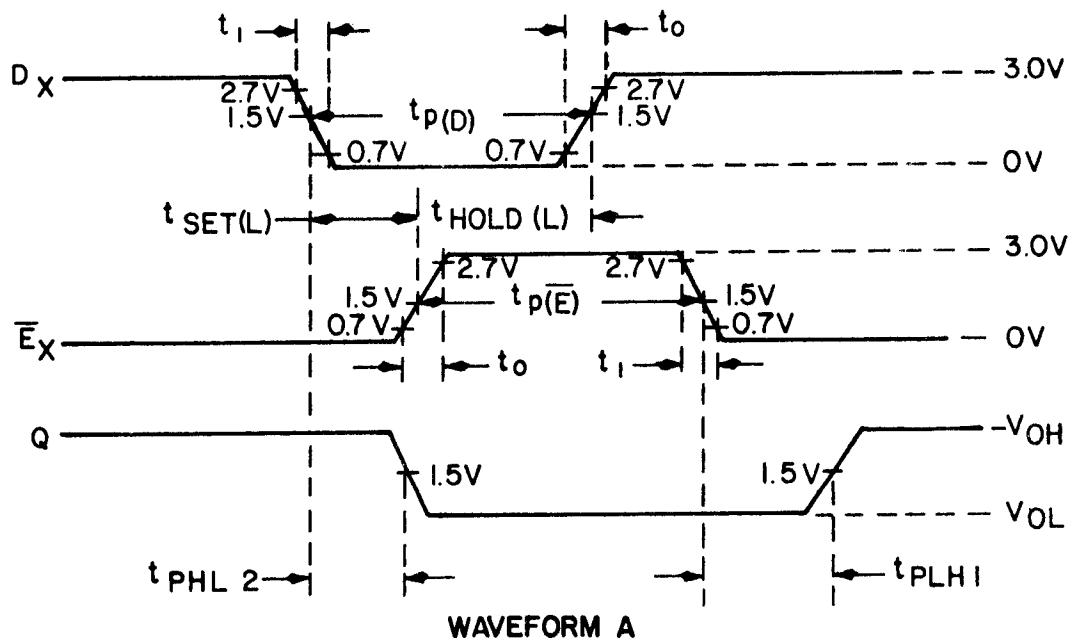
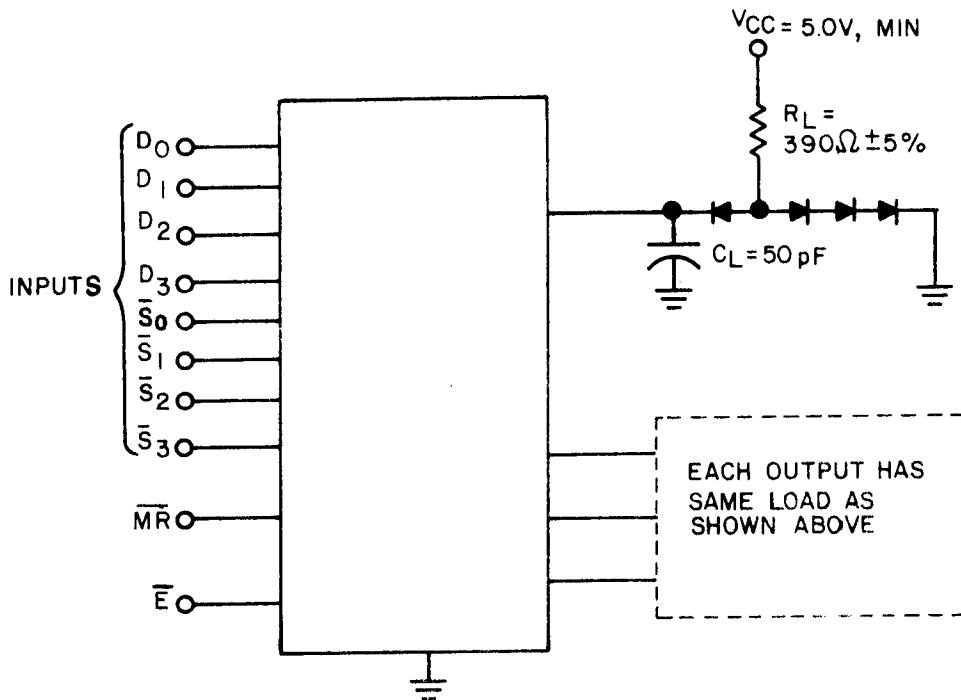
**NOTES:**

1. The data inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(D) = 26 \text{ ns}$, and PRR = 1 MHz.
2. The enable inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{SET(L)} = 16$, $t_{HOLD(L)} = 10$, $t_p(\bar{E}) = 20 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.

**NOTES:**

1. The master reset inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(\bar{MR}) = 20 \text{ ns}$ and PRR = 1 MHz.
2. The enable inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{REC} = 10 \text{ ns}$, $t_p(\bar{E}) = 20 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.

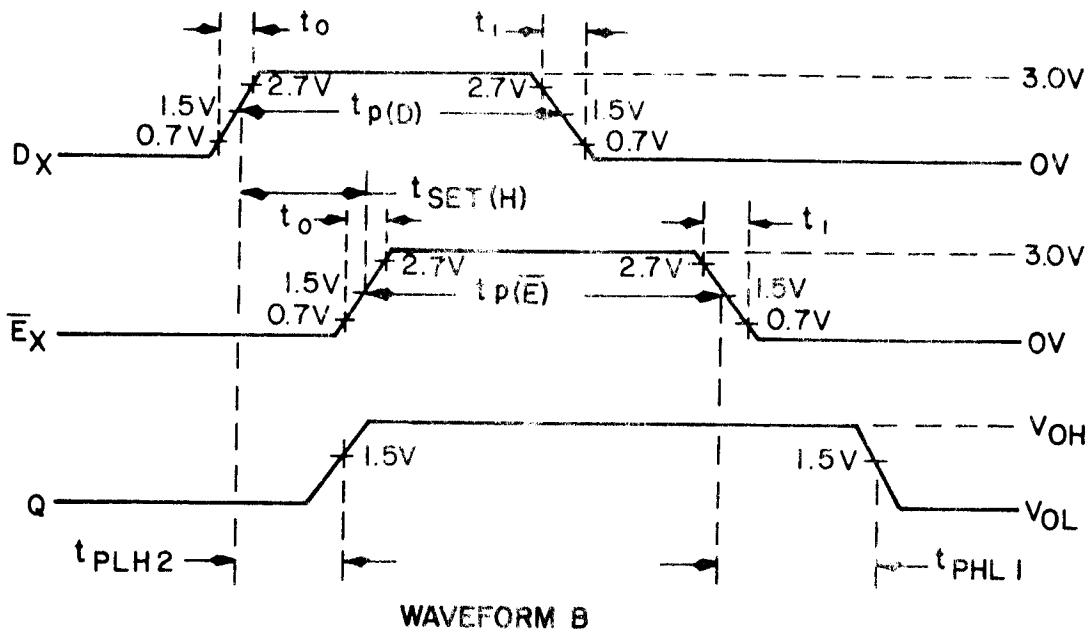
FIGURE 7. Switching time test circuit and waveforms for device type 03 - Continued.



NOTES:

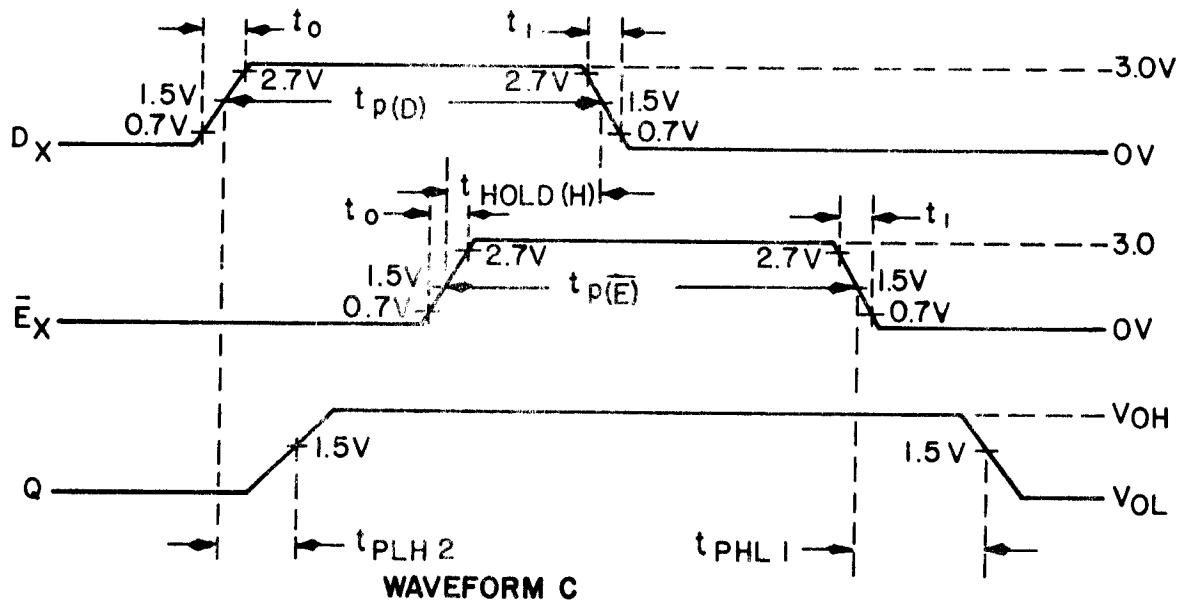
1. The data inputs have the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_{p(D)} = 32\text{ ns}$, and PRR = 1 MHz.
2. The enable input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_{p(E)} = 20\text{ ns}$, $t_{set(L)} = 25\text{ ns}$, $t_{HOLD(L)} = 7\text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.
3. Each latch is tested separately.
4. $C_L = 50\text{ pF}$, which includes probe and jig capacitance.
5. $R_L = 390\ \Omega \pm 5\%$.
6. All diodes are 1N3064 or equivalent.

FIGURE 8. Switching time test circuit and waveforms for device type 04.



NOTES:

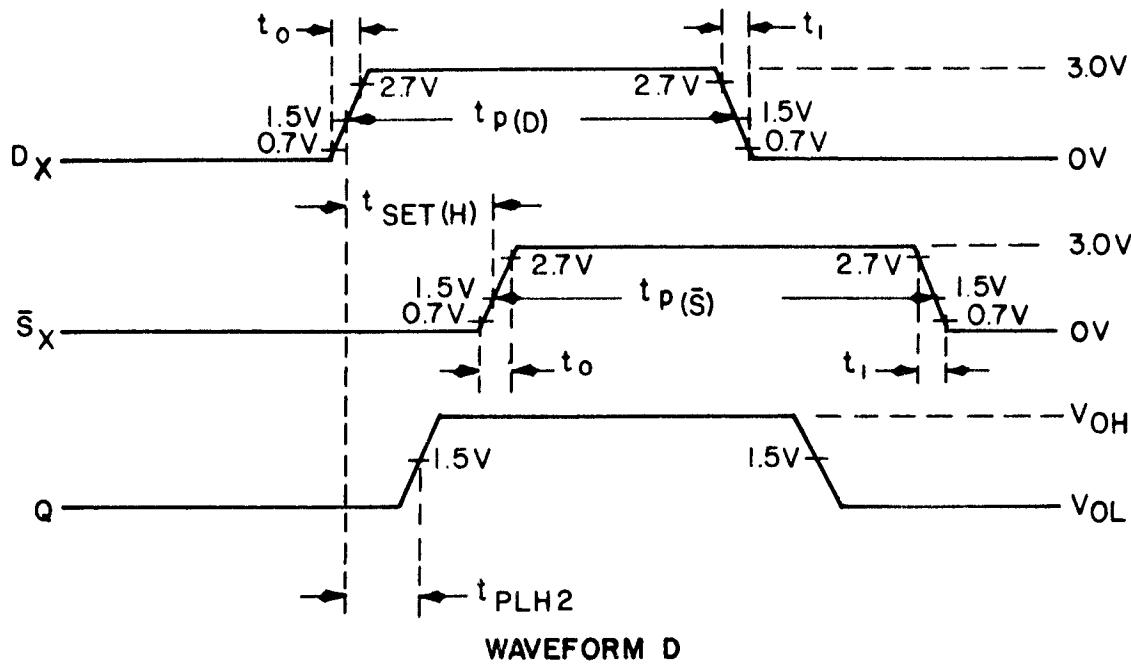
1. The data inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(D) = 20 \text{ ns}$ and PRR = 1 MHz.
2. The enable input has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(\bar{E}) = 20 \text{ ns}$, $t_{SET(H)} = 5 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.



NOTES:

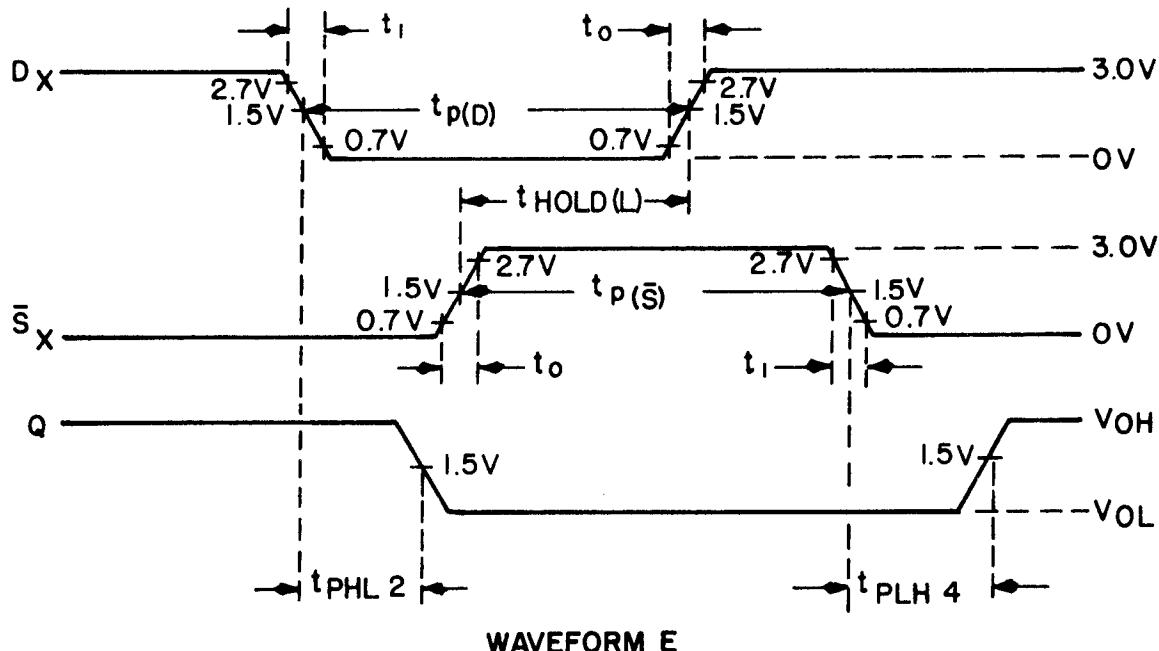
1. The data inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(D) = 20 \text{ ns}$ and PRR = 1 MHz.
2. The enable input has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_p(\bar{E}) = 20 \text{ ns}$, $t_{HOLD(H)} = 0 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.

FIGURE 8. Switching time test circuit and waveforms for device type 04 - Continued.



NOTES:

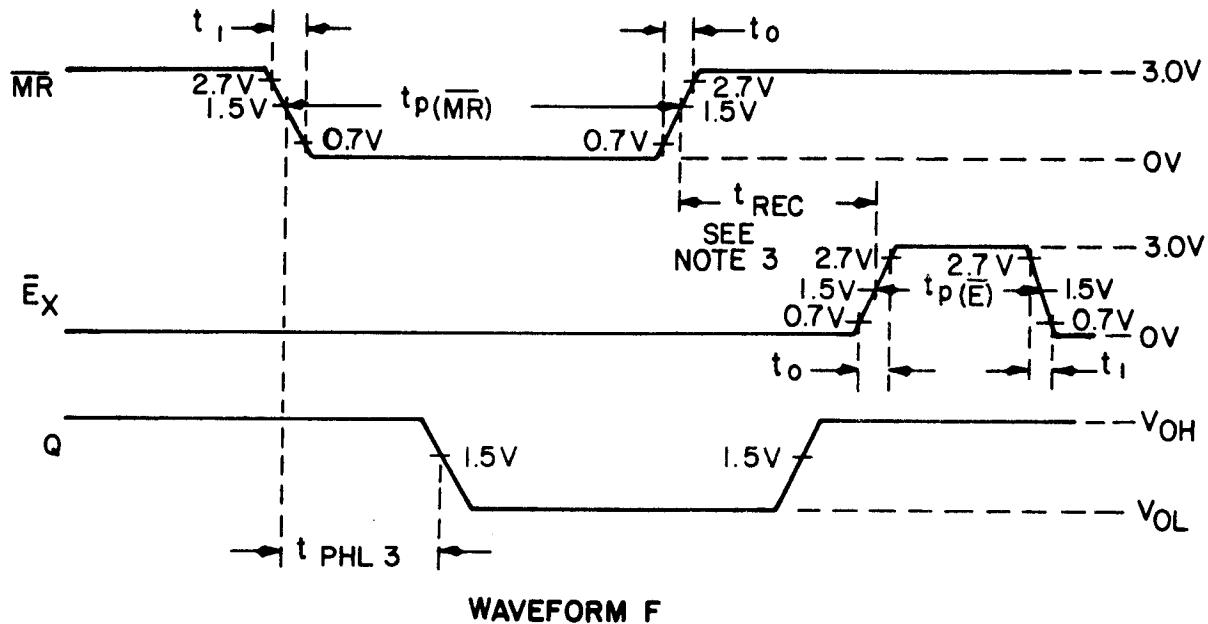
1. The data inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{p(D)} = 20 \text{ ns}$, and PRR = 1 MHz.
2. The set inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{p(\bar{S})} = 20 \text{ ns}$, $t_{SET(H)} = 8 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.



NOTES:

1. The data inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{p(D)} = 20 \text{ ns}$, and PRR = 1 MHz.
2. The set inputs have the following characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 \leq 10 \text{ ns}$, $t_{p(\bar{S})} = 20 \text{ ns}$, $t_{HOLD(L)} = 8 \text{ ns}$, PRR = 1 MHz and $Z_{out} \approx 50 \Omega$.

FIGURE 8. Switching time test circuit and waveform for device type 04 - Continued.



NOTES:

1. The master reset input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_p(\overline{MR}) = 18\text{ ns}$, and PRR 1 MHz.
2. The enable input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_p(\overline{E}) = 20\text{ ns}$, $t_{REC} = 0\text{ ns}$, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
3. Recovery time is the minimum time that enable must remain low after the master reset transition from low to high in order for the latch to recognize and store high data.

FIGURE 8. Switching time test circuit and waveforms for device type 04 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open)

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, or L \leq 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Max	Unit	Test limits
1			Test No.	1 \bar{Q}	1D	2D	3-4	V _{cc}	3D	4D	4 \bar{Q}	4Q	3Q	3 \bar{Q}	GND	Clock 1-2	2Q	1Q					
T _A = 25°C	V _{IC}			44	45	46	47	48	49	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	GND	-12 mA			1D	-1.5	V	
2																				CL 1-2			
3	T _A = 25°C	Truth table test		3014	50	51	52	L	53	54	55	56	57	H	B	5.0 v	B	B	GND	B			See note 2
																				A			
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TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits
			Test No.	1Q	1D	2D	3-4	V _{cc}	3D	4D	4Q	3Q	3Q	3Q	GND	IN	IN	OUT	OUT	Meas. terminal
$T_A = 25^\circ C$	t _{PHL3}	3003 (Fig 6)	90		IN			5.0 v											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q	
	t _{PHL4}		91						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH1}		92						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH2}		93						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
$T_A = 125^\circ C$	t _{PLH3}	3003 (Fig 6)	94	OUT	IN															CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		95						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH1}		96						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH2}		97						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 5)	98		IN-W	IN-W	A													CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		99		OUT	IN-X	A													CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		100						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		101						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 6)	102	OUT	IN-X	IN-X	A													CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		103						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		104						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		105						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 5)	106		IN															CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		107						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		108						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		109						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 6)	110	OUT	IN															CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		111						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		112						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		113						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 5)	114		IN-X	IN-X	A													CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		115						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		116						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		117						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL1}	3003 (Fig 5)	118	OUT	IN-W	IN-W	A													CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PHL2}		119						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH3}		120						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q
	t _{PLH4}		121						IN											CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions for pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F		Test No.	Terminal conditions												Test limits			
			1	2		3	4	Clock	5	6	7	8	9	10	11	12	13	14	15	16	
10	tPHL3	3003 (Fig. 6)	122	IN	1Q	1D	2D	3-4	V _{cc}	3D	4D	4Q	3Q	3Q	GND	1-2	2Q	1Q	25	ns	
T _A			123						5.0 v						GND	IN		OUT	CL (1-2) -1Q	2	
			124						IN							IN		OUT	CL (1-2) -2Q		
			125						IN										CL (3-4) -3Q		
			126	OUT	IN														CL (3-4) -4Q		
	tPHI4		127						IN										CL (1-2) -1Q		
			128						IN										CL (1-2) -2Q		
			129						IN										CL (3-4) -3Q		
																			CL (3-4) -4Q		
11																					

11 Same tests, terminal conditions and limits as subgroup 10, except T_A = -55° C.

NOTES:

A = Clock pulse A, see figure 5.
W and X = Various D-input pulses, see figure 5.

1/ Only a summary of attributes data is required.
2/ Output voltages shall be either:

- (a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or
- (b) H ≥ 1.5 volts and L ≤ 1.5 volts when using a high speed checker single comparator.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be $H \geq 2.0\text{ V}$, or $L \leq 0.8\text{ V}$, or open)

Subgroup	Symbol	MIL-STD-383 method	Case A,B,C,D	Test No.	Meas. terminal												Test limits		
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	Unit
$T_A = 25^\circ C$	V_{OH}	3006	1	2.0 v	2.0 v	4.5 v	2.0 v	vdc											
	V_{OL}	3007	4	0.8 v	0.8 v	0.8 v	2.0 v	2.0 v											
	I_{IL1}	3009	9	0.4 v	0.4 v	0.4 v	5.5 v	5.5 v											
	I_{IL2}	3010	10	0.4 v	0.4 v	0.4 v	4.5 v	4.5 v											
	I_{IH1}	15	2.4 v	2.4 v	2.4 v	2.4 v	GND	GND	2.4 v	2.4 v									
	I_{IH2}	19	5.5 v	5.5 v	5.5 v	GND	GND	GND	5.5 v	5.5 v									
	I_{IH3}	23	GND	GND	GND	GND	GND	GND	2.4 v	GND	GND								
	I_{IH4}	25	GND	GND	GND	GND	GND	GND	4.5 v	GND	GND								
	I_{OS}	3011	27	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v	4.5 v
	I_{CC}	3005	31	GND	GND	GND	GND	GND	4.5 v	GND	GND	4.5 v							
3	V_{IC}	32	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-1.5 Vdc
		33																	
		34																	
2		35																	
		36																	
3		37																	

2 Same tests, terminal conditions and limits as for subgroup 1, except $T_A = 125^\circ C$ and V_{IC} tests are omitted.

3 Same tests, terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ C$ and V_{IC} tests are omitted.

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. - Continued
Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open).

Subgroup		MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits
T _A	Symbol	(See fig 5)	Test No.	10	20	30	40	NC	40	30	NC	GND	Clock 1-2	2Q	1Q	Meas. terminal	Min Max Unit	
7 1/ 25°C	VLT-H1		38	IN-W	IN-W	5.0 V									OUT	1D -1Q 2D -2Q 3D -3Q	2.4 2.4 2.4 2.4 2.4	
	VLT-H1		39												OUT	1D -1Q 2D -2Q 3D -3Q	2.4 2.4 2.4 2.4 2.4	
	VLT-H1		40												OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-H1		41												OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-L1		42	IN-X											OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-L1		43		IN-X										OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-L1		44												OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-L1		45												OUT	1D -1Q 2D -2Q 3D -3Q	0.4 0.4 0.4 0.4 0.4	
	VLT-H3	(See fig 6)	46	IN											OUT	CL(1-2) -1Q	2.4	
	VLT-H3		47		IN										OUT	CL(1-2) -1Q	2.4	
	VLT-H3		48			IN									OUT	CL(1-2) -1Q	2.4	
	VLT-H3		49				IN								OUT	CL(1-2) -1Q	2.4	
	VLT-L3		50					IN							OUT	CL(1-2) -1Q	0.4	
	VLT-L3		51						IN						OUT	CL(1-2) -1Q	0.4	
	VLT-L3		52							IN					OUT	CL(1-2) -1Q	0.4	
	VLT-L3		53								IN				OUT	CL(1-2) -1Q	0.4	

81

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, or L \leq 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D		1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits			
			Test No.	1D	2D	Clock 3-4	V _{cc}	3D	4D	NC	4Q	3Q	NC	GND	A	OUT	OUT	Clock 1-2	2Q	1Q	Meas. terminal	Min. Max
9 $T_A = 25^\circ C$	t _{PLH1}	3003 (Fig 5-A)	54	IN-W	A		5.0 v											1D-1Q 2D-2Q 3D-3Q 4D-4Q	2	34	ns	
	t _{PHL1}	3003 (Fig 5-B)	55	IN-X	A			IN-W	A									1D-1Q 2D-2Q 3D-3Q 4D-4Q	29			
	t _{PLH3}	3003 (Fig 6)	57																			
	t _{PHL3}		58																			
	t _{PLH1}	3003 (Fig 5-A)	59	IN-X	A				IN-X	A												
	t _{PHL1}	3003 (Fig 5-B)	60																			
	t _{PLH3}	3003 (Fig 6)	61	IN																		
	t _{PHL3}		62																			
	t _{PLH1}	3003 (Fig 5-A)	63	IN																		
	t _{PHL1}	3003 (Fig 5-B)	64																			
10 $T_A = 125^\circ C$	t _{PLH3}	3003 (Fig 6)	65	IN																		
	t _{PLH1}	3003 (Fig 5-A)	66	IN																		
	t _{PHL1}	3003 (Fig 5-B)	67																			
	t _{PLH3}		68	IN																		
	t _{PHL3}		69																			
	t _{PLH1}	3003 (Fig 5-A)	70	IN-W	A			IN-W	A													
	t _{PHL1}	3003 (Fig 5-B)	71																			
	t _{PLH3}	3003 (Fig 6)	72																			
	t _{PHL3}		73																			
	t _{PLH1}	3003 (Fig 5-A)	74	IN-X	A				IN-X	A												
11	t _{PHL1}	3003 (Fig 5-B)	75																			
	t _{PLH3}	3003 (Fig 6)	76	IN																		
	t _{PHL3}		77																			
	t _{PLH1}	3003 (Fig 5-A)	78	IN																		
	t _{PHL1}	3003 (Fig 5-B)	79																			
	t _{PLH3}	3003 (Fig 6)	80	IN																		
	t _{PHL3}		81																			
	t _{PLH1}	3003 (Fig 5-A)	82	IN																		
	t _{PHL1}	3003 (Fig 5-B)	83																			
	t _{PLH3}	3003 (Fig 6)	84	IN																		
11	t _{PHL3}		85																			

NOTES:
11 Same tests, terminal conditions and limits as subgroup 10, except $T_A = -55^\circ C$. $A =$ Clock pulse A, see figure 5. W and $X =$ Various D-input pulses, see figure 5.1/ Latch voltage, V_{LT} , shall be measured no sooner than $10 \mu s$ after switching transition occurs.

TABLE III. Group A inspection for device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J, K, L, Z Test No.	Terminal conditions																Meas. terminal	Test limits							
				1	2	.3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
1 $T_A = 25^\circ C$	I _{IL2}	3009	39	0.4 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	5.5 V	0.4 V	
	I _{H1}	3010	45 CKT A 46 CKT B, C 47 CKT A 47 CKT B, C 48 CKT A 48 CKT B, C 49 CKT A 49 CKT B, C 50 CKT A 50 CKT B, C 51 CKT A 51 CKT B, C 52 CKT A 52 CKT B, C	45 CKT A 46 CKT A 46 CKT B, C 47 CKT A 47 CKT B, C 48 CKT A 48 CKT B, C 49 CKT A 49 CKT B, C 50 CKT A 50 CKT B, C 51 CKT A 51 CKT B, C 52 CKT A 52 CKT B, C	5.5 V	2.4 V	2.4 V	5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V											
	I _{H2}	3010	53 CKT A 53 CKT B, C 54 CKT A 54 CKT B, C 55 CKT A 55 CKT B, C 56 CKT A 56 CKT B, C 57 CKT A 57 CKT B, C 58 CKT A 58 CKT B, C 59 CKT A 59 CKT B, C 60 CKT A 60 CKT B, C	53 CKT A 53 CKT B, C 54 CKT A 54 CKT B, C 55 CKT A 55 CKT B, C 56 CKT A 56 CKT B, C 57 CKT A 57 CKT B, C 58 CKT A 58 CKT B, C 59 CKT A 59 CKT B, C 60 CKT A 60 CKT B, C	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V																
	I _{H3}	3010	61	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	2.4 V	GND	

TABLE III. Group A inspection for device type 03 - Continued.

Subgroup	Symbol	MIL-STD-883 Case J,K,L,Z Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	Test limits			
																										5.5 V	1MR	100 μ A	
1 $T_A = 25^\circ C$	I _{H4}	3010	67	5.5 V	5.5 V	2ND	5.5 V	5.5 V	GND	4.5 V	5.5 V	1E0	100 μ A																
	I _{OS}	3011	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94
	I _{OC}	3005	81	4.5 V	4.5 V	4.5 V																							

2 Same tests, terminal conditions and limits as to subgroup 1, except $T_A = 125^\circ C$ and V_{IC} tests are omitted.3 Same tests, terminal conditions and limits as to subgroup 1, except $T_A = -55^\circ C$ and V_{IC} tests are omitted.1/ Circuit B and C limits for I_{OS} shall be -20, minimum and -57, maximum.

TABLE III. Group A inspection for device type 03 - Continued.
 Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open)

Subgroup	Symbol	Case J1K, L, Z	Test No.	MLL-STD-883 method	Test limits		Meas. terminal	Max	Unit
					Min	Max			
9 TA = 25°C	tPLH1 (Fig. 7-B)	1 82	2 83	3 84	4 85	5 86	6 87	7 88	8 89
		1D0 5.0 v	1E0 GND	1D1 IN	1Q0 OUT	1D2 IN	1Q1 OUT	1D3 IN	1Q3 OUT
		2D0 2M&R 5.0 v	2E0 GND	2D1 IN	2Q0 OUT	2D2 IN	2Q1 OUT	2D3 IN	2Q3 OUT
		2D4 5.0 v	2E1 GND	2D5 IN	2Q4 OUT	2D6 IN	2Q5 OUT	2D7 IN	2Q6 OUT
		2D8 1E0-1Q0 2E0-1Q1 2E1-2Q2 2E1-1Q3 2E1-1Q4 2E2-1Q0 2E2-2Q1 2E3-2Q3 2E3-2Q4 2E3-2Q5 2D1-1Q1 2D2-1Q2 2D3-1Q3 2D4-2Q0 2D5-1Q0 2D6-1Q1 2D7-1Q2 2D8-1Q3 2D9-1Q4 2D10-1Q5 2D11-1Q6 2D12-1Q7 2D13-1Q8 2D14-1Q9 2D15-1Q10 2D16-1Q11 2D17-1Q12 2D18-1Q13 2D19-1Q14	3 33 ns						
	tPHL1 (Fig. 7-A)	90 98	91 100	92 101	93 102	94 103	95 104	96 105	97 106
		107 108	109 109	110 111	112 112	113 113			
		3003 (Fig. 7)	114 115	116 117	118 119	120 121	122 123	124 125	126 127
		127 129							

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open

Subgroup		Symbol	MLT-STD-883 method	Case J,K, L,2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas.	Test limits
		Test No.	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	IMR	Max	Unit	
9	T _A =25°C	tPHL2	3003 (Fig 7)	130	5.0 v	IN	GND	IN	OUT	5.0 v	ID ₁ -IQ ₁ ID ₂ -IQ ₂ ID ₃ -IQ ₃ ID ₄ -IQ ₄ ID ₅ -IQ ₅ ID ₆ -IQ ₆ ID ₇ -IQ ₇ ID ₈ -IQ ₈ ID ₉ -IQ ₉ ID ₁₀ -IQ ₁₀ ID ₁₁ -IQ ₁₁ ID ₁₂ -IQ ₁₂ ID ₁₃ -IQ ₁₃ ID ₁₄ -IQ ₁₄ ID ₁₅ -IQ ₁₅ ID ₁₆ -IQ ₁₆ ID ₁₇ -IQ ₁₇ ID ₁₈ -IQ ₁₈ ID ₁₉ -IQ ₁₉ ID ₂₀ -IQ ₂₀ ID ₂₁ -IQ ₂₁ ID ₂₂ -IQ ₂₂ ID ₂₃ -IQ ₂₃	ns																		
10	T _A =125°C	tPLH1	3003 (Fig 7-B)	162	5.0 v	IN	GND	IN	OUT	5.0 v	IE ₁ -IQ ₁ IE ₂ -IQ ₂ IE ₃ -IQ ₃ IE ₄ -IQ ₄ IE ₅ -IQ ₅ IE ₆ -IQ ₆ IE ₇ -IQ ₇ IE ₈ -IQ ₈ IE ₉ -IQ ₉ IE ₁₀ -IQ ₁₀ IE ₁₁ -IQ ₁₁ IE ₁₂ -IQ ₁₂ IE ₁₃ -IQ ₁₃ IE ₁₄ -IQ ₁₄ IE ₁₅ -IQ ₁₅ IE ₁₆ -IQ ₁₆ IE ₁₇ -IQ ₁₇ IE ₁₈ -IQ ₁₈ IE ₁₉ -IQ ₁₉ IE ₂₀ -IQ ₂₀ IE ₂₁ -IQ ₂₁ IE ₂₂ -IQ ₂₂ IE ₂₃ -IQ ₂₃	60																		

TABLE I-111. Group A inspection for device type 03 - Cont'd.
 Terminal conditions (pins not gritted may be H \geq 2.5 V, or L \leq 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case T,K,L,Z	Test No.	1		2		3		4		5		6		7		8		9		10		11		12		13		14		15		16		17		18		19		20		21		22		23		24		V_{cc}	2Q₃	2D₃	2Q₂	2D₂	2Q₁	2D₁	2E₁	2D₀	2Q₀	2D₀	2E₀	GND	2M_R	IN	1Q₃	1D₃	1Q₂	1D₂	1Q₁	1D₁	1E₀	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D₀	1E₁	IN	GND	5.0 v	GND	5.0 v	GND	10	9	8	7	6	5	4	3	2	1	0	1Q₀	1D_{0</sub}

TABLE III. Group A inspection for device type Q3 - Continued.
Terminal conditions (pins not designated may be R ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J.K. L.2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Test limits				
																											Meas.	terminal	Max	Unit		
10	t _{PHL3}	3003 (FIG. 7-C)	236	IN	GND	5.0 v	OUT	5.0 v	IMR-IQ0	3	37	ns																				
	T _A =125°C		227																									IMR-IQ1				
			228																									IMR-IQ2				
			229																									IMR-IQ3				
			230																									IMR-IQ4				
			231																									IMR-IQ5				
			232																									IMR-IQ6				
			233																									IMR-IQ7				
			234																									IMR-IQ8				
			235																									2MR-2C1				
			236																									2MR-2C2				
			237																									2MR-2C3				
			238																									2MR-2C4				
			239																									2MR-2C5				
			240																									2MR-2C6				
			241																									2MR-2C7				
11																																

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open)

Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open)

See note at end of device type 04.

TABLE III. Group A inspection for device type 04 - (Continued)
Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits				
			Test No.	Test No.	\bar{E}	\bar{S}_0	D ₀	D ₁	\bar{S}_2	D ₂	D ₃	GND	\overline{MR}	Q ₃	\bar{S}_3	Q ₂	Q ₁	\bar{S}_1	Q ₀	V _{cc}	Max	Unit				
$T_A = 25^\circ C$	IOS	3011	49	GND	GND	4.5 v	4.5 v	GND	4.5 v	GND	4.5 v	4.5 v	5.5 v	GND	GND	GND	GND	GND	GND	5.5 v	Q ₀ Q ₁ Q ₂ Q ₃	-20 -100	mA	V _{cc}	55 mA	
	ICC		50	51	52	52	53	53	54	54	55	55	56	GND	GND	GND	GND	GND	GND	5.5 v	Q ₀ Q ₁ Q ₂ Q ₃	-20 -100	mA			
2		Same tests, terminal conditions and limits as for subgroup 1, except $T_A = 125^\circ C$ and V_{IC} tests are omitted.																				V _{cc}	55 mA			
3		Same tests, terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ C$ and V_{IC} tests are omitted.																								
$T_A = 25^\circ C$		tpHL1 (Fig 8-A)	3003	54	IN	GND	IN	IN	GND	IN	IN	IN	IN	GND	5.0 v	GND	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	29
			50	57	GND	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpHL1 (Fig 8-B)	3003	58	IN	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	29
			59	60	61	61	61	61	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpHL1 (Fig 8-C)	3003	62	IN	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	29
			63	64	64	65	65	65	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpLH2 (Fig 8-B)	3003	66	IN	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	21
			67	68	69	69	69	69	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpLH2 (Fig 8-C)	3003	70	IN	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	21
			71	72	73	73	73	73	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpLH2 (Fig 8-D)	3003	74	IN	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	30
			75	76	77	77	77	77	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpHL2 (Fig 8-E)	3003	78	GND	IN	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	30
			79	80	81	81	81	81	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		
$T_A = 25^\circ C$		tpHL2 (Fig 8-A)	3003	82	IN	GND	IN	IN	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	30
			83	84	85	85	85	85	GND	IN	IN	IN	IN	OUT	GND	OUT	OUT	OUT	OUT	OUT	5.0 v	\bar{E} -Q ₁ \bar{E} -Q ₂ \bar{E} -Q ₃	9	30 ns		

See note at end of device type 04.

TABLE III. Terminal conditions Group A inspection for device type 04 - Continued.
 (pins not designated may be H > 2.0 V, or L < 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	Test Limits																
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
$T_A = 25^\circ C$	tPHL3	3003 (Fig 8-F)	86 87 88 89	IN	GND	5.0 v	5.0 v	GND	5.0 v	MR-Q0	9	23 ns								
	tPHL4	3003 (Fig 8-E)	90 91 92 93	GND	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	S1-Q1	S2-Q2	S3-Q3
$T_A = 125^\circ C$	tPHL1	3003 (Fig 8-A)	94 95 96 97	IN	GND	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	E-Q0	E-Q1	E-Q2
	tPHL1	3003 (Fig 8-B)	98 99 100 101	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	E-Q0	E-Q1	E-Q3
	tPHL1	3003 (Fig 8-C)	102 103 104 105	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	E-Q0	E1-Q1	E2-Q2
	tPHL2	3003 (Fig 8-B)	106 107 108 109	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	E-Q0	E-Q1	E-Q3
	tPHL2	3003 (Fig 8-C)	110 111 112 113	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	D0-Q0	D1-Q1	D2-Q2
	tPHL2	3003 (Fig 8-D)	114 115 116 117	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	D0-Q0	D1-Q1	D2-Q2
	tPHL2	3003 (Fig 8-E)	118 119 120 121	GND	IN	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	D0-Q0	D1-Q1	D2-Q2
	tPHL2	3003 (Fig 8-A)	122 123 124 125	IN	GND	IN	IN	GND	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	D0-Q0	D1-Q1	D3-Q3

See note at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be $H \geq 2.0V$, or $L \leq 0.8 V$, or open)

Subgroup	Symbol	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits	
																			Min	Max
10 $T_A = 125^\circ C$	t_{PHI3} (Fig 8-F)	3003	126 127 128 129	IN GND 5.0 v 5.0 v	D0 D1 S2 S1	D2 GND 5.0 v 5.0 v	D3 GND GND GND	\overline{MR} IN IN OUT	Q3 Q2 Q1 Q0	\overline{S}_3 Q2 Q1 \overline{S}_1	9 30 ns	5.0 v 1 1 1	$MR-Q_0$ $MR-Q_1$ $MR-Q_2$ $MR-Q_3$	9 30 ns	Meas. terminal					
	t_{PLH4} (Fig 8-E)	3003	130 131 132 133	GND IN IN IN	IN IN IN IN	IN IN IN IN	IN IN IN IN	IN IN IN IN	OUT OUT OUT OUT	GND GND GND GND	5.0 v 5.0 v 5.0 v 5.0 v	S_0-Q_0 S_1-Q_1 S_2-Q_2 S_3-Q_3	47							

11 Same tests, terminal conditions and limits as subgroup 10, except $T_A = -55^\circ C$.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	5475, 7475 (circuit A)
01	SN5475, SN7475 (circuit B)
02	5477, 7477 (circuit A)
02	SN5477, SN7477 (circuit B)
03	9308 (circuit A)
03	54116, 74116 and SN74116 (circuit B)
03	S54116 (circuit C)
04	9314 (circuit A)
04	AM9314 (circuit B)

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Air Force - 11, 80, 85
NASA - NA
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC, OS, SH
Air Force - 19

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0232)