MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL
TTL, BISTABLE LATCHES, MONOLITHIC SILICON

This amendment forms a part of Military Specification MIL-M-38510/15A, dated 27 July 1979, and is approved for use by all Departments and Agencies of the Department of Defense.

PAGE 2

1.4, Setup time, $t_{(setup)}$, types 01 and 02; add after 02; "data to output".

1.4, Input hold time, $t_{(hold)}$, types 01 and 02, data to clock: Delete "35ns" and substitute "30ns".

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FIGURE 3, delete and substitute new figure as printed on page 2 of this amendment.

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FIGURE 5, delete title and substitute as follows: "Switching test circuit and data to output waveforms for device types 01 and 02."

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FIGURE 6, delete and substitute new figure as printed on page 3 of this amendment.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Air Force - 11, 80, 85
NASA - NA
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC, OS, SH
Air Force - 19

Agent:
DLA - ES

Preparing activity:
Air Force - 17

(Project 5962-0476)

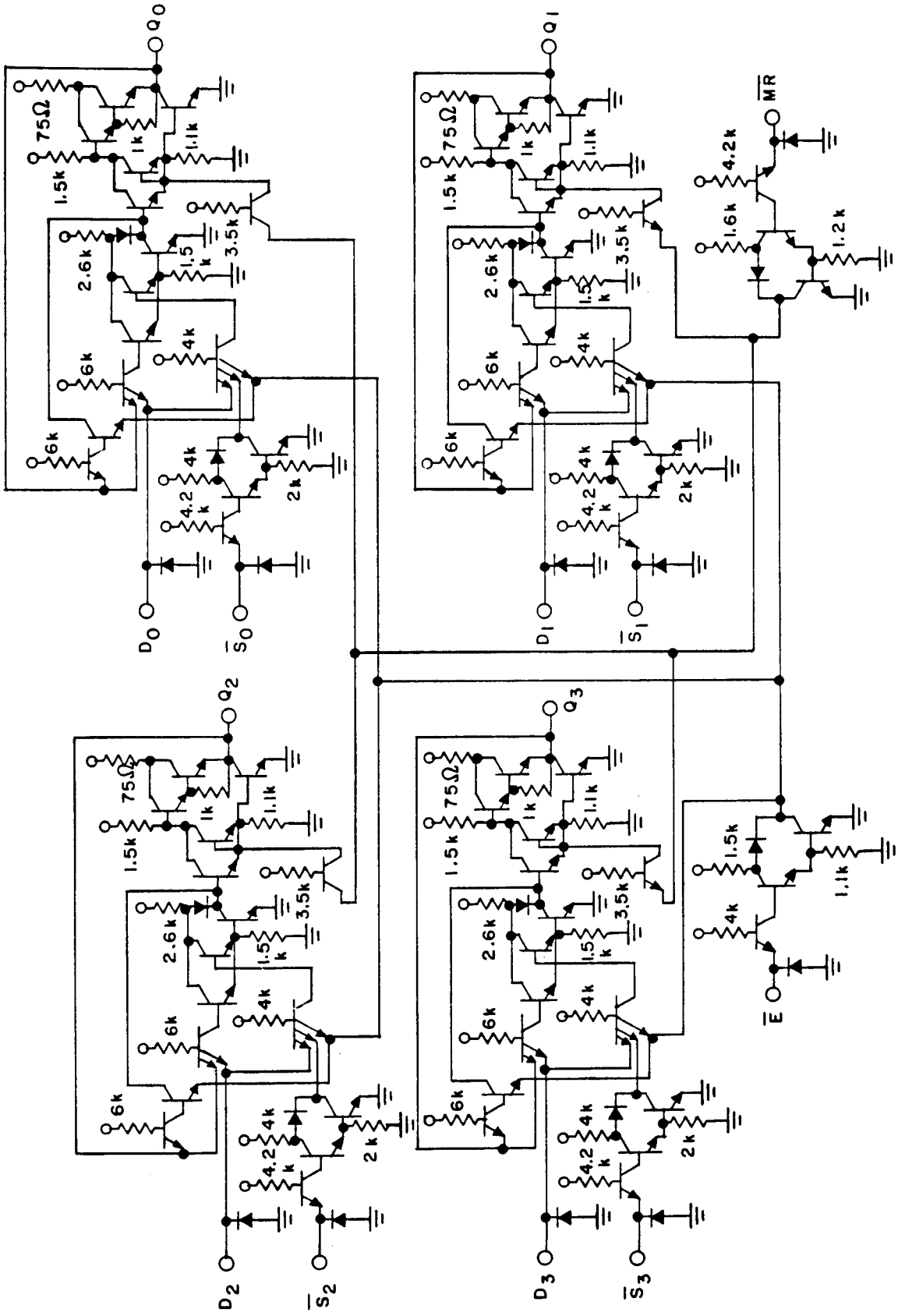
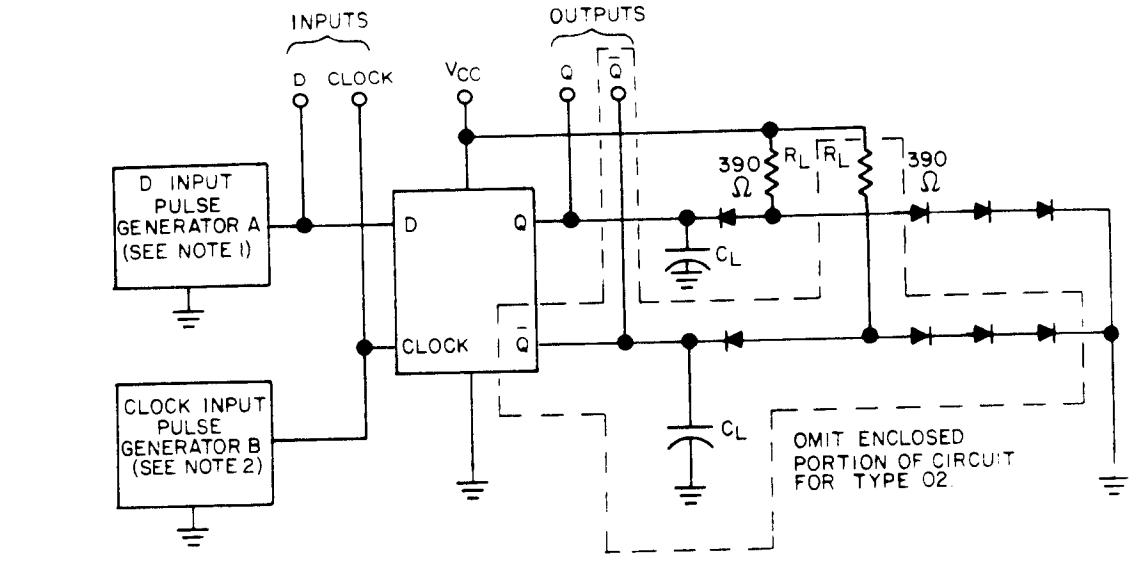
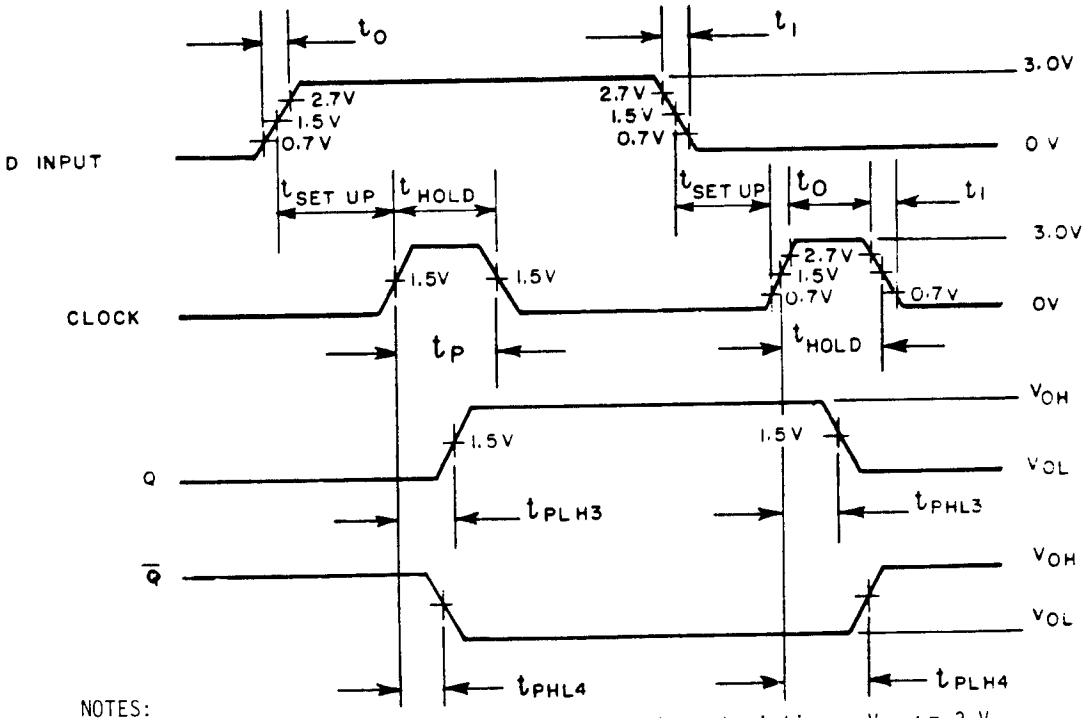


FIGURE 3. Logic diagram and schematic circuits for device type 04 - Continued.



TEST CIRCUIT



NOTES:
1. D input pulse generator has the following characteristics: V_{gen} = 3 V, minimum, $t_0 = t_1 \leq 10$ ns, and PRR = 500 kHz at 50% duty cycle. For subgroups 7 and 8, PRR $\leq$ 25 kHz at 50% duty cycle and PRR (D input) = 1/2 PRR (clock).
2. Clock input pulse generator has the following characteristics: V_{gen} = 3 V, minimum, $t_0 = t_1 \leq 10$ ns, $t_{HOLD} = t_{p\ CLOCK} = 30$ ns, $t_{(SETUP)} = 25$ ns and PRR = 1 MHz. For subgroups 7 and 8, PRR $\leq$ 50 kHz.
3. Each latch is tested separately.
4. C_L = 50 pF, which includes probe and jig capacitance.
5. R_L = 390Ω ±5%.
6. The $\overline{Q}$ waveforms are not applicable to device type 02.
7. All diodes are 1N3064 or equivalent.

FIGURE 6. Switching test circuit and CLK to output waveforms for device types 01 and 02.