

MIL-M-38510/17A(USAF)

1 May 1979

SUPERSEDING

MIL-M-38510/17(USAF)

21 November 1973

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

This specification is approved for use by Rome Air Development Center, Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. Device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	Hex, D-type, positive-edge-triggered, flip-flops, with clear and single outputs.
02	Quad, D-type, positive-edge-triggered, flip-flops, with clear and complementary outputs.

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline, MIL-M-38510, appendix C</u>
E	D-2 (16-lead, 1/4" x 7/8" dual-in-line pack)
F	F-5 (16-lead, 1/4" x 3/8" flat pack)

1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.5 to 7.0 Vdc
Input voltage range	- - - - -	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range	- - - - -	-65° to 150°C
Maximum power dissipation per flip-flop, $P_D$	1/- - - - -	73 mW (device type 01) 65 mW (device type 02)
Lead temperature (soldering, 10 seconds)		300°C
Thermal resistance, junction to case	- - - - -	$\theta_{JC} = \begin{cases} 0.09^\circ\text{C}/\text{mW} & \text{for flat pack} \\ 0.08^\circ\text{C}/\text{mW} & \text{for dual-in-line pack} \end{cases}$
Junction temperature	- - - - -	$T_J = 175^\circ\text{C}$

FSC 5962

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBRD, Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1/ Must withstand the added  $P_D$  due to short circuit test (e.g.,  $I_{OS}$ ).

1.4 Recommended operating conditions.

Supply voltage	- - - - -	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	- - - - -	2.0 Vdc
Maximum low level input voltage	- - - - -	0.8 Vdc
Normalized fanout (each output)	2/ - - - - -	10 maximum
Ambient operating temperature range	- - - - -	-55° to 125°C
Input set up time		
Data input	- - - - -	25 ns
Clear inactive state	- - - - -	30 ns
Input hold time	- - - - -	5 ns

2. APPLICABLE DOCUMENTS.

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer).

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Logic diagram and terminal connections. The logic diagram and terminal connections shall be as specified on figures 1 and 2, respectively.

3.2.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 3.

3.2.3 Schematic circuit. The schematic circuit shall be as specified on figure 4.

3.2.4 Case outlines. Case outlines shall be as specified in 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.

2/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -800 μA	A11	2.4	---	Volts
Low-level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V; I <sub>IN</sub> = 16 mA	A11	---	0.4	Volts
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V; I <sub>IN</sub> = -12 mA; T <sub>A</sub> = 25°C	A11	---	-1.5	Volts
Low-level input current	I <sub>IL1</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 0.4 V 2/	A11	-0.3	-1.6	mA
	I <sub>IL2</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 0.4 V 3/	A11	-0.4	-1.6	mA
	I <sub>IL3</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 0.4 V 4/	A11	-0.3	-0.8	mA
High-level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 2.4 V	A11	---	40	μA
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 5.5 V	A11	---	100	μA
Short-circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 0	A11	-20	-57	mA
Supply current per device	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V; V <sub>IN</sub> = 5.5 V	01	---	65	mA
			02	---	45	mA
Maximum clock frequency	f <sub>MAX</sub>		A11	25	---	MHz
Propagation delay to high logic level (clear to Q)	t <sub>PLH1</sub>	V <sub>CC</sub> = 5 V; CL = 50 pF ±10% RL = 390 Ω ±5%	02	5	36	ns
Propagation delay to low logic level (clear to Q)	t <sub>PHL1</sub>		A11	5	50	ns
Propagation delay to high logic level (clock to Q)	t <sub>PLH2</sub>		A11	5	43	ns
Propagation delay to low logic level (clock to Q)	t <sub>PHL2</sub>		A11	5	43	ns
Propagation delay to high logic level (clock to Q)	t <sub>PLH3</sub>		02	5	43	ns
Propagation delay to low logic level (clock to Q)	t <sub>PHL3</sub>		02	5	43	ns

1/ See table III for complete terminal conditions.

2/ Clock input for device types 01 and 02.

3/ Clear input for device types 01 and 02.

4/ All D inputs for device types 01 and 02.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)		
	Class A devices	Class B devices	Class C devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1	None
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9	1*, 2, 3, 7, 9	1
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9	1, 2, 3, 9
Group C end point electrical parameters (method 5005)	N/A	1, 2, 3	1
Group D end point electrical parameters (method 5005)	1, 2, 3	1, 2, 3	1
Additional electrical subgroups for group C periodic inspections	None	10, 11	None

\*PDA applies to subgroup 1 (see 4.3c.).

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II. (Subgroups 7 and 8 testing requires only a summary of attributes data).

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container:

- a. Country of origin.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 3 (see MIL-M-38510, appendix E).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, through 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
  1. Test condition D or E, using the circuit shown on figure 5, or equivalent.
  2.  $T_A = 125^\circ\text{C}$  minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Percent defective allowable (PDA) - The PDA for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

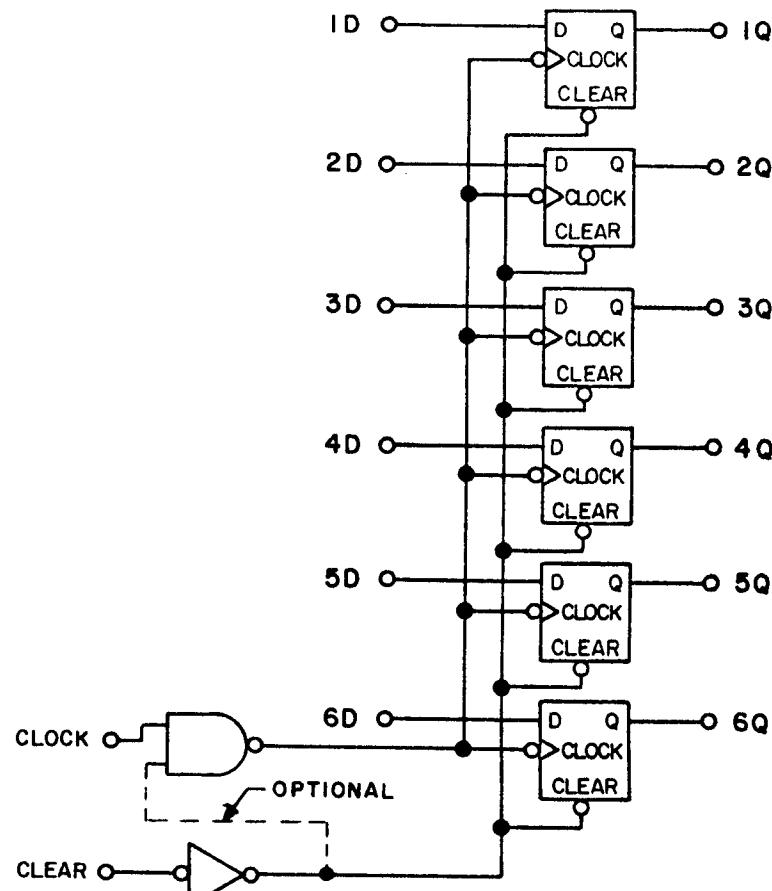


FIGURE 1. Logic diagrams.

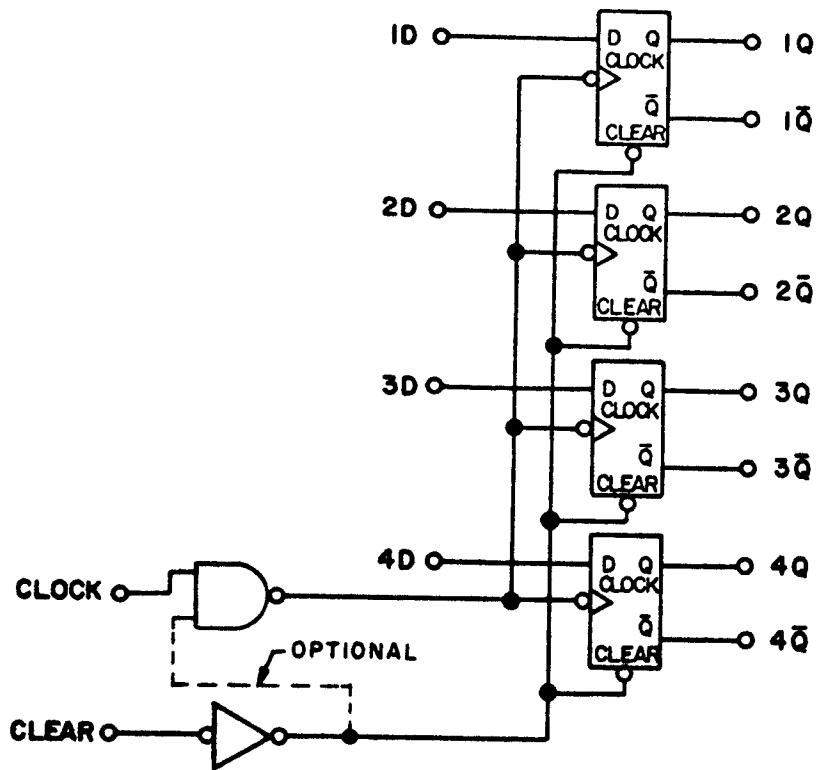
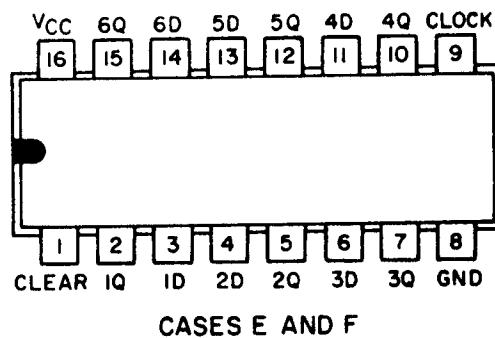


FIGURE 1. Logic diagrams - Continued.

Device type 01



Device type 02

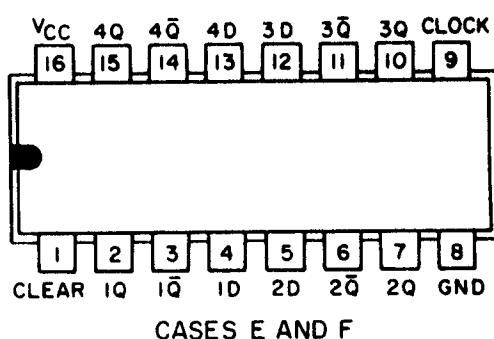


FIGURE 2. Terminal connections.

TRUTH TABLE FOR EACH FLIP-FLOP				
CLEAR	CLOCK	D	Q	$\bar{Q}$ *
L	X**	X	L	H
H	↑	H	H	L
H	↓	L	L	H
H	L	X	$Q_0$	$\bar{Q}_0$

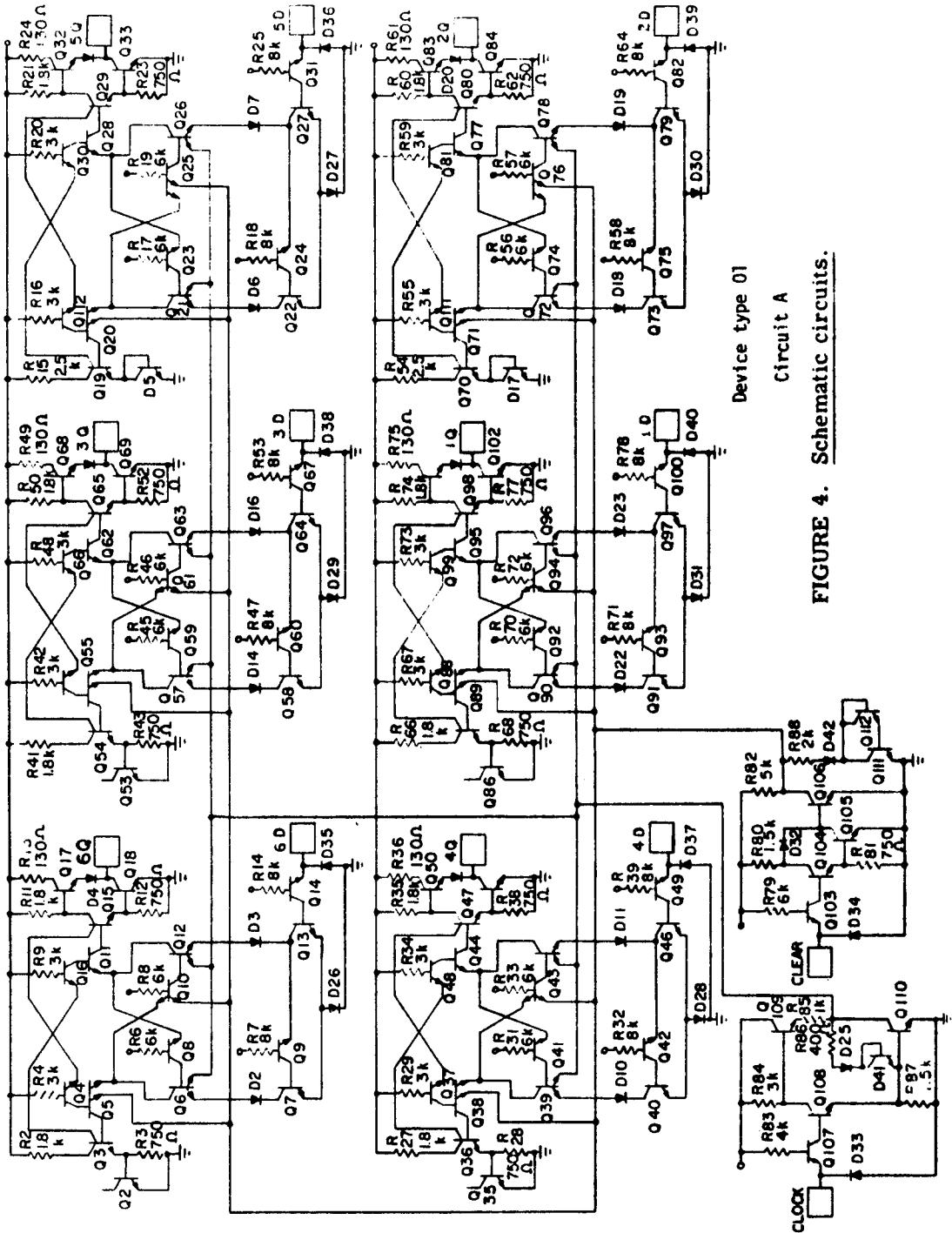
\* DEVICE TYPE 02 ONLY

\*\* INPUT MAY BE HIGH, LOW OR OPEN CIRCUIT

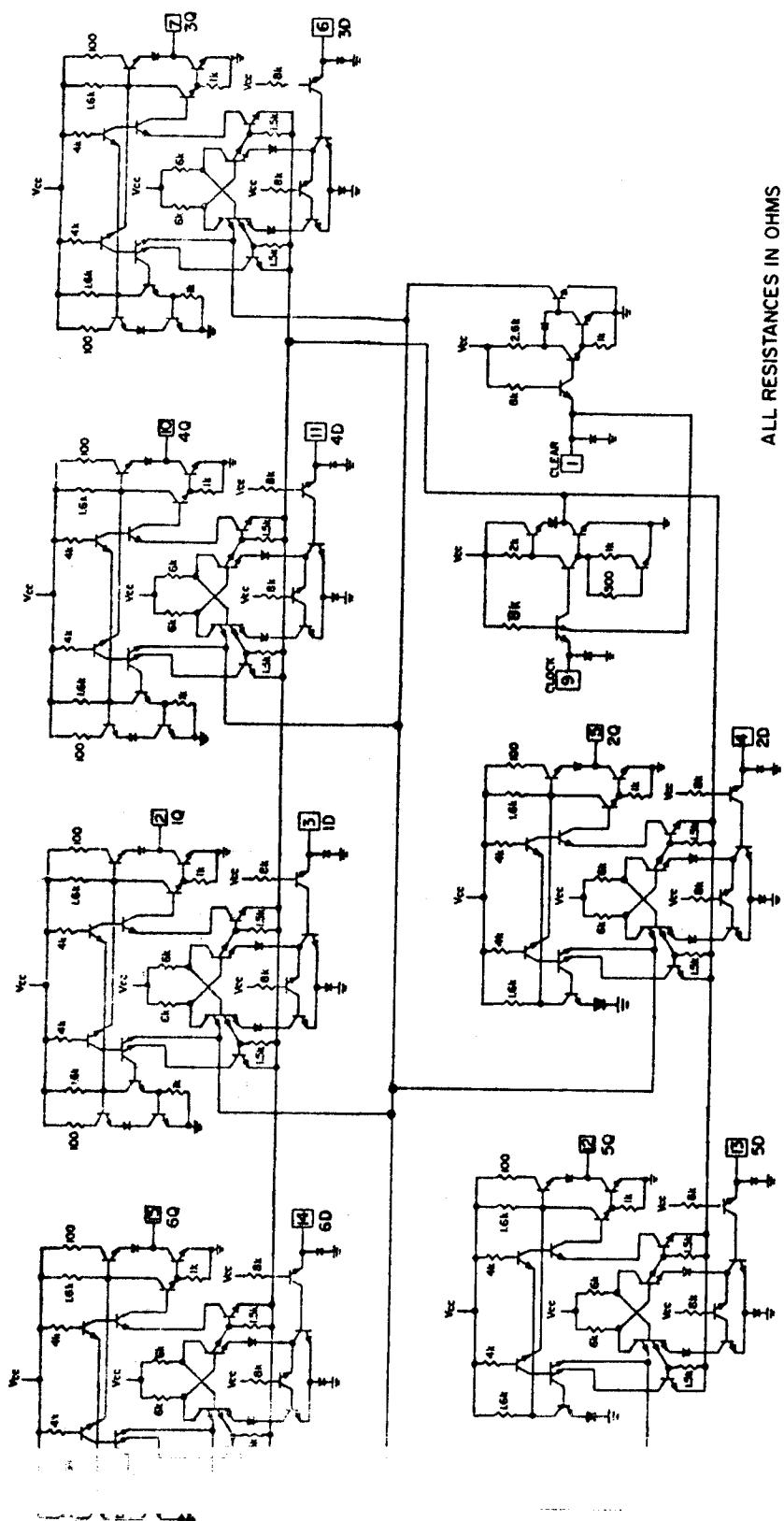
NOTE:

Clear is independent of clock. Information at the D input meeting the set-up time requirements is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either high or low level, the D input signal has no effect at the output.

FIGURE 3. Truth tables.



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Device type 01 (Circuit B)

**FIGURE 4.** Schematic circuits - Continued.

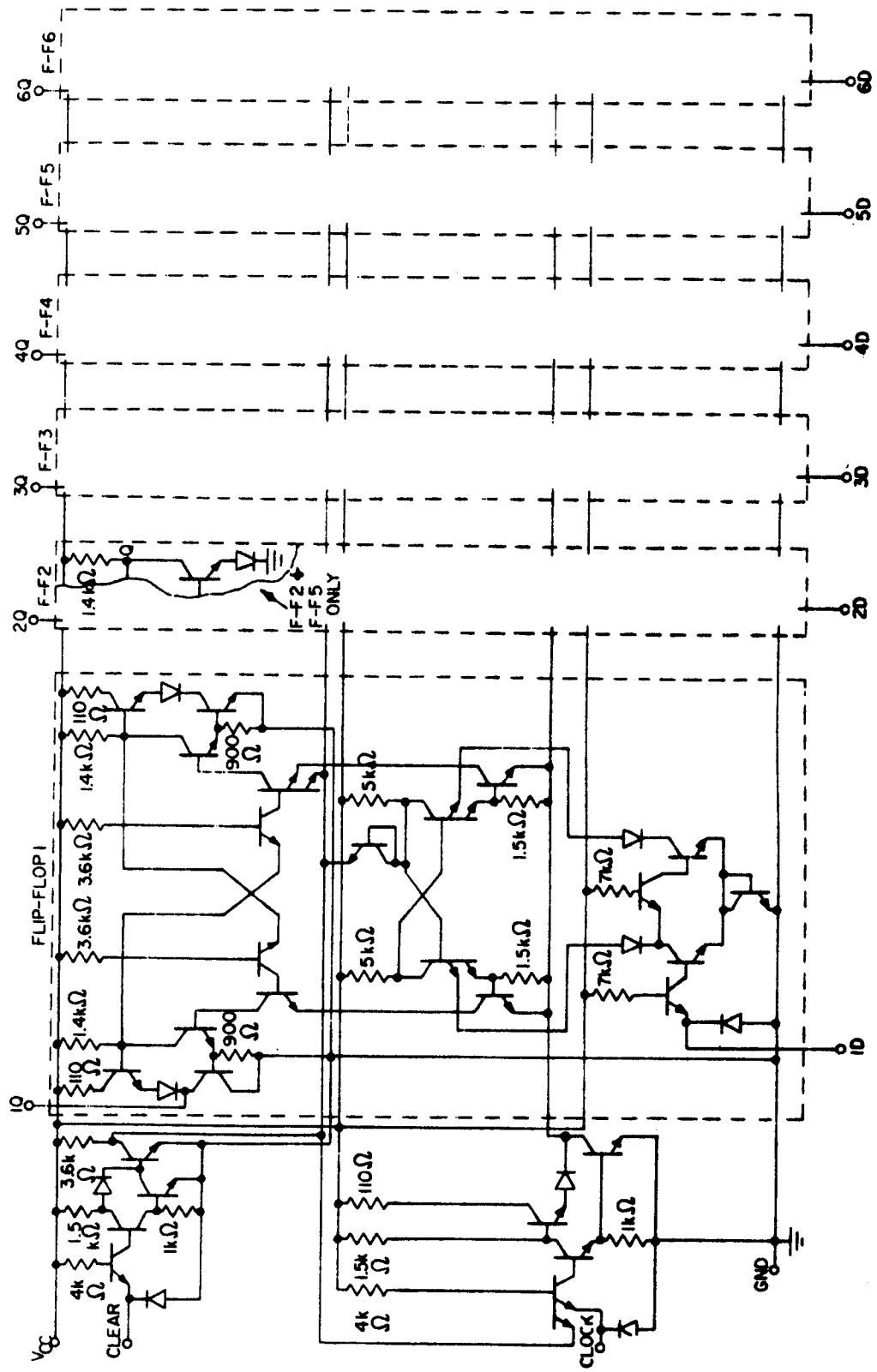
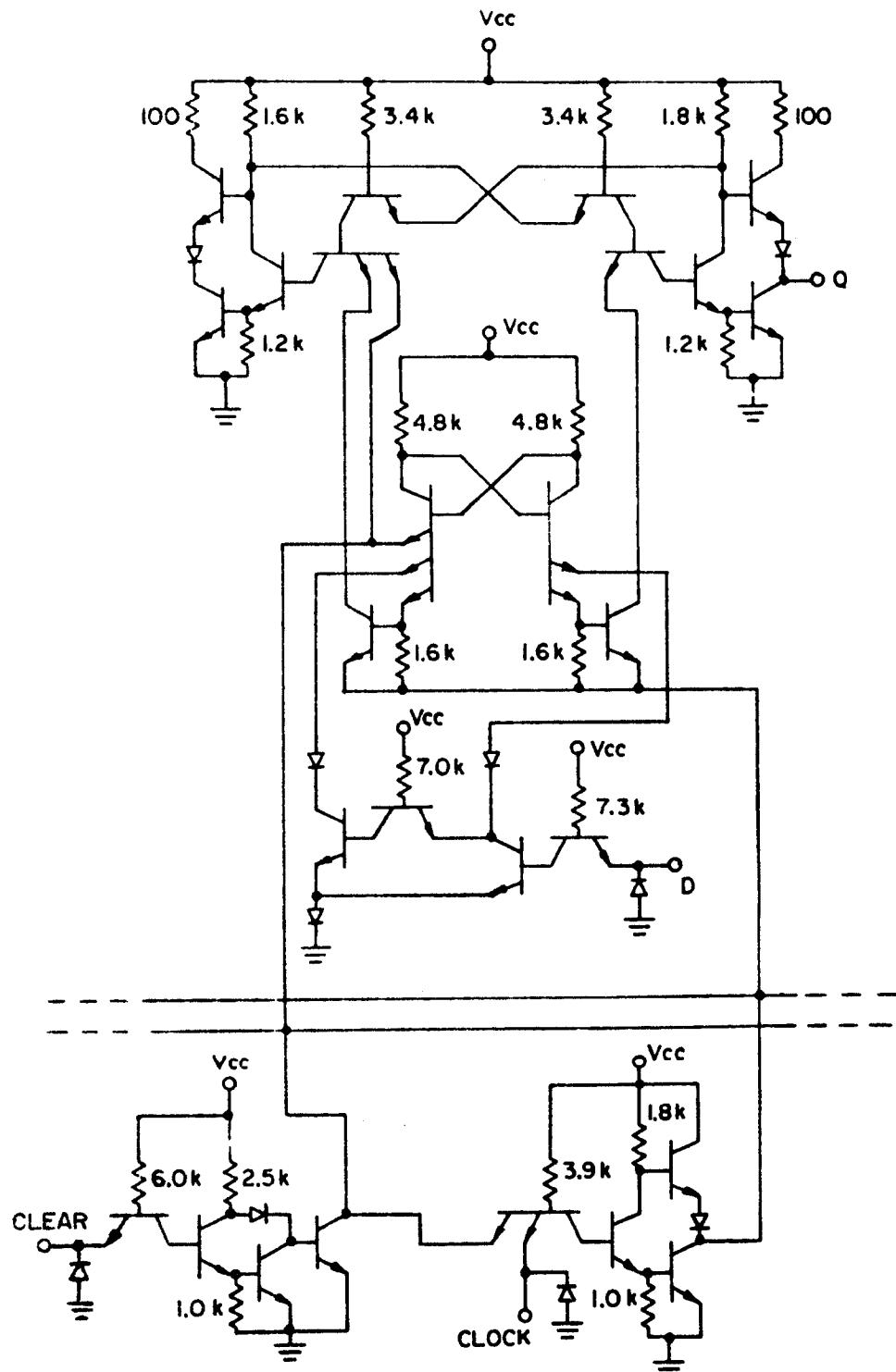
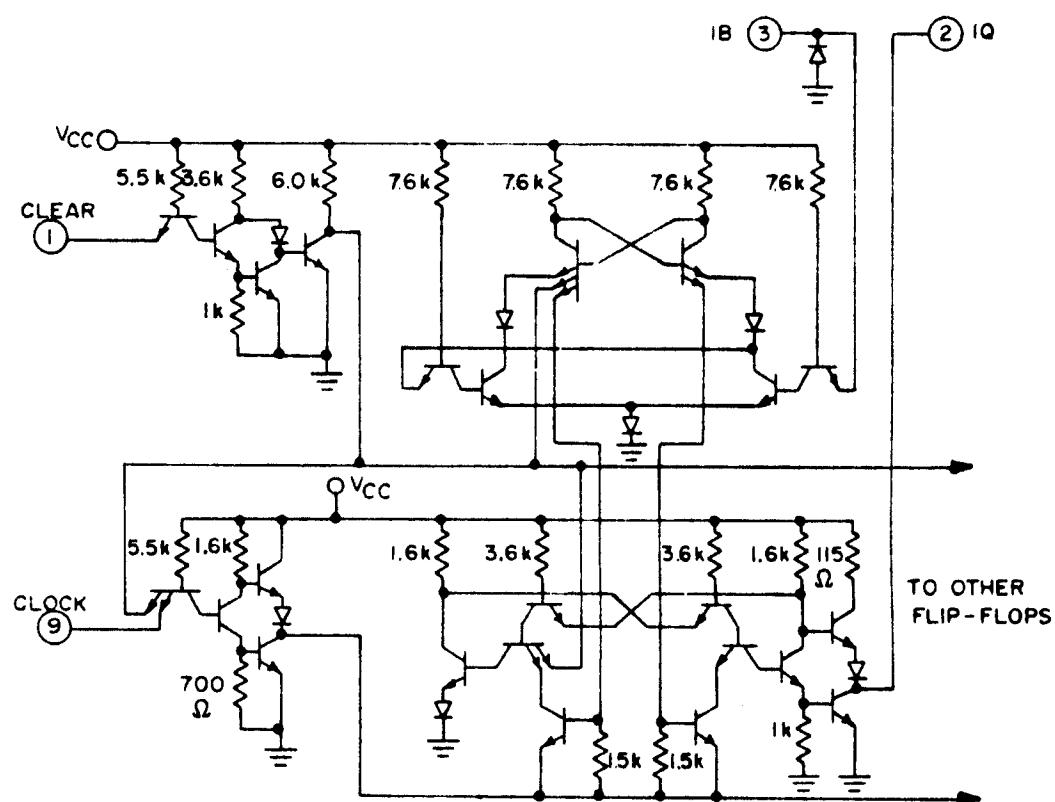


FIGURE 4. Schematic circuits - Continued.  
Device type 01 (Circuit C)



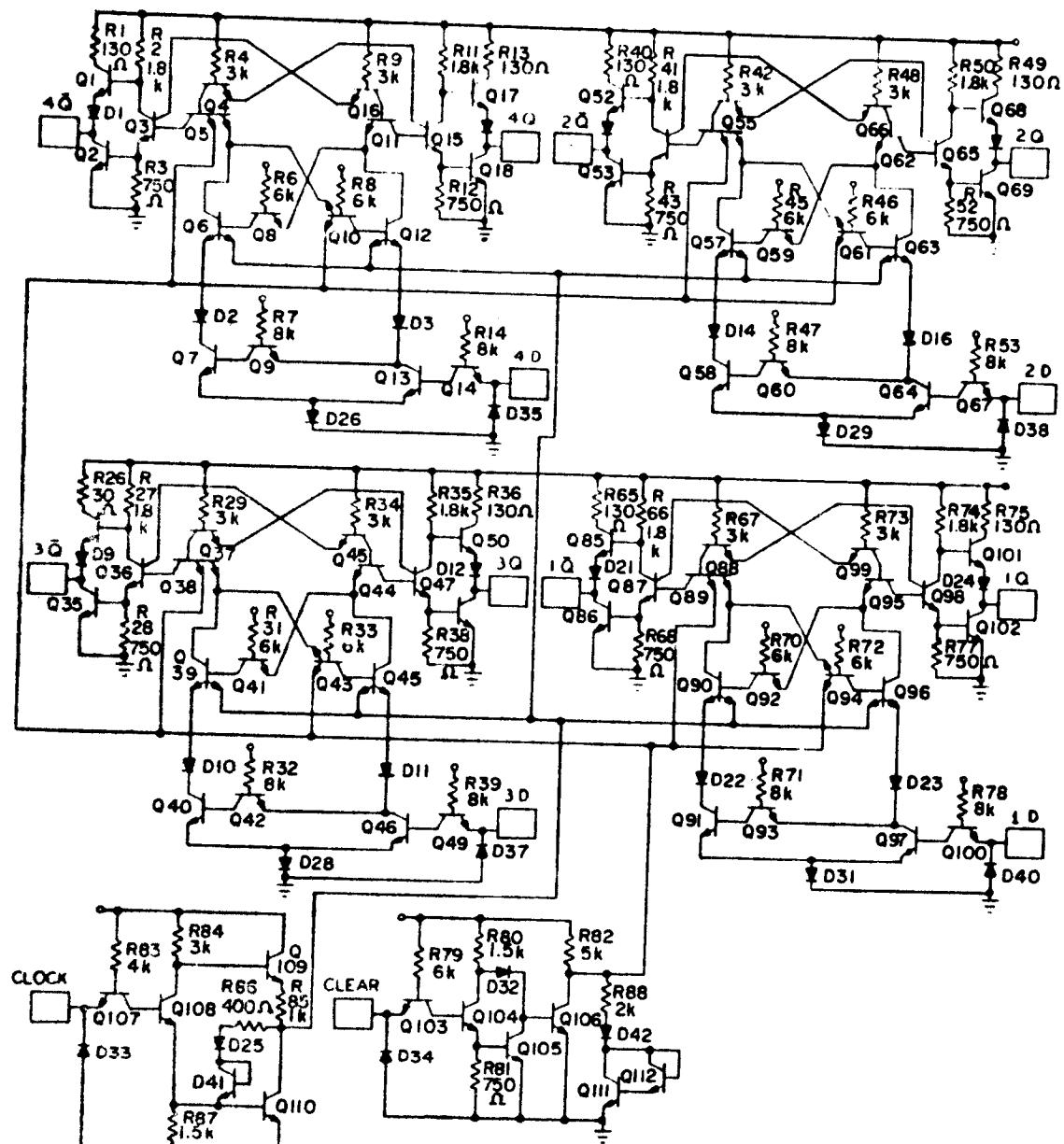
\* Device type 01 (Circuit D)

FIGURE 4. Schematic circuits - Continued.



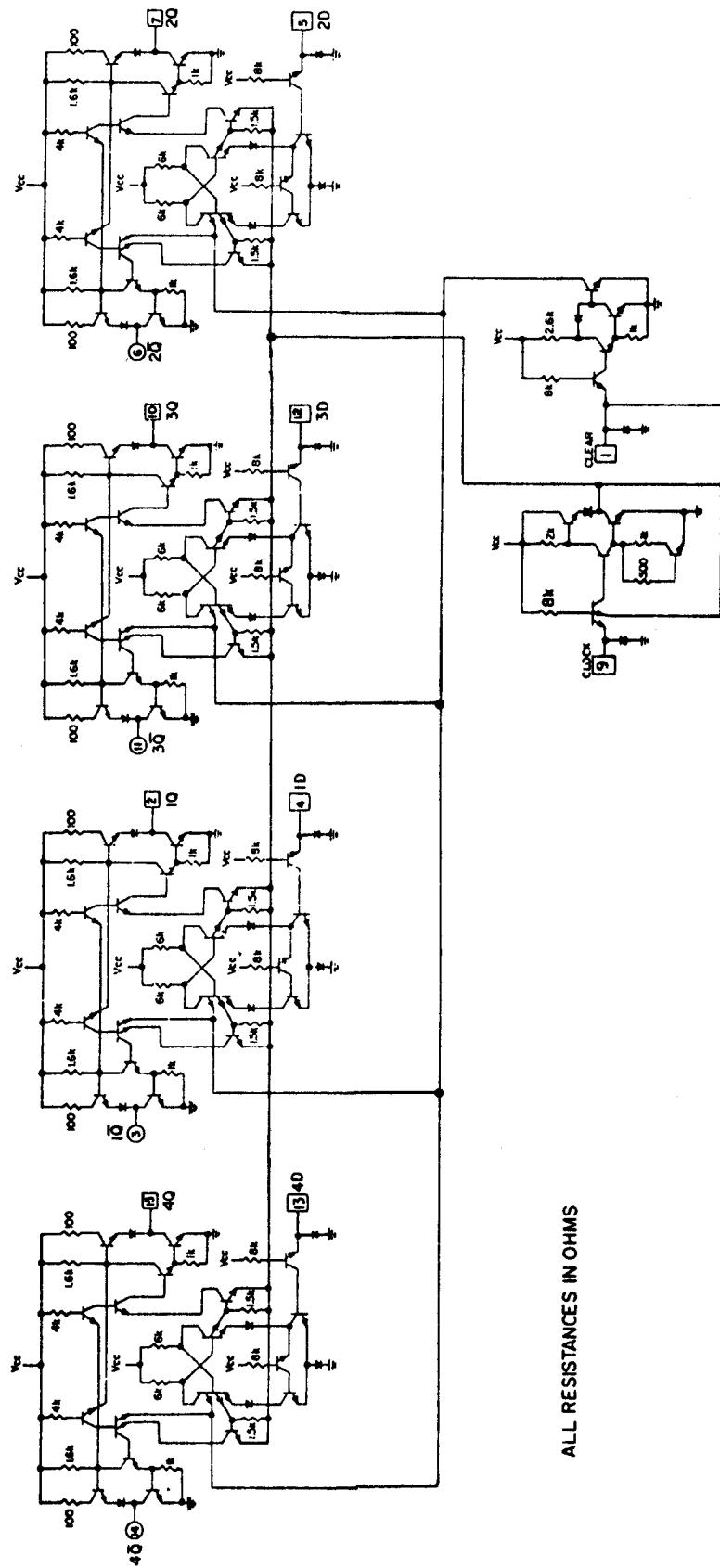
Device type 01 (Circuit E)

FIGURE 4. Schematic circuits - Continued.



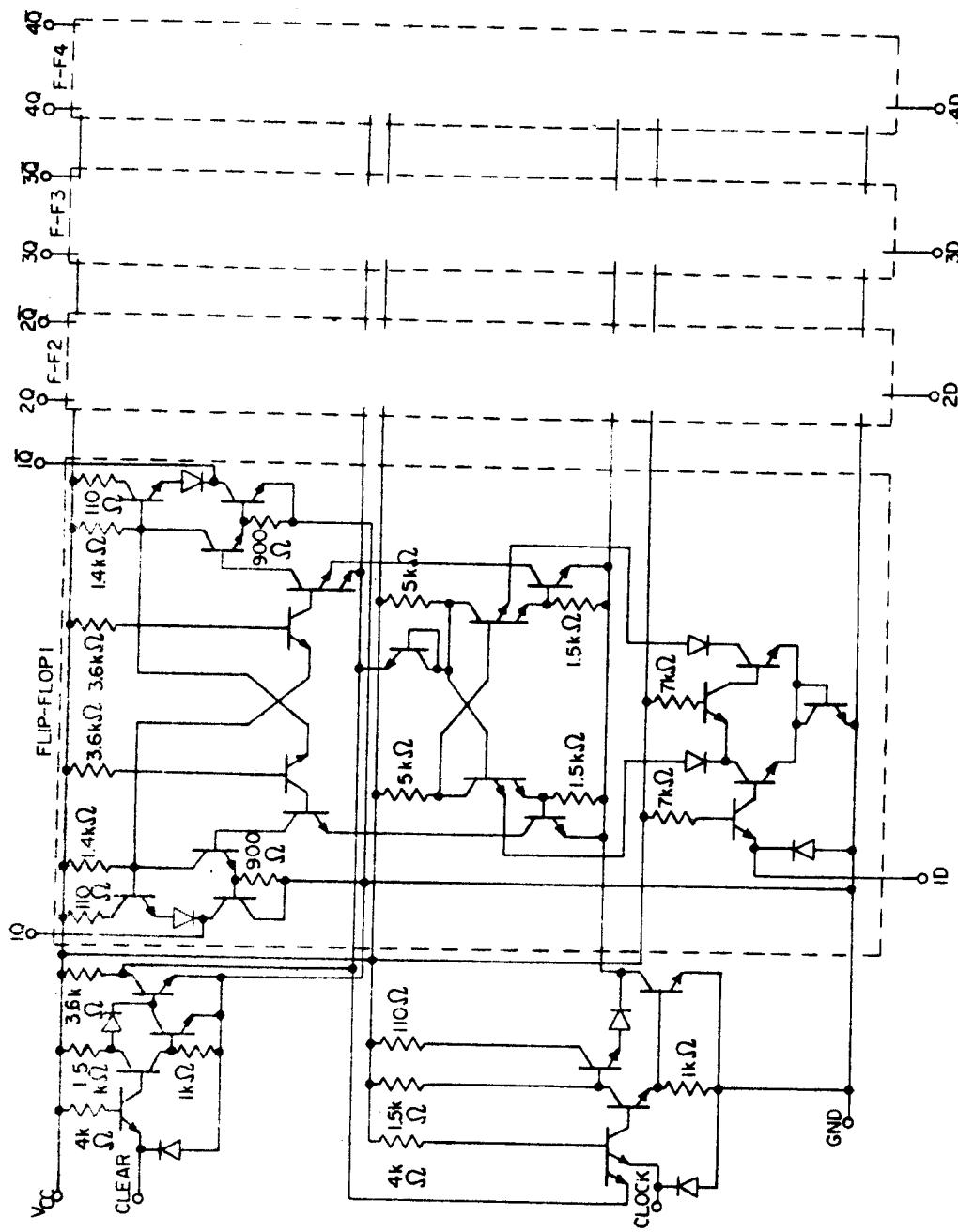
Device type 02  
Circuit A

FIGURE 4. Schematic circuits - Continued.

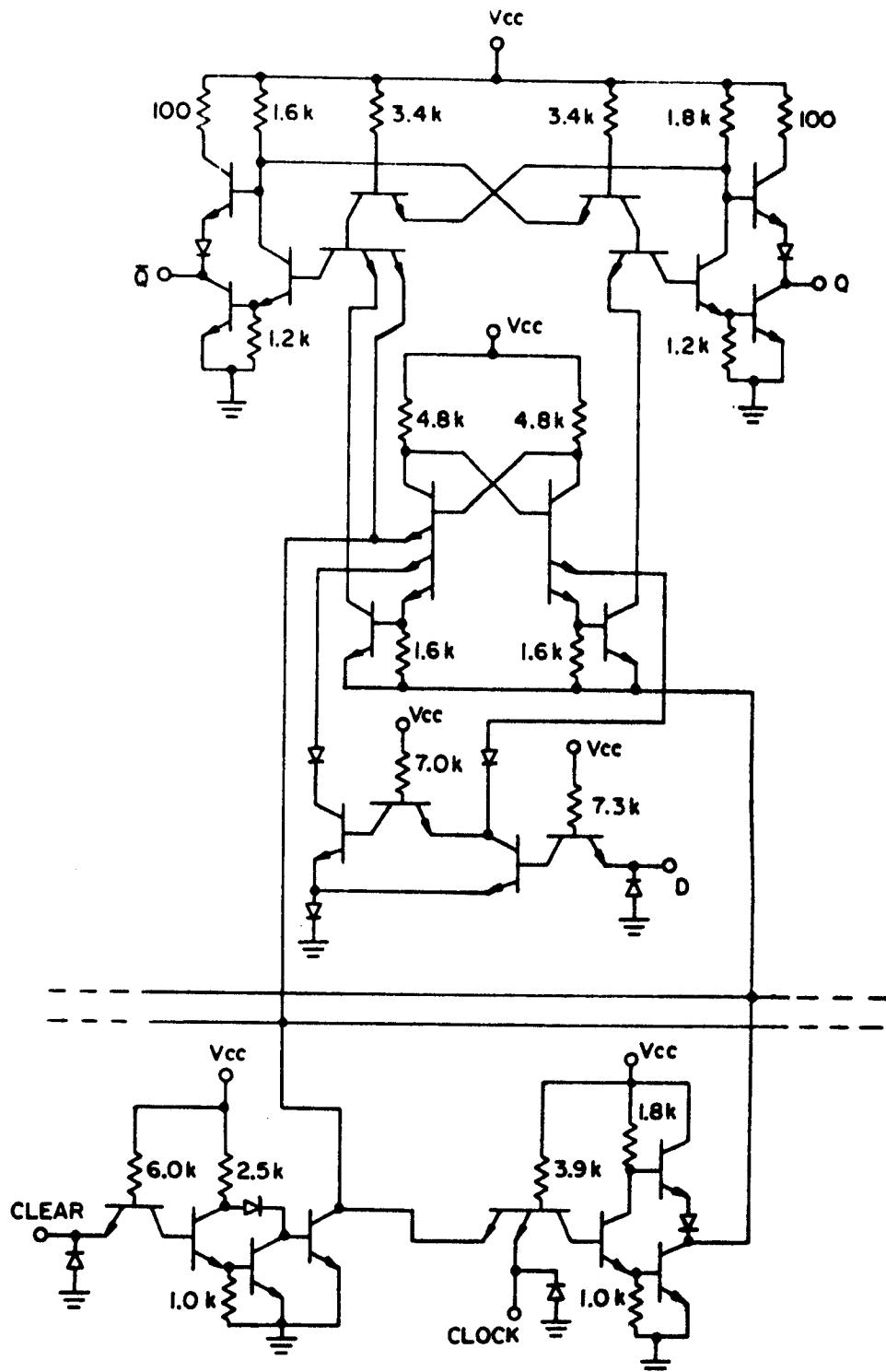


Device type 02 (Circuit B)

**FIGURE 4:** Schematic circuits - Continued.

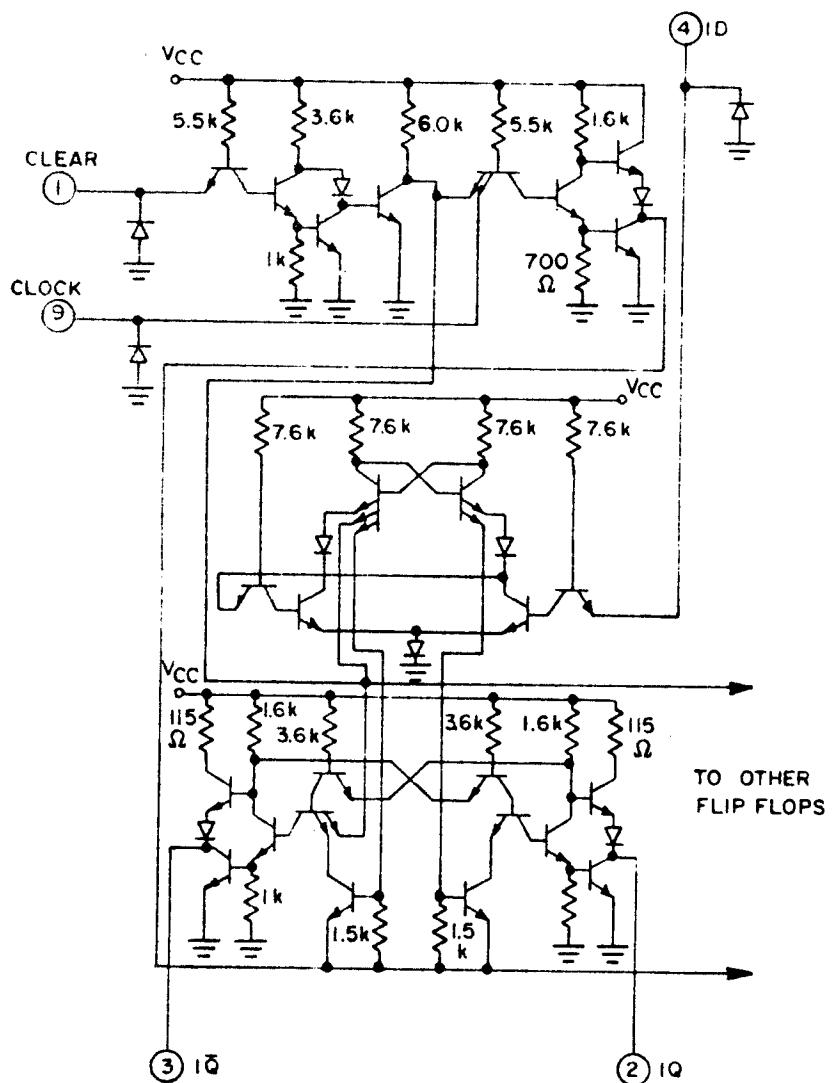


Device type 02 (Circuit C)  
FIGURE 4. Schematic circuits



\* Device type 02 (Circuit D)

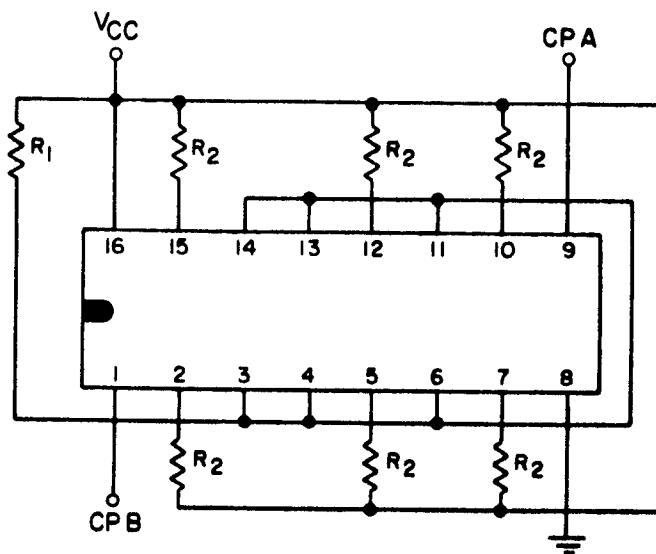
FIGURE 4. Schematic circuits - Continued.



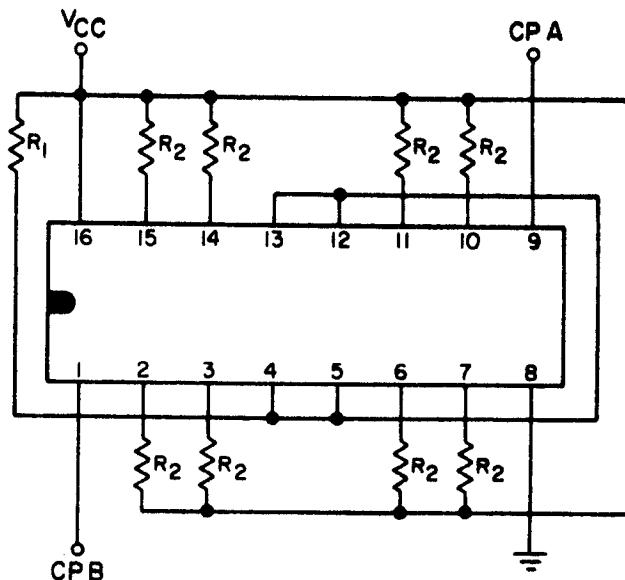
Device type 02 (Circuit E)

FIGURE 4. Schematic circuits - Continued.

## Device type 01



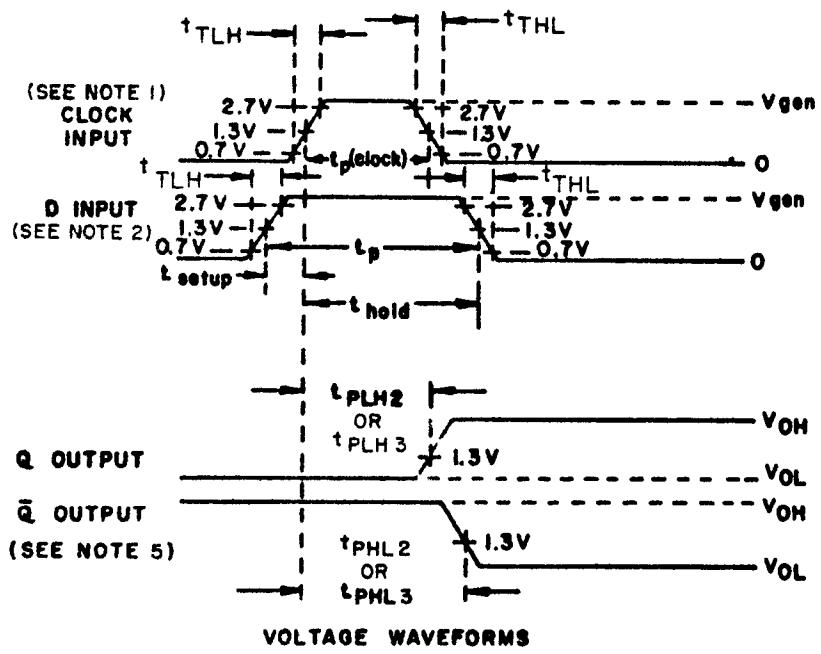
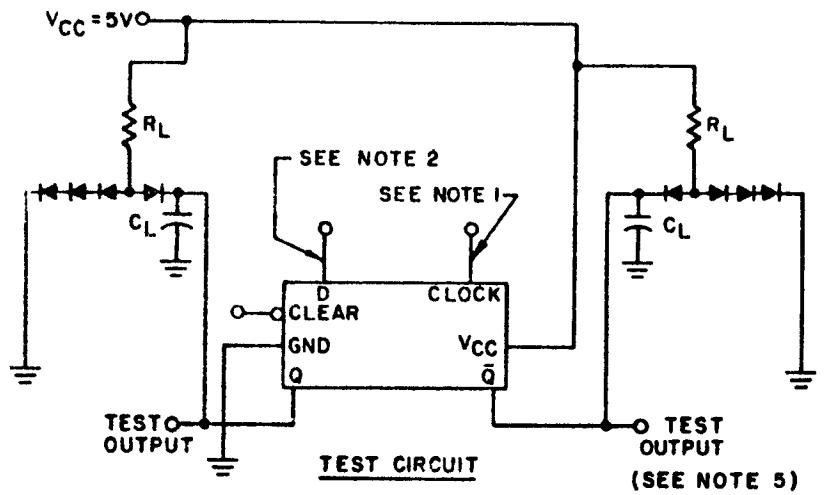
## Device type 02



## NOTES:

1. CPA = 100 kHz  $\pm$ 50% square wave; duty cycle = 50  $\pm$ 15%;  $V_{IL} = -0.5$  V minimum to +0.7 V maximum;  $V_{IH} = 2.0$  V minimum to 5.5 V maximum. CPB = Same as CPA, synchronized with CPA, except 50 kHz  $\pm$ 50% square wave.
2.  $R_1 = 1 \text{ k}\Omega \pm 5\%$ ;  $R_2 = 270\Omega \pm 5\%$ .
3.  $V_{CC}$  shall be high enough to insure that 5.0 V minimum is present at  $V_{CC}$  device terminal.

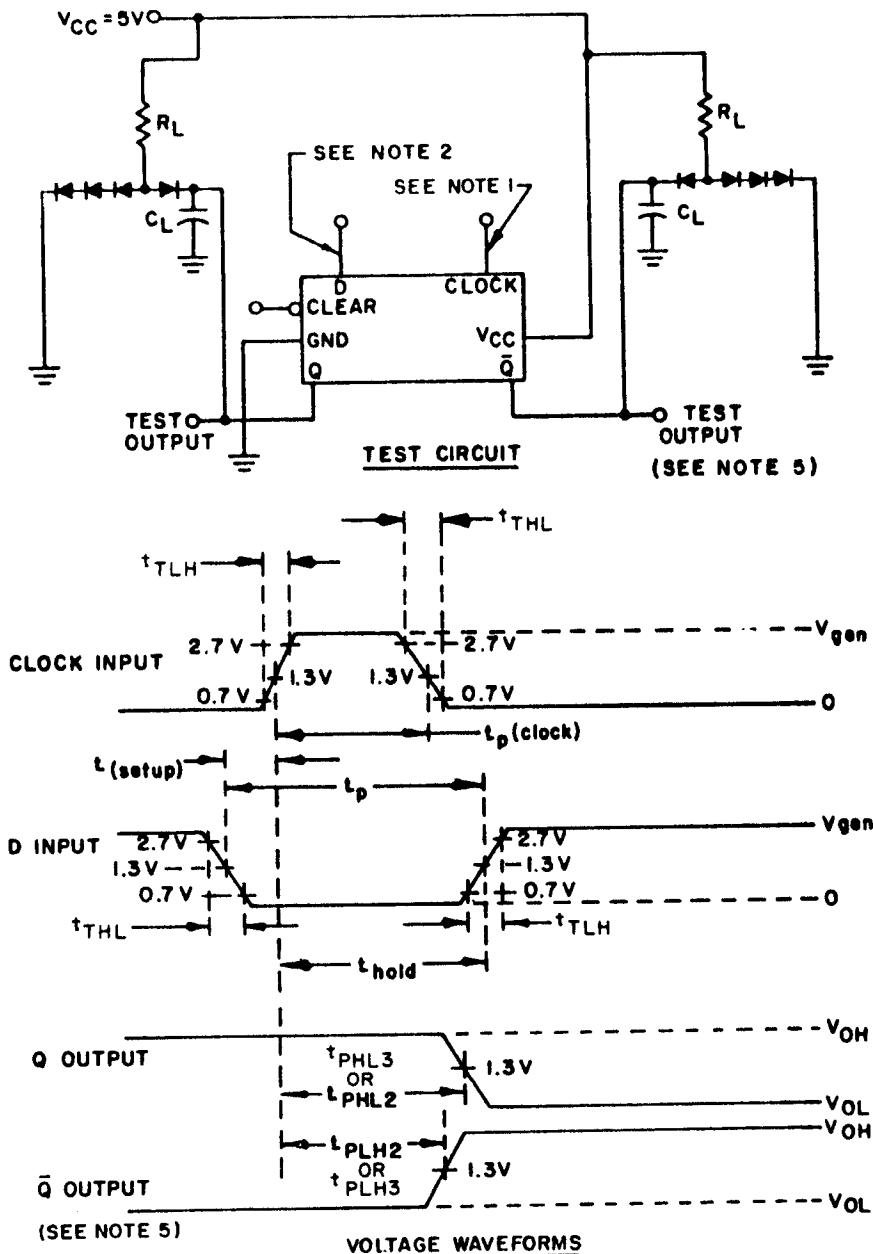
FIGURE 5. Burn-in and life test circuits.



## NOTES:

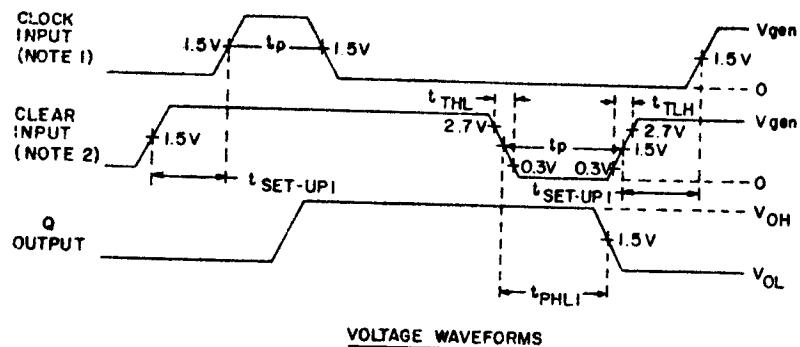
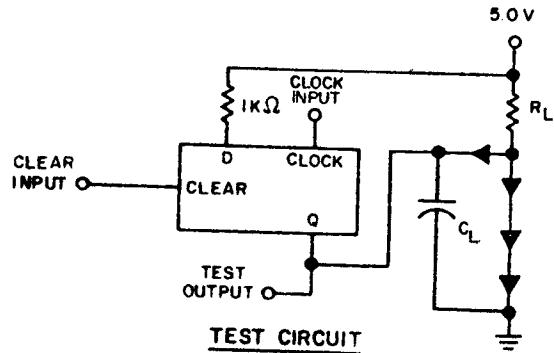
1. Clock input has the following characteristics:  $V_{gen} = 3\text{V}$  minimum,  $t_p = 17\text{ ns}$ ,  $t_{THL} = t_{TLH} \leq 10\text{ ns}$ , and PRR  $\leq 1\text{ MHz}$ . When testing  $F_{MAX}$ , PRR = 25 MHz.
2. D input pulse has the following characteristics:  $V_{gen} = 3\text{V}$  minimum,  $t_{TLH} = t_{THL} \leq 10\text{ ns}$ ,  $t_p = 30\text{ ns}$ ,  $t_{SETUP} = 25\text{ ns}$ ,  $t_{HOLD} = 5\text{ ns}$  and PRR  $\leq 0.5\text{ MHz}$ . When testing  $F_{MAX}$ , PRR = 12.5 MHz at 50% duty cycle.
3.  $R_L = 390\Omega \pm 5\%$ ;  $C_L = 50\text{ pF} \pm 10\%$  (including jig and probe capacitance).
4. All diodes are 1N3064, or equivalent.
5. Q output applies to device type 02 only.

FIGURE 6. Synchronous switching test circuit (high-level data) for device types 01 and 02.



- NOTES:**
1. Clock input has the following characteristics:  $V_{gen}$  = 3 V minimum,  $t_p$  = 17 ns,  $t_{THL} = t_{TLH} \leq 10$  ns, and PRR  $\leq 1$  MHz. When testing  $F_{MAX}$  PRR = 25 MHz.
  2. D input pulse has the following characteristics:  $V_{gen}$  = 3 V minimum,  $t_{TLH} = t_{THL} \leq 10$  ns,  $t_p = 30$  ns,  $t_{SETUP} = 25$  ns,  $t_{HOLD} = 5$  ns and PRR  $< 0.5$  MHz. When testing  $F_{MAX}$ , PRR = 12.5 MHz at 50% duty cycle.
  3.  $R_L = 390\Omega \pm 5\%$ ;  $C_L = 50$  pF  $\pm 10\%$  (including jig and probe capacitance).
  4. All diodes are 1N3064, or equivalent.
  5. Q output applies to device type 02 only.

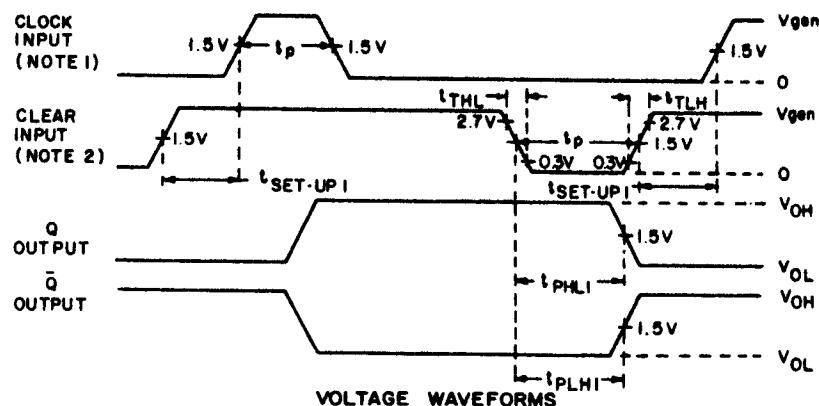
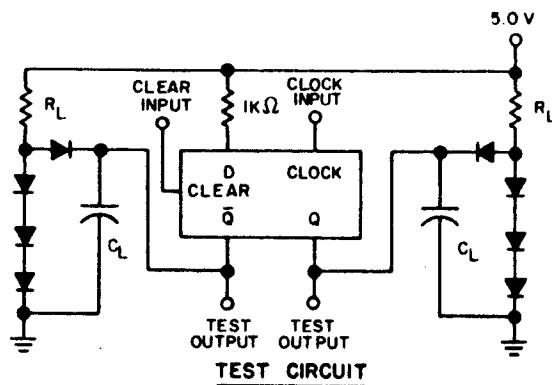
FIGURE 7. Synchronous switching test circuit (low-level data) for device types 01 and 02.



NOTES:

1. Clock input pulse is a preconditioning pulse and has the following characteristics:  
 $V_{gen} = 3 \text{ V minimum}$ ,  $t_p \leq 100 \text{ ns}$ ,  $t_{SETUP} = 25 \text{ ns}$  and  $PRR \leq 1 \text{ MHz}$ .
2. Clear input pulse has the following characteristics:  $V_{gen} = 3 \text{ V minimum}$ ,  
 $t_{THL} = t_{TLH} \leq 10 \text{ ns}$ ,  $t_p = 30 \text{ ns}$ , and  $PRR \leq 1 \text{ MHz}$ .
3. All diodes are IN3064 or equivalent.
4.  $R_L = 390\Omega \pm 5\%$ ;  $C_L = 50 \text{ pF} \pm 10\%$  (including jig and probe capacitance).

FIGURE 8. Clear switching test circuit and waveforms for device type 01.

**NOTES:**

1. Clock input pulse is a preconditioning pulse and has the following characteristics:  $V_{gen} = 3 \text{ V minimum}$ ,  $t_p \leq 100 \text{ ns}$ ,  $t_{SETUP} = 25 \text{ ns}$  and  $\text{PRR} \leq 1 \text{ MHz}$ .
2. Clear input pulse has the following characteristics:  $V_{gen} = 3 \text{ V minimum}$ ,  $t_{THL} = t_{TLH} \leq 10 \text{ ns}$ ,  $t_p = 30 \text{ ns}$ , and  $\text{PRR} \leq 1 \text{ MHz}$ .
3. All diodes are 1N3064, or equivalent.
4.  $R_L = 390\Omega \pm 5\%$ ;  $C_L = 50 \text{ pF} \pm 10\%$  (including jig and probe capacitance).

FIGURE 9. Clear switching test circuit and waveforms for device

TABLE III. Group A inspection for device type 01.  
Terminal conditions (pins not designated may be high  $\geq 2.0$  V or low  $\leq 0.7$  V or open).

Subgroup	Symbol	MIL-STD-383 method	Case E & F												Test limits													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min.	Max.	Unit						
1 $T_A = 25^\circ C$	V <sub>IC</sub>	Test No.	Clear 1Q	1D	2D	2Q	3D	3Q	GND	Clock	4Q	4D	5Q	5D	6Q	V <sub>CC</sub>	4.5 V	-1.5 V										
			1	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	GND	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA					Clear 1D	1D	2D	Clock 4D	5D	5D	5D	5D		
	V <sub>OH</sub>	3007	9	2.0 V	-0.8 mA	2.0 V	2.0 V	-0.8 mA	2.0 V	-0.8 mA	B	-0.8 mA	2.0 V	-0.8 mA	-12 mA				IQ	2.4								
	V <sub>OL</sub>	3008	10	11	12	13	14	15	0.8 V	16 mA									2Q	3Q	4Q	5Q	5Q	5Q	5Q	5Q		
	T <sub>LL1</sub>	3009	21	CKT A,C,D	20														IQ	0.4								
	T <sub>LL2</sub>	3010	22	CKT B,C	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5Q	5Q	5Q	5Q	5Q	5Q	5Q	5Q		
	T <sub>HH1</sub>	3011	23	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	1D	1D	2D	3D	4D	5D	6D	6D		
	T <sub>HH2</sub>	3012	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	
	I <sub>OS</sub>	3013	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	
	I <sub>CC</sub>	3005	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. - Continued  
 (pins not designated may be high -2.0 V or low 0.7 V or open).

Terminal conditions (pins not designated may be high or low) appear

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1. B - Monostable GND, then V<sub>CC</sub>.

2. The tests in subgroups 7 and 8 shall be performed in the sequence specified.

3. The output voltages shall be either:

  - (a) H = 2.4 V minimum and L = 0.4 V maximum when using a high-speed checker double comparator.
  - (b) H = 1.5 V minimum and L < 1.5 V when using a high-speed checker single comparator.

4. Only a summary of attributes data is required.

5. P<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A Inspection for device type 02.  
Terminal conditions (pins not designated may be high  $-2.0\text{ V}$  or low  $\leq 0.7\text{ V}$  or open).

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end of device type 02.

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. - Continued  
Terminal conditions (pins not designated may be high  $> 2.0$  V or low  $\leq 0.7$  V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
		Test No.	Clear	1Q	1Q	1D	2D	2Q	2Q	GND	Clock	3Q	3Q	3D	4D	4Q	4Q	VCC	Meas. terminal	Min	Max	Unit	
7.2/4/ $T_A = 25^\circ C$ Truth table test	3014	50	B	L	H	A	H	H	L	GND	B	L	H	A	H	L	5.0 V	All outputs					
		51	B	L	H	A	H	H	L		B	L	H	A	H	L							
		52	B	L	H	A	H	H	L		B	L	H	A	H	L							
		53	A	L	H	L	H	L	H		B	L	H	I	H	L							
		54	A	L	H	L	H	L	H		B	L	H	I	H	L							
		55	H	L	I	L	I	L	I		B	H	I	B	H	I							
		56	H	L	I	L	I	L	I		B	H	I	B	H	I							
		57	L	H	B	B	H	B	H		B	H	A	L	H	I							
		58	L	H	B	B	H	B	H		B	H	A	L	H	I							
		59	I	H	B	B	H	B	H		A	H	A	H	I	H							
		60	H	L	A	A	L	A	H		B	H	A	H	I	A							
		61	H	L	A	A	L	A	H		B	H	A	H	I	A							
		62	B	L	H	A	H	L	H		B	H	A	H	I	H							
8.2/4/ Repeat subgroup 7 at $T_A = 125^\circ C$ and $T_A = -55^\circ C$ .																							
9/25 C	FMAX	(Fig. 6)	63	5.0 V	OUT	IN	IN	IN	IN	OUT		IN	OUT	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	MHz
			64																				
			65																				
			66																				
			67	IN	OUT	5.0 V	5.0 V	OUT															
			68																				
			69																				
			70																				
			71																				
			72																				
			73																				
			74																				
			75	OUT	OUT	IN	IN	IN	IN	OUT		OUT	OUT										
			76																				
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			93																				
			94																				
			95	IN	OUT	5.0 V	5.0 V	OUT															
			96																				
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11 Same tests, terminal conditions and limits as subgroup 16, except  $T_A = -55^\circ C$ .

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NOTES:

1. B = Monostable GND, then VCC.
2. The tests in subgroups 7 and 8 shall be performed in the sequence specified.
3. Output voltages shall be either:
  - (a)  $H = 2.4$  V minimum and  $L = 0.4$  V maximum when using a high-speed checker double comparator.
  - (b)  $H > 1.5$  V and  $L < 1.5$  V when using a high-speed checker single comparator.
4. Only a summary of attributes data is required.
5. FMAX, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspections. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Operating life test (method 1005 of MIL-STD-883) conditions, or equivalent:
  1. Test condition D or E, using the circuit shown on figure 5, or equivalent.
  2.  $T_A = 125^\circ\text{C}$ , minimum.
  3. Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables and as follows:

4.5.1 Life-test cooldown procedure. When devices are measured at  $25^\circ\text{C}$  following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for the packaging of microcircuits shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logic support.

6.3 Ordering data. The contract or order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to procuring activity in addition to notification to qualifying activity, if applicable.
- e. Requirements for preservation and packing.
- f. Requirements for failure analysis (including required test condition of method 5003), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, MIL-STD-1331, and as follows:

GND - - - - - Electrical ground (common terminal)  
 V<sub>IN</sub> - - - - - Voltage level at an input terminal

6.4.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed Generic-Industry type. Generic-Industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of Generic-Industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military Device type	Generic-Industry type
01	54174
02	54175

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodian:  
Air Force - 17

Preparing activity:  
Air Force - 17

Review activities:  
Air Force - 11, 85, 99

Agent:  
DLA - ES

User activity:  
Air Force - 19

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