MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL,
FLIP-FLOPS, MONOLITHIC SILICON

This amendment forms a part of Military Specification MIL-M-38510/17A(USAF), dated 1 May 1979, and is approved for use by the Department of the Air Force and is available for use by all Departments and Agencies of the Department of Defense.

PAGE 3

* TABLE II, delete and substitute as follows:

"TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1
Final electrical test parameters (method 5004)	1*,2,3,7, 9,10,11	1,2,3,7, 9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7, 9
Group B test requirements (method 5005) subgroup 5	1,2,3,9, 10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3
Additional electrical subgroups for group C periodic inspections	N/A	10,11
Group D end-point electrical parameters (method 5005)	1,2,3	1,2,3

*PDA applies to subgroup 1 (see 4.3c)."

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* FIGURE 6: Delete and substitute new figure as printed on page 3 of this amendment.

PAGE 21

* FIGURE 7: Delete and substitute new figure as printed on page 4 of this amendment.

PAGE 24

* TABLE III, Terminal conditions (pins not designated may be high $\geq$ 2.0 V or low $\leq$ 0.7 V or open): Delete "0.7 V" and substitute: "0.8 V". Make this same change on pages 25 and 26.

PAGE 27

* TABLE III, Group A, device type 02: Delete and substitute new table III as printed on page 5 of this amendment.

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6.7, delete and substitute as follows:

"6.7 Manufacturers' designations. Manufacturers' circuits included in this specification are designated as shown in table IV.

TABLE IV. Manufacturers' designations.

Device type	National Semiconductor	Texas Instruments	Signetics	Motorola	Fairchild
	Circuits				
	A	B	C	D	E
01	X	X	X	X	X
02	X	X	X	X	X

"6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes."

The margins of this amendment are marked with asterisks to indicate where changes from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

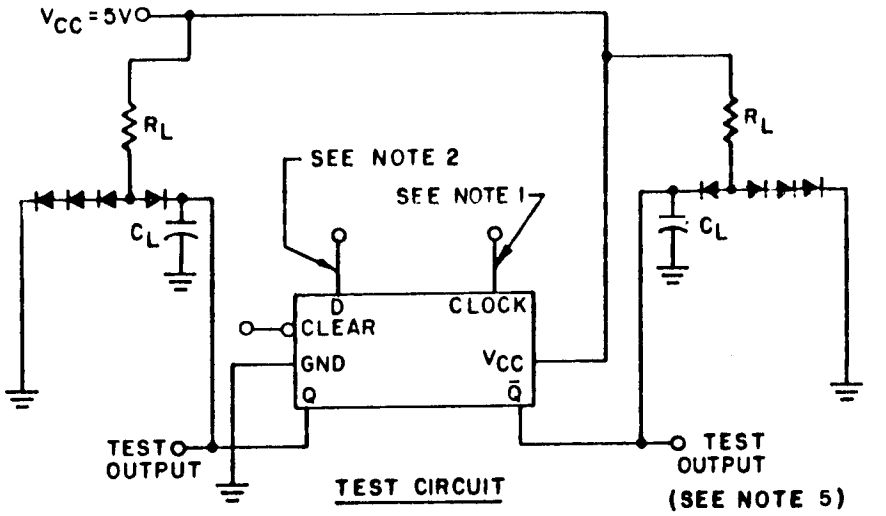
Custodian:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

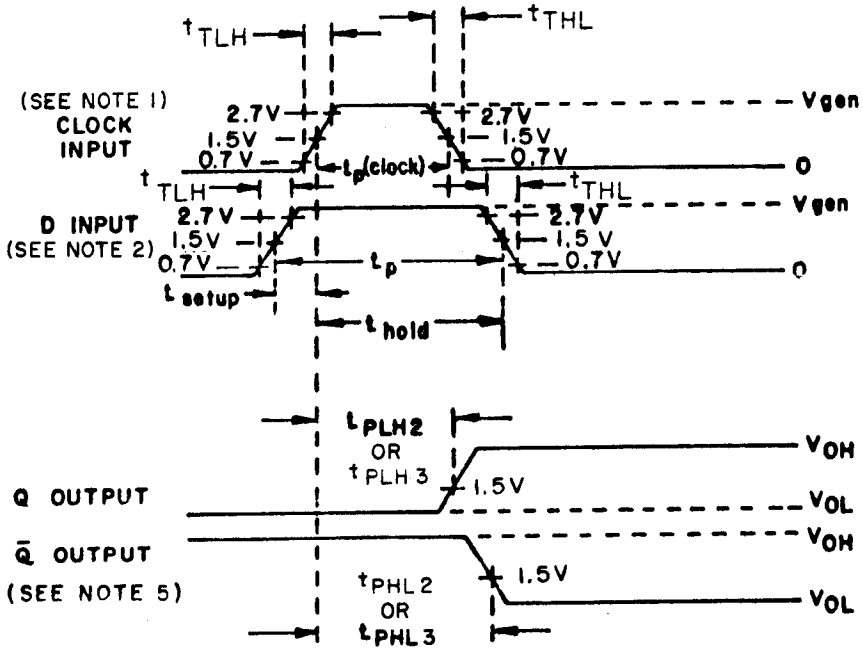
Agent:
DLA - ES

Preparing activity:
Air Force - 17

(Project 5962-F671)



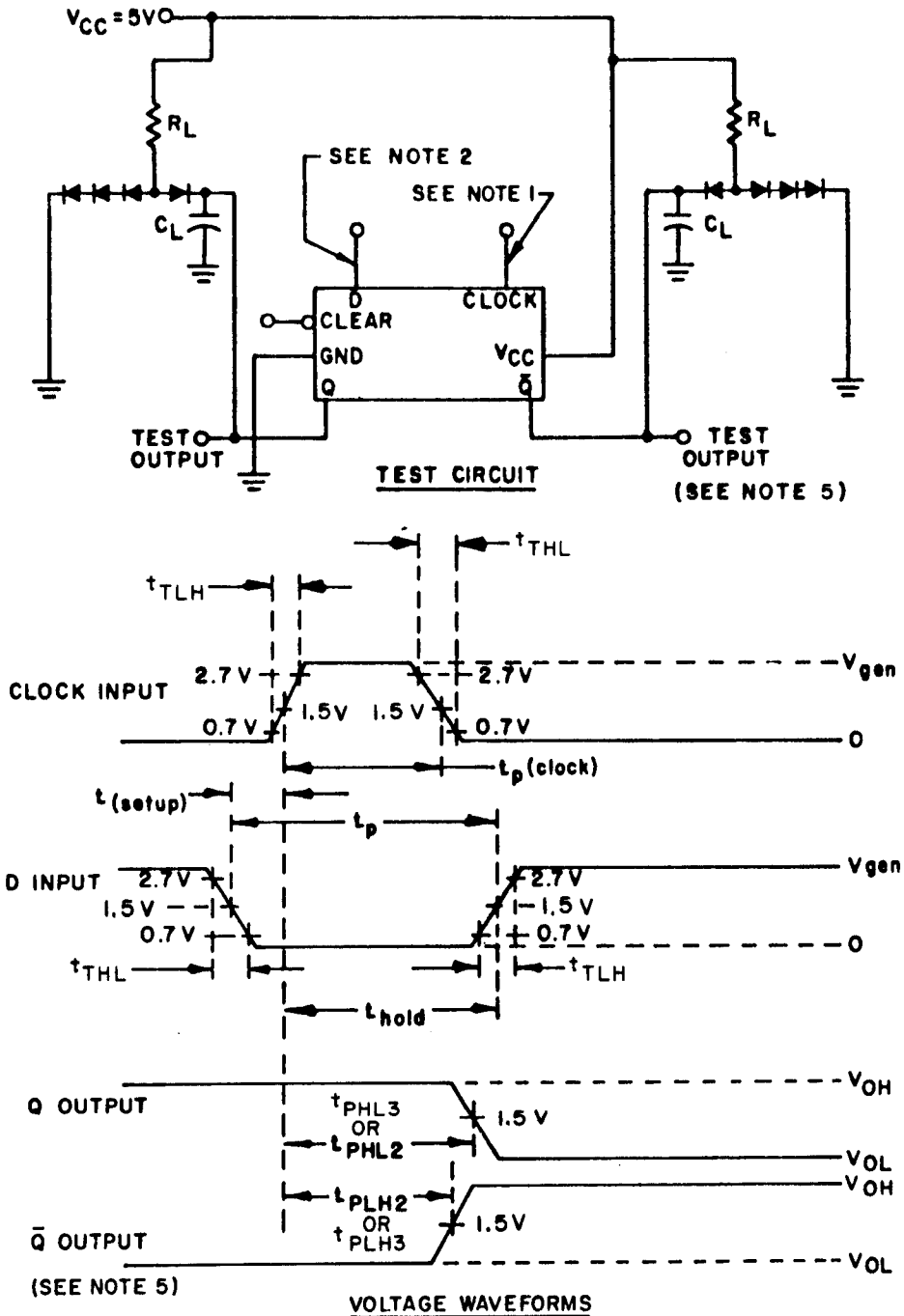
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Clock input has the following characteristics: V_{gen} = 3 V minimum, t_p = 20 ns, $t_{THL} = t_{TLH} \leq 10$ ns, and PRR $\leq$ 1 MHz. When testing F_{MAX} PRR = 25 MHz.
2. D input pulse has the following characteristics: V_{gen} = 3 V minimum, $t_{TLH} = t_{THL} \leq 10$ ns, t_p = 30 ns, t_{SETUP} = 25 ns, t_{HOLD} = 5 ns and PRR $\leq$ 0.5 MHz. When testing F_{MAX}, PRR = 12.5 MHz at 50% ±15% duty cycle.
3. R_L = 390Ω ± 5%; C_L = 50 pF ± 10% (including jig and probe capacitance).
4. All diodes are 1N3064, or equivalent.
5. $\overline{Q}$ output applies to device type 02 only.

FIGURE 6. Synchronous switching test circuit (high-level data) for device types 01 and 02.



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2. D input pulse has the following characteristics: V_{gen} = 3 V minimum, $t_{TLH} = t_{THL} \leq 10$ ns. t_p = 30 ns, t_{SETUP} = 25ns, t_{HOLD} = 5 ns and PRR $\leq$ 0.5 MHz. When testing F_{MAX}, PRR = 12.5 MHz at 50% ±15% duty cycle
3. R_L = 390Ω ± 5%; C_L = 50 pF ± 10% (including jig and probe capacitance).
4. All diodes are 1N3064, or equivalent.
5. Q̄ output applies to device type 02 only.

FIGURE 7. Synchronous switching test circuit (low-level data) for device types 01 and 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high > 2.0 V or low < 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 1$\overline{Q}$	4 1D	5 2D	6 2$\overline{Q}$	7 2Q	8 GND	9 Clock	10 3Q	11 3$\overline{Q}$	12 3D	13 4D	14 4$\overline{Q}$	15 4Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
7 2/ 4/ T_A = 25°C	Truth table test	3014	50	B	L	H	A	A	H	L	GND	B	L	H	A	A	H	L	5.0 V	All outputs	Limits per 3/		
			51	B	L	H			H	L		A	L	H			H	L					
			52	B	L	H			H	L		B	L	H			H	L					
			53	A	L	H			H	L		B	L	H			H	L					
			54		H	L			L	H		A	H	L			L	H					
			55		H	L			L	H		B	H	L			L	H					
			56		H	L	B	B	L	H		B	H	L	B	B	L	H					
			57		L	H	B	B	H	L		A	L	H	B	B	H	L					
			58		L	H	B	B	H	L		B	L	H	B	B	H	L					
			59		L	H	A	A	H	L		B	L	H	A	A	H	L					
			60		H	L	A	A	L	H		A	H	L	A	A	L	H					
			61		H	L	A	A	L	H		B	H	L	A	A	L	H					
			62	B	L	H	A	A	H	L		B	L	H	A	A	H	L					
8 2/ 4/	Repeat subgroup 7 at T_C = 125°C and T_C = -55°C.																						
9 T_A = 25°C	F_{MAX} 5/	(Fig 6)	63	5.0 V	OUT		IN	IN		OUT	GND	IN	OUT		IN	IN		OUT	5.0 V	1Q 2Q 3Q 4Q	25		MHz
			64																				
			65																				
			66																				
	t_{PLH1}	3003 (Fig 9)	67	IN		OUT	5.0 V	5.0 V	OUT			IN		OUT	5.0 V	5.0 V	OUT			Clear-1$\overline{Q}$ Clear-2$\overline{Q}$ Clear-3$\overline{Q}$ Clear-4$\overline{Q}$	5	28	ns
			68																				
			69																				
			70																				
	t_{PHL1}		71		OUT		5.0 V	5.0 V		OUT			OUT		5.0 V	5.0 V		OUT		Clear-1$\overline{Q}$ Clear-2$\overline{Q}$ Clear-3$\overline{Q}$ Clear-4$\overline{Q}$		38	
			72																				
			73																				
			74																				
	(t_{PLH2} t_{PHL2})	3003 Fig. 6&7	75 & 76	5.0 V	OUT		IN	IN		OUT			OUT		IN	IN		OUT		Clock-1$\overline{Q}$ Clock-2$\overline{Q}$ Clock-3$\overline{Q}$ Clock-4$\overline{Q}$		33	
			77 & 78																				
			79 & 80																				
			81 & 82																				
	(t_{PLH3} t_{PHL3})	3003 Fig. 6&7	83 & 84			OUT	IN	IN	OUT					OUT	IN	IN	OUT			Clock-1$\overline{Q}$ Clock-2$\overline{Q}$ Clock-3$\overline{Q}$ Clock-4$\overline{Q}$			
			85 & 86																				
			87 & 88																				
			89 & 90																				
10 T_A = 125°C	F_{MAX} 5/	(Fig 6)	91		OUT		IN	IN		OUT	GND		OUT		IN	IN		OUT	5.0 V	1Q 2Q 3Q 4Q	25		MHz
			92																				
			93																				
			94																				
	t_{PLH1}	3003 (Fig 9)	95	IN		OUT	5.0 V	5.0 V	OUT					OUT	5.0 V	5.0 V	OUT			Clear-1$\overline{Q}$ Clear-2$\overline{Q}$ Clear-3$\overline{Q}$ Clear-4$\overline{Q}$	5	36	ns
			96																				
			97																				
			98																				
	t_{PHL1}		99		OUT		5.0 V	5.0 V		OUT			OUT		5.0 V	5.0 V		OUT		Clear-1$\overline{Q}$ Clear-2$\overline{Q}$ Clear-3$\overline{Q}$ Clear-4$\overline{Q}$		50	
			100																				
			101																				
			102																				
	(t_{PLH2} t_{PHL2})	3003 Fig. 6&7	103 & 104	5.0 V	OUT		IN	IN		OUT			OUT		IN	IN		OUT		Clock-1$\overline{Q}$ Clock-2$\overline{Q}$ Clock-3$\overline{Q}$ Clock-4$\overline{Q}$		43	
			105 & 106																				
			107 & 108																				
			109 & 110																				
	(t_{PLH3} t_{PHL3})	3003 Fig. 6&7	111 & 112			OUT	IN	IN	OUT					OUT	IN	IN	OUT			Clock-1$\overline{Q}$ Clock-2$\overline{Q}$ Clock-3$\overline{Q}$ Clock-4$\overline{Q}$			
			113 & 114																				
			115 & 116																				
			117 & 118																				
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C.																						

NOTES:
1. B = Momentary GND, then V_{CC}.
2. The tests in subgroups 7 and 8 shall be performed in the sequence specified.
3. Output voltages shall be either:
   (a) H = 2.4 V minimum and L = 0.4 V maximum when using a high-speed checker double comparator, or
   (b) H > 1.5 V and L < 1.5 V when using a high-speed checker single comparator.
4. Only a summary of attributes data is required.
5. F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.