

QUALIFICATION  
REQUIREMENTS  
REMOVED

MIL-M-38510/18A  
9 August 1983  
SUPERSEDING  
MIL-M-38510/18(USAF)  
4 September 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, REGISTER FILE,  
MONOLITHIC SILICON

INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, register file microcircuits. One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, with the exception that the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	4 x 4 register files

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range- - - - -	-1.5 V dc at -12 mA to +5.5 V dc
Storage temperature range- - - - -	-65°C to +150°C
Maximum power dissipation per flip-flop, (P <sub>D</sub> ) <sup>1/</sup> -	770 mW
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ):	
Case E - - - - -	0.08°C/mW
Case F - - - - -	0.06°C/mW
Junction temperature (T <sub>J</sub> )- - - - -	+175°C

<sup>1/</sup> Must withstand the added P<sub>D</sub> due to short circuit test (e.g., I<sub>OS</sub>).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage- - - - -	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage ( $V_{IH}$ )-	+2.0 V dc
Maximum low-level input voltage ( $V_{IL}$ ) -	+0.8 V dc
Normalized fanout (each output) <u>2</u> /- - -	10 maximum
Case operating temperature range- - - -	-55°C to +125°C
Input setup time <u>3</u> /:	
Data input- - - - -	10 ns minimum
Write select <u>4</u> / - - - - -	15 ns minimum
Input hold time <u>3</u> /:	
Data input- - - - -	15 ns minimum
Write select <u>4</u> / - - - - -	5 ns minimum
Latch time for new data <u>5</u> /- - - - -	25 ns minimum

1.5 Description. The 16-bit TTL register file incorporates the equivalent of 98 gates on a monolithic chip measuring only 90 by 110 mils. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input,  $G_w$ , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input,  $G_r$ , is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement (data-entry addressing separate from data-read addressing and individual sense line) eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 246 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

2/ Device will fanout in both high- and low-levels to the specified number of inputs of the same device as that being tested.

3/ With respect to write-enable.

4/ Write select setup time will protect the data written into the previous address. If the protection of data in the previous address is not required, write select setup time can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during the write select hold time will result in data being written with that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

5/ Latch time is the time required for the internal output of the latch to assume the state of the new data. This is important only when attempting to read from a location immediately after that location has received new data.

## 2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

## SPECIFICATION

## MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

## STANDARD

## MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

## 3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Truth tables and functional description. The truth tables or functional description shall be as specified on figure 3.

3.2.4 Case outlines. Case outlines shall be as specified in MIL-M-38510 and in 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line. Not necessarily the line producing the device type described herein.

3.8 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

## MIL-M-38510/18A

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup>	Limits		Unit
			Min	Max	
Low-level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 16 mA		0.4	V
Maximum collector cut-off current	I <sub>CEX</sub>	V <sub>CC</sub> = 4.5 V, V <sub>O</sub> = 5.5 V		30	μA
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = 12 mA		-1.5	V
Low-level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V	-0.7	-1.6	mA
High-level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.4 V		40	μA
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V		100	μA
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V		140	mA
Propagation delay times	t <sub>PLH1</sub>	Read-enable to any output, V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 400Ω, C <sub>L</sub> = 50 pF	5	18	ns
	t <sub>PHL1</sub>		5	36	ns
	t <sub>PLH2</sub>	Write-enable to any output, V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 400Ω, C <sub>L</sub> = 50 pF	5	48	ns
	t <sub>PHL2</sub>		5	54	ns
	t <sub>PLH3</sub>	Read address to any output, V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 400Ω, C <sub>L</sub> = 50 pF	5	42	ns
	t <sub>PHL3</sub>		5	54	ns
	t <sub>PLH4</sub>	Data to any output, V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 400Ω, C <sub>L</sub> = 50 pF	5	36	ns
	t <sub>PHL4</sub>		5	54	ns

<sup>1/</sup> Complete terminal conditions are specified in table III.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class B devices
Interim electrical test parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,7,9
Group C end-point electrical parameters (method 5005)	1,2,3
Group D end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspection	10,11

\*PDA applies to subgroup 1 (see 4.2c).

## 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
  - (2)  $T_A = +125^\circ\text{C}$  minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510, and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data (see 6.6) may be used to satisfy the requirements for groups C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

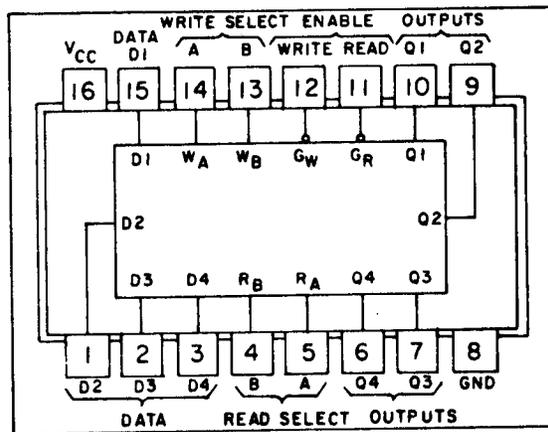
4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, and 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical parameters shall be as specified in table IV herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical test parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.



CASES E AND F

FIGURE 1. Terminal connections.

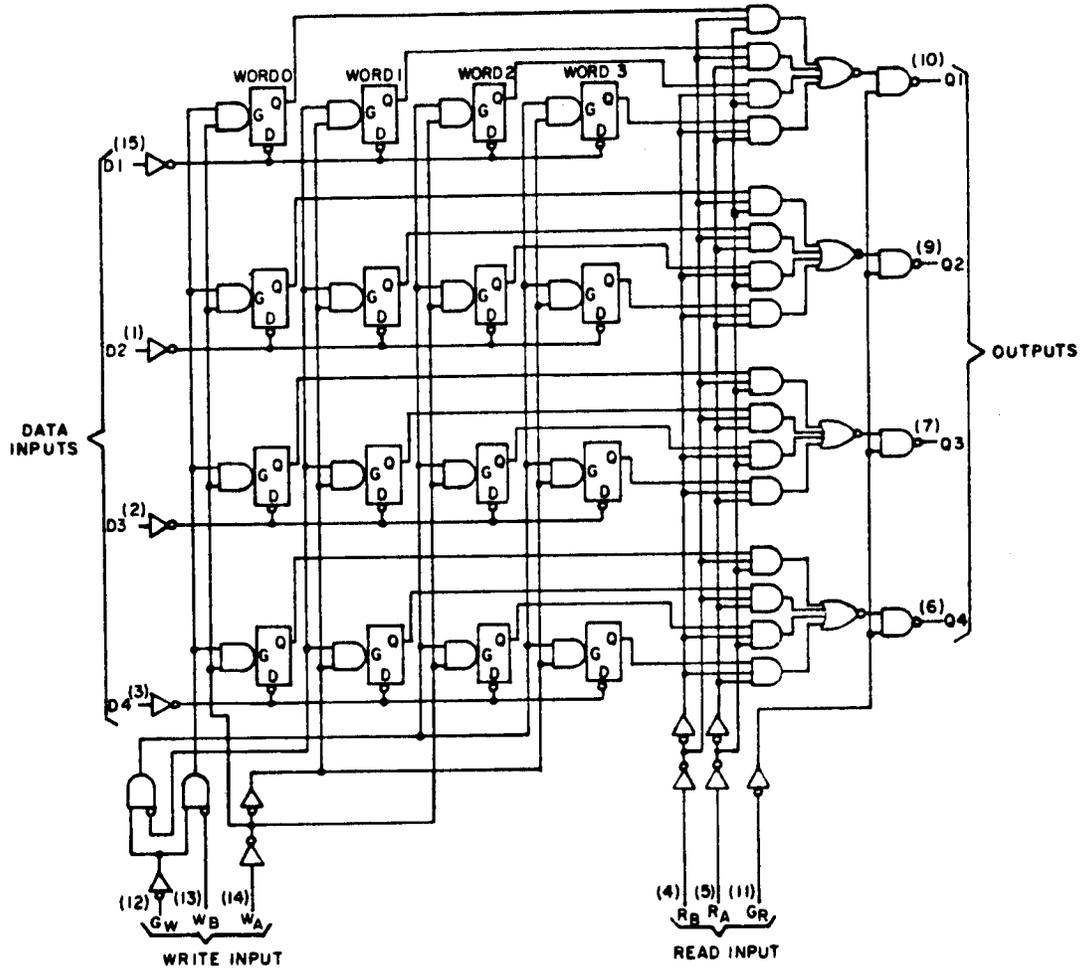


FIGURE 2. Logic diagram.

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
WB	WA	GW	0	1	2	3
L	L	L	Q = D	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>
L	H	L	Q <sub>0</sub>	Q = D	Q <sub>0</sub>	Q <sub>0</sub>
H	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q = D
X	X	H	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>

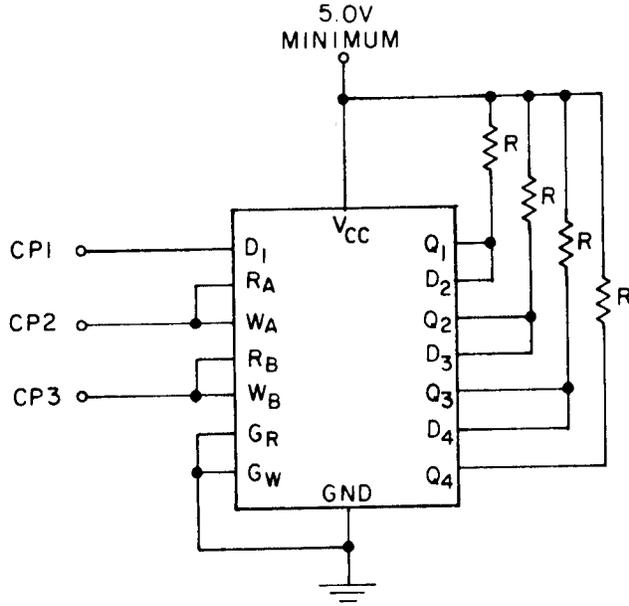
READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
RB	RA	GR	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

## NOTES:

- A. H = high level, L = low level, X = irrelevant.  
 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.  
 C. Q<sub>0</sub> = The level of Q before the indicated input conditions were established.  
 D. W0B1 = The first bit of word 0, etc.

FIGURE 3. Truth tables.



**NOTES:**

1.  $R = 270\Omega \pm 5\%$ .
2. All clock pulse generators have the following characteristics:  $V_{gen} = 3.0 V$  minimum, 50% duty cycle,  $t_{THL}$  and  $t_{TLH} \leq 10 ns$  and frequency as follows.

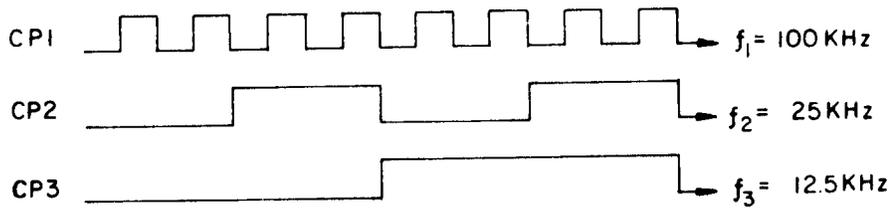
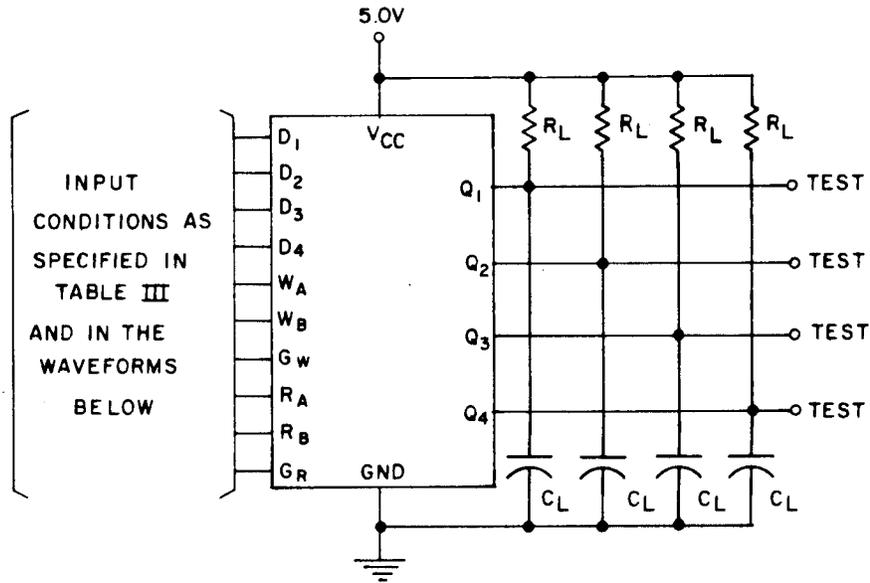
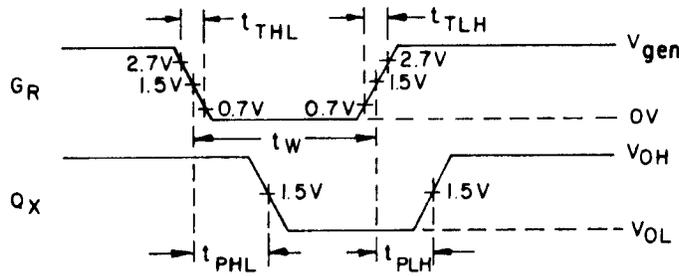


FIGURE 4. Burn-in and life test circuits.



A. READ-ENABLE TO ANY OUTPUT ( $t_{PHLI}$  &  $t_{PLHI}$ )

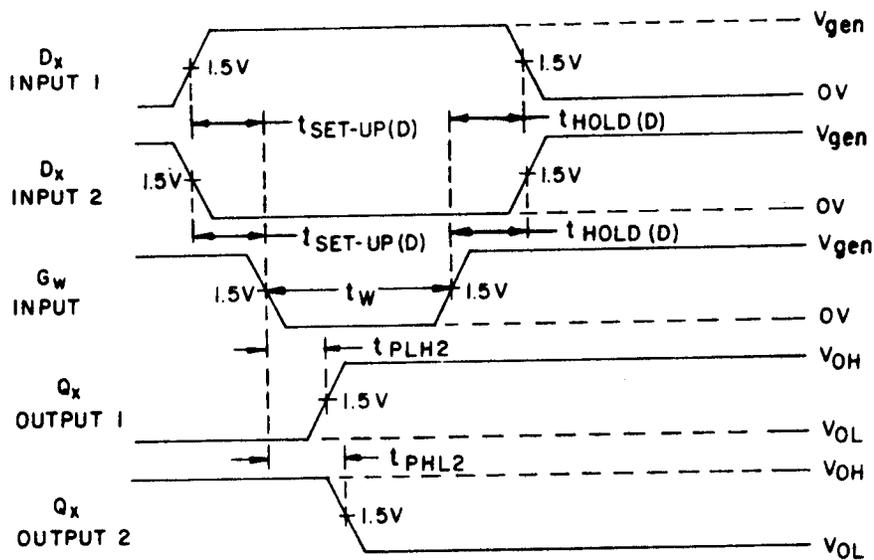


NOTES for A:

1.  $R_L = 400\Omega \pm 5\%$ .
2.  $C_L = 50 \text{ pF} \pm 10\%$ , including probe and jig capacitance.
3. Read enable (GR) pulse characteristics shall be as follows:  $V_{gen} = 3.0 \text{ V}$  minimum,  $t_{THL}$  and  $t_{TLH} \leq 10 \text{ ns}$ ,  $t_W = 25 \text{ ns}$ , and  $PRR = 1 \text{ MHz}$ .

FIGURE 5. Switching circuit and waveforms.

B. WRITE ENABLE TO ANY OUTPUT ( $t_{PLH2}$  AND  $t_{PHL2}$ )

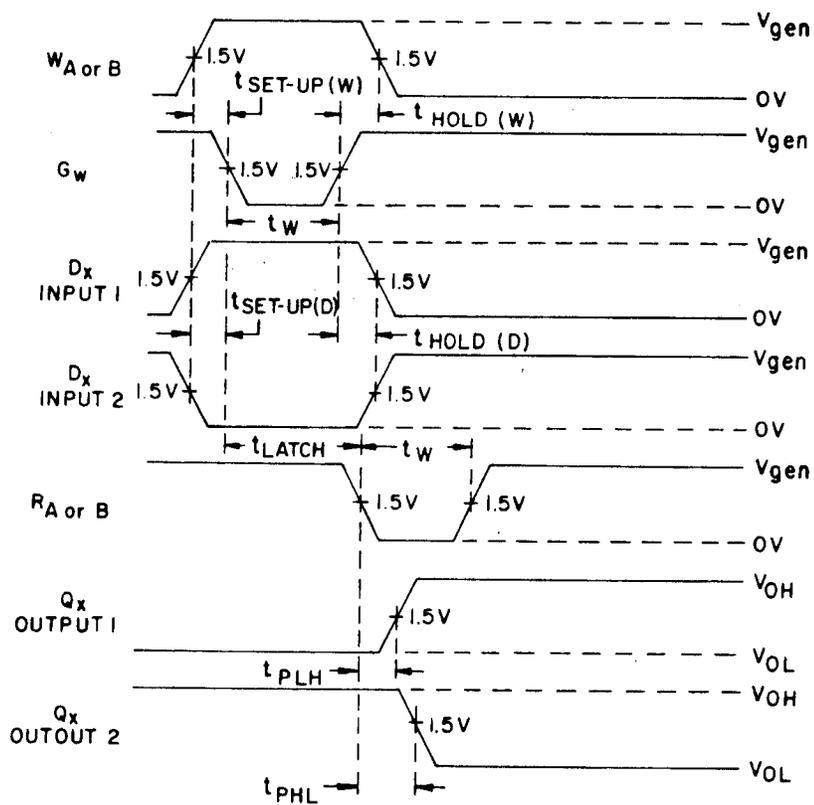


**NOTES for B:**

1. All pulse generators have the following characteristics:  $t_{TLH}$  (0.7 V to 2.7 V) and  $t_{THL}$  (2.7 V to 0.7 V)  $\leq 10$  ns and  $V_{gen} \geq 3.0$  V.
2. PRR for "D" pulse generator shall be 500 kHz. PRR for "GW" pulse generator shall be 1 MHz.
3.  $t_{SETUP(D)} = 10$  ns,  $t_{HOLD(D)} = 15$  ns and  $t_w = 25$  ns.

FIGURE 5. Switching circuit and waveforms - Continued.

C. READ-ADDRESS ( $R_A$  or  $R_B$ ) TO ANY OUTPUT ( $t_{PHL3}$  AND  $t_{PLH3}$ )

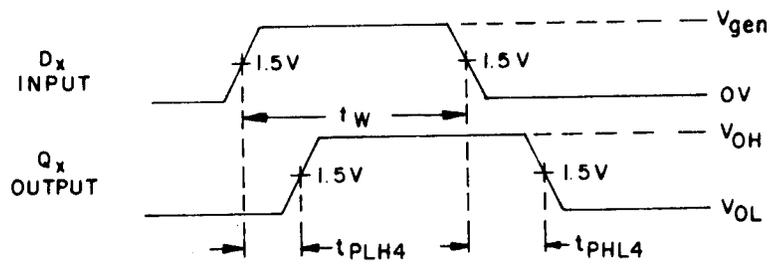


NOTES for C:

1. All pulse generators have the following characteristics:  $t_{TLH}$  (0.7 V to 2.7 V) and  $t_{THL}$  (2.7 V to 0.7 V)  $\leq$  10 ns, and  $V_{gen} \geq$  3.0 V.
2.  $t_{SETUP(W)} = 15$  ns,  $t_{HOLD(W)} = 5$  ns,  $t_{SETUP(D)} = 10$  ns,  $t_{HOLD(D)} = 15$  ns and  $t_w = 25$  ns.
3. PRR = 1 MHz for  $W_A$  or  $B$  and  $G_w$ ; PRR = 500 kHz for  $D_x$  and  $R_A$  or  $B$ .

FIGURE 5. Switching circuit and waveforms - Continued.

D. DATA INPUT TO Q OUTPUT ( $t_{PLH4}$  AND  $t_{PHL4}$ )



**NOTES for D:**

1. Data pulse generator has the following characteristics:  $t_{TLH}$  (0.7 V to 2.7 V) and  $t_{THL}$  (2.7 V to 0.7 V)  $\leq 10$  ns,  $V_{gen} \geq 3.0$  V,  $t_w \leq 100$  ns and PRR = 1 MHz.

FIGURE 5. Switching circuit and waveforms - Continued.

TABLE III. Group A inspection for device type 01.  
Terminal conditions (pins not designated are high level, low level or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
				D2	D3	D4	RB	RA	Q4	Q3	GND	Q2	Q1	GR	GW	WB	WA	D1	VCC	Meas. terminal	Min	Max	Unit	
1 TC = 25°C	VOL	3007	1	0.8 V			0.8 V	0.8 V			GND	16 mA	16 mA	0.8 V	0.4	V								
			2	0.8 V			0.8 V	0.8 V							0.8 V									
			3	0.8 V			0.8 V	0.8 V								0.8 V	0.8 V							
			4	0.8 V			0.8 V	0.8 V								0.8 V	0.8 V							
	ICEX	3008	5	2.0 V			2.0 V	2.0 V					5.5 V	5.5 V	2.0 V	30	μA							
			6	2.0 V			2.0 V	2.0 V							2.0 V									
			7	2.0 V			2.0 V	2.0 V								2.0 V								
			8	2.0 V			2.0 V	2.0 V								2.0 V								
	VIC	3009	9	-12 mA																				
			10	-12 mA																				
			11	-12 mA																				
			12	-12 mA																				
			13	-12 mA																				
			14	-12 mA																				
	I <sub>IL</sub>	3010	15	0.4 V			0.4 V	0.4 V																
			16	0.4 V			0.4 V	0.4 V																
			17	0.4 V			0.4 V	0.4 V																
			18	0.4 V			0.4 V	0.4 V																
19			0.4 V			0.4 V	0.4 V																	
20			0.4 V			0.4 V	0.4 V																	
I <sub>IH1</sub>	3010	21	2.4 V			2.4 V	2.4 V																	
		22	2.4 V			2.4 V	2.4 V																	
		23	2.4 V			2.4 V	2.4 V																	
		24	2.4 V			2.4 V	2.4 V																	
		25	2.4 V			2.4 V	2.4 V																	
		26	2.4 V			2.4 V	2.4 V																	
		27	2.4 V			2.4 V	2.4 V																	
		28	2.4 V			2.4 V	2.4 V																	
I <sub>IH2</sub>	3005	29	5.5 V			5.5 V	5.5 V																	
		30	5.5 V			5.5 V	5.5 V																	
		31	5.5 V			5.5 V	5.5 V																	
		32	5.5 V			5.5 V	5.5 V																	
		33	5.5 V			5.5 V	5.5 V																	
		34	5.5 V			5.5 V	5.5 V																	
		35	5.5 V			5.5 V	5.5 V																	
		36	5.5 V			5.5 V	5.5 V																	
I <sub>CC</sub>	3005	37	4.5 V			4.5 V	4.5 V																	
		38	4.5 V			4.5 V	4.5 V																	
2																								
3																								

Same tests, terminal conditions and limits as subgroup 1, except TC = 125°C and VIC tests are omitted.

Same tests, terminal conditions and limits as subgroup 1, except TC = -55°C and VIC tests are omitted.

TABLE III. Group A inspection for device type 01 - Continued.  
Terminal conditions (pins not designated are high level, low level or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits						
			Test No.	D2																	D3	D4	RB	RA	Q4	Q3	GND
7 TC = 25°C	(Truth table test)		50	0.8 V	L	L	L	GND	L	L	0.8 V	See note at the end of this table															
			51	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	H	H	H	H	H	GND	H	H	0.8 V				0.8 V						
			52	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	H	H	H	H	H	GND	H	H	0.8 V				0.8 V						
			53	0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			54	0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			55	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V					
			56	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V					
			57	2.0 V	0.8 V	0.8 V	0.8 V	0.8 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			58	2.0 V	0.8 V	0.8 V	0.8 V	0.8 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			59	0.8 V	2.0 V	2.0 V	2.0 V	0.8 V	H	H	H	H	H	H	H	H	H	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			60	0.8 V	2.0 V	2.0 V	2.0 V	0.8 V	H	H	H	H	H	H	H	H	H	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			61	0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			62	0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V	
			63	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V					
			64	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V					
			65	0.8 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V					
			66	0.8 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V					
			67	0.8 V	L	L	L	L	L	L	L	L	L	0.8 V	0.8 V	0.8 V	0.8 V				0.8 V	0.8 V					
			68	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V					
69	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	H	H	H	H	H	H	H	H	H	2.0 V												
8	Repeat subgroup 7 at TC = 125°C and TC = -55°C.																										
9 TC = 25°C	t <sub>PLH1</sub>	3003 (Fig 5)	70	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	GR to Q1	5	15	ns		
			71	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	GR to Q2	5	15	ns	
			72	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	GR to Q3	5	15	ns	
			73	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	GR to Q4	5	15	ns	
			74	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	CR to Q1	5	30	ns	
			75	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	CR to Q2	5	30	ns	
			76	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	CR to Q3	5	30	ns	
			77	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	GND	GND	5.0 V	CR to Q4	5	30	ns	
			78	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q1	5	40	ns
			79	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q2	5	40	ns
			80	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q3	5	40	ns
			81	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q4	5	40	ns
			82	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q1	5	40	ns
83	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q2	5	40	ns			
84	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q3	5	40	ns			
85	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q4	5	40	ns			
86	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q1	5	40	ns			
87	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q2	5	40	ns			
88	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q3	5	40	ns			
89	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q4	5	40	ns			
90	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q1	5	40	ns			
91	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q2	5	40	ns			
92	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q3	5	40	ns			
93	GND	IN1	IN1	IN1	IN1	IN1	IN1	IN1	OUT	OUT	OUT	OUT	OUT	OUT	IN	GND	GND	IN1	IN1	5.0 V	CW to Q4	5	40	ns			

TABLE III. Group A inspection for device type 01 - Continued.  
Terminal conditions (pins not designated are high level, low level or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits								
				D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	RB	RA	Q <sub>4</sub>	Q <sub>3</sub>	GND	Q <sub>2</sub>	Q <sub>1</sub>	GR	GW	WB	WA	D <sub>1</sub>	VCC	Meas. terminal	Min	Max	Unit					
9 T <sub>C</sub> = 25°C	t <sub>PHL2</sub>	3003 (Fig 5)	94	IN2	IN2	IN2	GND	GND	OUT	OUT	GND	OUT	OUT	OUT	GND	IN	GND	GND	IN2	5.0 V	5	45	ns					
			95	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	GND	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			96	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			97	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			98	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			99	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			100	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			101	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			102	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			103	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
10 T <sub>C</sub> = 125°C	t <sub>PLH3</sub>		104	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2										
			105	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2										
			106	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2										
			107	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			108	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			109	IN2	IN2	IN2	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0 V	IN	5.0 V	IN2									
			110	IN1	IN1	IN1	GND	GND	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	IN	IN	IN	IN1								
			111	IN1	IN1	IN1	GND	GND	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	IN	IN	IN	IN1								
			112	IN1	IN1	IN1	GND	GND	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	IN	IN	IN	IN1								
			113	IN1	IN1	IN1	GND	GND	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	OUT1	IN	IN	IN	IN1								
	t <sub>PHL3</sub>		114	IN2	IN2	IN2	IN	GND	OUT2	OUT2	OUT2	OUT2	OUT2	OUT2	GND	GND	IN	GND	IN2									
			115	IN2	IN2	IN2	IN	GND	OUT2	OUT2	OUT2	OUT2	OUT2	OUT2	GND	GND	IN	GND	IN2									
			116	IN2	IN2	IN2	IN	GND	OUT2	OUT2	OUT2	OUT2	OUT2	OUT2	GND	GND	IN	GND	IN2									
			117	IN2	IN2	IN2	IN	GND	OUT2	OUT2	OUT2	OUT2	OUT2	OUT2	GND	GND	IN	GND	IN2									
			118	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
			119	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
			120	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
			121	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
			122	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
			123	IN	IN	IN	GND	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN								
	t <sub>PLH4</sub>		124	IN	IN	IN	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN									
			125	IN	IN	IN	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN									
			126	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			127	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			128	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			129	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			130	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			131	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			132	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
			133	GND	GND	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	GND	GND	IN								
	t <sub>PHL1</sub>		134	IN1	IN1	IN1	GND	GND	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN1										
			135	IN1	IN1	IN1	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN1									
			136	IN1	IN1	IN1	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN1									
			137	IN1	IN1	IN1	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	GND	GND	IN	IN	IN1									

TABLE III. Group A inspection for device type 01 - Continued.  
Terminal conditions (pins not designated are high level, low level or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits						
				D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	R <sub>B</sub>	R <sub>A</sub>	Q <sub>4</sub>	Q <sub>3</sub>	GND	Q <sub>2</sub>	Q <sub>1</sub>	GR	GW	W <sub>B</sub>	W <sub>A</sub>	D <sub>1</sub>	VCC	Meas. terminal	Min	Max	Unit			
10 T <sub>C</sub> = 125°C	t <sub>PLH2</sub>	3003 (Fig 5)	138	IN1	IN1		GND	5.0 V				GND	OUT	OUT	GND	IN	GND	5.0 V	IN1	5.0 V	5	48	ns			
			139	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V			IN1							
			140	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			141	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			142	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			143	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			144	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			145	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			146	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			147	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			148	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			149	IN1	IN1	IN1	5.0 V	GND	OUT					OUT	OUT	5.0 V				IN1						
			150	IN2	IN2	IN2	GND	GND	OUT					OUT	OUT	OUT				IN2						
			151	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
			152	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
			153	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
			154	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
			155	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
			156	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2						
157	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
158	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
159	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
160	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
161	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
162	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
163	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
164	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
165	IN2	IN2	IN2	5.0 V	OUT	OUT					OUT	OUT	OUT				IN2									
166	IN1	IN1	IN1	GND	IN	OUT1					OUT1	OUT1	OUT1				IN1									
167	IN1	IN1	IN1	GND	IN	OUT1					OUT1	OUT1	OUT1				IN1									
168	IN1	IN1	IN1	GND	IN	OUT1					OUT1	OUT1	OUT1				IN1									
169	IN1	IN1	IN1	GND	IN	OUT1					OUT1	OUT1	OUT1				IN1									
170	IN2	IN2	IN2	IN	IN2	OUT2					OUT2	OUT2	OUT2				IN2									
171	IN2	IN2	IN2	IN	IN2	OUT2					OUT2	OUT2	OUT2				IN2									
172	IN2	IN2	IN2	IN	IN2	OUT2					OUT2	OUT2	OUT2				IN2									
173	IN2	IN2	IN2	IN	IN2	OUT2					OUT2	OUT2	OUT2				IN2									
174	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
175	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
176	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
177	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
178	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
179	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
180	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
181	IN	IN	IN	GND	IN	OUT					OUT	OUT	OUT				IN									
11				Same tests, terminal conditions and limits as subgroup 10, except T <sub>C</sub> = -55°C.																						

NOTE: Output voltages shall be either:  
(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or  
(b) H ≥ 1.0 volt and L < 1.0 volt when using a high speed checker single comparator.

c. Steady-state life test (method 1005 of MIL-STD-883) conditions:

- (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
- (2)  $T_A = +125^\circ\text{C}$  minimum.
- (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging of microcircuits shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity, if applicable.
- e. Requirements for packaging and packing.
- f. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal)
I <sub>IN</sub>	- - - - -	Current flowing into an input terminal
T <sub>C</sub>	- - - - -	Case temperature
V <sub>IN</sub>	- - - - -	Voltage level at an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54170

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:  
 Army - ER  
 Navy - EC  
 Air Force - 17

Preparing activity:  
 Air Force - 17  
 (Project 5962-0591-1)

Review activities:  
 Army - AR, MI  
 Navy - OS, SH  
 Air Force - 11, 19, 85, 99  
 DLA - ES

User activities:  
 Army - SM  
 Navy - AS, CG, MC

Agent:  
 DLA - ES