

MILITARY SPECIFICATION

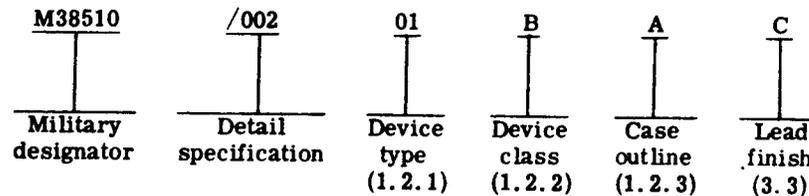
MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. Device type shall be as shown in the following:

Device type	Circuit
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline, MIL-M-38510, appendix C
A	F-1 (14-pin, 1/4" x 1/4", flat pack)
B	F-3 (14-pin, 1/8" x 1/4", flat pack)
C	D-1 (14-pin, 1/4" x 3/4", dual-in-line)
D	F-2 (14-pin, 1/4" x 3/8", flat pack)
E	D-2 (16-pin, 1/4" x 7/8", dual-in-line)
F	F-5 (16-pin, 1/4" x 3/8", flat pack)

1.2.4 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 to 7.0 Vdc
Input voltage range - - - - -	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range - - - - -	-65° C to 150° C
Maximum power dissipation per flip-flop, P _D - - - - -	110 mW ^{1/}
Lead temperature (soldering, 10 seconds) - - - - -	300° C
Thermal resistance, junction to case - -	$\theta_{JC} = \begin{cases} 0.09^\circ \text{C/mW} & \text{for flat packs} \\ 0.08^\circ \text{C/mW} & \text{for dual-in-line pack} \end{cases}$
Junction temperature - - - - -	T _J = 175° C

^{1/} Must withstand the added P_D due to short circuit condition (e.g. IOS) at one output for 5 seconds duration.

1.2.5 Recommended operating conditions.

Supply voltage	-----	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	-----	2.0 Vdc
Maximum low level input voltage	-----	0.8 Vdc
Normalized fanout (each output) ^{1/}	-----	10 maximum
Ambient operating temperature range	-----	-55° C to 125° C
Input set up time		
Device type		
01, 02, 03, 04	-----	> clock pulse width
05, 06, 07	-----	20 ns minimum
Input hold time		
Device type		
01, 02, 03, 04,	-----	0
05, 06, 07	-----	5 ns minimum

2. APPLICABLE DOCUMENT

2.1 The following document, of the issue in effect on date of invitation for bids or request for proposal, forms a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. In the event of conflict between MIL-M-38510 and this detail specification, this detail specification shall govern.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Logic diagram and terminal connections. The logic diagram and terminal connections shall be as specified on figure 1.

3.2.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.

3.2.3 Schematic circuit. The schematic circuit shall be as specified on figure 3.

3.2.4 Case outlines. Case outlines shall be as specified in MIL-M-38510 and in 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

^{1/} Device will fanout in both high and low levels to the specified number of I_{IL1}/I_{IH1} inputs of the same device type as that being tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{9/}	Device type	Limits		Units
				Min	Max	
High-level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -400 μA	All	2.4	---	Volts
Low-level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 16 mA	All		0.4	Volts
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{OL} = -12 mA T _A = 25° C	All		-1.5	Volts
Low-level input current	I _{IL1}	V _{CC} = 5.5 V V _{IN} = 0.4 V <u>1/</u>	01, 02, 03, 04, 05, 06	-0.7	-1.6	mA
			07	-0.5	-1.6	mA
Low-level input current	I _{IL2}	V _{CC} = 5.5 V V _{IN} = 0.4 V <u>2/</u>	01, 02, 03, 04, 05	-1.4	-3.2	mA
			07	-1.0	-3.2	mA
Low-level input current	I _{IL3}	V _{CC} = 5.5 V V _{IN} = 0.4 V <u>6/</u>	01, 02, 03, 04	-0.7	-3.2	mA
High-level input current	I _{IH1}	V _{CC} = 5.5 V V _{IN} = 2.4 V <u>5/</u>	All	0	40	μA
High-level input current	I _{IH2}	V _{CC} = 5.5 V V _{IN} = 5.5 V <u>5/</u>	All	0	100	μA
High-level input current	I _{IH3}	V _{CC} = 5.5 V V _{IN} = 2.4 V <u>3/</u>	All	0	80	μA
High-level input current	I _{IH4}	V _{CC} = 5.5 V V _{IN} = 5.5 V <u>3/ 7/</u>	All	0	200	μA
High-level input current	I _{IH5}	V _{CC} = 5.5 V V _{IN} = 2.4 V <u>7/ 8/</u>	01, 02, 03, 04, 05, 07	-850	-50	μA
				0	120	μA
High-level input current	I _{IH6}	V _{CC} = 5.5 V V _{IN} = 5.5 V <u>8/</u>	05, 07	0	300	μA
Short-circuit output current	I _{OS}	V _{CC} = 5.5 V V _{IN} = 0 <u>4/</u>	All	-20	-57	mA
Supply current per device	I _{CC}	V _{CC} = 5.5 V V _{IN} = 5 V	01		20	mA
			02, 03, 04, 05, 06, 07		40	
					30	
Maximum clock frequency	f _{MAX}		01, 02, 03, 04, 05, 07	5		MHz
Propagation delay to high logic level (clear or preset to output)	t _{PLH}		06	7.5		
			01, 02, 03, 04, 05	5	39	ns
			06	5	62	
Propagation delay to low logic level (clear or preset to output)	t _{PHL}	V _{CC} = 5 V CL = 50 pF minimum RL = 390 Ω ± 5%	01, 02, 03, 04, 05	5	50	ns
			06	5	62	
			07	5	39	
Propagation delay to high logic level (clock to output)	t _{PLH}		06	5	62	ns
			01, 02, 03, 04, 05	5	39	
			07	5	31	
Propagation delay to low logic level (clock to output)	t _{PHL}		06	5	62	ns
			01, 02, 03, 04, 05	5	50	
			07	5	39	

1/ Input condition - J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.

2/ Input condition - Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.

3/ Input condition - Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.

4/ Nor more than one output should be shorted at a time.

5/ Input condition - J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.

6/ Input condition - Clear or preset for device types 01, 02, 03 and 04.

7/ Input condition - Clock for device types 01, 02, 03, and 04.

8/ Input condition - Clear for device types 05 and 07.

9/ See table III for complete terminal conditions.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II. (Subgroups 7 and 8 testing requires only a summary of attributes data.)

TABLE II. Electrical test requirements.

MIL-STD-883 Test requirements	Subgroups (see table III)		
	Class A devices	Class B devices	Class C devices
Interim electrical parameters (Pre Burn-In) (Method 5004)	1	1	Not reqd
Final electrical test parameters (Method 5004)	1*, 2, 3, 7, 8, 9	1*, 2, 3, 7, 9	1, 7
Group A test requirements (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9	1, 2, 3, 7, 9
Group C end point electrical parameters (Method 5005)	1, 2, 3	1, 2, 3	1
Additional electrical subgroups for Group C periodic inspections	None	10, 11	None

* PDA applies to subgroup 1 (see 4.3(h)).

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container:

(a) Country of origin.

4. PRODUCT ASSURANCE PROVISIONS.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and Method 5005 of MIL-STD-883 except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, and C inspections (see 4.4.1, 4.4.2, and 4.4.3). After qualification of one or more electrically and structurally similar types with a single lead finish, other lead finishes of the same case outline may be qualified by submitting a single type in the qualified case outline to the group B, subgroup 3 test and the group C, subgroup 1, 3, and 4 test.

4.3 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- (a) Test samples for the group B bond strength test specified in Method 5005 of MIL-STD-883 may, at the manufacturer's option, be randomly selected immediately following the internal visual (precap) inspection and prior to sealing (see 4.4.2(b)).
- (b) Temperature cycling (Method 1010 of MIL-STD-883).
 - (1) Omit seal test as post-test measurement.
- (c) Thermal shock (Method 1011 of MIL-STD-883), when substituted for temperature cycling.
 - (1) Omit seal test as post-test measurement.
- (d) Burn-in test (Method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^\circ \text{C}$ minimum.
- (e) Reverse bias burn-in and interim electrical test in accordance with 3.1.10 of Method 5004 of MIL-STD-883 may be omitted.
- (f) Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- (g) External visual inspection shall not include measurement of case and lead dimensions.
- (h) Percent defective allowable (PDA) - The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of Group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of Method 5005 of MIL-STD-883 and as follows:

- (a) Tests shall be as specified in table II.
- (b) Subgroups 4, 5, 6, 7, and 8 of table I of Method 5005 of MIL-STD-883 shall be omitted.

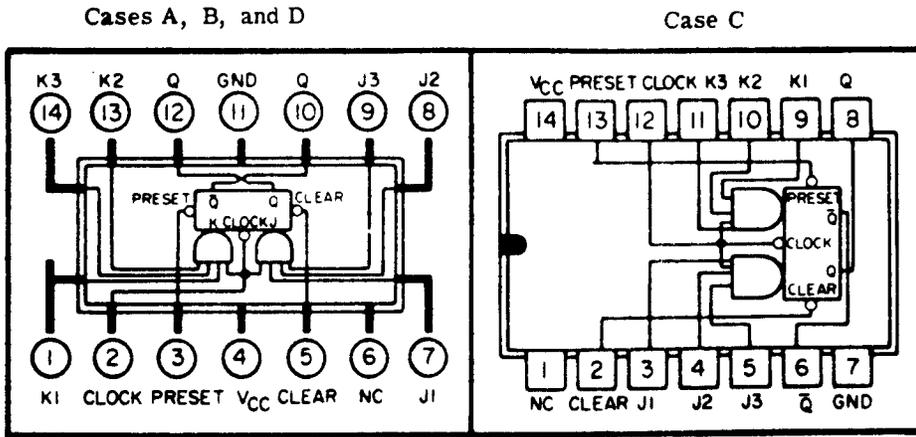
4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of Method 5005 of MIL-STD-883 and as follows:

- (a) Bond strength test may be conducted on samples collected prior to sealing (see 4.3(a)).

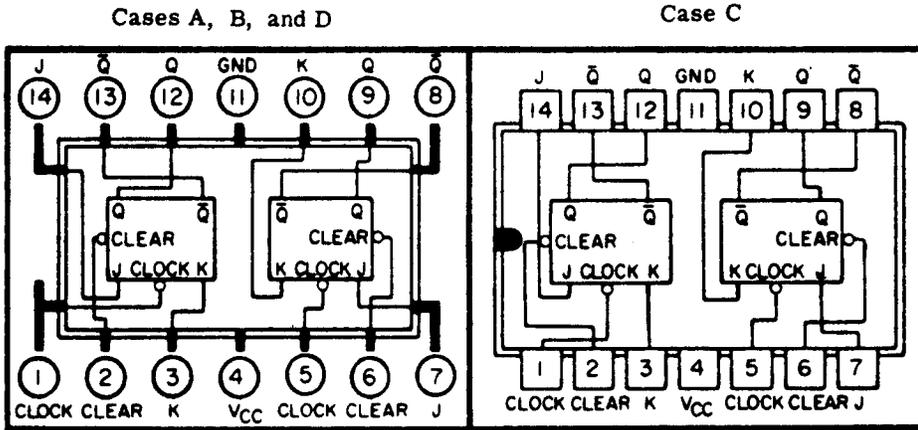
4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of Method 5005 of MIL-STD-883 and as follows:

- (a) End point electrical parameters shall be as specified in table II.
- (b) Subgroups 7 and 8 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.

Device type 01



Device type 02



Device type 03

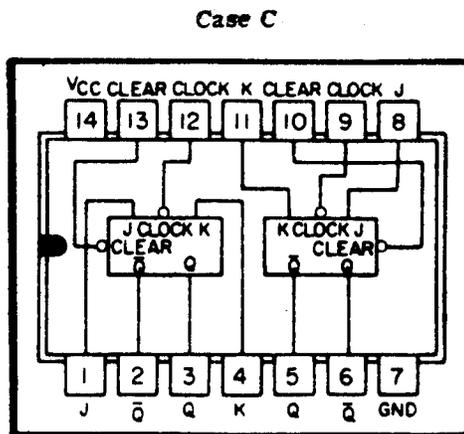
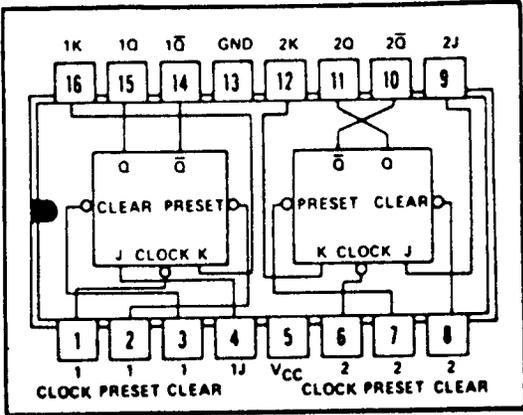


FIGURE 1. Logic diagram and terminal connections.

Device type 04

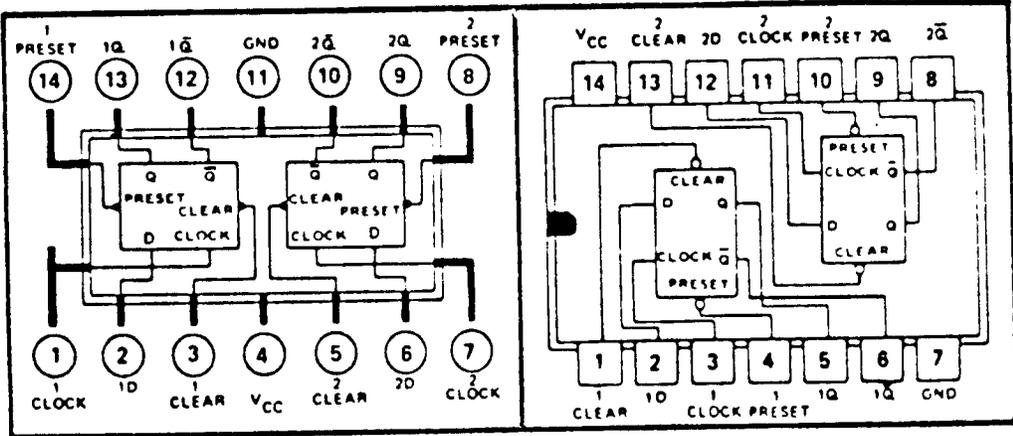
Cases E and F



Cases A, B, and D

Device types 05 and 07

Case C



Cases A, B, and D

Device type 06

Case C

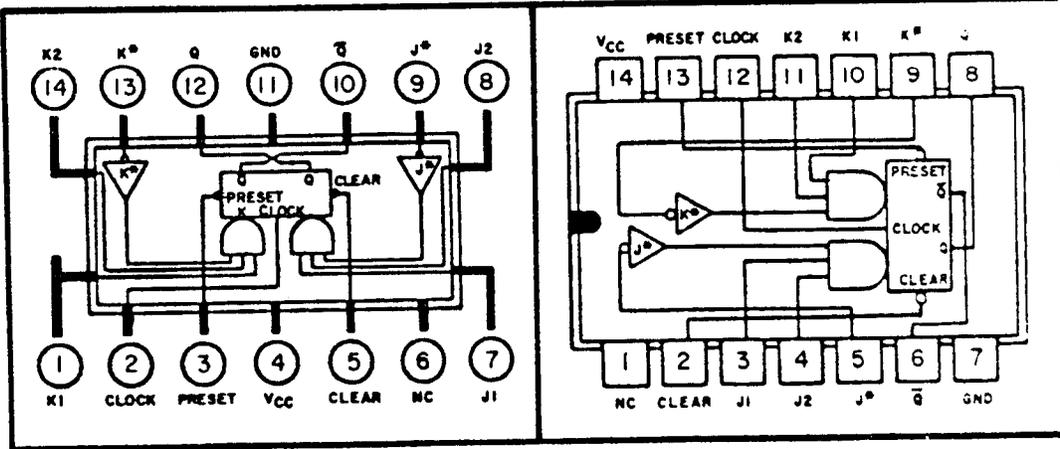


FIGURE 1. Logic diagram and terminal connections - Continued.

Device type 01

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\bar{Q}_n

Positive logic: Low input to preset sets Q to high-level
 Low input to clear sets Q to low-level
 Preset and clear are independent of clock and dominate
 regardless of the state of clock or J or K inputs.

- NOTES: 1. $J = J_1 \cdot J_2 \cdot J_3$
 2. $K = K_1 \cdot K_2 \cdot K_3$
 3. t_n = Bit time before clock pulse.
 4. t_{n+1} = Bit time after clock pulse.

Device types 02 and 03

Truth table each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\bar{Q}_n

Positive logic: Low input to clear sets Q to low-level
 Clear is independent of clock and dominate
 regardless of the state of clock or J or K inputs.

- NOTES: 1. t_n = Bit time before clock pulse.
 2. t_{n+1} = Bit time after clock pulse.

FIGURE 2. Truth tables.

Device type 04

Truth table each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\bar{Q}_n

Positive logic: Low input to preset sets Q to high-level.
 Low input to clear sets Q to low-level.
 Preset and clear are independent of clock and dominate
 regardless of the state of clock or J or K inputs.

- NOTES: 1. t_n = Bit time before clock pulse.
 2. t_{n+1} = Bit time after clock pulse.

Device types 05 and 07

Truth table each flip-flop		
t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT \bar{Q}
L	L	H
H	H	L

Positive logic: Low input to preset sets Q to high-level.
 Low input to clear sets Q to low-level.
 Clear and preset are independent of clock and dominate
 regardless of the state of clock or D input.

- NOTES: 1. t_n = Bit time before clock pulse.
 2. t_{n+1} = Bit time after clock pulse.

FIGURE 2. Truth tables - Continued.

Device type 06

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\bar{Q}_n

Positive logic: Low input to preset sets Q to high-level.
 Low input to clear sets Q to low-level.
 Preset or clear function can occur only
 when clock input is low.

- NOTES: 1. $J = J1 \cdot J2 \cdot \bar{J}^*$
 2. $K = K1 \cdot K2 \cdot \bar{K}^*$
 3. t_n = Bit time before clock pulse.
 4. t_{n+1} = Bit time after clock pulse.
 5. If inputs J^* or K^* are not used they must be grounded.

FIGURE 2. Truth tables - Continued.

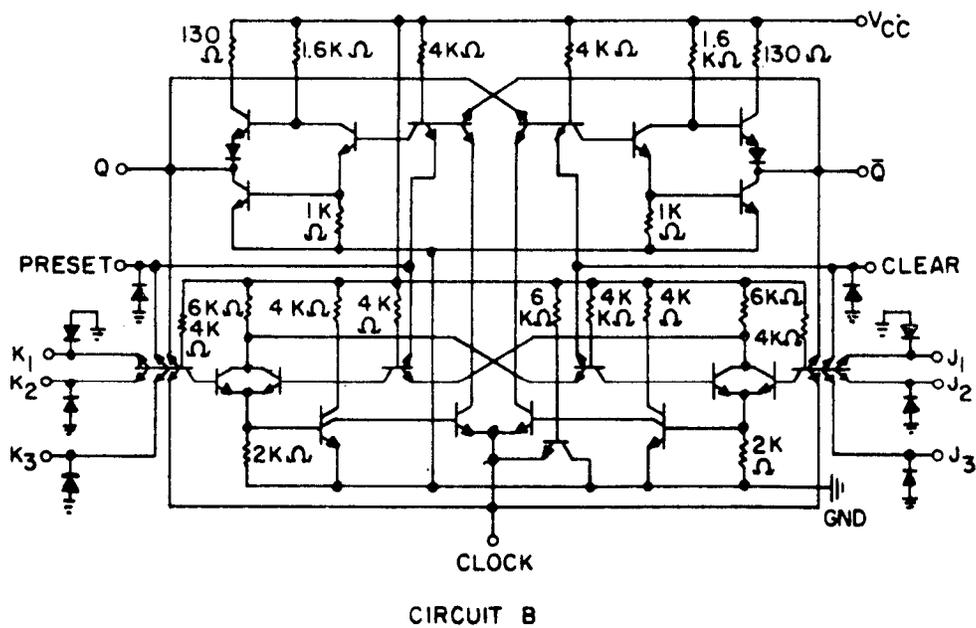
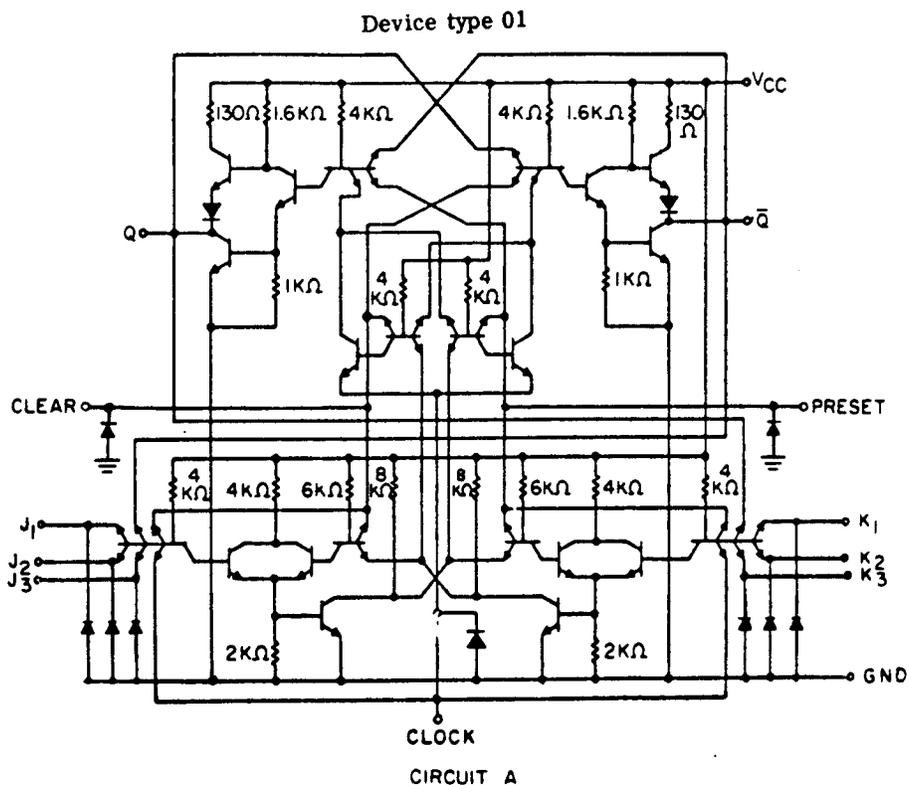
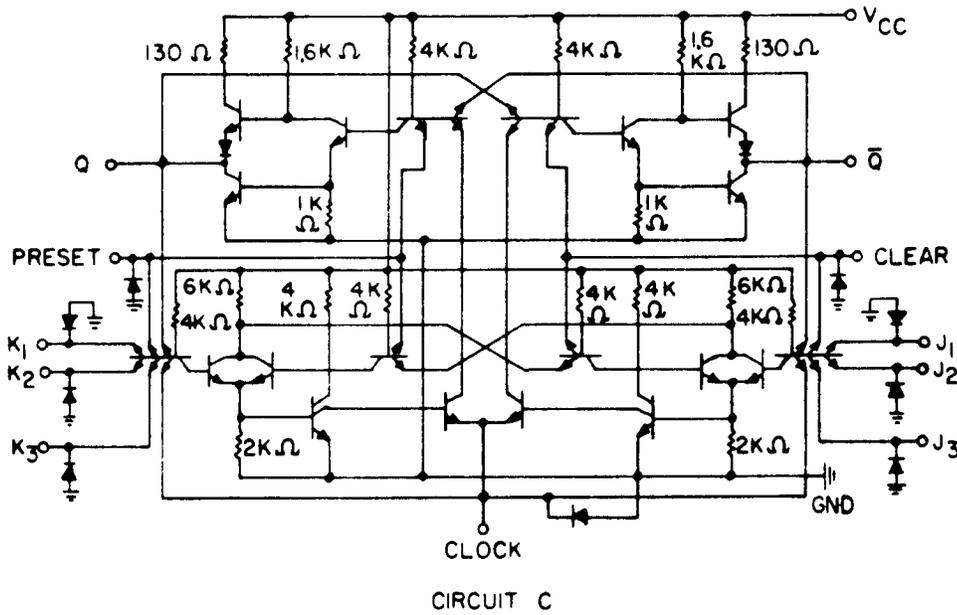


FIGURE 3. Schematic circuits.

Device type 01 - Continued.

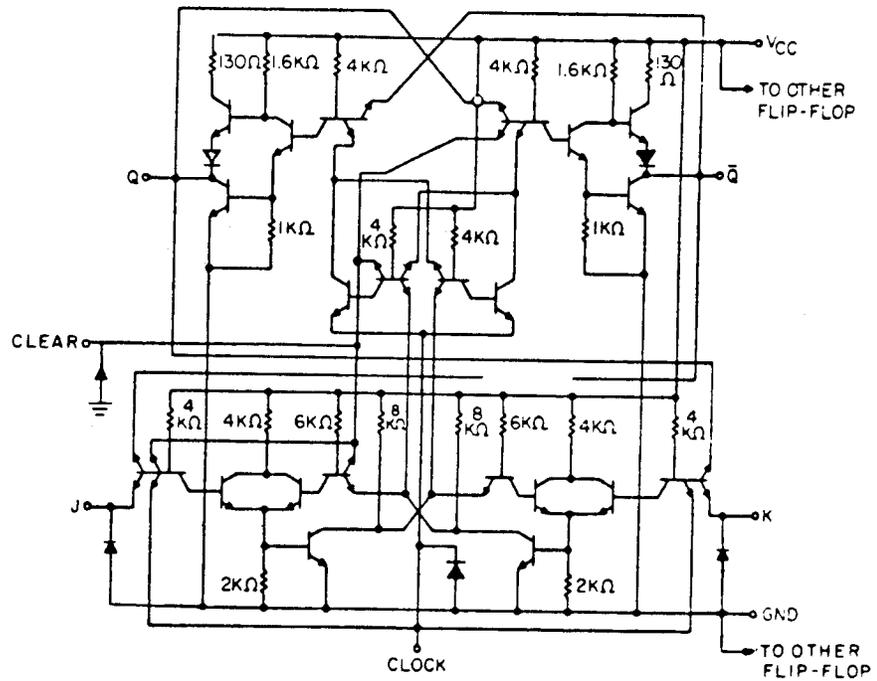


NOTES:

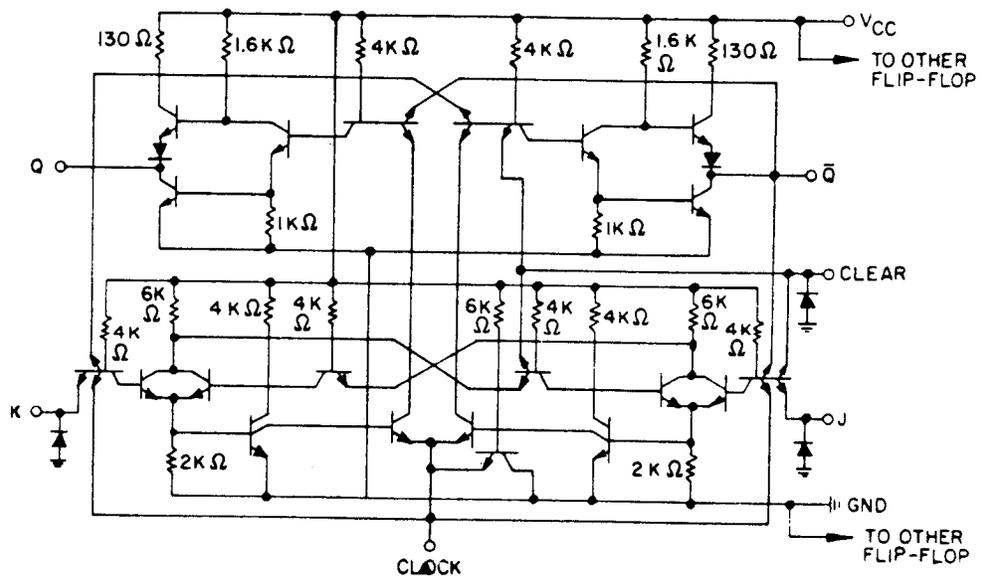
1. Circuits A, B and C are the only acceptable variations for device type 01.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

Device types 02 and 03



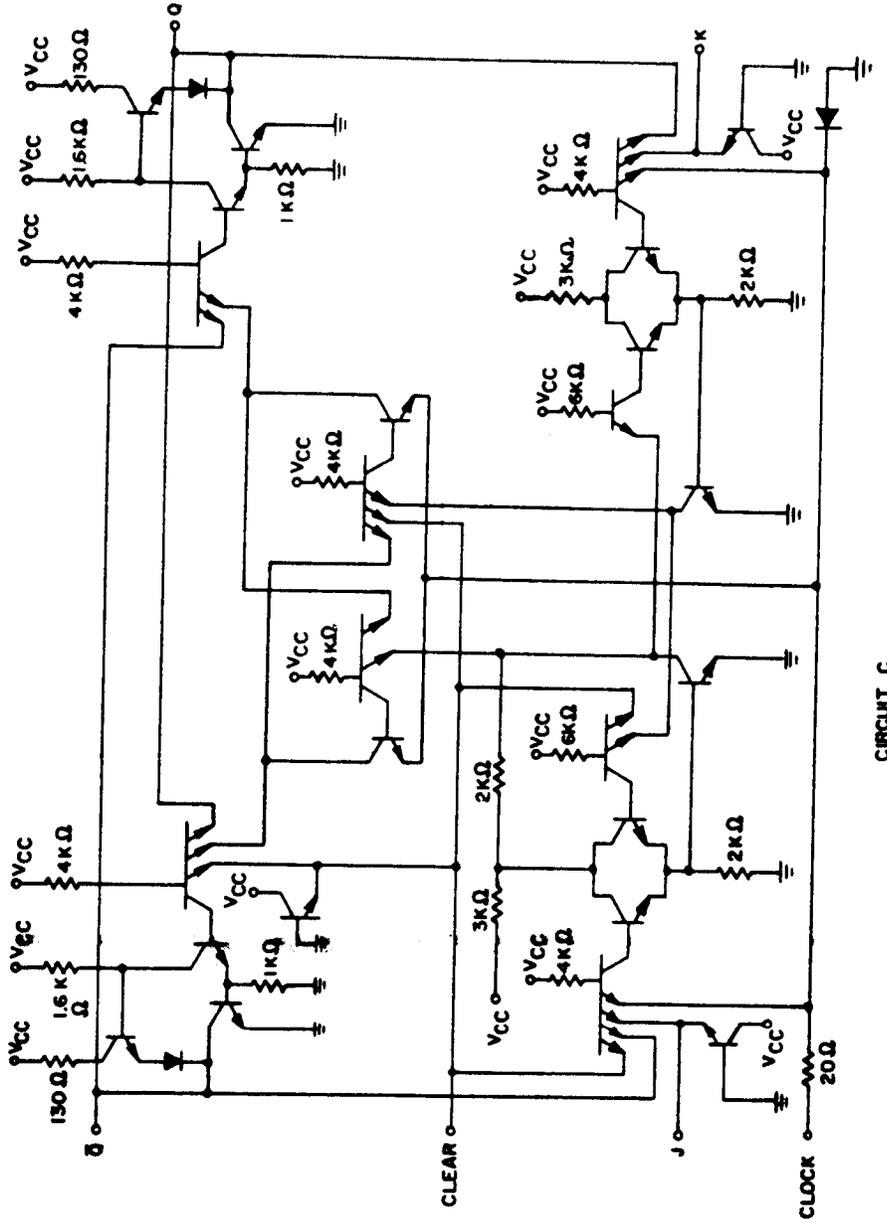
CIRCUIT A



CIRCUIT B

FIGURE 3. Schematic circuits - Continued.

Device types 02 and 03



CIRCUIT C

- NOTES:
1. Circuits A, B and C are the only acceptable variations for device types 02 and 03.
 2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

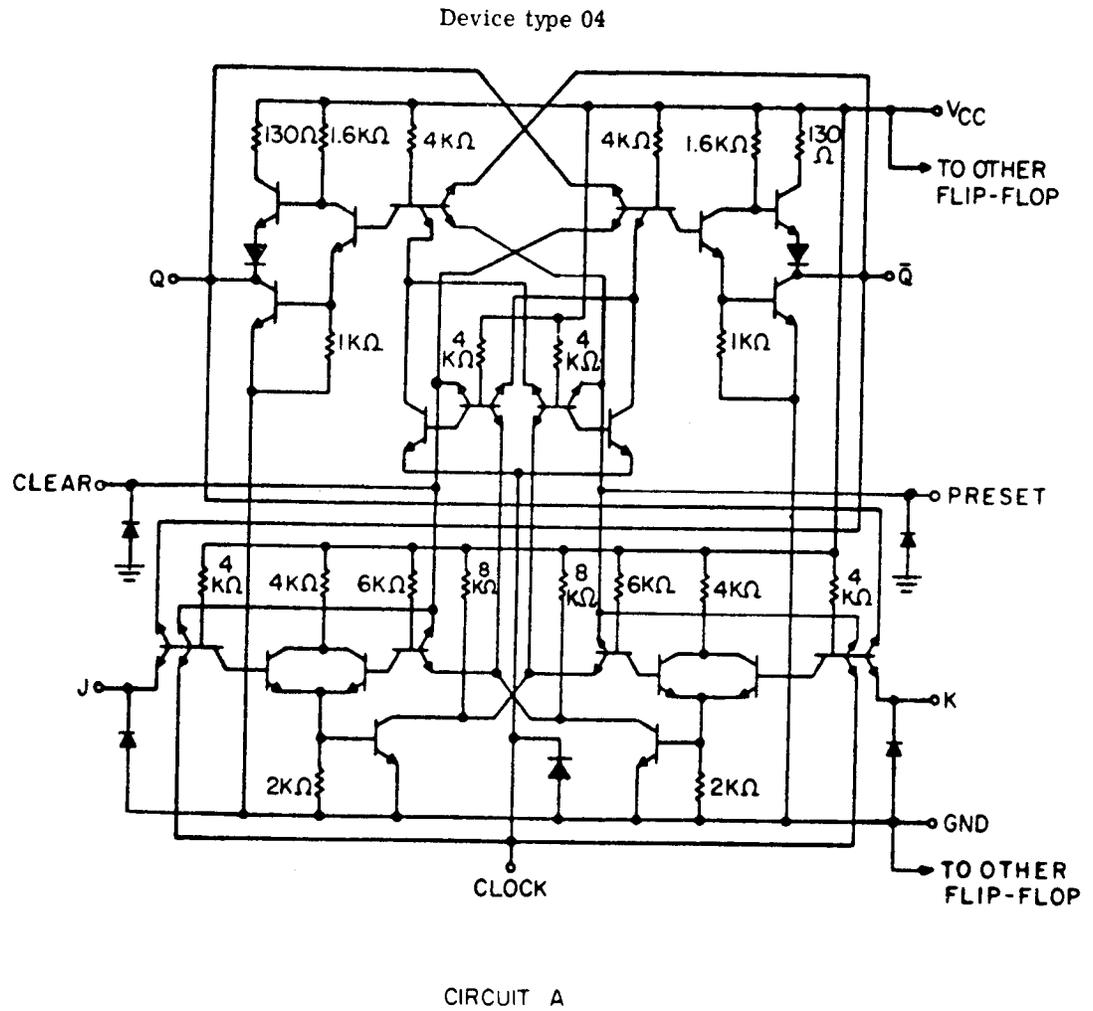


FIGURE 3. Schematic circuits - Continued.

Device type 04 - Continued.

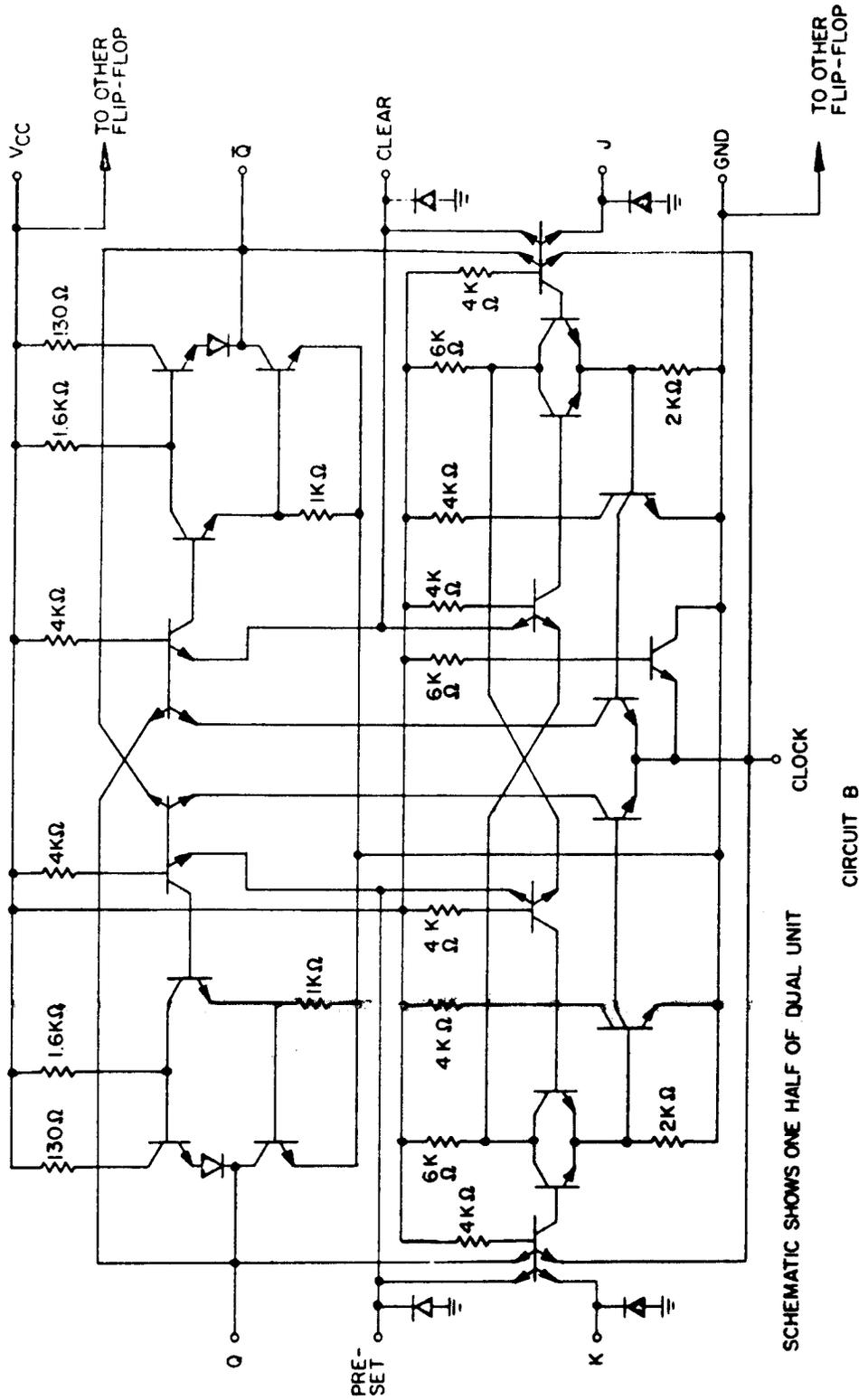
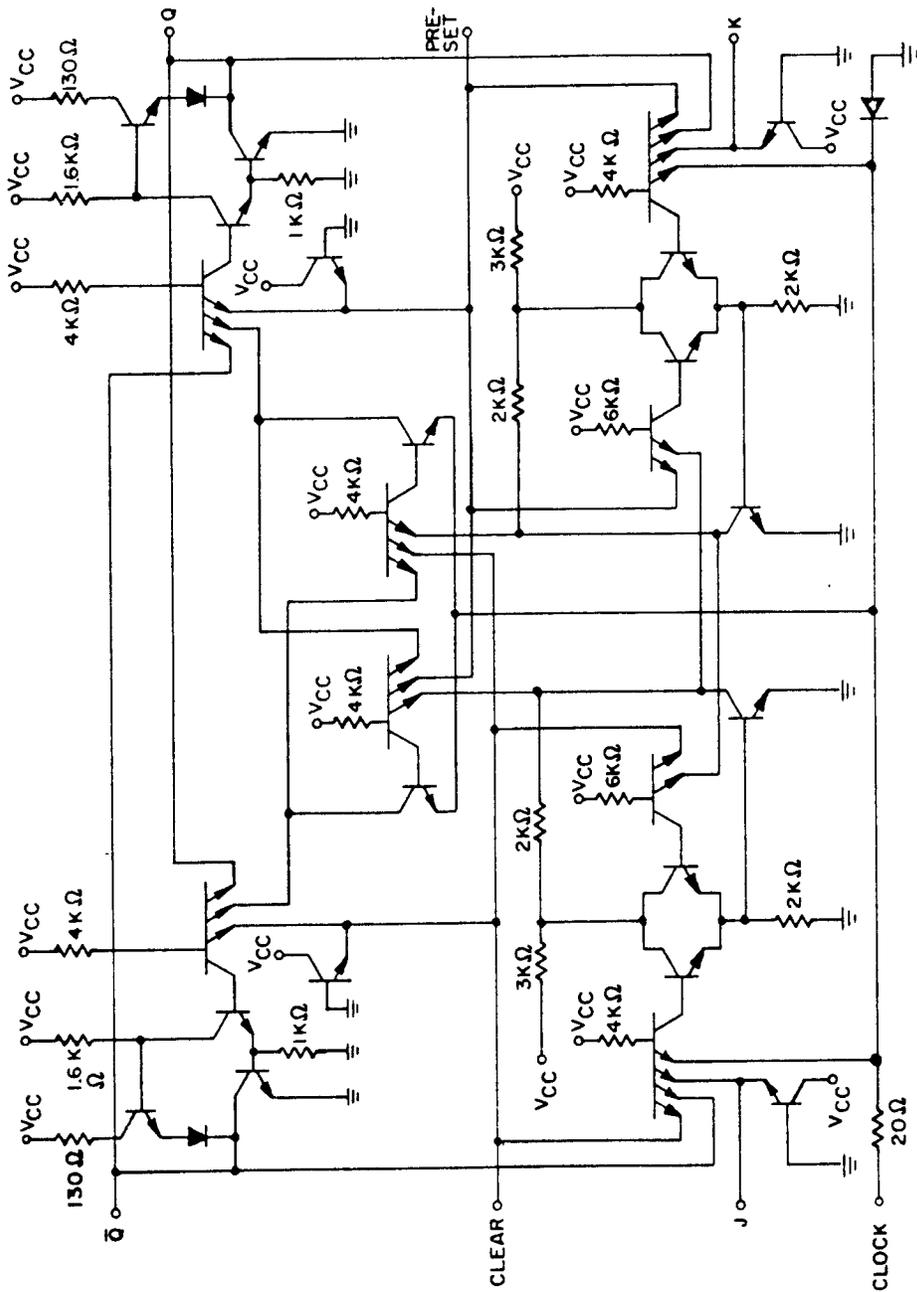


FIGURE 3. Schematic circuits - Continued.

Device type 04 - Continued.

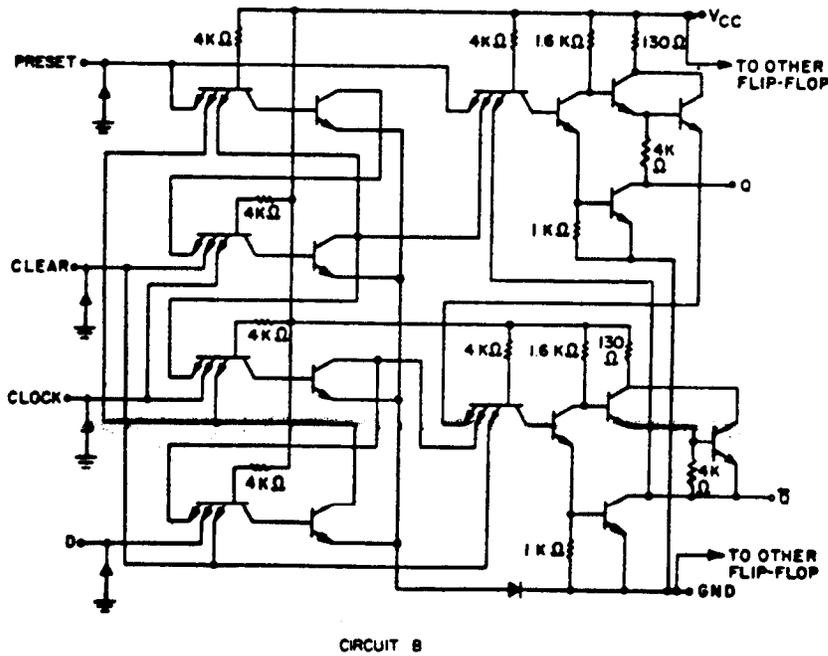
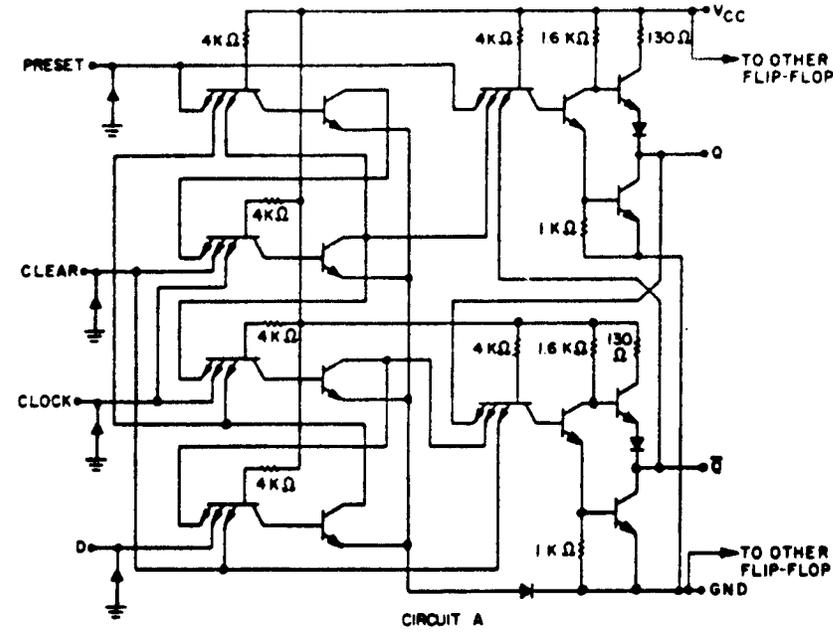


CIRCUIT C

- NOTES:
1. Circuits A, B and C are the only acceptable variations for device type 04.
 2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

Device type 05

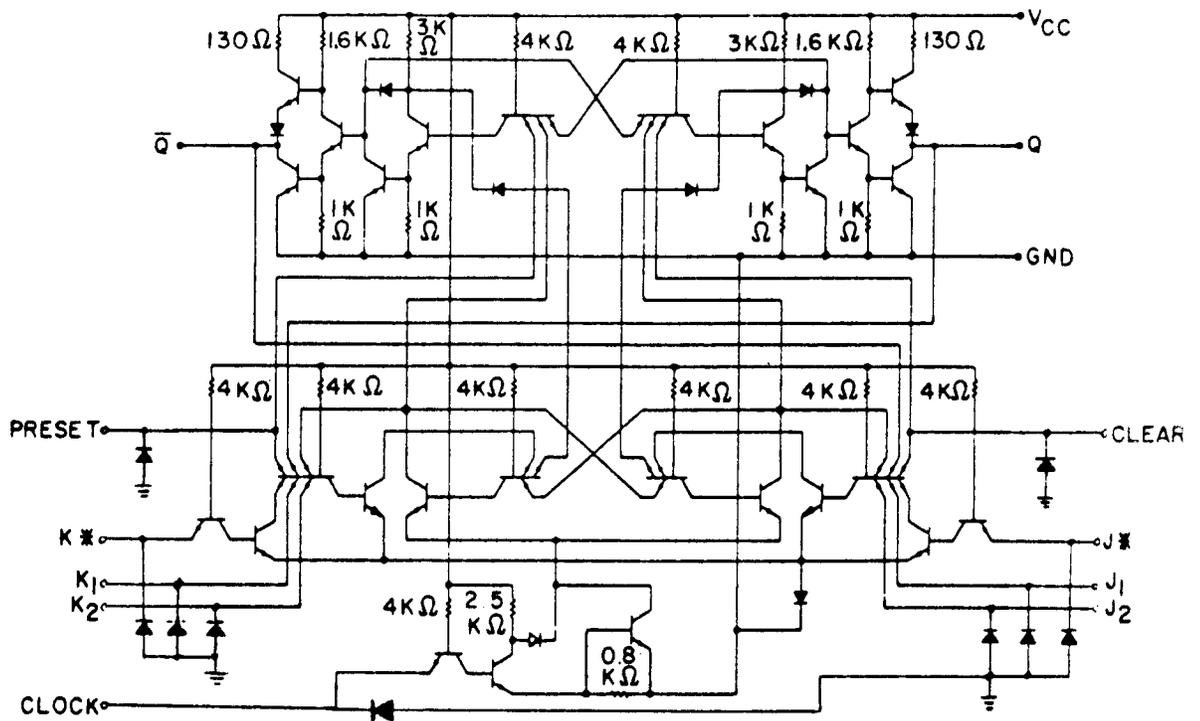


NOTES:

1. Circuits A and B are the only acceptable variations for device type 05.
2. All resistance values shown are nominal.

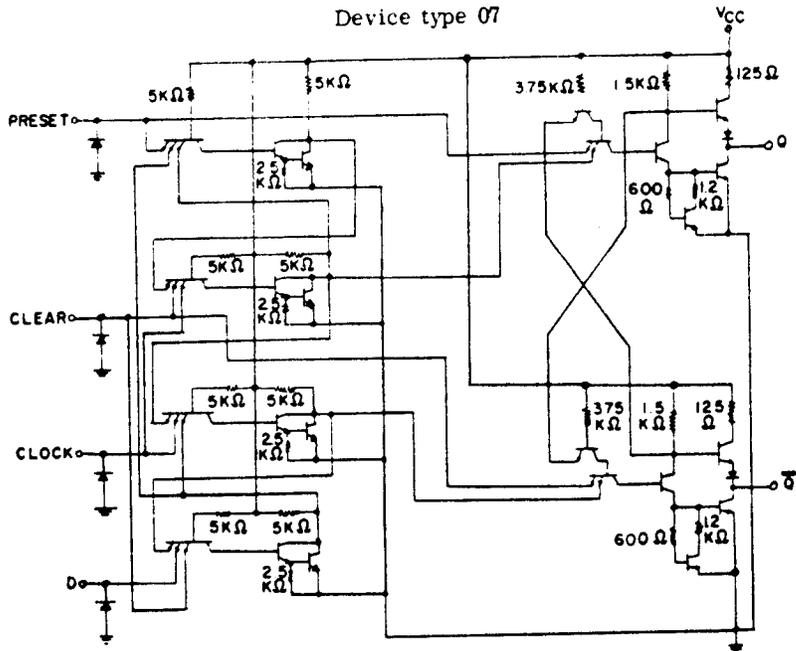
FIGURE 3. Schematic circuits - Continued.

Device type 06

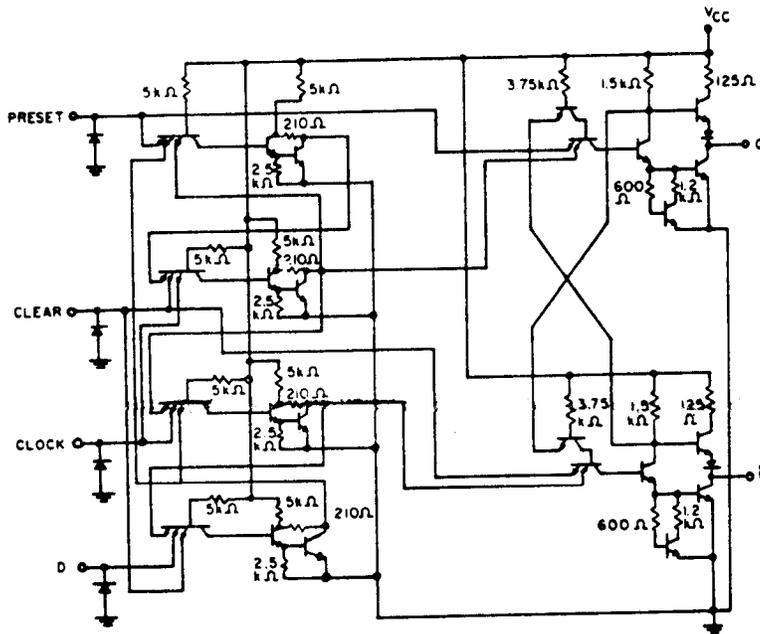


NOTE: All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.



CIRCUIT A



CIRCUIT B

NOTES:

1. Circuits A and B are the only acceptable variations for device type 07.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

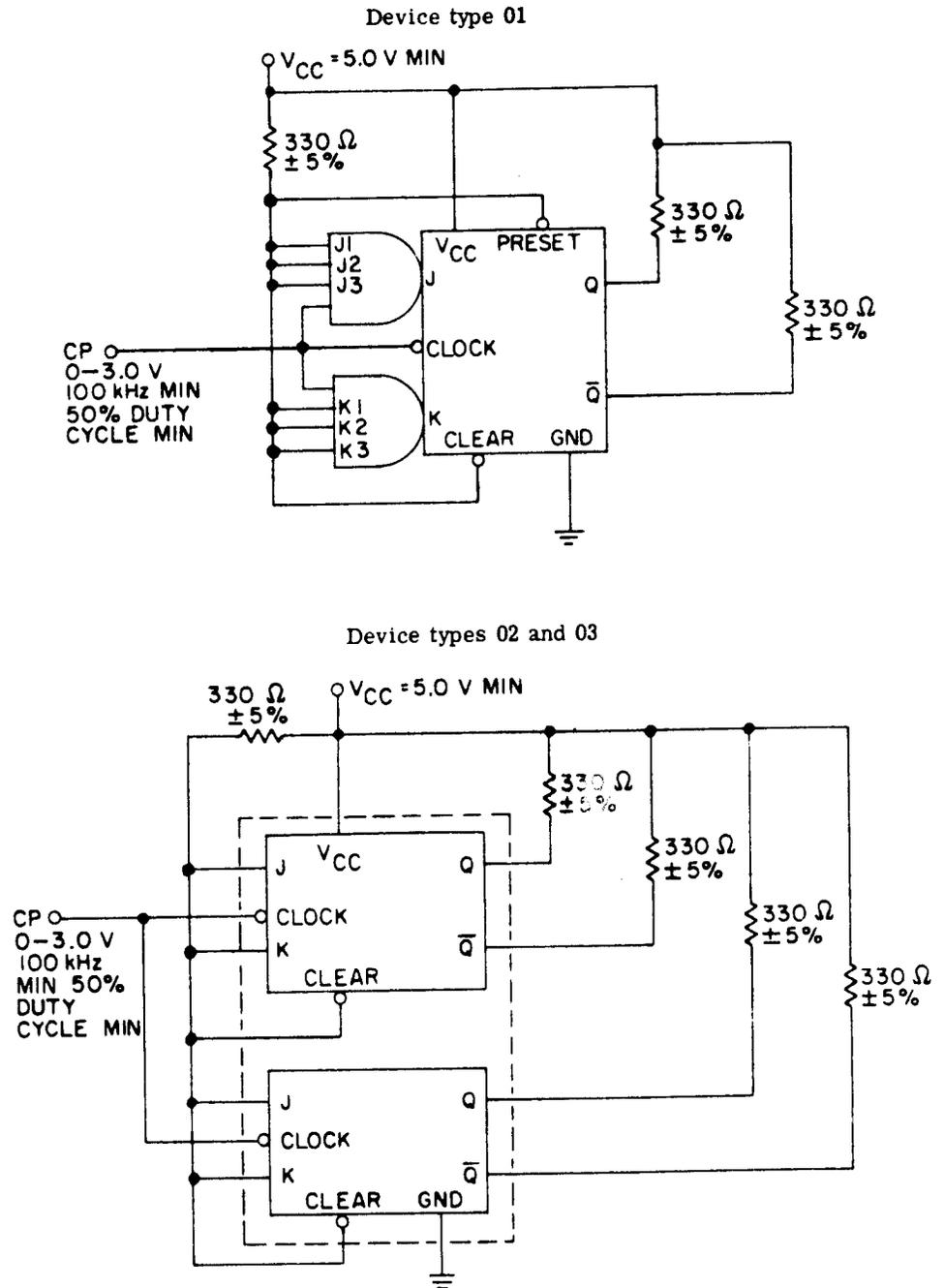


FIGURE 4. Burn-in and life-test circuits.

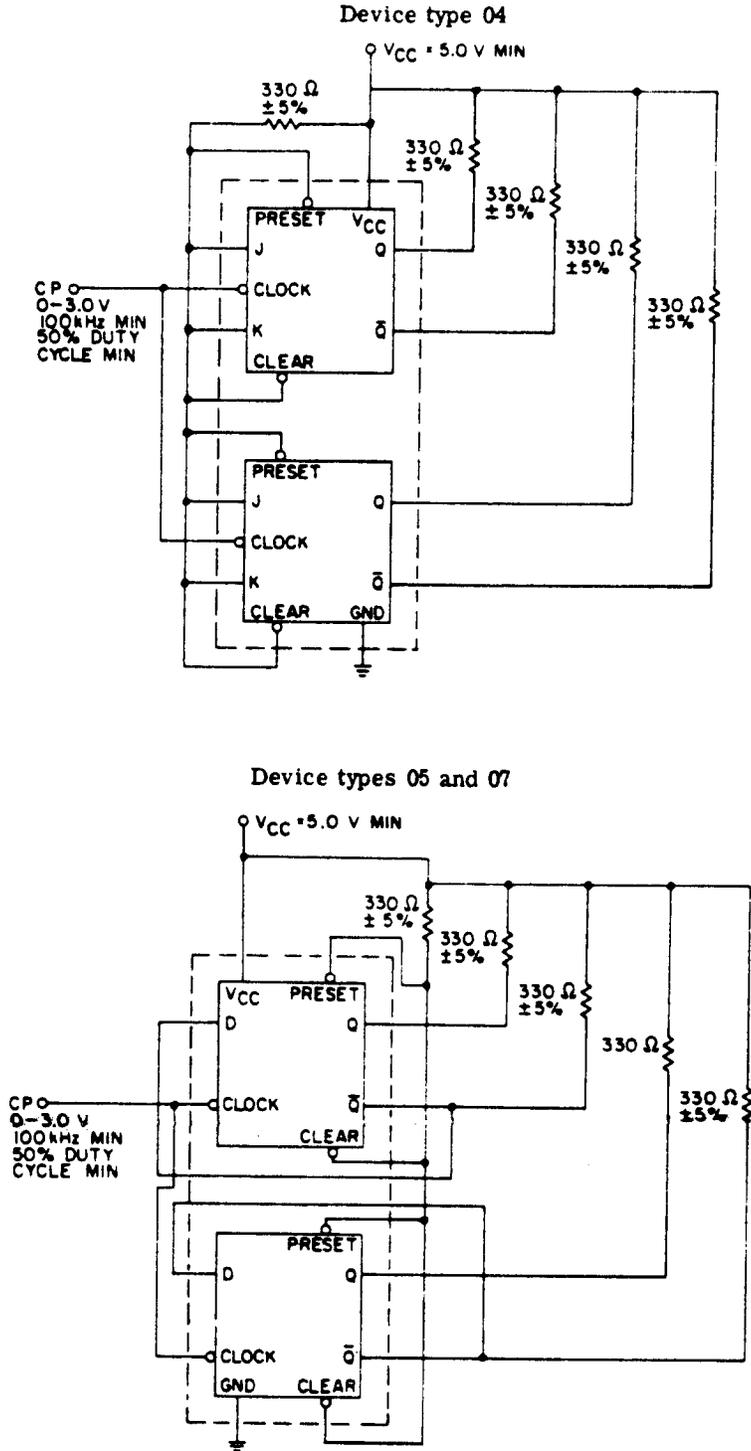


FIGURE 4. Burn-in and life-test circuits - Continued.

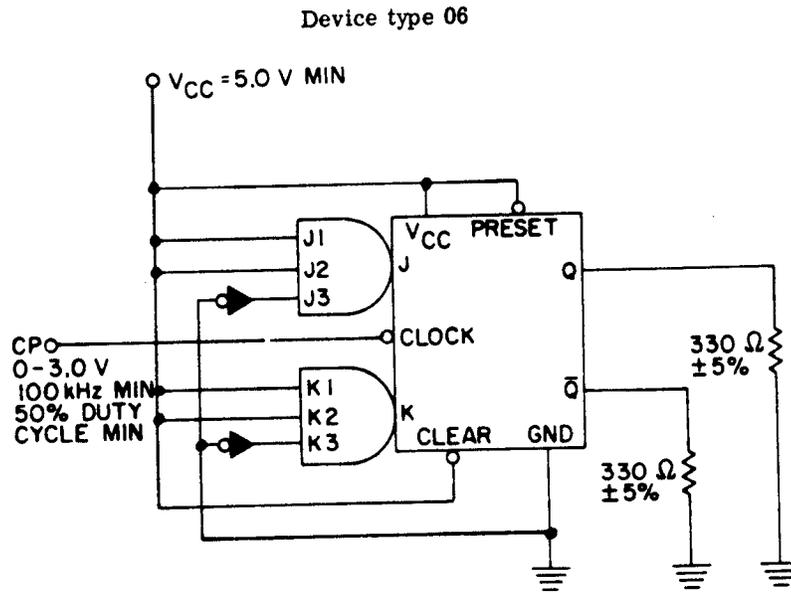
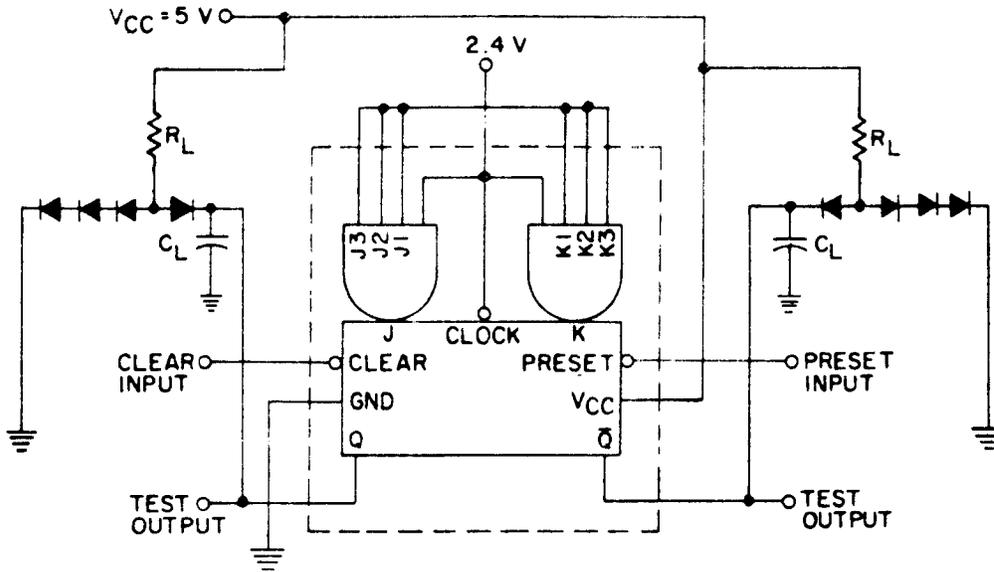
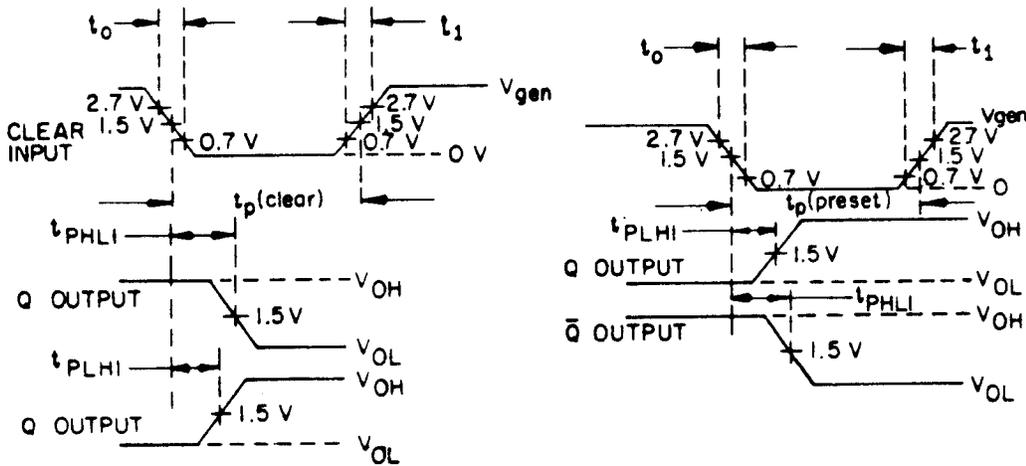


FIGURE 4. Burn-in and life-test circuits - Continued.



TEST CIRCUIT

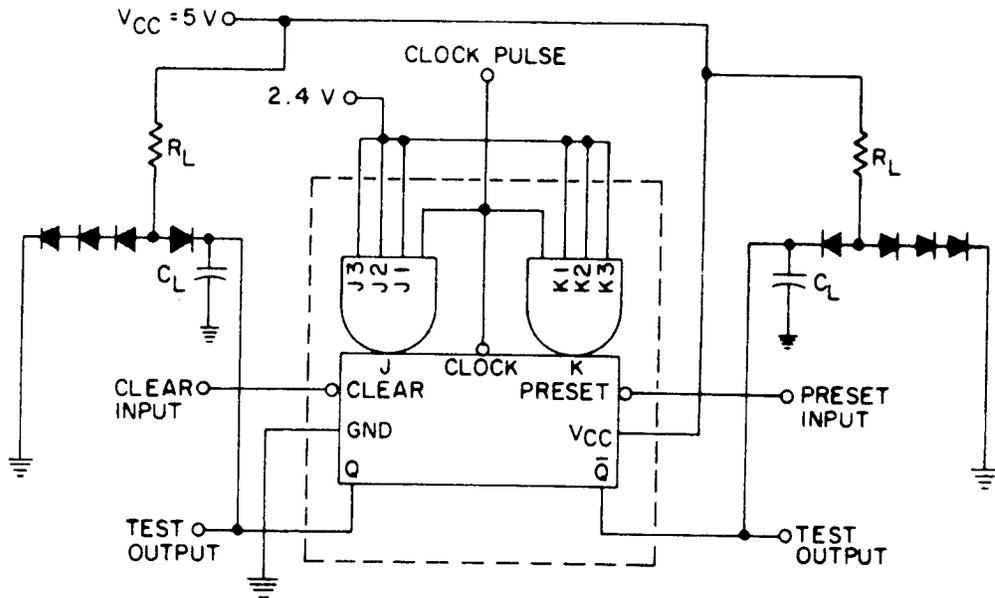


VOLTAGE WAVEFORMS

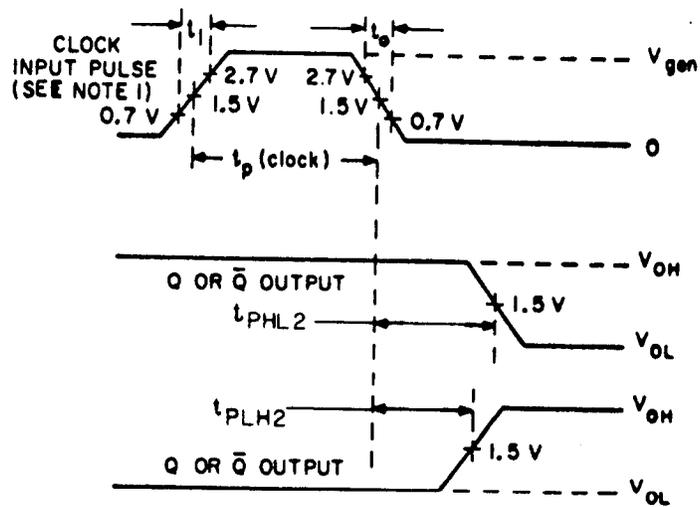
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 = 10\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 30\text{ ns}$, $\text{PRR} = 1\text{ MHz}$, and $Z_{out} \approx 50\ \Omega$.
3. $C_L = 50\text{ pF}$, minimum (C_L includes probe and jig capacitance).
4. $R_L = 390\ \Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 5. Clear and preset switching test circuit and waveforms for device type 01.



TEST CIRCUIT

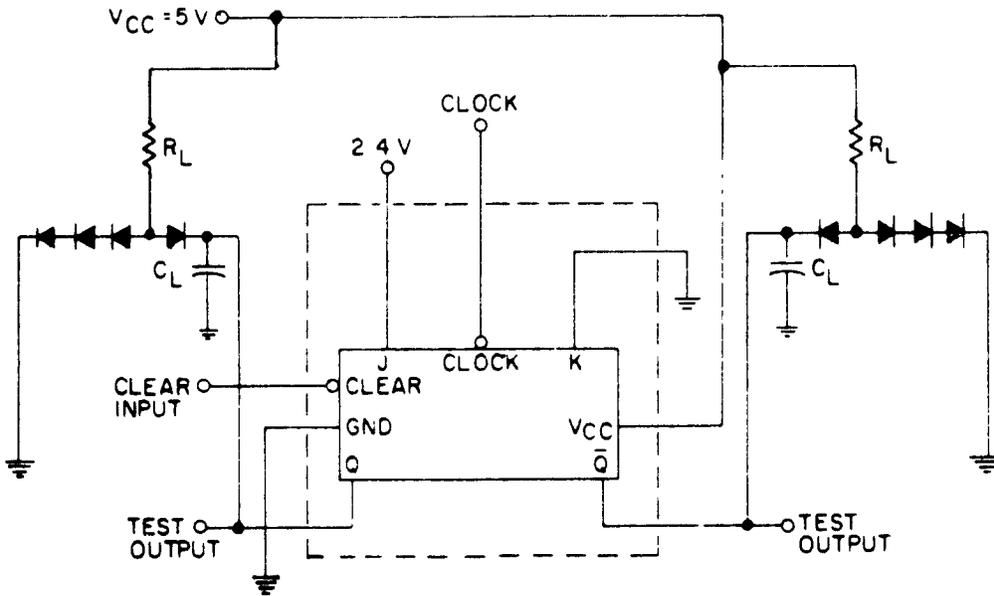


VOLTAGE WAVEFORMS

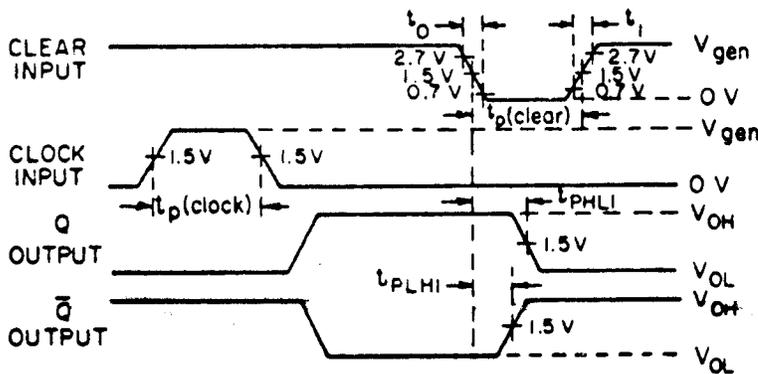
NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 10\text{ ns}$, $t_p(\text{clock}) = 25\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$. All J and K inputs are at 2.4 V . When testing f_{MAX} the clock input characteristics are $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 10\text{ ns}$, $t_p(\text{clock}) = 20\text{ ns}$, and $\text{PRR} = \text{see table III}$.
2. $J = J1 \cdot J2 \cdot J3$; and $K = K1 \cdot K2 \cdot K3$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF}$ minimum (C_L includes probe and jig capacitance).
4. $R_L = 390\Omega \pm 5\%$.

FIGURE 6. Synchronous switching test circuit for device type 01.



TEST CIRCUIT

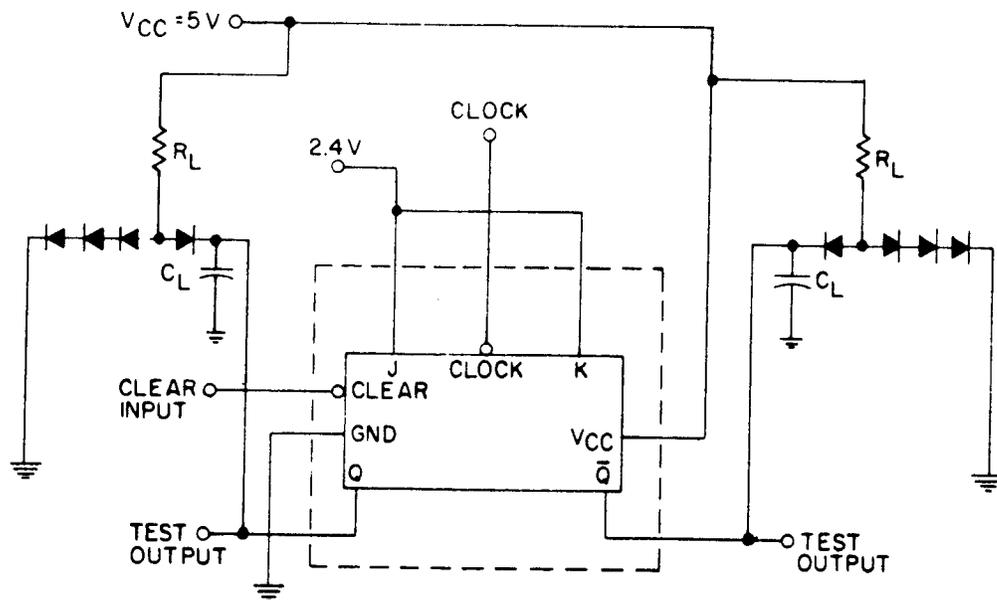


VOLTAGE WAVEFORMS

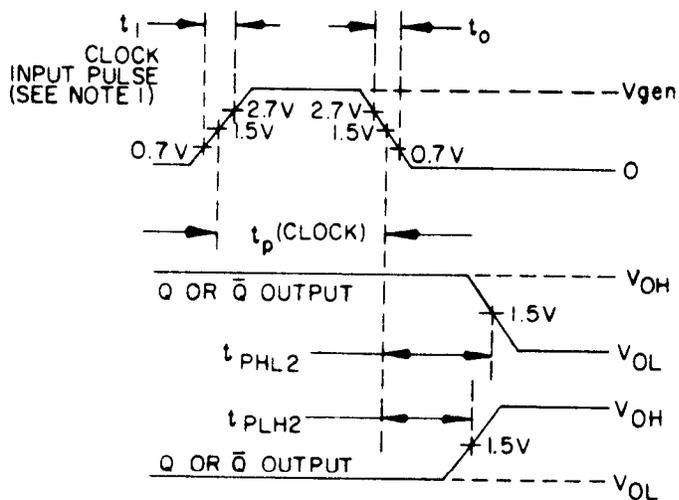
NOTES:

1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 = 10\text{ ns}$, $t_p(\text{clear}) = 30\text{ ns}$, $\text{PRR} = 1\text{ MHz}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF}$, minimum (including jig and probe capacitance).
5. $R_L = 390\ \Omega \pm 5\%$.
6. Clock input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_p(\text{clock}) \geq 25\text{ ns}$, $\text{PRR} = 1\text{ MHz}$.

FIGURE 7. Clear switching test circuit and waveforms for device types 02 and 03.



TEST CIRCUIT

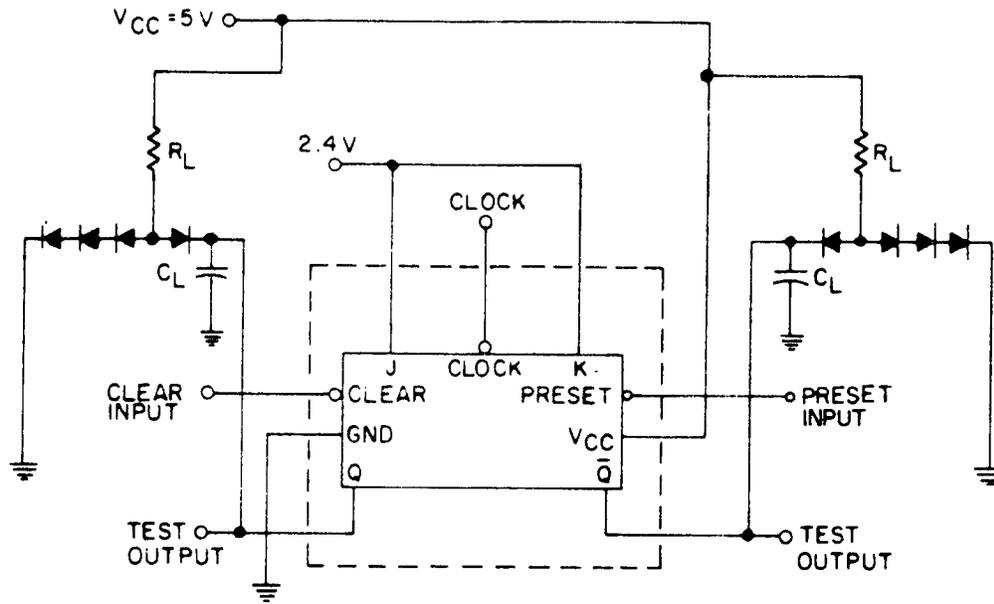


VOLTAGE WAVEFORMS

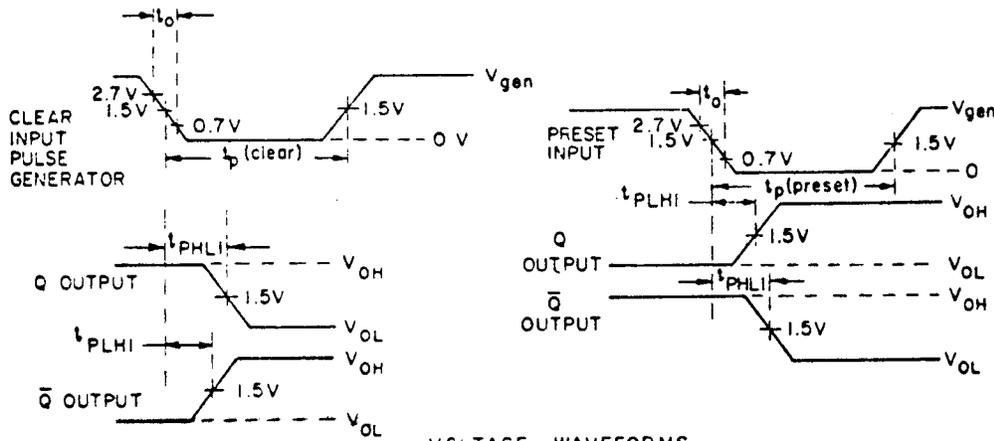
NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 10\text{ ns}$, $t_p(\text{clock}) = 25\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$. All J and K inputs are at 2.4 V . When testing f_{MAX} the clock input characteristics are $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 10\text{ ns}$, $t_p(\text{clock}) = 20\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF}$ minimum (including jig and probe capacitance).
4. $R_L = 390\ \Omega \pm 5\%$.

FIGURE 8. Synchronous switching test circuit for device types 02 and 03.



TEST CIRCUIT

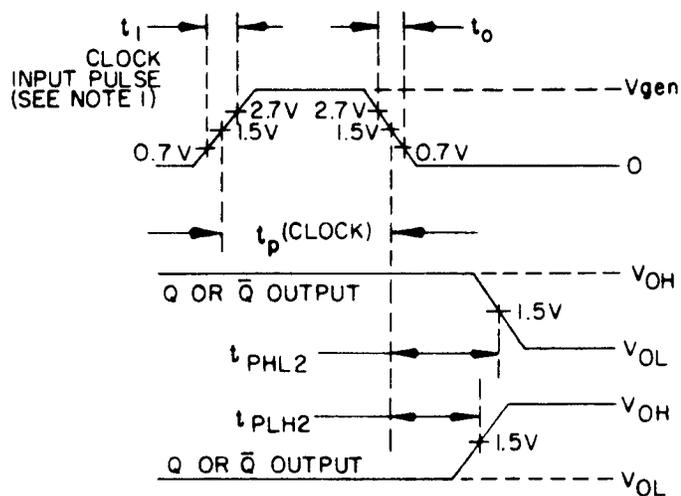
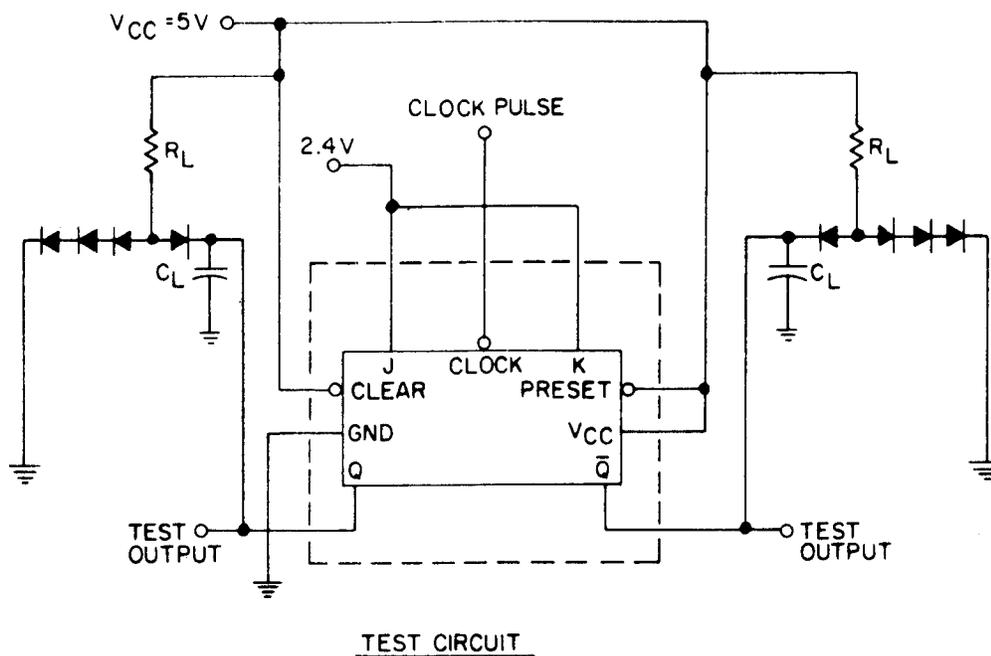


VOLTAGE WAVEFORMS

NOTES:

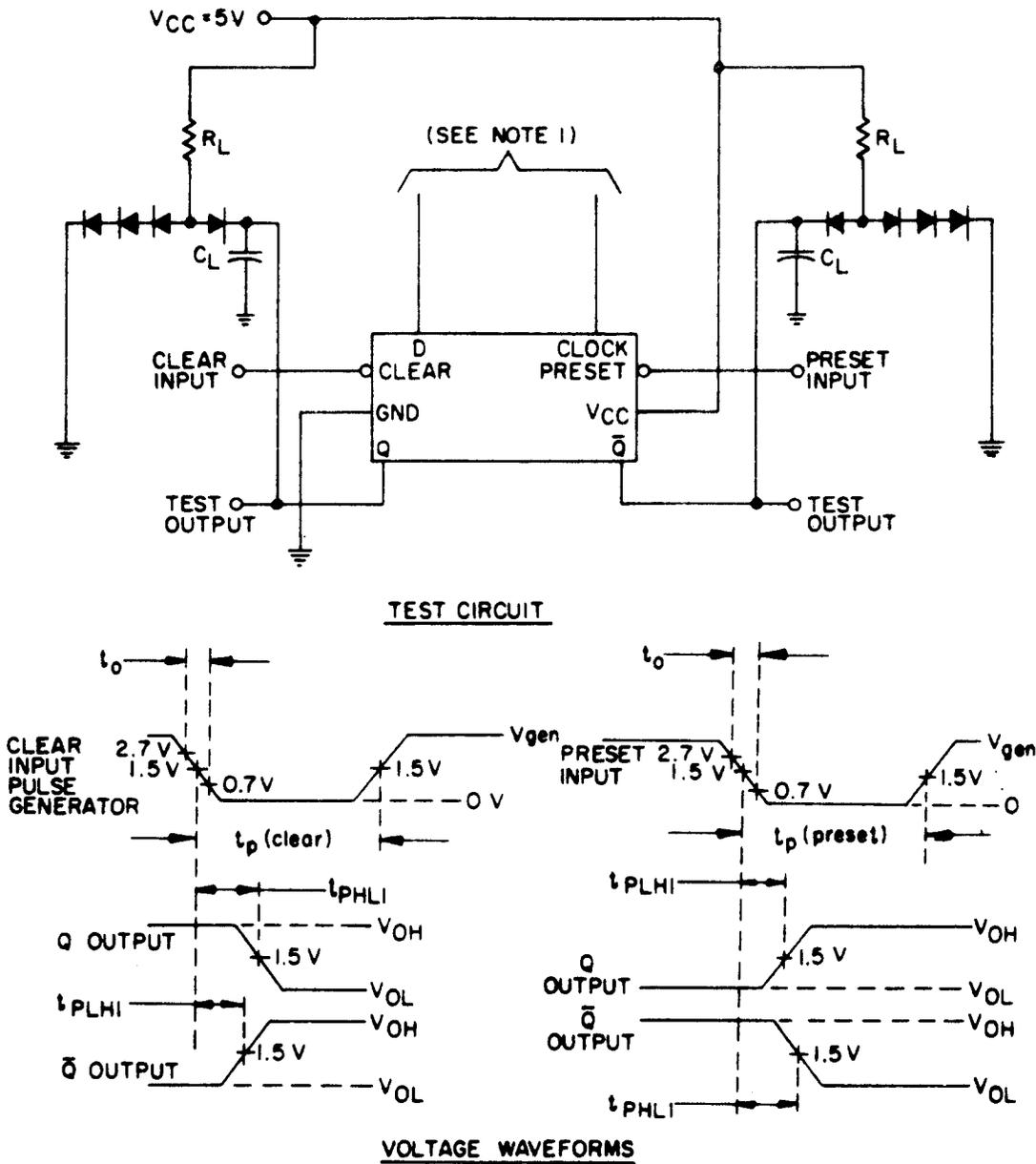
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 = 10\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 30\text{ ns}$, $\text{PRR} = 1\text{ MHz}$, and $Z_{out} \approx 50\ \Omega$.
3. $C_L = 50\text{ pF}$, minimum (including jig and probe capacitance).
4. $R_L = 390\ \Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 9. Clear and preset switching test circuit and waveforms for device type 04.

**NOTES:**

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3V$, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen} = 3V$, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50$ pF minimum (including jig and probe capacitance).
4. $R_L = 390\Omega \pm 5\%$.

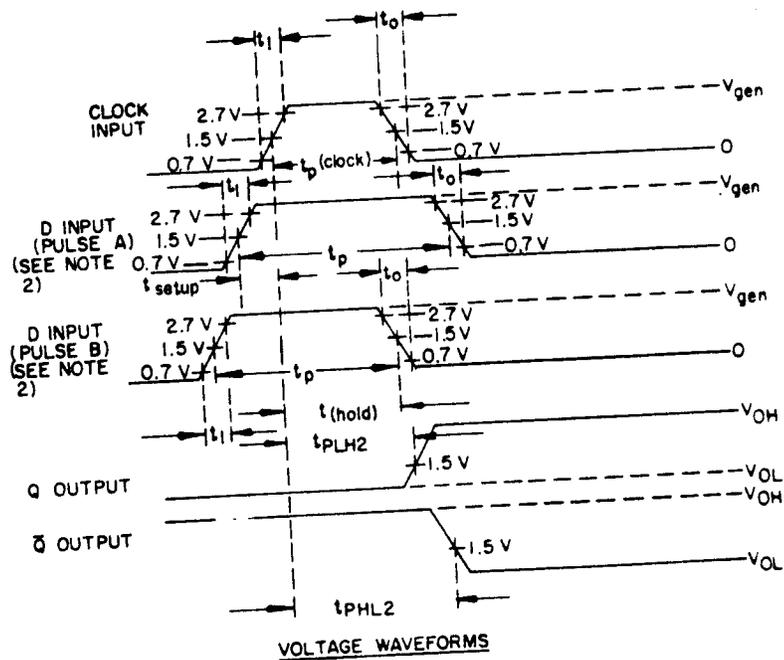
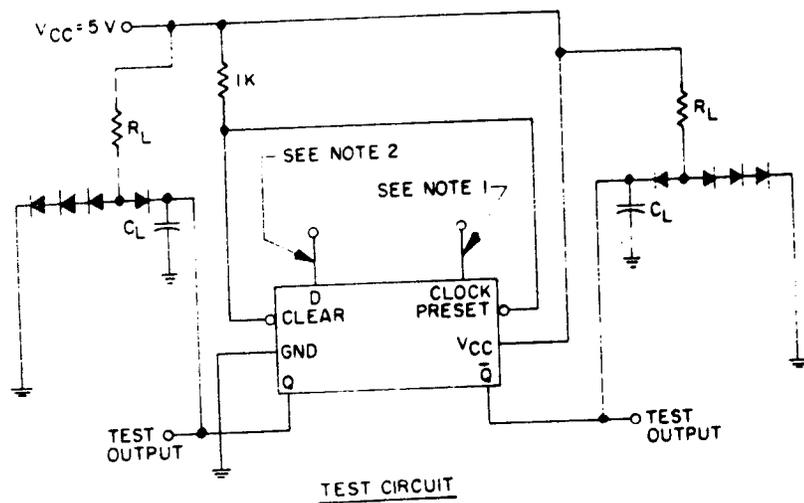
FIGURE 10. Synchronous switching test circuit for device type 04.



NOTES:

1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear or preset input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 \leq 7\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 35\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$.
4. $C_L = 50\text{ pF}$, minimum (including jig and probe capacitance).
5. $R_L = 390\ \Omega \pm 5\%$.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 11. Clear and preset switching test circuit and waveforms for device types 05 and 07.



NOTES:

1. Clock input pulse has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_p(\text{clock}) = 30\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$. When testing f_{MAX} , $\text{PRR} = \text{see table III}$.
2. D input (pulse A) has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 10\text{ ns}$, $t_{setup} = 25\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR . D input (pulse B) has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 < 7\text{ ns}$, $t_{hold} = 6\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF}$, minimum (including jig and probe capacitance).
5. $R_L = 390\ \Omega \pm 5\%$.

FIGURE 12. Synchronous switching test circuit (high level data) for device types 05 and 07.

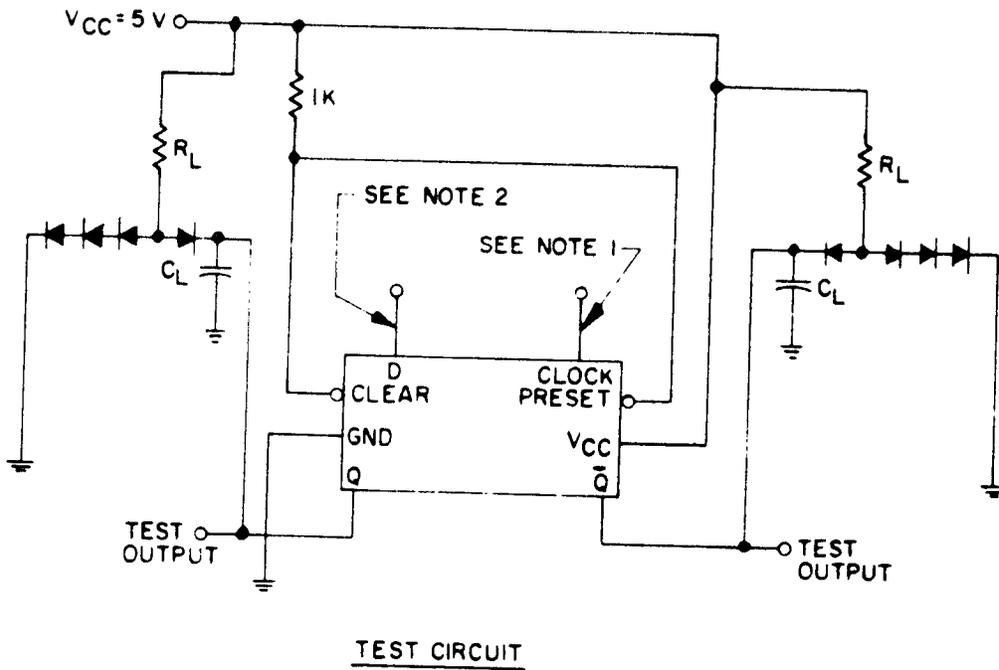
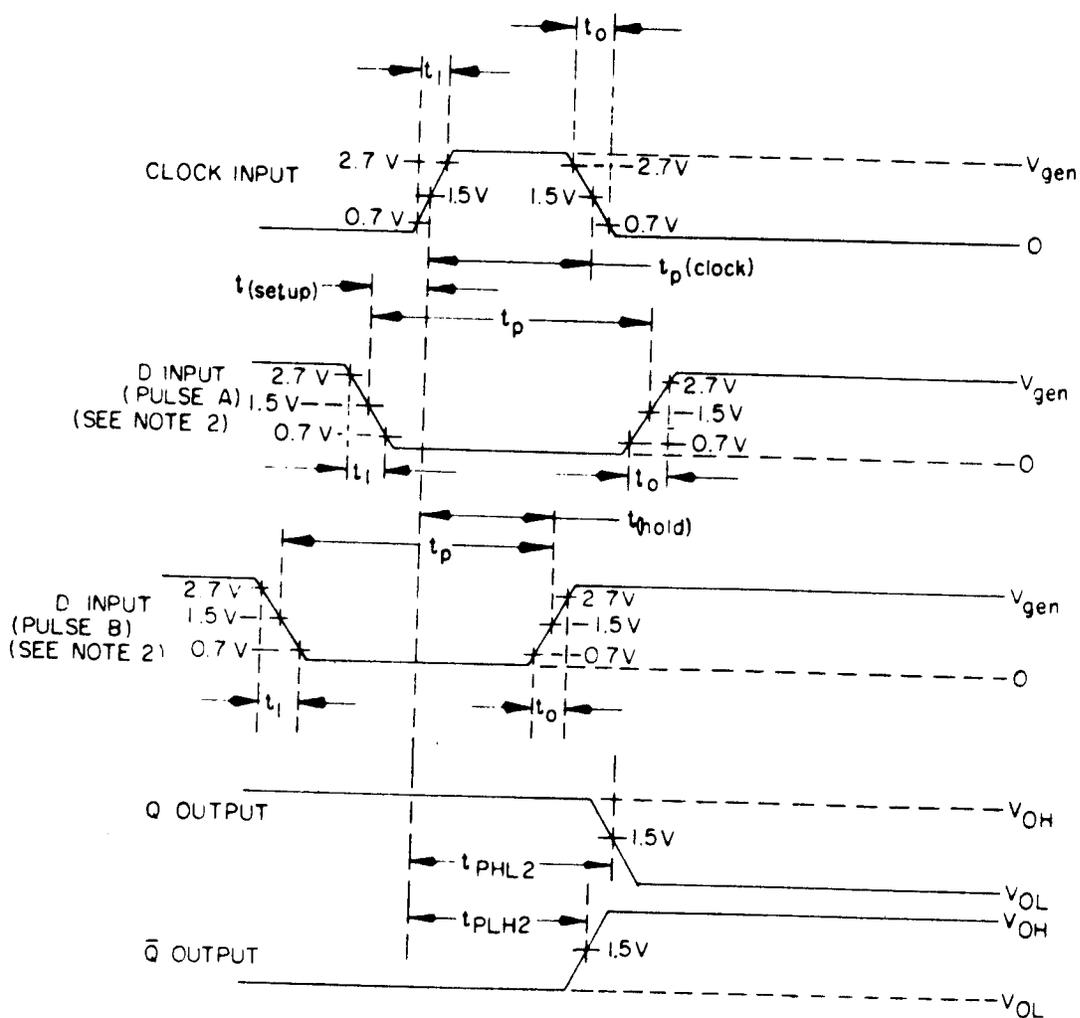


FIGURE 13. Synchronous switching test circuit (low-level data) for device types 05 and 07.

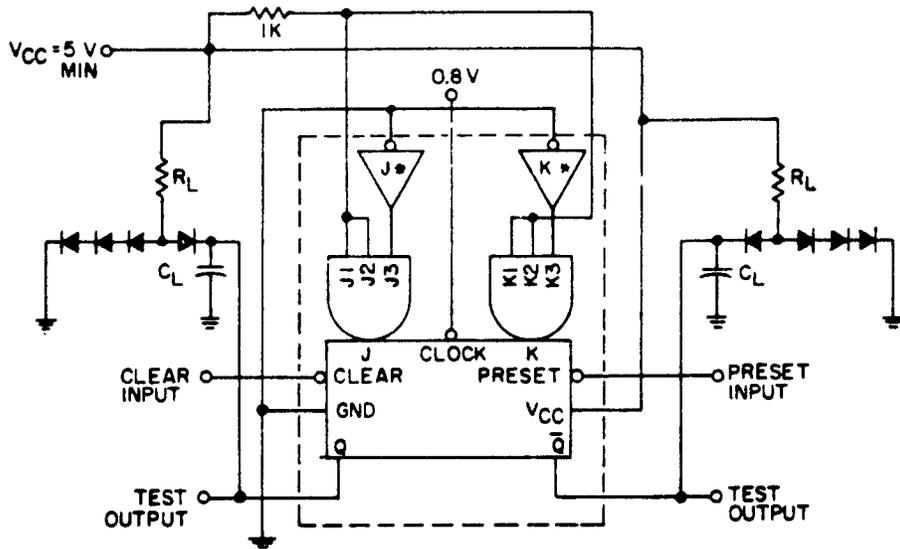


VOLTAGE WAVEFORMS

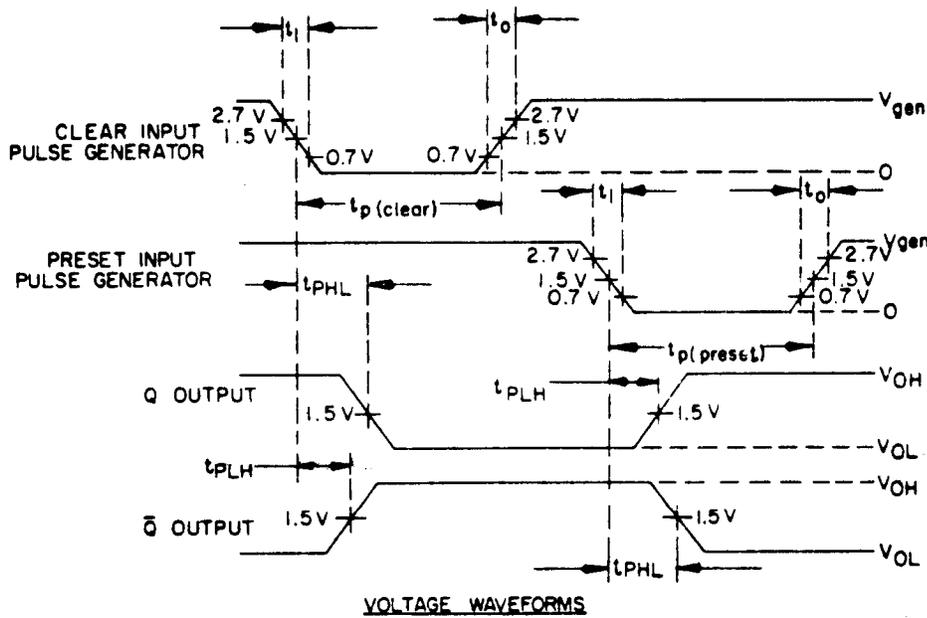
NOTES:

1. Clock input pulse has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 < 10\text{ ns}$, $t_p(\text{clock}) = 30\text{ ns}$, and $\text{PRR} = 1\text{ MHz}$.
2. D input (pulse A) has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 < 10\text{ ns}$, $t_{\text{setup}} = 25\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR . D input (pulse B) has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 < 10\text{ ns}$, $t_{\text{hold}} = 6\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF}$, minimum (including jig and probe capacitance).
5. $R_L = 390\ \Omega \pm 5\%$.

FIGURE 13. Synchronous switching test circuit (low-level data) for device types 05 and 07 - Continued.



TEST CIRCUIT

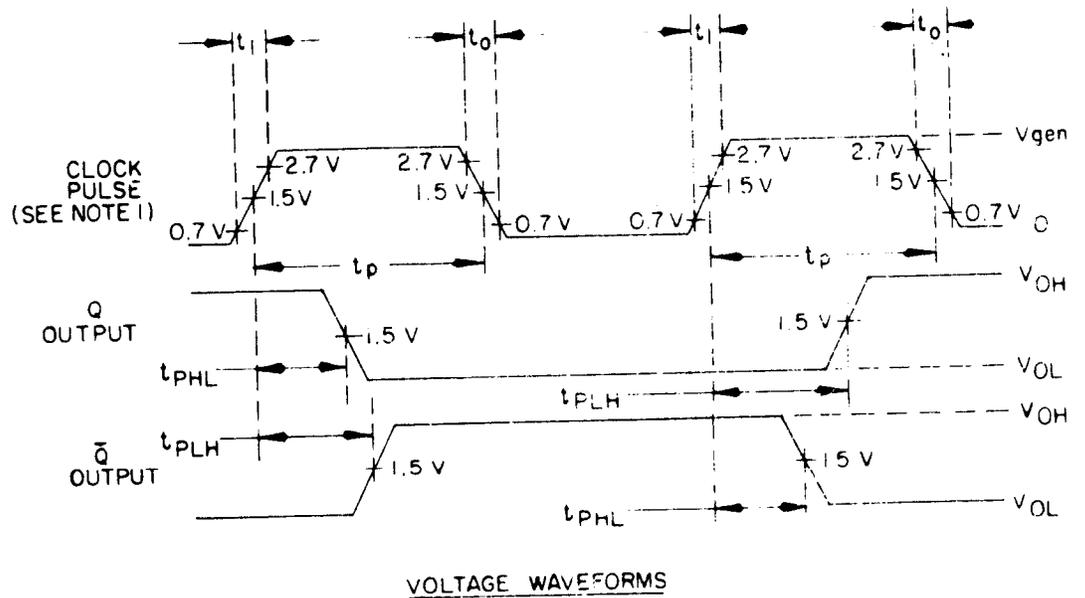
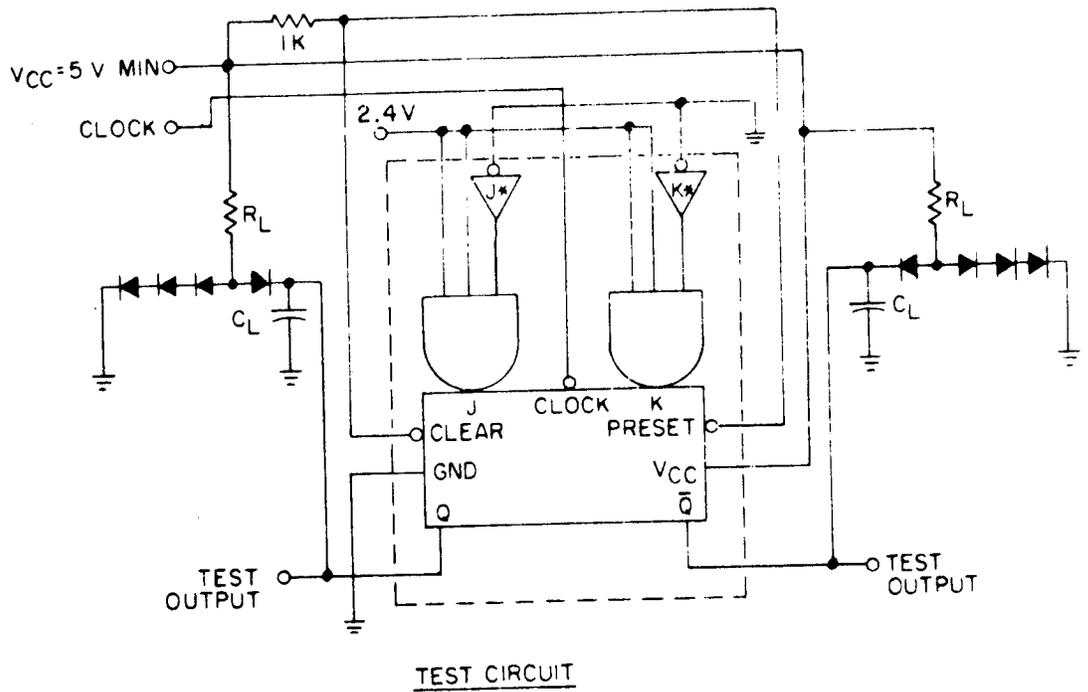


VOLTAGE WAVEFORMS

NOTES:

1. Preset or clear function can occur only when clock input is low. Gated inputs are inhibited.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50 \text{ pF}$ minimum, including jig and probe capacitance.
4. Clear or preset input pulse characteristics: $V_{gen} = 3.0 \text{ V}$, $t_0 = 5 \text{ ns}$, $t_1 \leq 10 \text{ ns}$, $t_p = 25 \text{ ns}$.
5. $R_L = 390 \Omega \pm 5\%$.

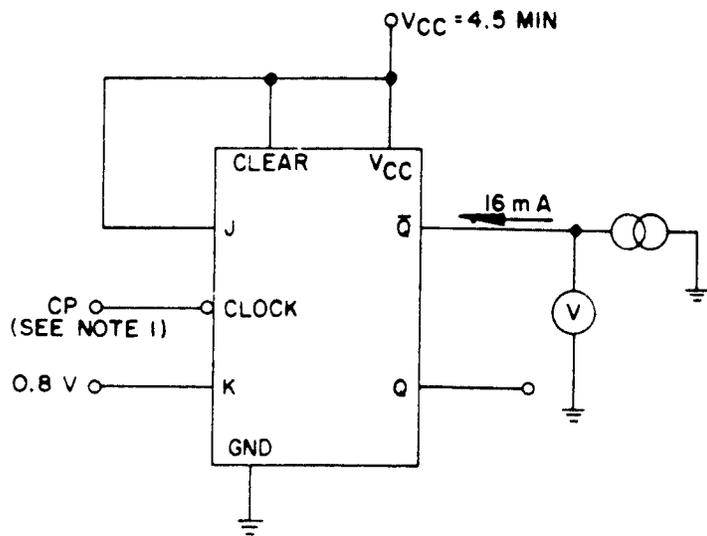
FIGURE 14. Clear and preset switching test circuit and waveforms for device type 06.



NOTES:

1. Clock pulse characteristics: $V_{gen} = 3.0\text{ V}$, $t_{r1} = t_{r0} = 10\text{ ns}$, $t_p = 30\text{ ns}$, and $PRR = 1\text{ MHz}$. When testing f_{MAX} , $PRR = \text{see table III}$.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF}$ minimum, including jig and probe capacitance.
4. $R_L = 390\Omega \pm 5\%$.

FIGURE 15. Synchronous switching test circuit for device type 06.



NOTES:

1. Apply normal clock pulse, then sink -12 mA on the clock input.
2. The output \bar{Q} is measured after -12 mA is applied to the clock to insure it is still in the low state.

FIGURE 16. Input clamp voltage test circuit for device types 01, 02, 03 and 04 (circuit B).

TABLE III. Group A inspection for device type 01 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D				Case C				Test limits										
			1	2	3	4	5	6	7	8	9	10	11	12	13	14					
7/ 4/ TA = 25°C			9	12	13	14	2	1	3	4	5	6	7	8	9	10	11	Meas. terminal	Min	Max	Unit
8/ 4/ TA = 25°C	F _{MAX} (Fig 6)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clear to Q	5	5	MHz
	F _{MAX} (Fig 6)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Preset to Q	5	5	ns
	t _{PLH1} (PLH1)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clear to Q	40	40	ns
	t _{PLH1} (PLH1)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Preset to Q	40	40	ns
	t _{PHL1} (PHL1)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	30	30	ns
	t _{PHL1} (PHL1)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	30	30	ns
	t _{PLH2} (PLH2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	40	40	MHz
	t _{PLH2} (PLH2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	40	40	MHz
	t _{PHL2} (PHL2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	5	5	MHz
	F _{MAX} (Fig 6)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clear to Q	5	5	ns
	F _{MAX} (Fig 6)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Preset to Q	5	5	ns
	t _{PLH1} (PLH1)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clear to Q	50	50	ns
t _{PHL1} (PHL1)		2.4 V	IN	2.4 V	J	IN	J	IN	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Preset to Q	50	50	ns	
t _{PLH2} (PLH2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	39	39	ns	
t _{PLH2} (PLH2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	39	39	ns	
t _{PHL2} (PHL2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	50	50	ns	
t _{PHL2} (PHL2)		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	OUT	2.4 V	2.4 V	Q	Clock to Q	50	50	ns	

Some tests, terminal conditions and limits as for subgroup 7, except TA = 125 and -55°C.

Some tests, terminal conditions and limits as subgroup 10, except TA = -55°C.

- NOTES:
- A Normal clock pulse.
 - B = Secondary GND, then 4.5 V.
 - J Input pulse 40-100 ns, PRR = 1 MHz, VOL = 0 V, VOH = 4.5 V.
 - K At clock pulse apply -12 max to clock pin to insure Q is still in the low state (see figure 16).
 - L Terminal conditions (pins not designated may be H = 2.0 V, or L = 0.8 V, or open).
 - M Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
 - N Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator, or (b) H = 1.5 V and L = 1.5 V when using a high speed checker single comparator.
 - O Tests shall be performed in sequence.

TABLE III. Group A inspection for device type 02

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	Case C										Meas. terminal	Test limits							
				1	2	3	4	5	6	7	8	9	10		11	12	13	14	Min	Max	Unit	
I T _A 25°C	V _{OH}	3006	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2.4		V	
	V _{OL}	3007	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0.4		V	
	V _{IC}		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{HL1}	3009	18 CKT B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{HL2}		20 CKT B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{HL3}		27 CKT A, C	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{IH1}		28 CKT B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{IH2}		30	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{IH3}		31	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{IH4}		32	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
	I _{IH5}		33	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
			34	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
			35	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
			36	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
			37	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
		38	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		39	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		40	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		41	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		42	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		43 CKT A, C	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
		44 CKT B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					

See notes at end of device type 02.

Subgroup	Symbol	MIL-STD-883 method (FIG 8)	Table A, B, C, D																Test limits			
			Case C Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit	
9 T _A 25°C	F _{MAX}		89	IN	5.0 V	2.4 V	2.4 V	5.0 V										5			MHz	
	t _{PLH1}		90	IN	5.0 V	2.4 V	2.4 V	5.0 V	5.0 V	2.4 V	2.4 V	OUT						5	25		ns	
	t _{PLH1}		91	IN	5.0 V	2.4 V	2.4 V	5.0 V	5.0 V	2.4 V	2.4 V	OUT						5	25		ns	
	t _{PHL1}		92	IN	5.0 V	2.4 V	2.4 V	5.0 V	5.0 V	2.4 V	2.4 V	OUT						5	25		ns	
10 T _A 125°C	t _{PLH1}		93	IN	IN	GND												5	25		ns	
	t _{PLH1}		94	IN	IN	GND												5	25		ns	
	t _{PHL1}		95	IN	IN	GND												5	25		ns	
	t _{PHL1}		96	IN	IN	GND												5	25		ns	
	t _{PLH2}		97	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		98	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		99	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		100	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		101	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		102	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		103	IN	J	2.4 V												5	30		ns	
	t _{PHL2}		104	IN	J	2.4 V												5	30		ns	
	F _{MAX}		105	IN	5.0 V	2.4 V												5				MHz
	t _{PLH1}		106	IN	5.0 V	2.4 V												5				ns
	t _{PLH1}		107	IN	5.0 V	2.4 V												5				ns
	t _{PLH1}		108	IN	5.0 V	2.4 V												5				ns
t _{PLH1}		109	IN	IN	GND												5	39			ns	
t _{PLH1}		110	IN	IN	GND												5	39			ns	
t _{PHL1}		111	IN	IN	GND												5	39			ns	
t _{PHL1}		112	IN	IN	GND												5	39			ns	
t _{PLH2}		113	IN	J	2.4 V												5	39			ns	
t _{PLH2}		114	IN	J	2.4 V												5	39			ns	
t _{PHL2}		115	IN	J	2.4 V												5	39			ns	
t _{PHL2}		116	IN	J	2.4 V												5	39			ns	

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02 1/ - Continued.

Subgroup	Symbol	MIL - STD-883 method	Case A, B, D										Meas. terminal	Test limits												
			1	2	3	4	5	6	7	8	9	10		11	12	13	14	Min	Max	Unit						
10 TA 125 C	PHIL2	3003	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Clock 1 to Q1 Clock 1 to Q1 Clock 2 to Q2 Clock 2 to Q2	5	50	ns					
			Test No.	117	118	119	120	Clear 1	K1	VCC	Clock 2	Clear 2	J2	Q2	K2	GND	Q1					Q1				
			IN	J	2.4 V	5.0 V																				
			IN	J	2.4 V		IN	J	2.4 V																	
11	Same tests, terminal conditions and limits as subgroup 10, except TA = -55° C.																									

NOTES:

- A Normal clock pulse.
 - B Momentary GND, then 4.5 V.
 - C Momentary GND, then open.
 - D Momentary 4.5 V, then GND.
 - E Momentary ground, then 2.4 volts.
 - F Momentary ground, then 5.5 volts.
 - J Input pulse $t_p \geq 100$ ns, PRR = 1 MHz, VOL = 0 V, VOH = 4.5 V.
 - * After clock pulse apply -12 mA to clock pin to insure Q is still in the low state (see figure 16).
 - ** Test time limit 100 ms.
- 1/ Terminal conditions (pins not designated may be H $>$ 2.0 V, or L $<$ 0.8 V, or open).
 - 2/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
 - 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H \geq 1.5 V and L $<$ 1.5 V when using a high speed checker single comparator.
 - 4/ Tests shall be performed in sequence.

TABLE III. Group A inspection for device type 03

Subgroup	Symbol	MIL-STD-883 method	Case C Test No.	Case C														Test limits		
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max
I T _A 25 C	V _{OH}	3006	1	J1	Q1	K1	Q2	Q2	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{CC}	Q1	2.4		V
																		Q1		
	V _{OL}	3007	2	2.0 V	4 mA	0.8 V	2.0 V	4 mA	GND	2.0 V	A	0.8 V	0.8 V	A	0.8 V	4.5 V	Q1			
				3	0.8 V	4 mA	2.0 V				0.8 V	A		2.0 V	A			Q1		
	V _{IC}	3009	4	0.8 V	16 mA	2.0 V	0.8 V	16 mA		0.8 V	A	0.8 V	2.0 V	A	0.8 V	4.5 V	Q1	0.4		
				5	2.0 V	16 mA	0.8 V	16 mA			2.0 V	A		0.8 V	A			Q1		
		3010	6	-12 mA		-12 mA				-12 mA							J1			
				7														J1		
	I _{IL1}	3009	8	0.4 V		0.4 V				4.5 V	A*	4.5 V	0.8 V	4.5 V	B	5.5 V	J1	-0.7	1.6	mA
				9	0.4 V		0.4 V				4.5 V	A*	4.5 V	0.8 V	4.5 V	B	5.5 V	J1		
	I _{IL2}	3010	10	4.5 V		4.5 V				0.4 V	4.5 V	B	0.4 V	0.4 V	B		K1			
				11	4.5 V		4.5 V				0.4 V	4.5 V	B	0.4 V	0.4 V	B		K1		
	I _{IL3}	3010	12	4.5 V		4.5 V				4.5 V	0.4 V	4.5 V	0.4 V	4.5 V	B		K2			
				13	4.5 V		4.5 V				4.5 V	0.4 V	4.5 V	0.4 V	4.5 V	B		K2		
	I _{IH1}	3010	14	2.4 V		2.4 V				2.4 V	GND	GND	2.4 V	GND	GND		J1	0	40	µA
				15	2.4 V		2.4 V				2.4 V	GND	GND	2.4 V	GND	GND		J1		
	I _{IH2}	3010	16	5.5 V		5.5 V				5.5 V	GND	GND	5.5 V	GND	GND		J2			
				17	5.5 V		5.5 V				5.5 V	GND	GND	5.5 V	GND	GND		J2		
	I _{IH3}	3010	18	GND		GND				GND	GND	E	5.5 V	E			J2			
				19	GND		GND				GND	GND	E	5.5 V	E			J2		
	I _{IH4}	3010	20	GND		GND				GND	GND	E	5.5 V	E			K2			
				21	GND		GND				GND	GND	E	5.5 V	E			K2		
	I _{IH5}	3010	22	GND		GND				GND	GND	E	5.5 V	E			Clear 1			
				23	GND		GND				GND	GND	E	5.5 V	E			Clear 1		
		3010	24	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				25	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	26	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				27	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	28	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				29	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	30	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				31	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	32	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				33	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	34	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				35	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	36	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				37	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	38	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				39	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	40	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				41	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	42	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				43	GND		GND				GND	GND	E	5.5 V	E			Clear 2		
		3010	44	GND		GND				GND	GND	E	5.5 V	E			Clear 2			
				45	GND		GND				GND	GND	E	5.5 V	E			Clear 2		

See notes at end of device type 03.

TABLE III. Group A inspection for device type 03 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method (Fig 8)	Case C Test No.	Case C							12	13	14	Test limits							
				J1	Q1	K1	Q2	Q2	GND	J2				Clock 2	Clear 2	K2	Clock 1	Clear 1	VCC	Meas. terminal	Min
9 TA 25°C	FMAX	3003	89	2.4 V	OUT	2.4 V	OUT	OUT	GND	2.4 V	IN	5.0 V	5.0 V	Q1	5						
			90	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			91	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q2	5						
			92	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	25		ns	
			93	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	25		ns	
			94	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	40		ns	
	tPHL	3003	95	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	40		ns	
			96	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	40		ns	
			97	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	Q1 to Q2	5	30		ns	
			98	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	Q1 to Q2	5	30		ns	
			99	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	Q1 to Q2	5	30		ns	
			100	2.4 V	QUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	5.0 V	5.0 V	Q1 to Q2	5	30		ns	
10 TA 125°C	FMAX	3003	101	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			102	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			103	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			104	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			105	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			106	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
11	tPHL	3003	107	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			108	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1	5						
			109	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns	
			110	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns	
			111	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	50		ns	
			112	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	A	2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	50		ns	
11	tPHL	3003	113	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			114	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			115	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			116	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			117	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			118	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
11	Same tests, terminal conditions and limits as subgroup 10, except TA = -55°C.		119	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			
			120	2.4 V	OUT	2.4 V	OUT	OUT		2.4 V	IN	5.0 V	5.0 V	Q1 to Q2	5	39		ns			

NOTES:

- A Normal clock pulse.
 - B Momentary GND, then 4.5 V.
 - C Momentary GND, then open.
 - D Momentary 4.5 V, then GND.
 - E Momentary ground, then 2.4 V.
 - F Momentary ground, then 5.5 V.
 - * After clock pulse apply -12 mA to clock pin to insure Q is still in the low state (see figure 16).
 - ** Test time limit - 100 ms.
- 1/ Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open).
 - 2/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
 - 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
 - 4/ Tests shall be performed in sequence.

TABLE III. Group A inspection for device type 04 1/

Subgroup	Symbol	MIL-STD-883 method	Case E & F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
			Test No.	Test No.																	Min	Max	Unit	
1 T _A 25 C	V _{OH}	3006	1	A	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2		Clear 2	J2	Q ₂	Q ₂	K2	GND	Q ₁	Q1	K1	Q1	2.4		
			2	A				2.0 V	4.5 V					2.0 V					-4 mA	-4 mA	0.8 V	Q1		
			3					0.8 V			A													
			4					2.0 V			A													
			5					0.8 V																
			6					2.0 V																
			7					0.8 V																
			8					2.0 V																
		V _{OL}	3007	9	A			0.8 V																
				10	A			2.0 V																
				11				0.8 V																
				12				2.0 V																
				13				0.8 V																
				14				2.0 V																
				15				0.8 V																
				16				2.0 V																
	V _{IC}	3009	17				-12mA																	
			18																					
			19																					
			20																					
			21																					
			22																					
			23																					
			24																					
			25																					
			26																					
	I _{IH1}	3010	27																					
			28																					
			29																					
			30																					
			31																					
			32																					
			33																					
			34																					
			35 A, D																					
			35 B, C																					
		36 A, D																						
		36 B, C																						
		37 A, D																						
		37 B, C																						
		38 A, D																						
		38 B, C																						
	I _{IH1}		39																					
			40																					
			41																					
			42																					
			43																					
			44																					
			45																					
			46																					

See notes at end of device type 04.

TABLE III - Group A inspection for device type 04 V - Continued

Subgroup	Symbol	MIL STD-883 method	C, E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit
FA	PHI.2	3003 (Fig. 10)	IN	IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	GND	OUT	Q1	Q1	Clear 1 to Q1	5	40	ns
				IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	GND	OUT	Q1	Clear 2 to Q2	5	40
FA	PHI.1	3003 (Fig. 9)	IN	IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	2.4 V	OUT	Q1	Q1	Clear 1 to Q1	5	39	ns
				IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	2.4 V	OUT	Q2	Clear 2 to Q2	5	39
FA	PHI.2	3003 (Fig. 10)	IN	IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	2.4 V	OUT	Q1	Q1	Clear 1 to Q1	5	36	ns
				IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	2.4 V	OUT	Q2	Clear 2 to Q2	5	36
FA	PHI.1	3003 (Fig. 9)	IN	IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	2.4 V	OUT	Q1	Q1	Clear 1 to Q1	5	39	ns
				IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	2.4 V	OUT	Q2	Clear 2 to Q2	5	39
FA	PHI.2	3003 (Fig. 10)	IN	IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	2.4 V	OUT	Q1	Q1	Clear 1 to Q1	5	50	ns
				IN	5.0 V	5.0 V	2.4 V	5.0 V	IN	5.0 V	5.0 V	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	2.4 V	OUT	Q2	Clear 2 to Q2	5	50

11 Same tests, terminal conditions and limits as subgroup 10, except TA -55 C.

NOTES:

- A Normal clock pulse.
- B Momentary GND, then 4.5 V.
- C Momentary GND, then open.
- E Momentary ground, then 2.4 V.
- F Momentary ground, then 5.5 V.
- ** Test time limit 100 ns.
- J Input pulse 100 ns, PRR 1 MHz, VOL 0 V, VOH 4.5 V.
- 1 Terminal conditions (pins not designated may be H \geq 2.0 V, or L \leq 0.8 V, or open).
- 2 Input voltages shown are: A 2.0 volts minimum and B 0.8 volts maximum.
- 3 Output voltages shall be either: (a) H 2.4 V, minimum and L 0.4 V, maximum when using a high speed checker double comparator, or (b) H 1.5 V and L 1.5 V when using a high speed checker single comparator.
- 4 Tests shall be performed in sequence.

TABLE III. Group A inspection for device type 05 I_V - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D		Case C		Test No.		Clock		Clear		D2		D1		VCC		Preset		Q1		Q2		Q3		Q4		Q5		Q6		Q7		Q8		Q9		Q10		Q11		Q12		Q13		Q14		Q15		Q16		Q17		Q18		Q19		Q20		Q21		Q22		Q23		Q24		Q25		Q26		Q27		Q28		Q29		Q30		Q31		Q32		Q33		Q34		Q35		Q36		Q37		Q38		Q39		Q40		Q41		Q42		Q43		Q44		Q45		Q46		Q47		Q48		Q49		Q50		Q51		Q52		Q53		Q54		Q55		Q56		Q57		Q58		Q59		Q60		Q61		Q62		Q63		Q64		Q65		Q66		Q67		Q68		Q69		Q70		Q71		Q72		Q73		Q74		Q75		Q76		Q77		Q78		Q79		Q80		Q81		Q82		Q83		Q84		Q85		Q86		Q87		Q88		Q89		Q90		Q91		Q92		Q93		Q94		Q95		Q96		Q97		Q98		Q99		Q100		Q101		Q102		Q103		Q104		Q105		Q106		Q107		Q108		Q109		Q110		Q111		Q112		Q113		Q114		Q115		Q116		Q117		Q118		Q119		Q120		Q121		Q122		Q123		Q124		Q125		Q126		Q127		Q128		Q129		Q130		Q131		Q132		Q133		Q134		Q135		Q136		Q137		Q138		Q139		Q140		Q141		Q142		Q143		Q144		Q145		Q146		Q147		Q148		Q149		Q150		Q151		Q152		Q153		Q154		Q155		Q156		Q157		Q158		Q159		Q160		Q161		Q162		Q163		Q164		Q165		Q166		Q167		Q168		Q169		Q170		Q171		Q172		Q173		Q174		Q175		Q176		Q177		Q178		Q179		Q180		Q181		Q182		Q183		Q184		Q185		Q186		Q187		Q188		Q189		Q190		Q191		Q192		Q193		Q194		Q195		Q196		Q197		Q198		Q199		Q200		Q201		Q202		Q203		Q204		Q205		Q206		Q207		Q208		Q209		Q210		Q211		Q212		Q213		Q214		Q215		Q216		Q217		Q218		Q219		Q220		Q221		Q222		Q223		Q224		Q225		Q226		Q227		Q228		Q229		Q230		Q231		Q232		Q233		Q234		Q235		Q236		Q237		Q238		Q239		Q240		Q241		Q242		Q243		Q244		Q245		Q246		Q247		Q248		Q249		Q250		Q251		Q252		Q253		Q254		Q255		Q256		Q257		Q258		Q259		Q260		Q261		Q262		Q263		Q264		Q265		Q266		Q267		Q268		Q269		Q270		Q271		Q272		Q273		Q274		Q275		Q276		Q277		Q278		Q279		Q280		Q281		Q282		Q283		Q284		Q285		Q286		Q287		Q288		Q289		Q290		Q291		Q292		Q293		Q294		Q295		Q296		Q297		Q298		Q299		Q300		Q301		Q302		Q303		Q304		Q305		Q306		Q307		Q308		Q309		Q310		Q311		Q312		Q313		Q314		Q315		Q316		Q317		Q318		Q319		Q320		Q321		Q322		Q323		Q324		Q325		Q326		Q327		Q328		Q329		Q330		Q331		Q332		Q333		Q334		Q335		Q336		Q337		Q338		Q339		Q340		Q341		Q342		Q343		Q344		Q345		Q346		Q347		Q348		Q349		Q350		Q351		Q352		Q353		Q354		Q355		Q356		Q357		Q358		Q359		Q360		Q361		Q362		Q363		Q364		Q365		Q366		Q367		Q368		Q369		Q370		Q371		Q372		Q373		Q374		Q375		Q376		Q377		Q378		Q379		Q380		Q381		Q382		Q383		Q384		Q385		Q386		Q387		Q388		Q389		Q390		Q391		Q392		Q393		Q394		Q395		Q396		Q397		Q398		Q399		Q400		Q401		Q402		Q403		Q404		Q405		Q406		Q407		Q408		Q409		Q410		Q411		Q412		Q413		Q414		Q415		Q416		Q417		Q418		Q419		Q420		Q421		Q422		Q423		Q424		Q425		Q426		Q427		Q428		Q429		Q430		Q431		Q432		Q433		Q434		Q435		Q436		Q437		Q438		Q439		Q440		Q441		Q442		Q443		Q444		Q445		Q446		Q447		Q448		Q449		Q450		Q451		Q452		Q453		Q454		Q455		Q456		Q457		Q458		Q459		Q460		Q461		Q462		Q463		Q464		Q465		Q466		Q467		Q468		Q469		Q470		Q471		Q472		Q473		Q474		Q475		Q476		Q477		Q478		Q479		Q480		Q481		Q482		Q483		Q484		Q485		Q486		Q487		Q488		Q489		Q490		Q491		Q492		Q493		Q494		Q495		Q496		Q497		Q498		Q499		Q500		Q501		Q502		Q503		Q504		Q505		Q506		Q507		Q508		Q509		Q510		Q511		Q512		Q513		Q514		Q515		Q516		Q517		Q518		Q519		Q520		Q521		Q522		Q523		Q524		Q525		Q526		Q527		Q528		Q529		Q530		Q531		Q532		Q533		Q534		Q535		Q536		Q537		Q538		Q539		Q540		Q541		Q542		Q543		Q544		Q545		Q546		Q547		Q548		Q549		Q550		Q551		Q552		Q553		Q554		Q555		Q556		Q557		Q558		Q559		Q560		Q561		Q562		Q563		Q564		Q565		Q566		Q567		Q568		Q569		Q570		Q571		Q572		Q573		Q574		Q575		Q576		Q577		Q578		Q579		Q580		Q581		Q582		Q583		Q584		Q585		Q586		Q587		Q588		Q589		Q590		Q591		Q592		Q593		Q594		Q595		Q596		Q597		Q598		Q599		Q600		Q601		Q602		Q603		Q604		Q605		Q606		Q607		Q608		Q609		Q610		Q611		Q612		Q613		Q614		Q615		Q616		Q617		Q618		Q619		Q620		Q621		Q622		Q623		Q624		Q625		Q626		Q627		Q628		Q629		Q630		Q631		Q632		Q633		Q634		Q635		Q636		Q637		Q638		Q639		Q640		Q641		Q642		Q643		Q644		Q645		Q646		Q647		Q648		Q649		Q650		Q651		Q652		Q653		Q654		Q655		Q656		Q657		Q658		Q659		Q660		Q661		Q662		Q663		Q664		Q665		Q666		Q667		Q668		Q669		Q670		Q671		Q672		Q673		Q674		Q675		Q676		Q677		Q678		Q679		Q680		Q681		Q682		Q683		Q684		Q685		Q686		Q687		Q688		Q689		Q690		Q691		Q692		Q693		Q694		Q695		Q696		Q697		Q698		Q699		Q700		Q701		Q702		Q703		Q704		Q705		Q706		Q707		Q708		Q709		Q710		Q711		Q712		Q713		Q714		Q715		Q716		Q717		Q718		Q719		Q720		Q721		Q722		Q723		Q724		Q725		Q726		Q727		Q728		Q729		Q730		Q731		Q732		Q733		Q734		Q735		Q736		Q737		Q738		Q739		Q740		Q741		Q742		Q743		Q744		Q745		Q746		Q747		Q748		Q749		Q750		Q751		Q752		Q753		Q754		Q755		Q756		Q757		Q758		Q759		Q760		Q761		Q762		Q763		Q764		Q765		Q766		Q767		Q768		Q769		Q770		Q771		Q772		Q773		Q774		Q775		Q776		Q777		Q778		Q779		Q780		Q781		Q782		Q783		Q784		Q785		Q786		Q787		Q788		Q789		Q790		Q791		Q792		Q793		Q794		Q795		Q796		Q797		Q798		Q799		Q800		Q801		Q802		Q803		Q804		Q805		Q806		Q807		Q808		Q809		Q810		Q811		Q812		Q813		Q814		Q815		Q816		Q817		Q818		Q819		Q820		Q821		Q822		Q823		Q824		Q825		Q826		Q827		Q828		Q829		Q830		Q831		Q832		Q833		Q834		Q835		Q836		Q837		Q838		Q839		Q840		Q841		Q842		Q843		Q844		Q845		Q846		Q847		Q848		Q849		Q850		Q851		Q852		Q853		Q854		Q855		Q856		Q857		Q858		Q859		Q860		Q861		Q862		Q863		Q864		Q865		Q866		Q867		Q868		Q869		Q870		Q871		Q872		Q873		Q874		Q875		Q876		Q877		Q878		Q879		Q880		Q881		Q882		Q883		Q884		Q885		Q886		Q887		Q888		Q889		Q890		Q891		Q892		Q893		Q894		Q895		Q896		Q897		Q898		Q899		Q900		Q901		Q902		Q903		Q904		Q905		Q906		Q907		Q908		Q909		Q910		Q911		Q912		Q913		Q914		Q915		Q916		Q917		Q918		Q919		Q920		Q921		Q922		Q923		Q924		Q925		Q926		Q927		Q928		Q929		Q930		Q931		Q932		Q933		Q934		Q935		Q936		Q937		Q938		Q939	
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TABLE III. Group A inspection for device type 05 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D Case C	Pin														Test limits					
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	Min	Max	Unit			
			Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal					
9 T _A = 25°C	t _{PLH1}	3003 (Fig 11)	86	IN	D1	Clear 1	VCC	Clear 2	D2	Clock 2	Preset 2	Q2	Q2	GND	Q1	Q1	J	Clear 1 to Q1	5	25	ns		
			87	J								J	OUT					IN	Preset 1 to Q1	5	25	ns	
			88					IN					IN	OUT					J	Clear 2 to Q2	5	25	ns
	t _{PHL1}	3003 (Fig 11)	89	J					J			IN	OUT					IN	Preset 2 to Q2	5	25	ns	
			90	IN								J	OUT					IN	Clear 1 to Q1	5	25	ns	
			91	J								IN	OUT						Preset 1 to Q1	5	25	ns	
			92					IN				J	OUT						Clear 2 to Q2	5	25	ns	
			93					J				IN	OUT						Preset 2 to Q2	5	25	ns	
	t _{PLH2}	3003 5/ (Fig 12) (Fig 13)	94	IN	IN	5.0 V											OUT	5.0 V	Clock 1 to Q1	5	30	ns	
			95	IN	IN	5.0 V												OUT	5.0 V	Clock 1 to Q1	5	30	ns
			96					5.0 V		IN	IN	5.0 V	OUT						5.0 V	Clock 2 to Q2	5	30	ns
			97					5.0 V		IN	IN	5.0 V	OUT						5.0 V	Clock 2 to Q2	5	30	ns
			98	IN	IN	5.0 V												OUT	5.0 V	Clock 1 to Q1	5	30	ns
t _{PHL2}	3003 (Fig 12) (Fig 13)	99	IN	IN	5.0 V												OUT	5.0 V	Clock 1 to Q1	5	30	ns	
		100					5.0 V		IN	IN	5.0 V	OUT						5.0 V	Clock 2 to Q2	5	30	ns	
		101					5.0 V		IN	IN	5.0 V	OUT						5.0 V	Clock 2 to Q2	5	30	ns	
		102	IN	E	5.0 V	5.0 V											OUT	5.0 V	Q1	5	30	ns	
		103	IN	E	5.0 V	5.0 V											OUT	5.0 V	Q2	5	30	ns	
10 T _A = 125°C	F _{MAX}	(Fig 12)	102	IN	E	5.0 V	5.0 V									OUT	5.0 V	Q1	5	30	ns		
	t _{PLH1}	3003 (Fig 11)	104	IN	E	5.0 V	5.0 V										OUT	5.0 V	Q2	5	30	ns	
			105	IN	E	5.0 V	5.0 V											OUT	5.0 V	Q2	5	30	ns
	t _{PHL1}	3003 (Fig 11)	106	IN													OUT	J	Clear 1 to Q1	5	39	ns	
			107	J													OUT	IN	Preset 1 to Q1	5	39	ns	
			108					IN				J	OUT				OUT	Clear 2 to Q2	5	39	ns		
109							J				IN	OUT				OUT	Preset 2 to Q2	5	39	ns			
t _{PHL1}	3003 (Fig 11)	110	IN													OUT	J	Clear 1 to Q1	5	39	ns		
		111	IN													OUT	IN	Preset 1 to Q1	5	39	ns		
		112					IN				J	OUT				OUT	Clear 2 to Q2	5	39	ns			
113					J				IN	OUT					OUT	Preset 2 to Q2	5	39	ns				

See notes at end of device type 05.

TABLE III. Group A inspection for device type 06

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D														Meas. terminal	Test limits									
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13		14	Min	Max	Unit						
1 T _A = 25°C	V _{OH}	3006	1	0.8 v	10	K1	2.0 v	14	VCC	4.5 v	4	J2	2.0 v	8	J*	0.8 v	10	Q	0.8 v	14	Q	0.8 v	2.4	V			
			2	2.0 v	10	K1	2.0 v	14	VCC	4.5 v	4	J2	0.8 v	8	J*	2.0 v	10	Q	0.8 v	14	Q	2.0 v					
			3																								
			4																								
	V _{OL}	3007	5	2.0 v	10	K1	2.0 v	14	VCC	4.5 v	4	J2	0.8 v	8	J*	0.8 v	10	Q	0.8 v	14	Q	0.8 v	0.4	V			
			6	0.8 v	10	K1	0.8 v	14	VCC	4.5 v	4	J2	2.0 v	8	J*	2.0 v	10	Q	2.0 v	14	Q	2.0 v					
			7																								
			8																								
	V _{IC}		9																								
			10																								
			11																								
			12																								
			13																								
	I _{HL1}	3009	14																								
			15																								
			16																								
			17																								
18																											
19																											
20																											
21																											
22																											
23																											
I _{IH1}	3010	24																									
		25																									
		26																									
		27																									
		28																									
		29																									
		30																									
		31																									
I _{IH2}		32																									
		33																									
		34																									
		35																									
I _{IH3}		36																									
		37																									
I _{IH4}		38																									
		39																									
I _{DS}		40																									
		41																									
I _{CC}		42																									
		43																									
I _{CC}		44																									
		45																									
I _{CC}		46																									
		47																									
I _{CC}		48																									
		49																									
2	Same tests, terminal conditions and limits as for subgroup 1, except T _A = 125°C and VIC tests are omitted.																										
3	Same tests, terminal conditions and limits as for subgroup 1, except T _A = -55°C and VIC tests are omitted.																										

See notes at end of device type 06.

TABLE III. Group A inspection for device type 06 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D														Meas. terminal		Test limits				
			Case C	10	1	2	3	4	5	6	7	8	9	10	11	12	13	14	11	14	Min	Max	Unit
9 TA = 25°C	FMAX (Fig. 15)	93	2.4 v	K1	IN	5.0 v	VCC	5.0 v	Clear	NC	J1	2.4 v	J2	GND	Q	2.4 v	9	11	Q	10		MHz	
	FMAX (Fig. 15)	94	2.4 v		IN	5.0 v					2.4 v			GND	Q	2.4 v			Q	10		MHz	
	tPLH (Fig. 14)	95	5.0 v		0.8 v	IN			IN		5.0 v			GND	Clear to Q	5.0 v			Clear to Q	5	50	ns	
	tPLH (Fig. 14)	96													Clear to Q				Clear to Q				
	tPHL (Fig. 14)	97																					
	tPHL (Fig. 14)	98																					
	tPLH (Fig. 15)	99	3003	2.4 v		IN	5.0 v		5.0 v		2.4 v			GND	OUT	2.4 v			OUT	5	50	ns	
	tPLH (Fig. 15)	100																					
tPHL (Fig. 15)	101																						
tPHL (Fig. 15)	102																						
10 TA = 125°C	FMAX (Fig. 15)	103	2.4 v		IN	5.0 v		5.0 v		2.4 v				GND	OUT	2.4 v			OUT	5	50	ns	
	FMAX (Fig. 15)	104	2.4 v		IN	5.0 v		5.0 v		2.4 v				GND	OUT	2.4 v			OUT	5	50	ns	
	tPLH (Fig. 14)	105	5.0 v		0.8 v	IN			IN		5.0 v			GND	OUT	5.0 v			OUT	5	62	ns	
	tPLH (Fig. 14)	106													Clear to Q	5.0 v			Clear to Q	5	62	ns	
	tPHL (Fig. 14)	107																					
	tPHL (Fig. 14)	108																					
	tPLH (Fig. 15)	109	3003	2.4 v		IN	5.0 v		5.0 v		2.4 v			GND	OUT	2.4 v			OUT	5	62	ns	
	tPLH (Fig. 15)	110																					
tPHL (Fig. 15)	111																						
tPHL (Fig. 15)	112																						
11	Same tests, terminal conditions and limits as subgroup 10, except TA = -55°C.																						

NOTES:

- A - Normal clock pulse.
- B - Momentary GND, then 4.5 v.

- 1/ Terminal conditions (pins not designated may be H > 2.0 v, or L < 0.8 v, or open).
- 2/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
- 3/ Output voltages shall be either: (a) H = 2.4 v, minimum and L = 0.4 v, maximum when using a high speed checker double comparator; or (b) H > 1.5 v and L < 1.5 v when using a high speed checker single comparator.
- 4/ Tests shall be performed in sequence.

TABLE III. Group A inspection for device type 97 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D		Case C		1		2		3		4		5		6		7		8		9		10		11		12		13		14		Test limits	
			Test No.	1	2	Clear	1	Clear	1	Clear	1	D1	Clear	1	VCC	2	Clear	2	D2	1	2	1	2	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2	Min	Max	Unit
9 T _A = 25°C	F _{MAX}	(Fig. 12)	82	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	OUT	5	5	ns														
	t _{PLH}	3003 (Fig. 11)	83	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		84	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		85	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PLH}		86	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		87	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		88	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		89	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		90	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		91	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
	t _{PHL}		92	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns															
t _{PHL}		93	IN	E	5.0 v	5.0 v	5.0 v	5.0 v	E	5.0 v	E	E	IN	IN	IN	IN	OUT	5	5	ns																
t _{PLH}		3003 5/ (Fig. 12) (Fig. 13)	94	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 12)	95	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 13)	96	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 13)	97	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 13)	98	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 12)	99	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 13)	100	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	
t _{PHL}		(Fig. 12)	101	IN	IN	5.0 v	5.0 v	5.0 v	5.0 v	IN	5.0 v	IN	IN	IN	IN	5.0 v	5	5	ns																	

See notes at end of device type 97.

TABLE III. Group A inspection for device type 01 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D		Case C		Pin Connections														Test limits		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit			
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14							
10 T _A = 125°C	FMAX	(Fig. 12)	102	IN	E	5.0 v	Clear 1	5.0 v	D2	IN	IN	5.0 v	OUT	GND	OUT	OUT	Q1	5					
			103	IN	E	5.0 v	Clear 2	5.0 v	E	IN	IN	5.0 v	OUT	GND	OUT	OUT	Q1	5					
			104	IN	E	5.0 v	Clear 2	5.0 v	E	IN	IN	5.0 v	OUT	GND	OUT	OUT	Q1	5					
	tPLH	(Fig. 11)	106	IN	IN	5.0 v	Clear 1	5.0 v									OUT	5	31			ns	
			107	IN	IN	5.0 v	Clear 1	5.0 v										OUT	5	31			ns
			108	IN	IN	5.0 v	Clear 1	5.0 v										OUT	5	31			ns
	tPHL	(Fig. 11)	109	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
			110	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
			111	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
	tPHL	(Fig. 11)	112	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
			113	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
			114	IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
	11	Same tests, terminal conditions and limits as subgroup 10, except T _A = -55°C.	(Fig. 12)	115	IN	IN	5.0 v	Clear 1	5.0 v									OUT	5	31			ns
116				IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
117				IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
118				IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns
119				IN	IN	5.0 v	Clear 1	5.0 v	IN	IN	5.0 v	OUT						OUT	5	31			ns

NOTES:

- A Normal clock pulse.
 - B Momentary GND, then 4.5 v.
 - C Momentary GND, then open.
 - D Momentary 4.5 v, then GND.
 - E Input D connected to Q.
- 1 Terminal conditions (pins not designated may be H ≥ 2.0 v, or L < 0.8 v, or open).
 - 2 Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
 - 3 Output voltages shall be either: (a) H = 2.4 v, minimum and L = 0.4 v, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 v and L < 1.5 v when using a high speed checker single comparator.
 - 4 Tests shall be performed in sequence.
 - 5 Tests shall be performed for both D input pulses (A and B).

- (c) Lead bend in only one direction is required for initial conditioning prior to moisture resistance and salt atmosphere tests.
- (d) High temperature storage test (Method 1008 of MIL-STD-883) conditions:
 - (1) Temperature: $150 \pm 10^\circ \text{C}$.
 - (2) Duration: 1,000 hours, except as otherwise permitted by Appendix B to MIL-M-38510.
- (e) Operating life test (Method 1005 of MIL-STD-883) conditions, or equivalent:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^\circ \text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by Appendix B of MIL-M-38510.
- (f) Omit steady state reverse bias test.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits shall be prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic support.

6.3 Ordering data. The contract or order should specify the following:

- (a) Complete part number (see 1.2).
- (b) ~~Requirements for delivery~~ of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- (c) Requirement for certificate of compliance, if applicable.
- (d) Requirements for notification of change of product or process to procuring activity in addition to notification to qualifying activity, if applicable.
- (e) Requirements for packaging and packing.
- (f) Requirements for failure analysis (including required test condition of Method 5003), corrective action, and reporting of results, if applicable.
- (g) Requirements for product assurance options.
- (h) Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, MIL-STD-1331, and as follows:

GND - - - - Electrical ground (common terminal)

V_{IN} - - - - Voltage level at an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. Microcircuits covered by this specification are substitutable for the following commercial device types:

<u>Device type</u>	<u>Commercial type</u>
01	SN5472 (Circuit A)
01	DM5472 (Circuit B)
01	MC5472 (Circuit C)
02	SN5473 (Circuit A)
02	DM5473 (Circuit B)
02	S5473 (Circuit C)
03	SN54107 (Circuit A)
03	DM54107 (Circuit B)
03	S54107 (Circuit C)
04	SN5476 (Circuit A)
04	DM5476 (Circuit B)
04	S5476 (Circuit C)
05	5474 (Circuit A)
05	DM5474 (Circuit B)
06	5470
07	SN5479 (Circuit A)
07	MC5479 (Circuit B)

Custodians:
 Army - EL
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17

Review activities:
 Army - EL, MI, MU
 Air Force - 11, 17, 80
 DSA - ES
 NASA - NA

Agent:
 DSA - ES

(Project 5962-0071)

User activities:
 Army - SM
 Navy - CG, MC, AS, OS, SH
 Air Force - 19

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