

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 2048-BIT SCHOTTKY, BIPOLAR,
 PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome (NiCr) resistors, tungsten (W) or titanium tungsten (TiW) as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the part number. A special test requirement is included in this specification to screen against devices which may contain excess moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01, 03	512 word/4 bits per word PROM with uncommitted collector
02, 04	512 word/4 bits per word PROM with active pullup and a third high-impedance state output

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}) 1/:	See MIL-M-38510, Appendix C
Output voltage	-0.5 V dc to +V _{CC}
Output sink current	100 mA
Maximum power dissipation (P _D) 2/:	794 mW
Maximum junction temperature (T _J) 3/:	+175°C

- 1/ Heat sinking is recommended to reduce the junction temperature.
 2/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).
 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage range - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V _{IH}) - - -	2.0 V dc
Maximum low-level input voltage (V _{IL}) - - -	0.8 V dc
Normalized fanout (each output) - - - - -	16 mA
Case operating temperature range (T _C) - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Functional block diagrams. The functional block diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -2\text{ mA}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$	02, 04	2.4	---	V
Low-level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 16\text{ mA}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$	01, 02 03, 04	---	0.5	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\text{ V}$, $I_{IN} = -10\text{ mA}$, $T_C = 25^{\circ}\text{C}$	01, 02 03, 04	---	-1.5	V
Maximum collector cut-off current	I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_o = 5.2\text{ V}$	01, 03	---	100	μA
High-impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5\text{ V}$, $V_o = 5.2\text{ V}$	02, 04	---	100	μA
High-impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5\text{ V}$, $V_o = 0.5\text{ V}$	02, 04		-100	μA
High-level input current	I_{IH1}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 5.5\text{ V}$	01, 02 03, 04	---	50	μA
	I_{IH2}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 4.5\text{ V}$, special program- ming pin	01, 02 03, 04	---	100	μA
Low-level input current	I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0.5\text{ V}$	01, 02 03, 04	-1.0	-250	μA
Short circuit output current	I_{OS}	$V_{CC} = 5.5\text{ V}$, $V_o = 0.0\text{ V}$ <u>2/</u>	02, 04	-10	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0$, out- puts = open	01, 02 03, 04	---	140	mA
Propagation delay time, high-to-low level logic, address to output	t_{PHL1}	$V_{CC} = 4.5\text{ V}$ and 5.5 V , $C_L = 30\text{ pF}$ (see figure 5)	01, 02	---	85	ns
			03, 04	---	35	ns
Propagation delay time, low-to-high level logic, address to output	t_{PLH1}		01, 02	---	85	ns
			03, 04	---	35	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C < T _C ≤ +125°C	Device type	Limits		Unit
				Min	Max	
Propagation delay time, high-to-low level logic, enable to output	tPHL2	V _{CC} = 4.5 V and 5.5 V, C _L = 30 pF (see figure 5)	01, 02	---	40	ns
			03, 04	---	20	ns
Propagation delay time, low-to-high level logic, enable to output	tPLH2		01, 02	---	40	ns
			03, 04	---	20	ns

1/ Complete terminal conditions shall be as specified on table III.

2/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical tests (method 5004)	1	1
Final electrical tests (method 5004) for unprogrammed devices	1*,2,3,7*, 8	1*,2,3,7*, 8
Final electrical tests (method 5004) for programmed devices	1*,2,3,7*, 8,9,10,11	1*,2,3,7*, 8,9
Group A electrical tests (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11
Group B electrical tests (method 5005, subgroup 5)	1,2,3,7,8, 9,10,11	N/A
Group C end-point electrical tests (method 5005)	N/A	1,2,3,7,8
Group D end-point electrical tests (method 5005)	1,2,3,7,8	1,2,3,7,8

- * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
- Any or all subgroups may be combined when using high-speed testers.
- Subgroups 7 and 8 shall consist of verifying the pattern specified.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics of table I apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II and (where applicable), the altered item drawing. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing options. Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspections. The following additional criteria shall apply:

- a. Interim and final electrical tests shall be as specified in table II; the interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- b. Burn-in test (method 1015 of MIL-STD-883), using the circuit shown on figure 4, or equivalent.
 - (1) Test condition D or E.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. Freeze-out test: This test shall be conducted as a 100-percent screen on all class S devices having nichrome as the fusing link. Within no more than 24 hours after completion of burn-in and prior to the final electrical test, all devices containing nichrome as the fusing link shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned at 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical tests shall be completed within 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:

- Step 1. Connect devices in the electrical configuration of figure 7 or in the burn-in configuration of figure 4 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - Step 2. Reduce device temperature to $T_A = -10^{\circ}\text{C} \pm 2^{\circ}\text{C}$ with bias cycled and maintain at that temperature for a minimum of 5 hours.
 - Step 3. With the cycled bias maintained, allow T_A to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_A shall not exceed 35°C during this period.
 - Step 4. Remove bias and subject all devices to subgroup 1 final electrical tests to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.
- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 through 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy the programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowed.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1.c.) shall be included in the subgroup 5 tests.
- b. Steady state life test for class S devices shall be in accordance with subgroup 5, table IIa of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883, test condition D or E), using the circuit shown on figure 4 or equivalent.
 - (1) $T_A = +125^\circ\text{C}$ minimum.
 - (2) Test duration = 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross referenced in paragraph 6.6 herein with the manufacturer's symbol or FSCM number.

4.7 Programming procedures for circuit A. The waveforms on figure 6a, the programming characteristics of table IVA, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6a and the programming characteristics of table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.
- c. Apply V_{PL} voltage to V_{CC} .
- d. Bring the \overline{CE}_x inputs high and the CE_x inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.

Text continues on page 24.

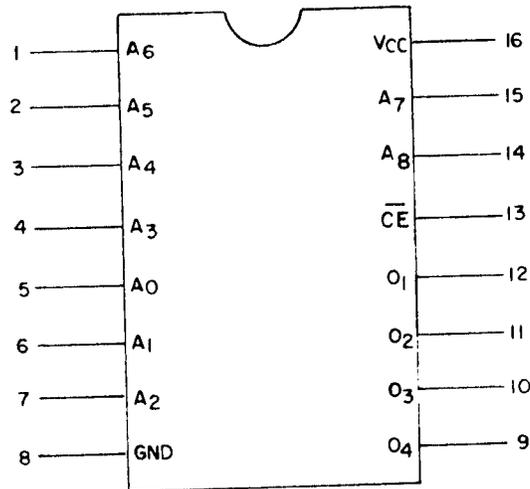


FIGURE 1. Terminal connections.

WORD NO.	CE	ADDRESS									DATA			
		A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₄	O ₃	O ₂	O ₁
NA	L	X	X	X	X	X	X	X	X	X	<u>5/</u>	<u>5/</u>	<u>5/</u>	<u>5/</u>
NA	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be high for circuits A, B, D, and F; and shall be low for circuits C and G.

FIGURE 2. Truth table (unprogrammed).

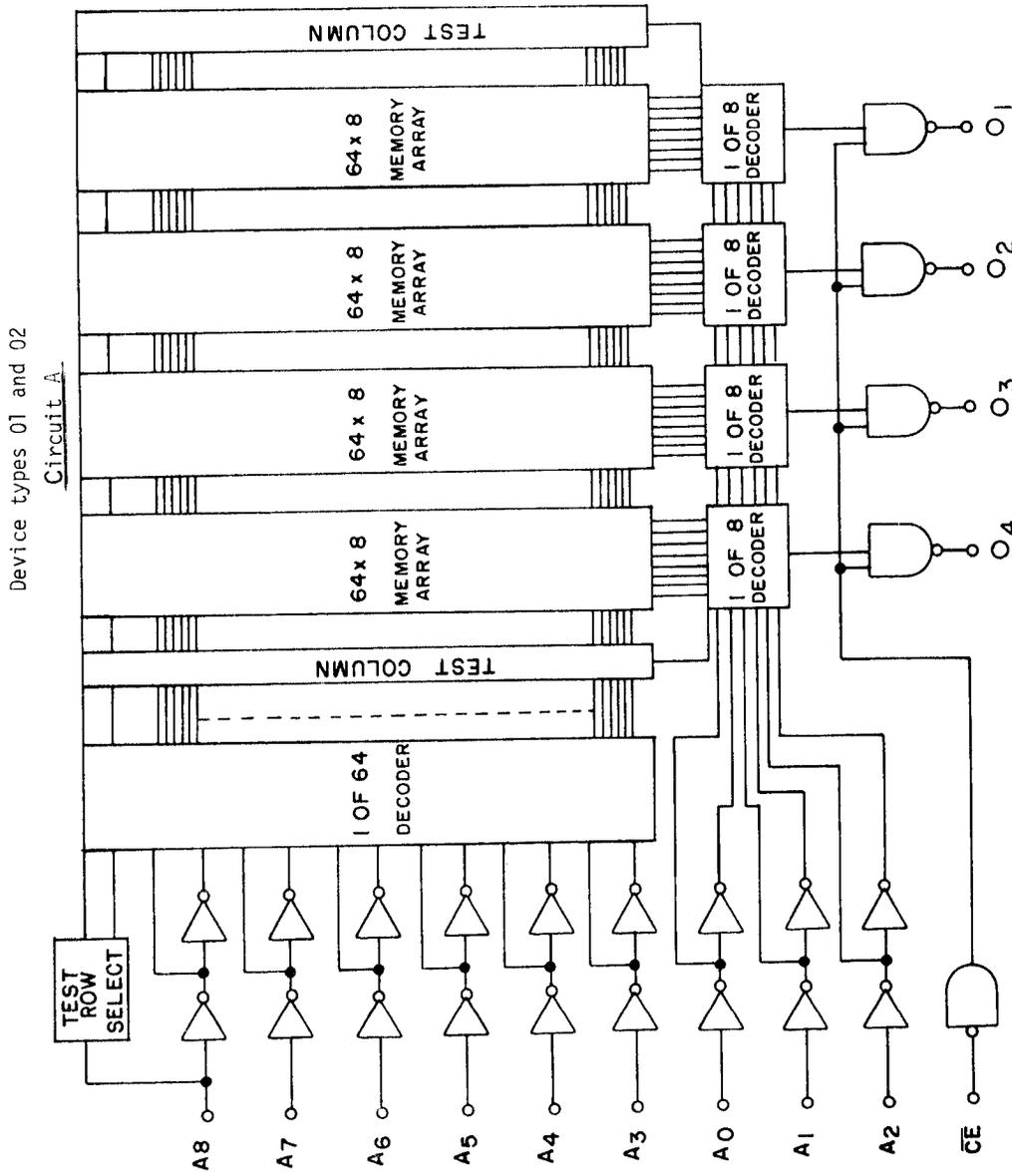


FIGURE 3. Functional block diagrams.

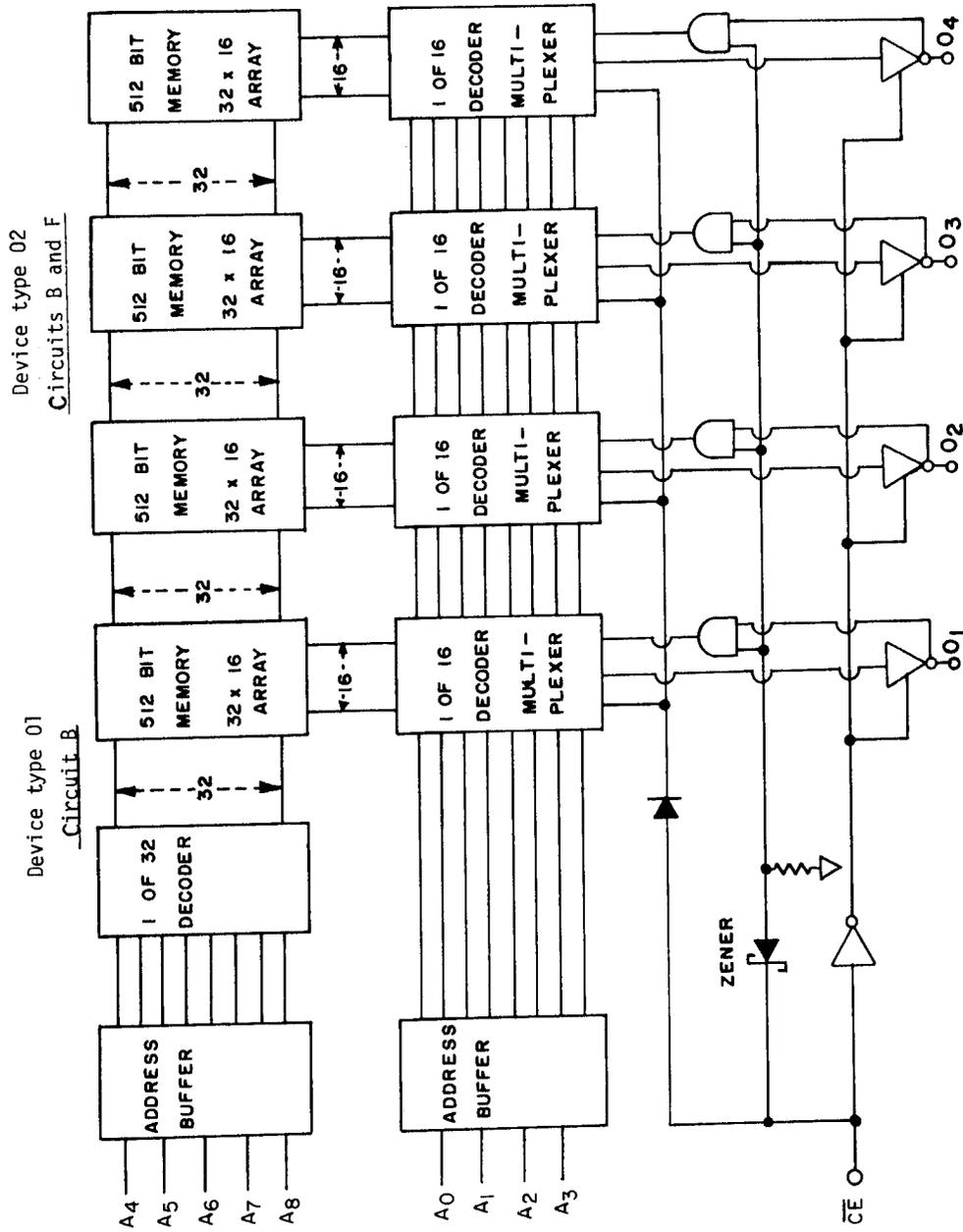


FIGURE 3. Functional block diagrams - Continued.

Device types 01 and 02

Circuit D

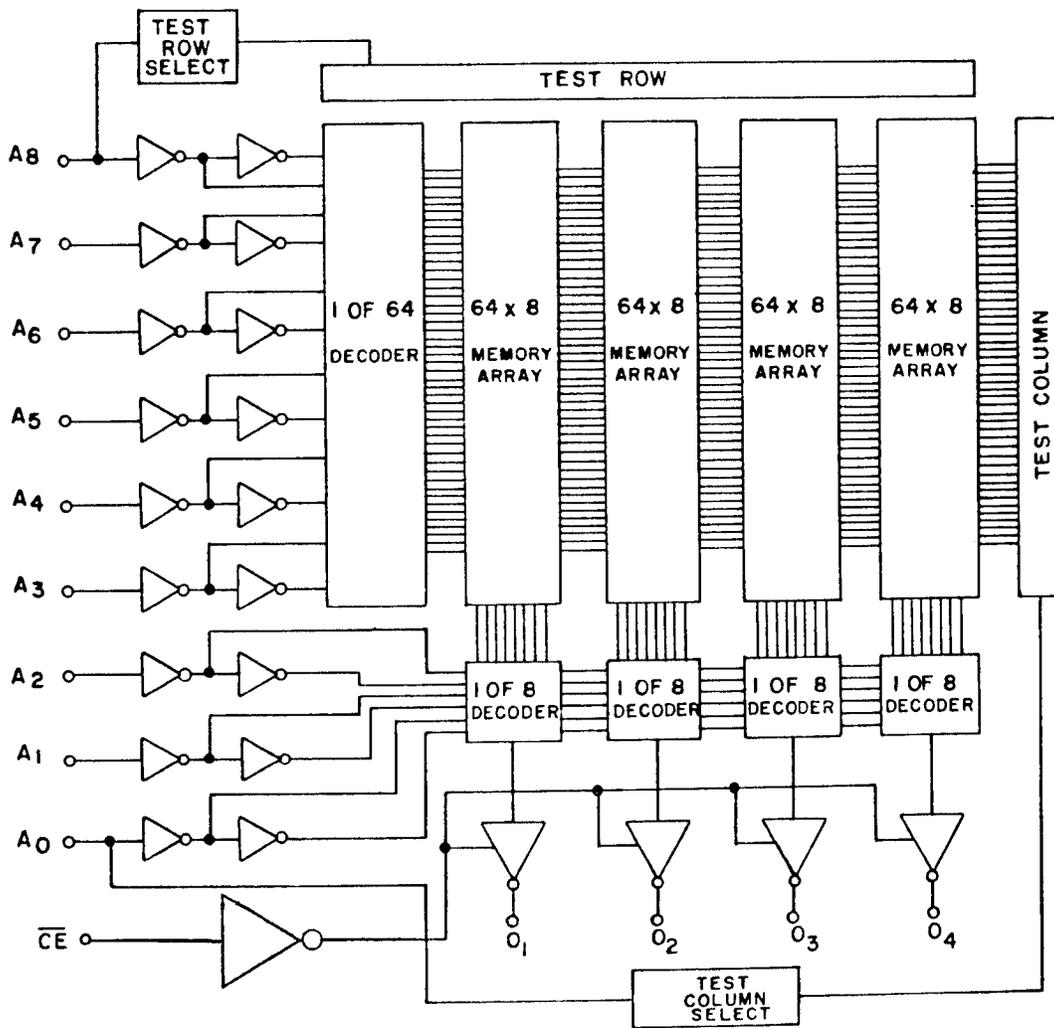


FIGURE 3. Functional block diagrams - Continued.

Device types 01 and 02
Circuit G

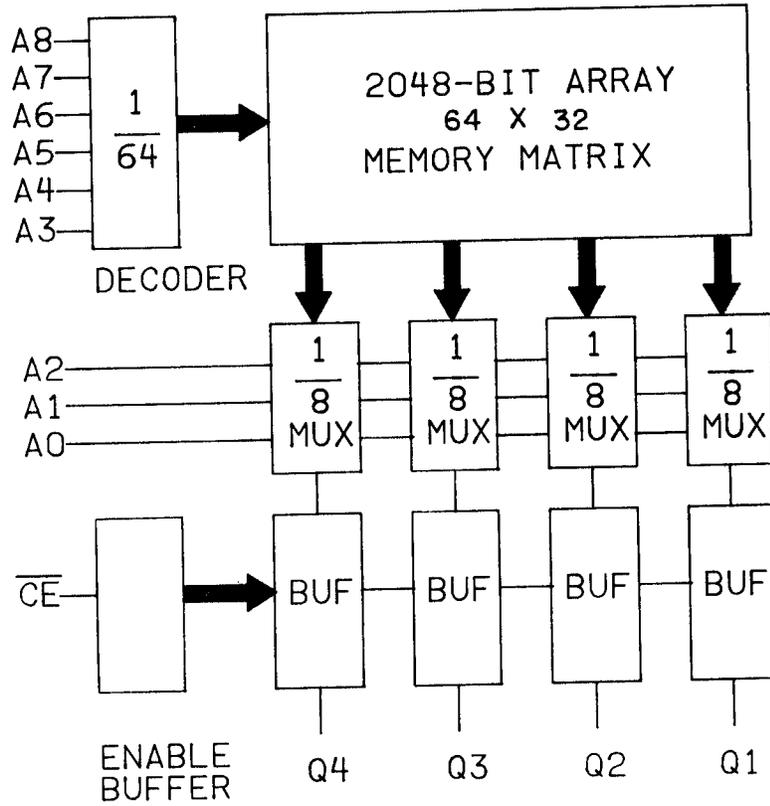
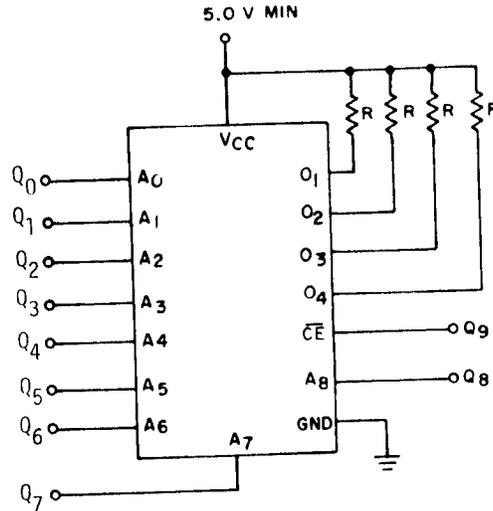


FIGURE 3. Functional block diagrams - Continued.

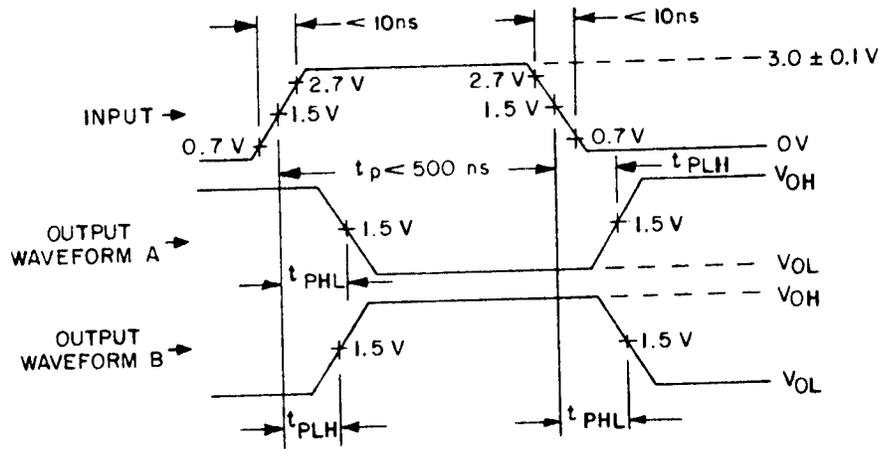
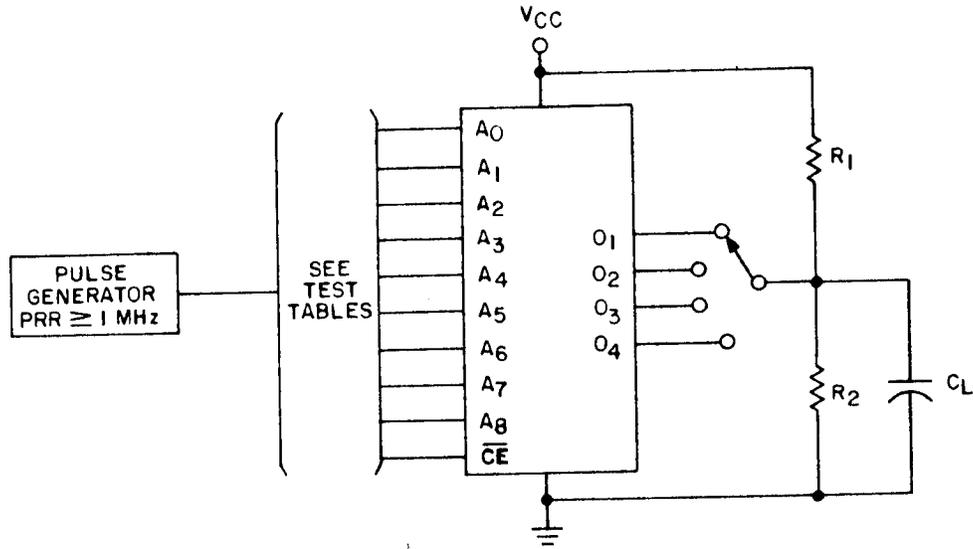


NOTES:

1. $R = 300\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum;
 $50 \pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies ($\pm 50\%$) are as follows:

Input	Frequency
Q ₀	$f_0 = 100$ kHz min.
Q ₁	$f_1 = 1/2 f_0$
Q ₂	$f_2 = 1/2 f_1$
Q ₃	$f_3 = 1/2 f_2$
Q ₄	$f_4 = 1/2 f_3$
Q ₅	$f_5 = 1/2 f_4$
Q ₆	$f_6 = 1/2 f_5$
Q ₇	$f_7 = 1/2 f_6$
Q ₈	$f_8 = 1/2 f_7$
Q ₉	$f_9 = 1/2 f_8$

FIGURE 4. Burn-in and steady state life test circuit.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 660\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

FIGURE 5. Switching time test circuit.

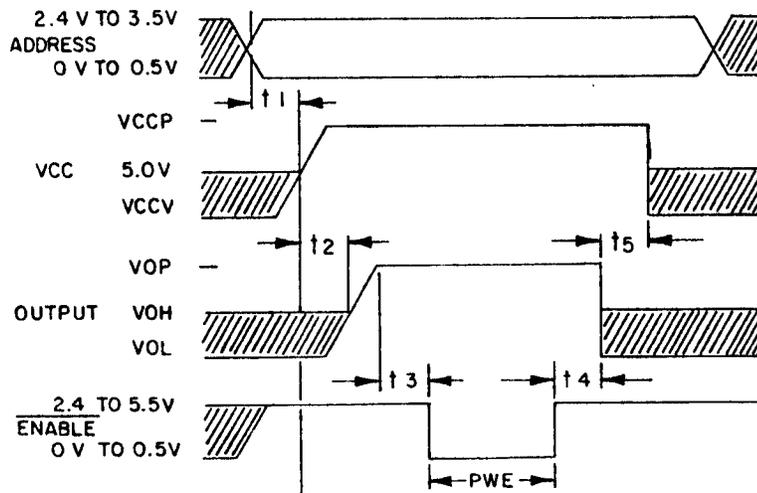
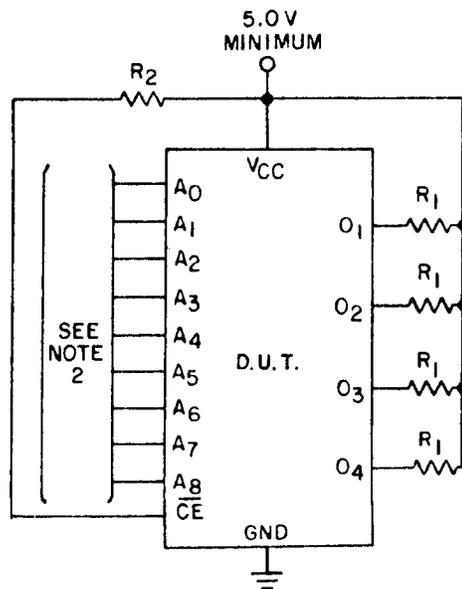


FIGURE 6c. Programming voltage waveforms during programming for circuit G.



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low or open.
2. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
3. Burn-in circuit may be used to perform this test. (See 4.2d.)

FIGURE 7. Freeze-out test bias configuration for device types 01, 02, 03 and 04.

TABLE III. Group A inspection for device type 01 and 03.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage;
inputs not designated are ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
				A6	A5	A4	A3	A0	A1	A2	GND	04	03	01	CE	A8	A7	VCC	Measured terminal	Min	Max	Unit	
1 T _C = 25°C	VIC		1	-10 mA																			
			2	-10 mA																			
			3	-10 mA																			
			4	-10 mA																			
			5	-10 mA																			
			6	-10 mA																			
			7	-10 mA																			
			8	-10 mA																			
			9	-10 mA																			
			10	-10 mA																			
VOL 18/ 10/		3007	11																				
			12																				
			13																				
			14																				
I _{IL}		3009	15	0.5 V																			
			16	0.5 V																			
			17	0.5 V																			
			18	0.5 V																			
			19	0.5 V																			
			20	0.5 V																			
			21	0.5 V																			
			22	0.5 V																			
			23	0.5 V																			
			24	0.5 V																			
I _{IH1}		3010	25	5.5 V																			
			26	5.5 V																			
			27	5.5 V																			
			28	5.5 V																			
			29	5.5 V																			
			30	5.5 V																			
			31	5.5 V																			
I _{IH2}			34																				
			34																				
I _{CEX}			35																				
			36																				
			37																				
			38																				
I _{CC}		3005	39																				
			39																				
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																						

See footnotes at end of table.

TABLE III. Group A Inspection for device type 01 and 03 - Continued.
 Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage;
 inputs not designated are ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		
				A6	A5	A4	A3	A0	A1	A2	GND	04	03	02	01	CE	A8	A7	V _{CC}	Measured terminal	Min	Max
7	Functional test	3014	40	5/	5/	5/	5/	5/	5/	5/	GND	5/	5/	5/	5/	5/	5/	5/	5/	Outputs	5/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = 125°C and -55°C.																					
9 T _C = 25°C	tpLH1	GALPAT (Fig. 5)	41	6/	6/	6/	6/	6/	6/	6/	GND	8/	8/	8/	8/	8/	GND	6/	6/	Outputs	16/	ns
	tpHL1	GALPAT (Fig. 5)	42	6/	6/	6/	6/	6/	6/	6/							GND	6/	6/			
	tpLH2	Sequential (Fig. 5)	43	7/	7/	7/	7/	7/	7/	7/							7/	7/	7/			
	tpHL2	Sequential (Fig. 5)	44	7/	7/	7/	7/	7/	7/	7/							7/	7/	7/			
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = 125°C.																					
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																					

See footnotes at end of table.

TABLE III. Group A inspection for device type 02 and 04.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage;
inputs not designated are ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E _F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits									
				A6	A5	A4	A3	A0	A1	A2	GND	04	03	02	01	CE	A8	A7	V _{CC}	Measured terminal	Min	Max	Unit						
1 T _C = 25°C	V _{IC}		1	-10 mA	GND	GND								4.5 V	A6	-1.5	V												
				2																									
				3																									
				4																									
				5																									
				6																									
				7																									
				8																									
				9																									
				10																									
3007	V _{OL} 18/ 10/		11									16 mA	16 mA	16 mA	16 mA	0.5 V	0.5 V				04	0.5	V						
				12																									
				13																									
				14																									
3006	V _{OH} 19/ 10/		15									-2 mA	-2 mA	-2 mA	-2 mA						04	2.4	V						
				16																									
				17																									
				18																									
3009	I _{IL}		19	0.5 V										5.5 V	A6	-1.0	-250	μA											
				20																									
				21																									
				22																									
				23																									
				24																									
				25																									
				26																									
				27																									
				28																									
3010	I _{IHI}		29	5.5 V											A6	50	V												
				30																									
				31																									
				32																									
				33																									
				34																									
				35																									
36																													
37																													
	I _{IHQ} 15/		38													4.5 V					CE	100	V						
	I _{OHZ}		39									5.2 V				04		V											
				40																									
				41																									
				42																									
	I _{OLZ}		43									0.5 V				04	-100	V											
				44																									
				45																									
				46																									

See footnotes at end of table.

- 1/ For unprogrammed devices (circuit B), apply 12.0 to 15.0 V on pin 1 (A_6).
- 2/ For programmed devices, select an appropriate address to acquire the desired output state, $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V.
- 3/ For unprogrammed devices (circuit D), apply 10.8 V on pin 5 (A_0).
- 4/ For unprogrammed devices (circuit A), apply 13.0 V on pins 1 (A_6) and 2 (A_5).
- 5/ The functional test shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. The functional tests shall be performed with $V_{CC} = 4.5$ V and $V_{CC} = 5.5$ V. Terminal conditions shall be as follows:
 - a. Inputs: $H = 3.0$ V, $L = 0.0$ V.
 - b. Outputs: Output voltage shall be:
 $H \geq 1.0$ V and $L < 1.0$ V
- 6/ GALPAT (PROGRAMMED PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PLH1} and t_{PHL1} . Each bit in the pattern is fixed by being programmed with an "H" or "L". The GALPAT tests shall be performed with $V_{CC} = 4.5$ V and 5.5 V.

Description:

- Step 1. Word 0 is read.
 - Step 2. Word 1 is read.
 - Step 3. Word 0 is read.
 - Step 4. Word 2 is read.
 - Step 5. Word 0 is read.
 - Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 511 is reached, then increments to the next word and reads back and forth as in step 1 through step 6 and shall include all words.
 - Step 7. Pass execution time = $(n^2 + n) \times$ cycle time. $n = 512$.
- 7/ SEQUENTIAL (PROGRAMMED PROM). This program will test all bits in the array for t_{PLH2} and t_{PHL2} . The sequential tests shall be performed with $V_{CC} = 4.5$ V and 5.5 V.

Description:

- Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
 - Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t_{PLH2} and t_{PHL2} are read.
 - Step 3. Word 1 is addressed. Same enable sequence as above.
 - Step 4. The reading procedure continues until word 511 is reached.
 - Step 5. Pass execution time = $512 \times$ cycle time.
- 8/ The outputs are loaded per figure 5.
 - 9/ For unprogrammed devices (circuit F), apply 12.0 V on pin 5 (A_0) and 0.0 V on pin 4 (A_3).
 - 10/ The V_{OL} and V_{OH} test shall be performed with $V_{CC} = 4.5$ V.
 - 11/ For unprogrammed 02 devices (circuit C), apply 10.0 V on pin 14 (A_8); 0.5 V on pins 3 (A_4), 2 (A_5), and 1 (A_6); and 5.0 V on all other addresses.
 - 12/ For unprogrammed device type 01 and 02 (circuit G) select an appropriate address to obtain the desired output state.
 - 13/ For programmed device type 01 and 02 (circuit G) apply 10.5 V to pin 2 and 7; 4.5 V to pin 16; 3.0 V to pins 1, 3, 4, 5, 6, 14, and 15; 0.0 V to pins 8 and 13.

- 14/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 7 and 2; 4.5 V to pin 16; 3.0 V to pins 1, 4, 5, 6, 14 and 15; 0.0 V to pins 3, 8, and 13.
- 15/ At the manufacturer's option, this may be performed with $V_{IH} = 5.5$ V and test limits of 50 μ A maximum.
- 16/

Device 01, 02		Device 03, 04	
tPLH1	85 ns	tPLH1	35 ns
tPHL1	85 ns	tPHL1	35 ns
tPLH2	40 ns	tPLH2	20 ns
tPHL2	40 ns	tPHL2	20 ns

- 17/ For unprogrammed 04 devices (circuit C) apply 10.0 V on pin 5 (A0) and 5.0 V on all other address pins.
- 18/ V_{OL} conditions are as follows:

Test	Ckt A	B	C	D	F	G
V_{OL}	<u>2/ 4/</u>	<u>1/ 2/</u>	<u>2/</u>	<u>2/ 3/</u>	<u>2/ 9/</u>	<u>13/</u>

- 19/ V_{OH} conditions are as follows:

Test	Ckt A	B	C	D	F	G
V_{OH}	<u>2/</u>	<u>2/</u>	<u>2/ 11/</u> <u>17/</u>	<u>2/</u>	<u>2/</u>	<u>2/ 14/</u>

- e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.
- f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH} .
- g. After a delay equal to or greater than t_{D1} apply only one pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
- h. Lower V_{CC} to V_{PL} following a delay of t_{D2} from programming enable pulse applied to an output.
- i. Enable the PROM for verification by applying V_{IL} to \overline{CE}_x and V_{IH} to CE_x .
- j. Apply V_{PHV} to V_{CC} and verify bit is programmed.
- k. Repeat steps a through j for all other bits to be programmed in the PROM.
- l. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits ^{1/}			Unit	
		Min	Recommended	Max		
Address input voltage ^{2/}	V_{IH}	2.4	5.0	5.0	Volts	
	V_{IL}	0.0	0.4	0.5	"	
Programming Voltage to V_{CC} low	V_{PH} ^{3/}	10.75	11.0	11.25	"	
Program verify	V_{PHV}	---	5.5	---	"	
Verify voltage	V_R ^{4/}	4.5	---	5.5	"	
Programming input low current at V_{PH}	I_{ILP}	---	-300	-600	μA	
Programming voltage (V_{CC}) transition time	t_{TLH}	1	5	10	μs	
	t_{THL}	1	5	10	"	
Programming delay	t_{D1}	10	10	20	"	
	t_{D2}	1	5	5	"	
Programming pulse width	t_p ^{5/}	90	100	110	"	
Programming duty cycle	PDC	---	30	60	%	
Output voltage	Enable	V_{OPE}	10.5	10.5	11.0	Volts
	Disable	V_{OPD} ^{6/}	0.0	5.0	5.5	Volts

During the programming the chip must be disabled for proper operation.

NOTES:

1/ $T_C = 25^\circ C$.

2/ No inputs should be left open for V_{IH} .

3/ V_{PH} source must be capable of supplying one ampere.

4/ It is recommended that post programming dual verification be made at V_R min and V_R max.

5/ Note step j in programming procedure.

6/ V_{OPE} source must be capable of supplying 10 mA minimum.

4.8 Programming procedures for circuit C. The waveforms on figure 6b, the programming characteristics of table IVB, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all device outputs with a 10-kilohm resistor to V_{CC} .
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a t_D delay (10 μ s), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.
- e. After a t_D delay (10 μ s), pulse \overline{CE} input to logic "0" for a duration of t_p .
- f. After a t_D delay (10 μ s), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 6b.
- h. Repeat 4.8c through 4.8g for all other bits to be programmed.
- i. To verify programming after t_D (10 μ s) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both CE inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVB. Programming characteristics for circuit C.

Characteristics	Symbol	Conditions	Limits			Unit
			Min	Recom- mended	Max	
Programming voltage to V_{CC}	V_{CCP} 1/	$I_{CCP} = 375 \pm 75$ mA, transient or steady state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	$V_{CCP} = 8.75 \pm .25$ V	300		450	mA
Input voltage, high level "1"	V_{IH}		2.4		5.5	V

See footnotes at end of table.

TABLE IVB. Programming characteristics for circuit C - Continued.

Characteristics	Symbol	Conditions	Limits			Unit
			Min	Recom- mended	Max	
Input voltage, low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	$V_{IH} = 5.5$ V			50	μ A
Input current	I_{IL}	$V_{IL} = 0.4$ V			-500	μ A
Output programming voltage	V_{OUT} ^{3/}	$I_{OUT} = 200 \pm 20$ mA, transient or steady state	16	17	18	V
Output programming current	I_{OUT}	$V_{OUT} = 17 \pm 1$ V	180	200	220	mA
Programming voltage transition time	t_{TLH}		10		50	μ s
\overline{CE} programming pulse width	t_p		300	400	500	μ s
Pulse sequence delay	t_D		10			μ s

1/ Bypass V_{CC} to GND with a 0.01 μ F capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ± 1 output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4.9 Programming procedure for circuit G. The programming characteristics on table IVC and the following procedures shall be used for programming:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6c and the programming characteristics of table IVC shall apply to these procedures.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more active low chip enable inputs. NOTE: Address and enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase V_{CC} from nominal to V_{CCP} (10.5 ± 0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 v/ μ s). Since V_{CC} is the source of the current required to program the fuse, as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.

- d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ± 0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 V/ μ s). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP} , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kilohms minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip enable(s) to a low level. This is done with a pulse PWE for 10 μ s. The 10 μ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 V (± 0.25 V). The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.
- g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of step f is to be performed at a V_{CC} level of 4.0 volts (plus or minus 0.2 V). V_{OH} , during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.
- h. Repeat steps 4.9b thru 4.9f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.
- i. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVC. Programming characteristics for circuit G.

Characteristic	Symbol	Conditions	Limits <u>1/</u>		Max	Unit
			Min	Recom- mended		
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	$V_{CC} = 11$ V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.0	11.0	V
Output current while programming	I_{OP}	$V_{OUT} = 11$ V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/ μ s

See footnotes at end of table.

TABLE IVC. Programming characteristics for circuit G - Continued.

Characteristic	Symbol	Conditions	Limits <u>1/</u>		Max	Unit
			Min	Recom- mended		
Programming pulse width (enabled)	P_{WE}		9	10	11	μs
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address setup time	t_1		100			ns
V_{CCP} setup time	t_2	<u>2/</u>	5			μs
V_{CCP} hold time	t_5		100			ns
V_{OP} setup time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ $T_C = 25^\circ C$

2/ V_{CCP} setup time may be >0 if V_{CCP} rises at the same rate or faster than V_{OP} .

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The acquisition documents should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.

- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- i. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal).
IIN	- - - - -	Current flowing into an input terminal.
VIC	- - - - -	Input clamp voltage.
VIN	- - - - -	Voltage level at an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type/manufacturer</u>	<u>Circuit designator</u>	<u>Fusible link</u>	<u>Symbol/FSCM number</u>
01	7620/Harris Corporation	A	NiCr	CDW0/34371
01	54S570/National Semiconductor	G	TiW/W	CCXP/27014
01	5305-1/Monolithic Memories, Inc.	B	NiCr	CECD/50364
01, 03	82S130A/Signetics Corporation	C	NiCr	CDKB/18324
01	93436/Fairchild Corporation	D	NiCr	CFJ/07263
02	7621/Harris Corporation	A	NiCr	---
J2	5305-1/Monolithic Memories, Inc.	B	NiCr	---
02, 04	82S131A/Signetics Corporation	C	NiCr	---
02	93446/Fairchild Corporation	D	NiCr	---
02	29611/Raytheon Company	F	NiCr	CRP/07933
02	54S571/National Semiconductor	G	TiW/W	---

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0905)