

Thermal resistance, junction-to-case (θ_{JC}) <u>1/</u> :	
Cases E, F, and V - - - - -	See MIL-M-38510, appendix C
Case Y - - - - -	30°C/W <u>2/</u>
Case Z - - - - -	0.08°C/W
Output voltage applied - - - - -	-0.5 V dc to +V _{CC}
Output sink current - - - - -	100 mA
Maximum power dissipation (P _D) <u>3/</u> - - - - -	794 mW dc
Maximum junction temperature (T _J) - - - - -	+175°C <u>4/</u>

1.4 Recommended operating conditions.

Supply voltage range (V _{CC}) - - - - -	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage (V _{IH}) - - - - -	2.0 V dc
Maximum low-level input voltage (V _{IL}) - - - - -	0.8 V dc
Normalized fanout (each output) - - - - -	16 mA
Case operating temperature range (T _C) - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in tis specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

- 1/ Heat sinking is recommended to reduce the junction temperature.
- 2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
- 3/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).
- 4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 4. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V};$ $I_{OH} = -2\text{ mA}$ $V_{IL} = 0.8\text{ V};$ $V_{IH} = 2.0\text{ V}$	02, 03, 04	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V};$ $I_{OL} = 16\text{ mA}$ 2/ $V_{IL} = 0.8\text{ V};$ $V_{IH} = 2.0\text{ V}$	01,02, 03,04		0.5	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\text{ V};$ $I_{IN} = -12\text{ mA};$ $T_C = +25^{\circ}\text{C}$	01,02, 03,04		-1.5	V
Maximum collector cut-off current	I_{CEX}	$V_{CC} = 5.5\text{ V};$ $V_{OH} = 5.2\text{ V}$	01		100	μA
High-impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5\text{ V};$ $V_{OH} = 5.2\text{ V}$	02,04		100	μA
High-impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5\text{ V};$ $V_{OL} = 0.5\text{ V}$	02,04		-100	μA
High level input current	I_{IH1}	$V_{CC} = 5.5\text{ V};$ $V_{IN} = 5.5\text{ V}$	01,02, 03,04		50	μA
High level input current	I_{IH2}	$V_{CC} = 5.5\text{ V};$ $V_{IN} = 4.5\text{ V}$ Special program pin	01,02, 04		100	μA
Low level input current	I_{IL}	$V_{CC} = 5.5\text{ V};$ $V_{IN} = 0.5\text{ V}$	01,02, 03,04	-1.0	-250	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Short circuit output current	I_{OS}	$V_{CC} = 5.5\text{ V};$ $V_O = 0.0\text{ V}$ <u>3/</u>	02,03, 04	-10	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5\text{ V};$ $V_{IN} = 0$ outputs open	01,02, 03,04		140	mA
Propagation delay time, high to low level logic, address to output	t_{PHL1}	$V_{CC} = 5.5\text{ V}$ and 4.5 V $C_L = 30\text{ pF}$	01,02, 03 04		85 55	ns
Propagation delay time, low to high level logic, address to output	t_{PLH1}	See figure 6	01,02 03 04		85 55	ns
Propagation delay time, high to low level logic, enable to output	t_{PHL2}		01,02, 03 04		40 35	ns
Propagation delay time, low to high level logic, enable to output	t_{PLH2}		01,02 04		40 35	ns

1/ Complete terminal conditions shall be specified in table III.

2/ $I_{OL} = 8\text{ mA}$ for circuit A only.

3/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

3.5 Electrical test requirements. The electrical test requirements shall be as specified in table II and where applicable, the altered item drawing. The electrical tests for each subgroup are described in table III.

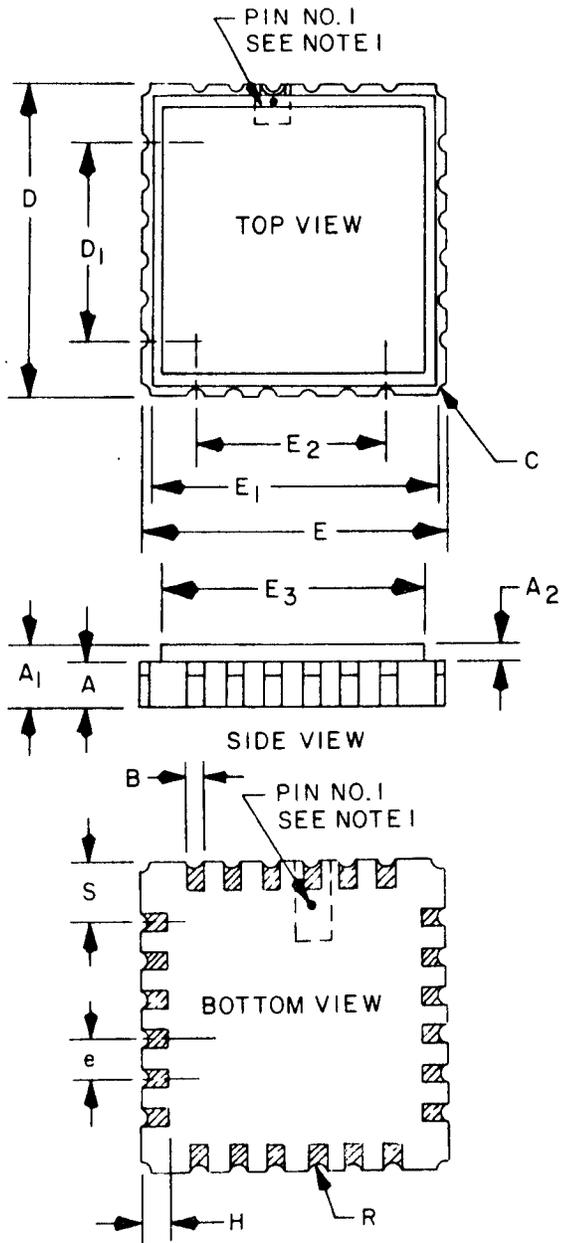
TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) <u>1/</u> , <u>2/</u> , <u>3/</u>	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7,*8	1*,2,3,7,*8
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*, 8,9,10,11	1*,2,3,7*, 8,9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8,9, 10,11
Group B end-point electrical parameters (method 5005) subgroup 5	1,2,3,7,8, 9,10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3,7,8
Group D test requirements (method 5005)	1,2,3,7,8	1,2,3,7,8

1/ * indicates PDA applies to subgroups 1 and 7 (see 4.2c).

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

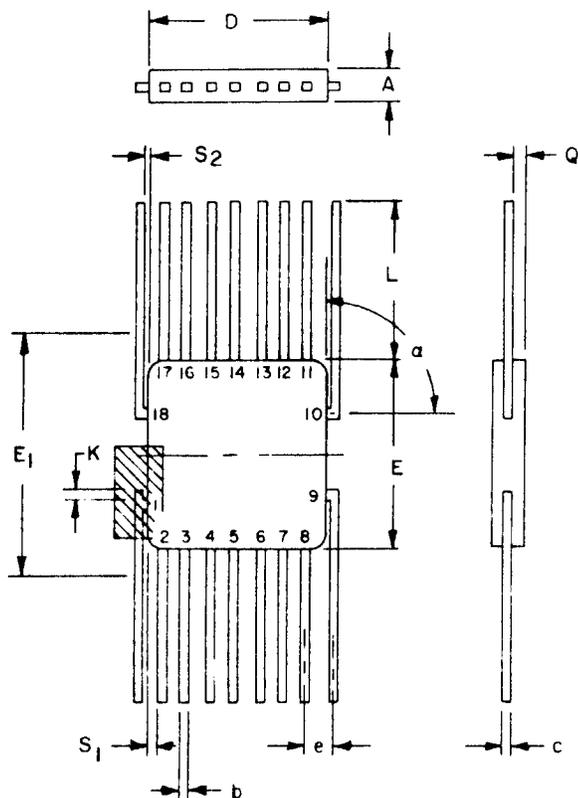


Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.053	.088	1.35	2.24	
A ₁	.064	.100	1.63	2.54	
A ₂	.010	.022	0.25	0.56	
B	.018	.028	0.46	0.71	3,4
C	.012R	---	0.30R	---	2
D	.395	.410	10.03	10.41	
D ₁	.250		6.35		7
E	.395	.410	10.03	10.41	
E ₁	.372	.388	9.45	9.86	6
E ₂	.250		6.35		7
E ₃	.352	.358	8.94	9.09	
e	.050 BSC		1.27 BSC		7
H	.030	.035	0.76	0.89	
R	.008R	---	0.20R	---	4
S	.065	.085	1.65	2.16	

NOTES:

1. Index area: A notch, identification mark or elongation shall be used to identify pin 1.
2. Applies to all four corners. Corners may also be chamfered.
3. Shaded areas are metallized.
4. 24 Locations.
5. No organic or polymeric materials shall be molded to the package.
6. Sealing metallization.
7. Dimensions vary in direct proportion to feature size of D and E.

FIGURE 1. Case outline Y (24 terminal, 0.40" x 0.40", chip carrier).



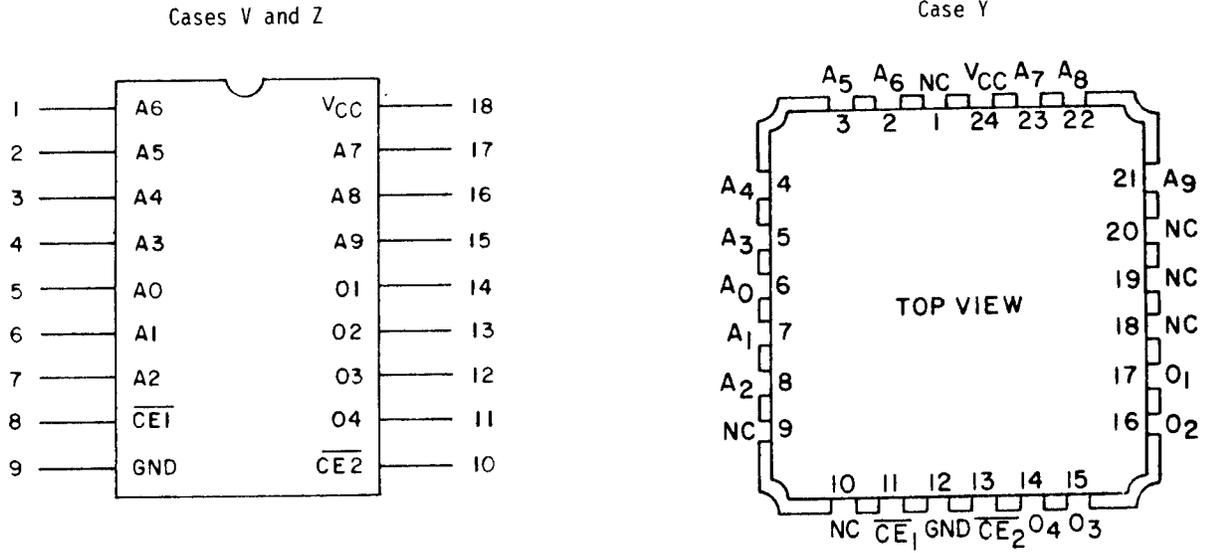
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.045	.085	1.14	2.16	
b	.014	.017	0.36	0.43	5
c	.003	.006	0.08	0.15	5
D		.380		9.65	3
E	.340	.380	8.64	9.65	
E ₁		.400		10.16	3
e	.050 BSC		1.27 BSC		4,6
K	.008	.015	0.20	0.38	9
L	.250	.370	6.35	9.40	
Q	.010	.040	0.25	1.02	2
S ₂	.004		0.10		10
S ₁	.005		0.13		7,8
alpha	30°	90°	30°	90°	11

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dim K) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 18.
5. All leads - increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads number 2, 8, 11, and 17).
8. Dimension S₁ may be .000 (0.00 mm) if leads number 2, 8, 11, and 17 bend toward the cavity of the package within one lead width from the point of entry of the lead, into the body or if the leads are brazed to the metallized ceramic body (see appendix C of MIL-M-38510).
9. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension K does not apply.
10. Applies to leads number 1, 9, 10, and 18.
11. Lead configuration is optional within dimension E except dimensions b and c apply (see appendix C of MIL-M-38510).

FIGURE 1. Case outline Z (18-lead, 3/8" x 3/8") - Continued.

Device types 01, 02 and 04



Device type 03

Cases E and F

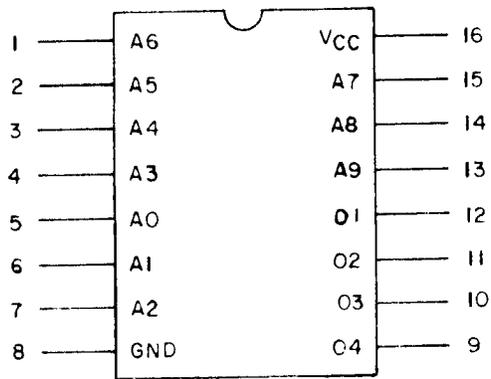


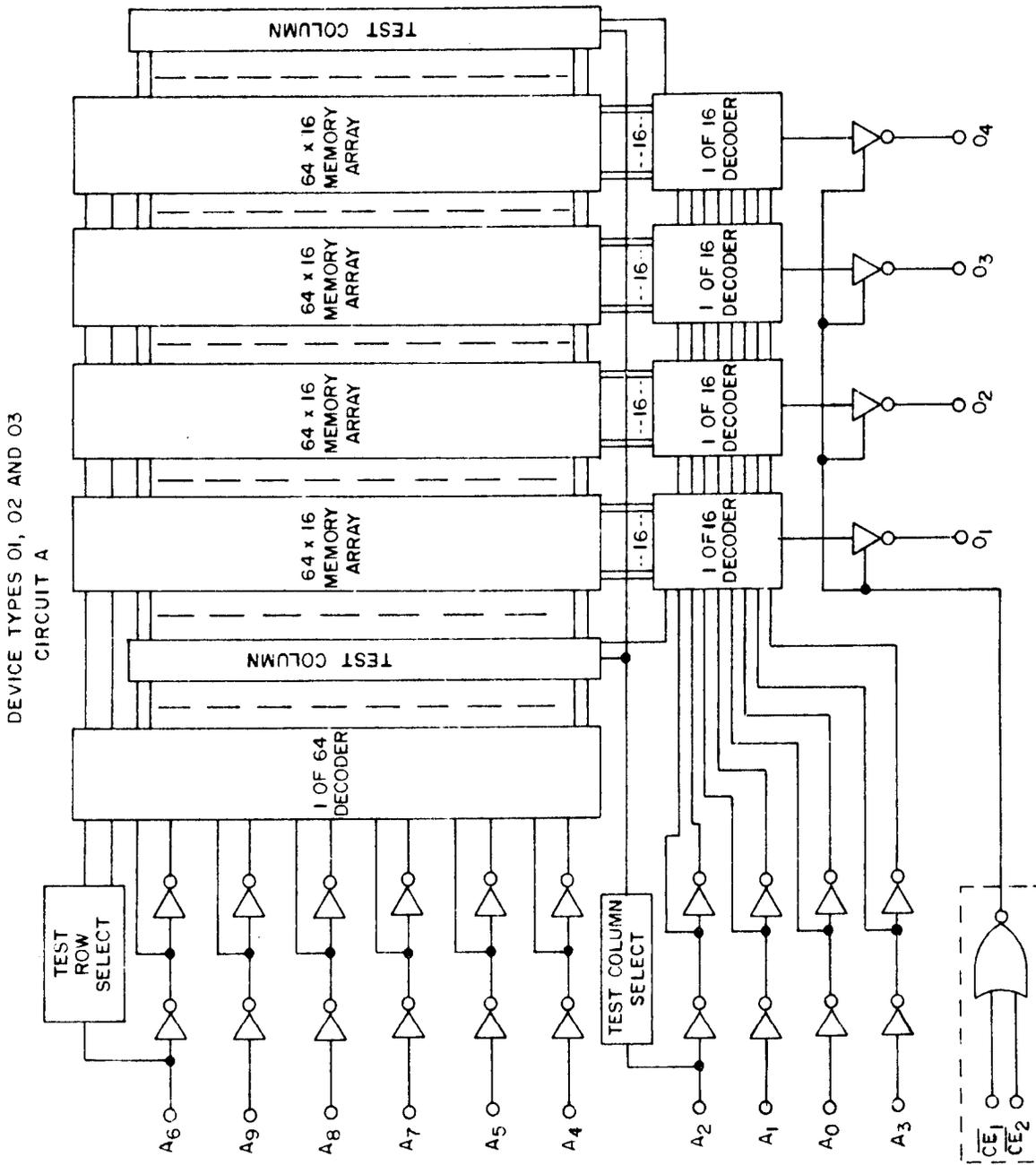
FIGURE 2. Terminal connections.

Word no.	Enable		Address										Data			
	$\overline{CE1}$	$\overline{CE2}$	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	01	02	03	04
NA	L	L	X	X	X	X	X	X	X	X	X	X	<u>5/</u>	<u>5/</u>	<u>5/</u>	<u>5/</u>
NA	L	H	X	X	X	X	X	X	X	X	X	X	0C	0C	0C	0C
NA	H	L	X	X	X	X	X	X	X	X	X	X	0C	0C	0C	0C
NA	H	H	X	X	X	X	X	X	X	X	X	X	0C	0C	0C	0C

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. 0C = Open circuit (high resistance output).
4. Program readout can only be accomplished with both enable inputs at low level.
5. The outputs for an unprogrammed device shall be high for circuits A, and D, and shall be low for circuit B, C, and G.

FIGURE 3. Truth table (unprogrammed).



Dashed line indicates no enable circuitry for device type 03.

FIGURE 4. Functional block diagram.

CIRCUIT B

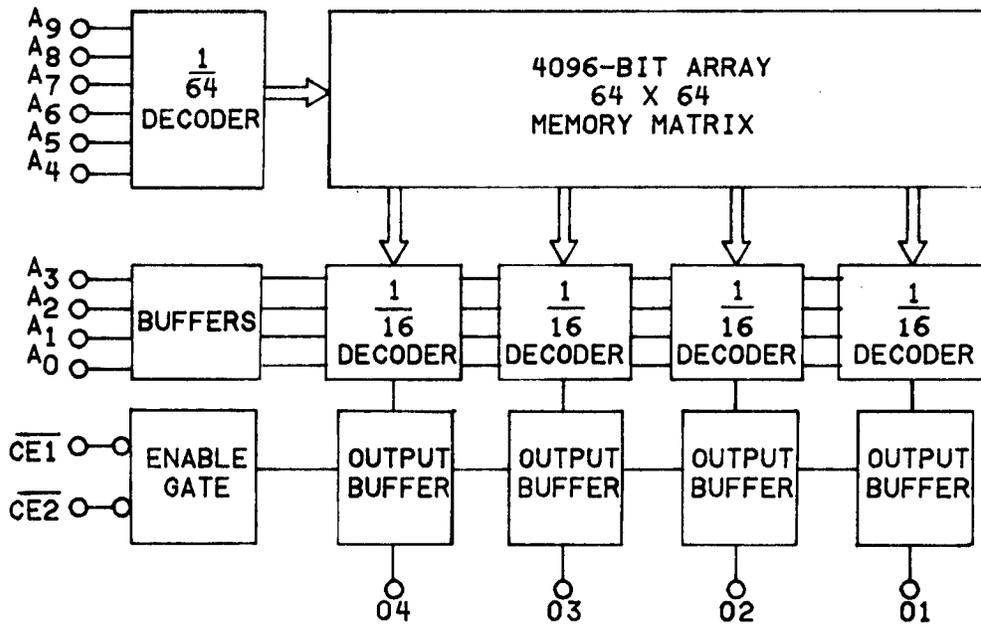


FIGURE 4. Functional block diagram - Continued.

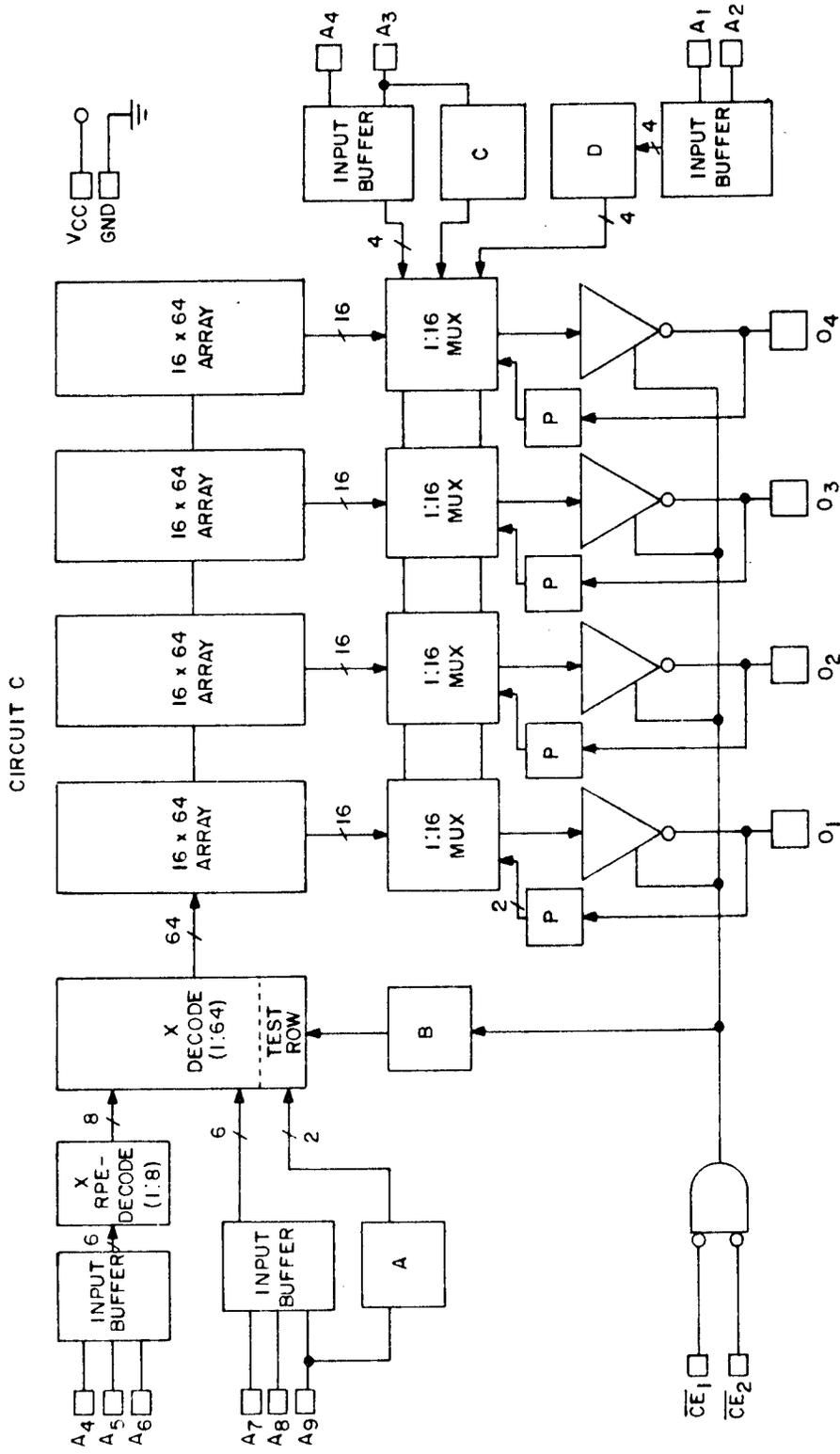


FIGURE 4. Functional block diagram - Continued.

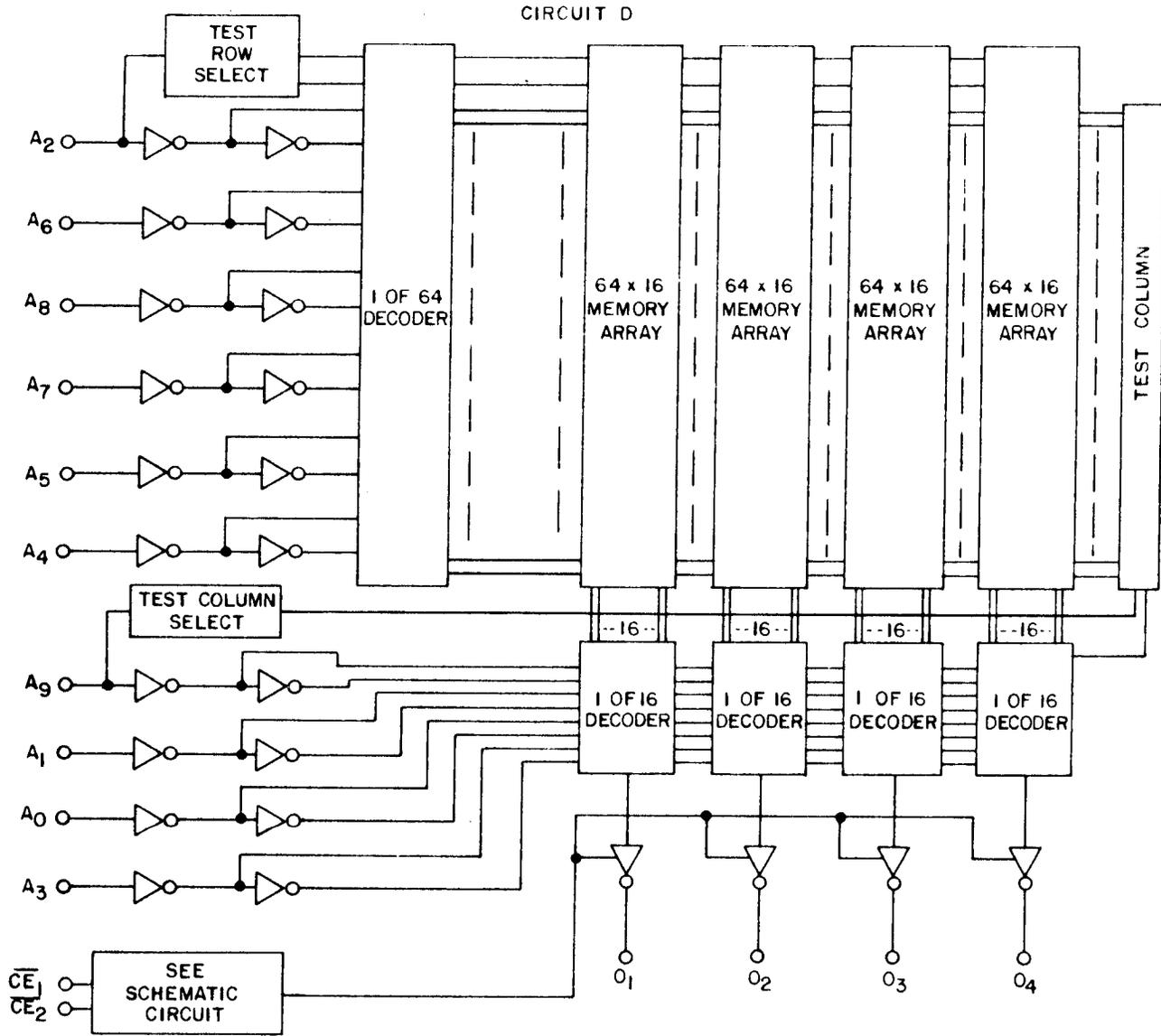


FIGURE 4. Functional block diagram - Continued.

CIRCUIT G (Device type 01)

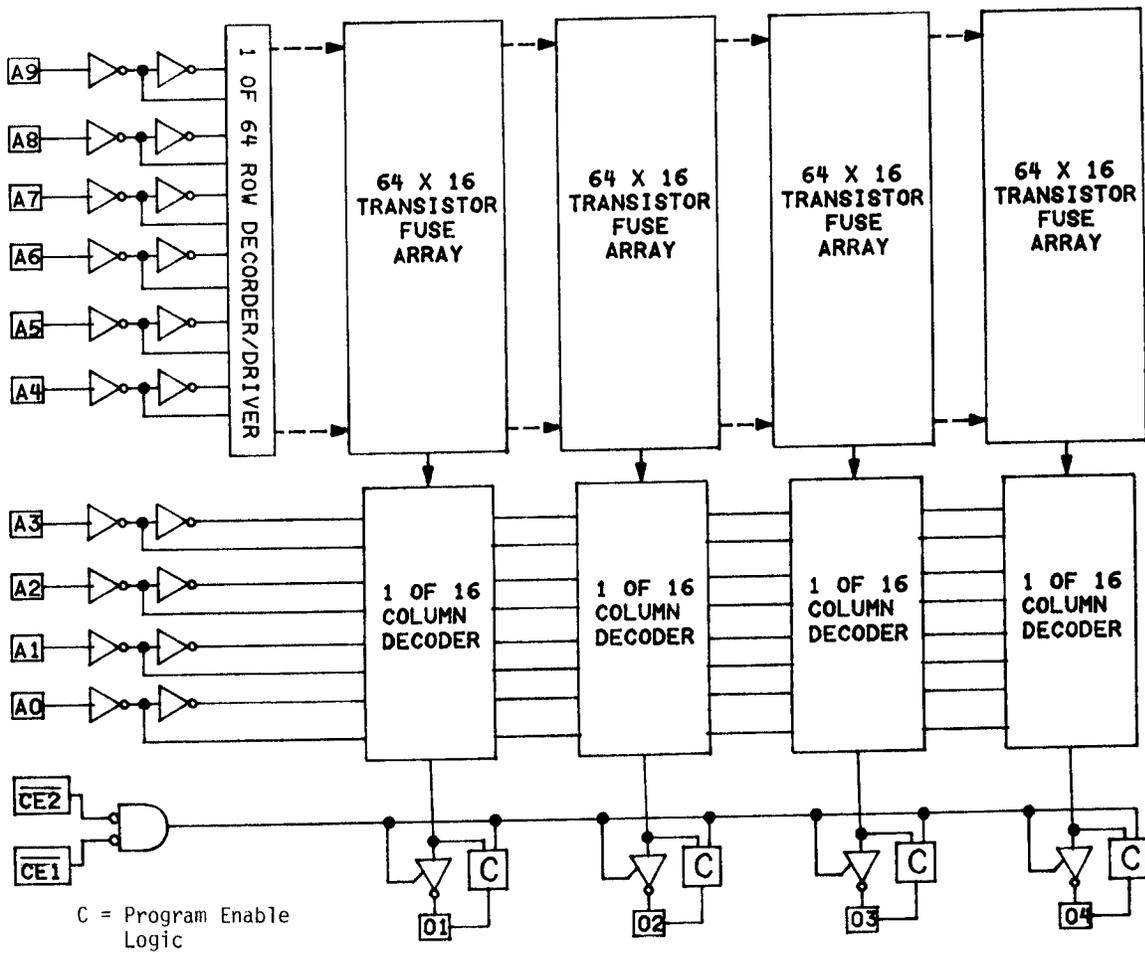


FIGURE 4. Functional block diagram - Continued.

CIRCUIT G (Device type 02)

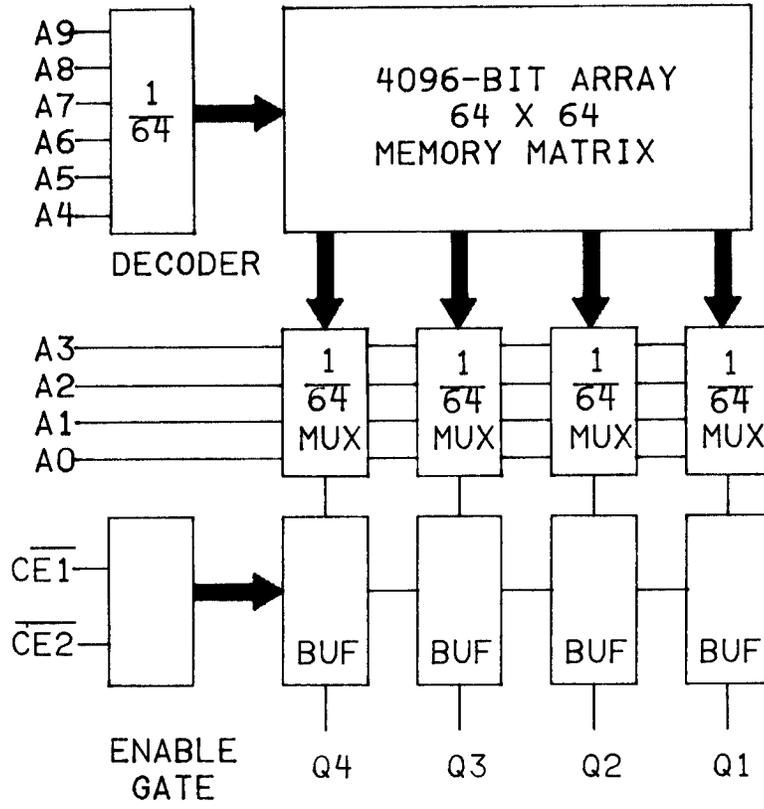
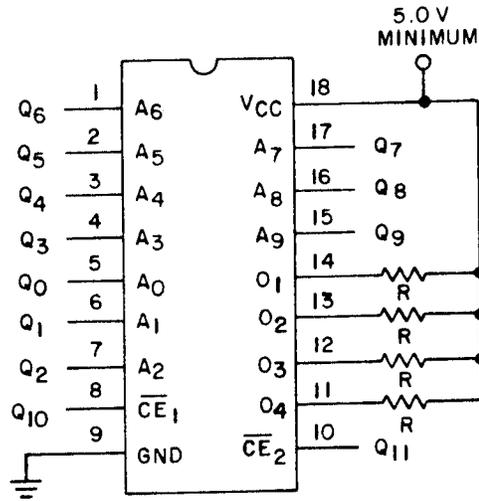


FIGURE 4. Functional block diagram - Continued.

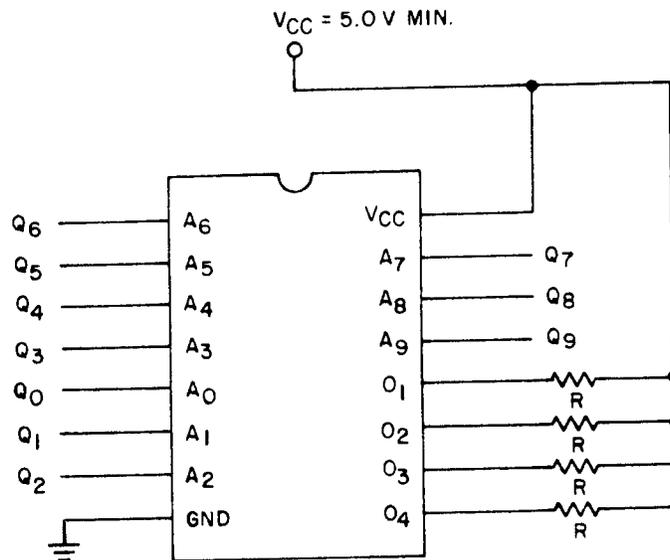


NOTES:

1. $R = 270\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = -1.5\text{ V minimum to } 0.8\text{ V maximum}$; $V_{IH} = 2.0\text{ V minimum to } 5.5\text{ V maximum}$;
 $50\% \pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies ($\pm 50\%$) are as follows:

Input	Frequency
Q ₀	$f_0 = 100\text{ kHz min.}$
Q ₁	$f_1 = 1/2 f_0$
Q ₂	$f_2 = 1/2 f_1$
Q ₃	$f_3 = 1/2 f_2$
Q ₄	$f_4 = 1/2 f_3$
Q ₅	$f_5 = 1/2 f_4$
Q ₆	$f_6 = 1/2 f_5$
Q ₇	$f_7 = 1/2 f_6$
Q ₈	$f_8 = 1/2 f_7$
Q ₉	$f_9 = 1/2 f_8$
Q ₁₀	$f_{10} = 1/2 f_9$
Q ₁₁	$f_{11} = 1/2 f_{10}$

FIGURE 5. Burn-in and life test circuit, device types 01, 02, and 04.

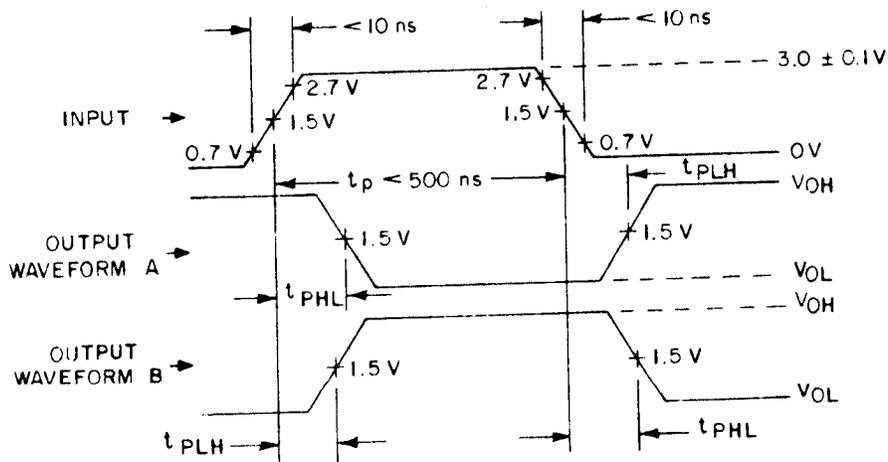
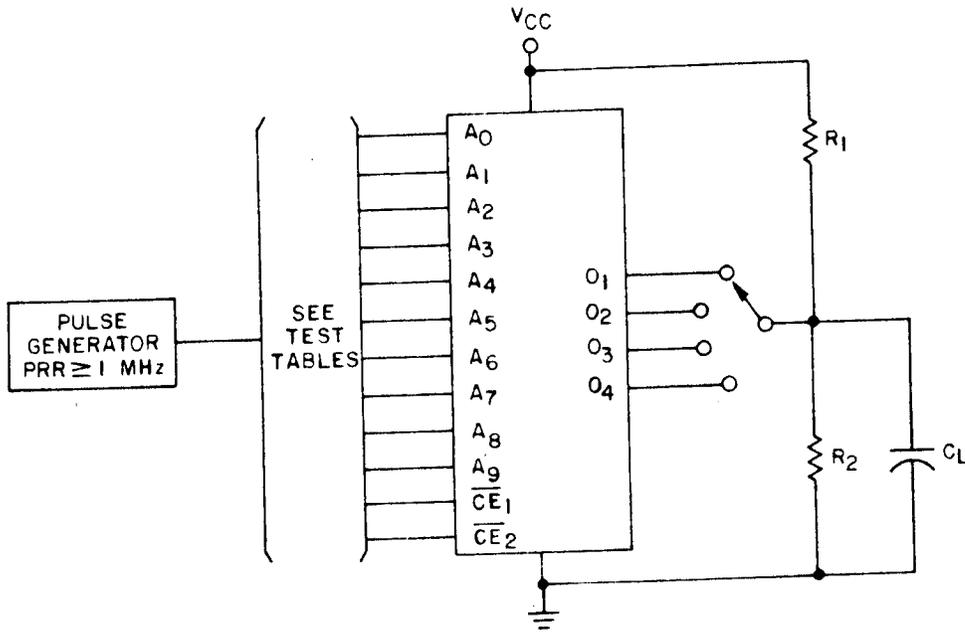


NOTES:

1. $R = 270\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = -1.5 \text{ V minimum to } 0.8 \text{ V maximum; } 50\% \pm 15\% \text{ duty cycle and frequencies}$
as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies ($\pm 50\%$) are as follows:

Input	Frequency
Q_0	$f_0 = 100 \text{ kHz min.}$
Q_1	$f_1 = 1/2 f_0$
Q_2	$f_2 = 1/2 f_1$
Q_3	$f_3 = 1/2 f_2$
Q_4	$f_4 = 1/2 f_3$
Q_5	$f_5 = 1/2 f_4$
Q_6	$f_6 = 1/2 f_5$
Q_7	$f_7 = 1/2 f_6$
Q_8	$f_8 = 1/2 f_7$
Q_9	$f_9 = 1/2 f_8$

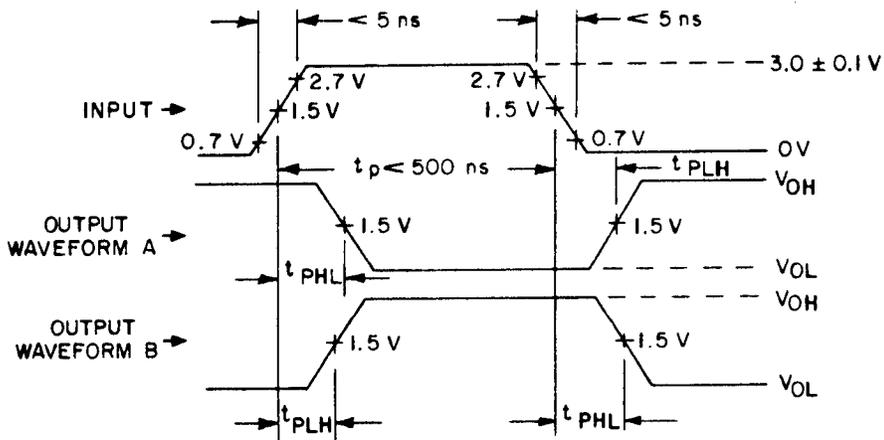
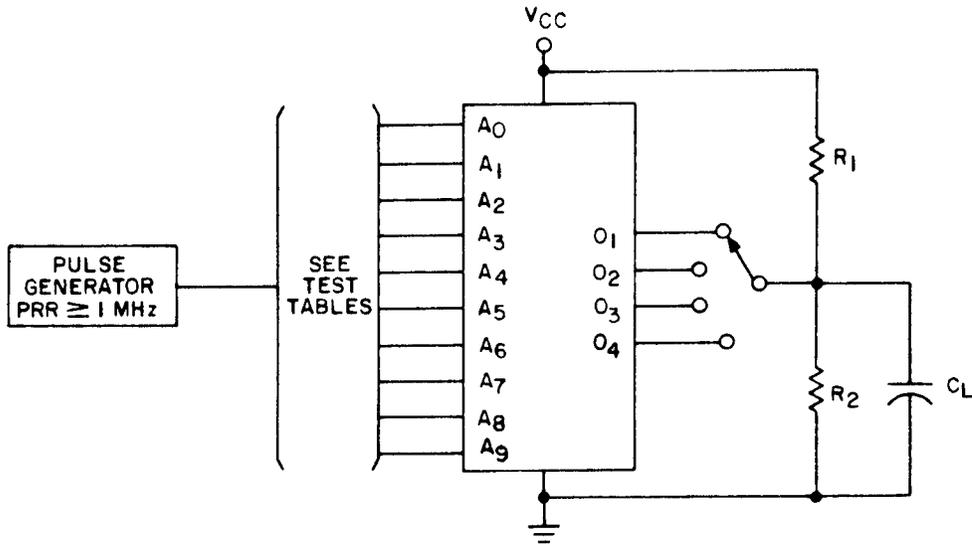
FIGURE 5. Burn-in and life test circuit, device type 03.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30 \text{ pF}$ minimum, including jig and probe capacitance, $R_1 = 330\Omega \pm 25\%$, and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

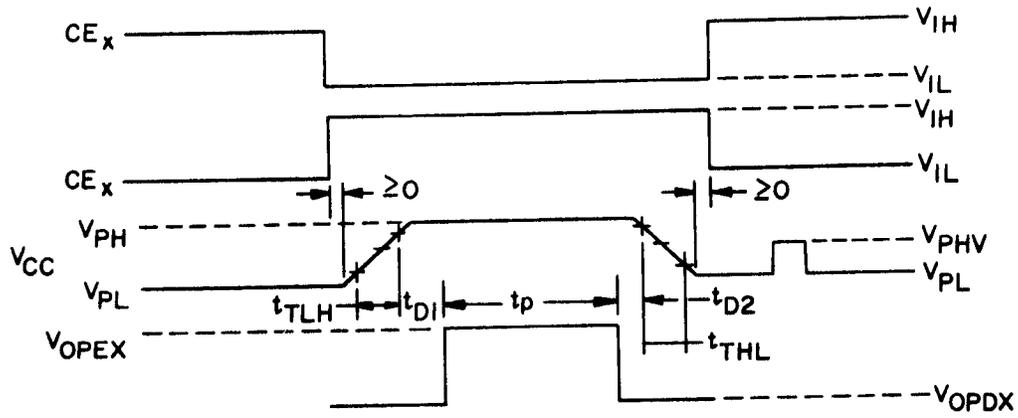
FIGURE 6. Switching time test circuit, device types 01, 02, and 04.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30 \text{ pF}$ minimum, including jig and probe capacitance, $R_1 = 300\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

FIGURE 6. Switching time test circuit, device type 03.



NOTE: All other waveform characteristics shall be as specified in table IVA.

FIGURE 7A. Programming voltage waveforms during programming for circuit A.

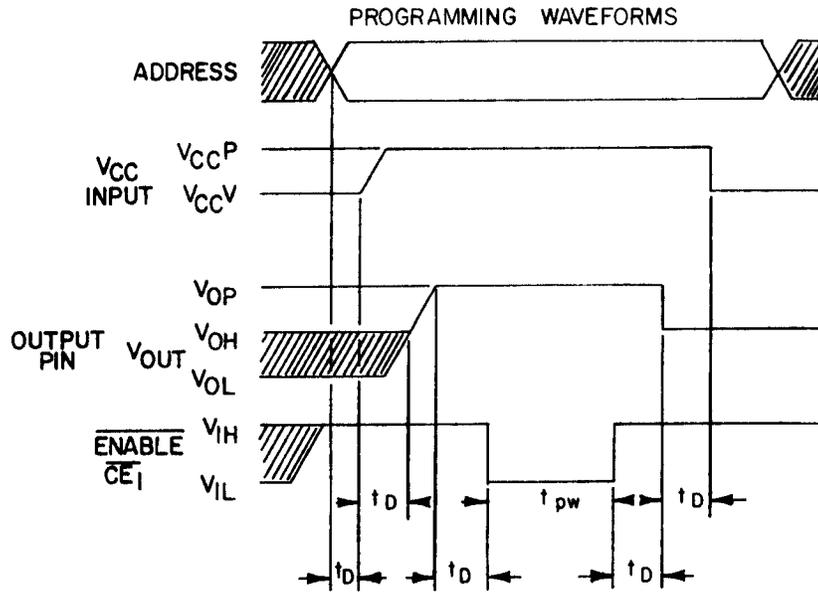
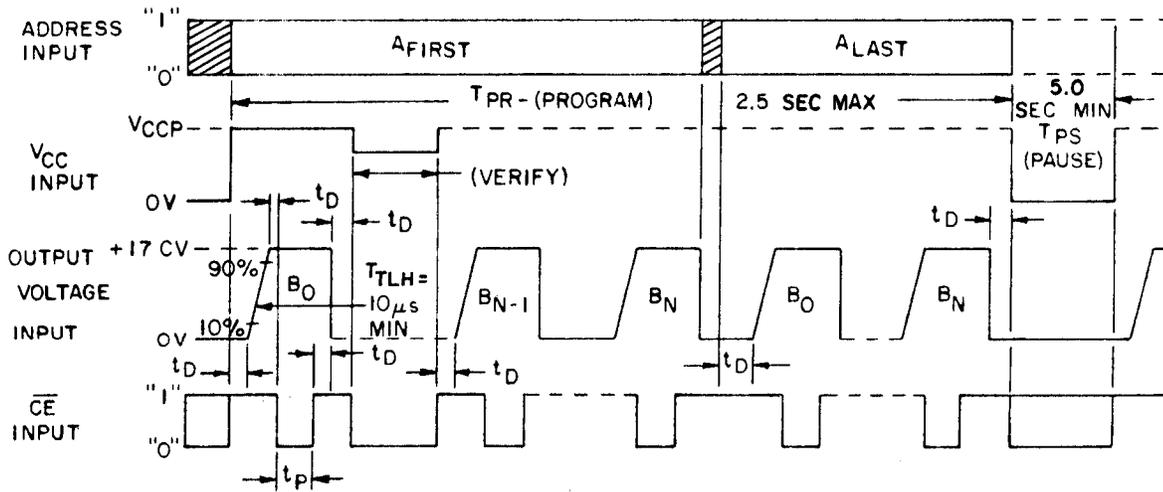


FIGURE 7B. Typical programming voltage waveforms during programming for circuit B.



NOTE: All other waveform characteristics shall be as specified in table IV C.

FIGURE 7C. Typical programming voltage waveforms during programming for circuit C.

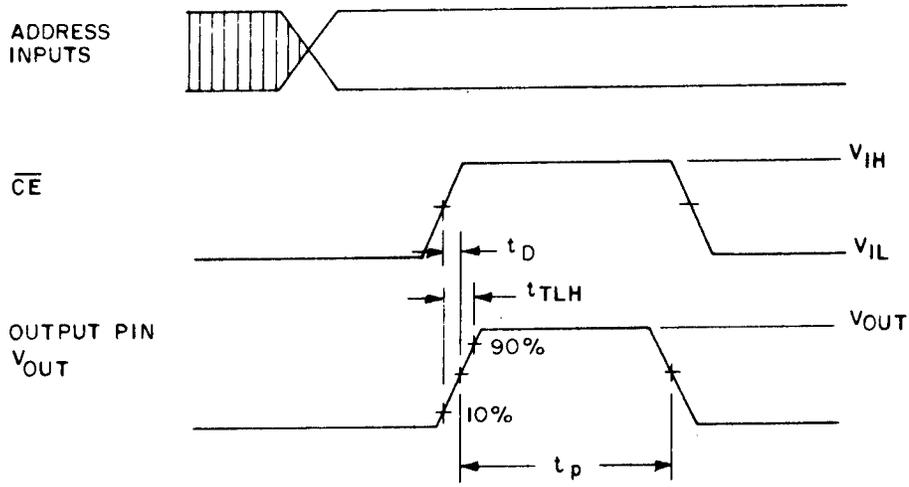


FIGURE 7D. Programming voltage waveforms during programming for circuit D.

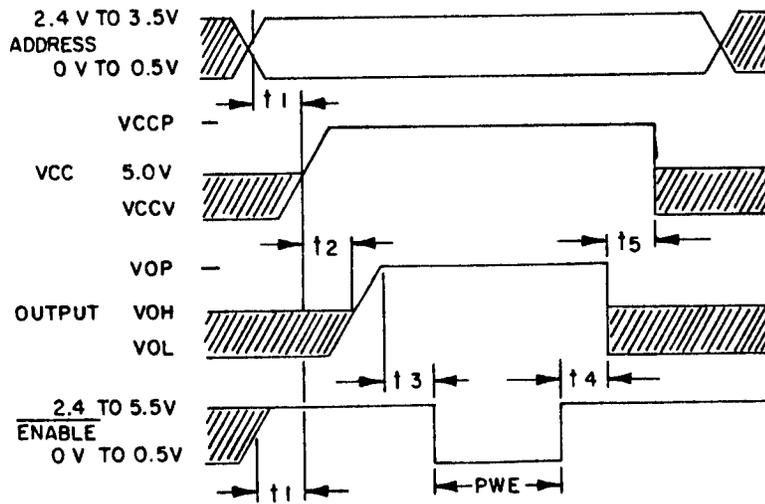
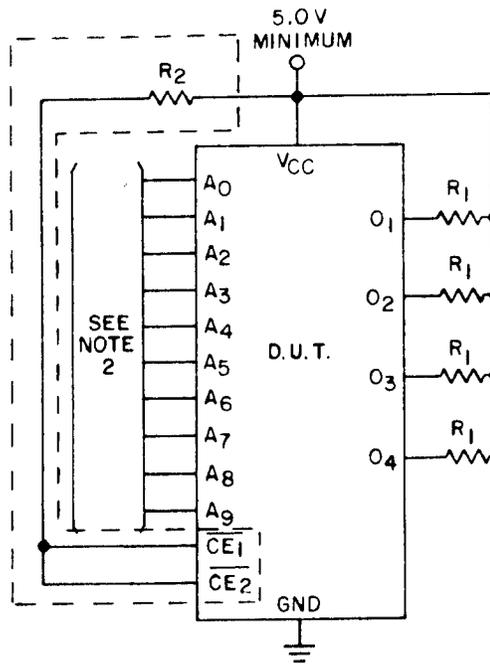


FIGURE 7G. Programming voltage waveforms during programming for circuit G.



NOTES:

1. $R_1 = 4.7\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. $R_2 = 1\text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test (see 4.3d). All Address inputs shall be either high, low, or open.
5. For device type 03, the circuitry within the dashed lines is not present.

FIGURE 8. Freeze-out test bias configuration.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in (method 1015 of MIL-STD-883):
 - (1) Test condition D, using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. Freeze-out test: This test shall be conducted as a 100 percent screen on all class S devices having nichrome as the fusing link. Within no more than 24 hours after completion of burn-in and prior to final electrical test, all devices containing nichrome resistors (see 3.7.1 and 3.7.2) shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the $+125^{\circ}\text{C}$ burn-in exposure, devices shall be conditioned with at least $+125^{\circ}\text{C}$ for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed the $+25^{\circ}\text{C}$ final electrical test parameters shall be completed 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:
 - (1) Connect devices in the electrical configuration of figure 8 or in the burn-in configuration of figure 5 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - (2) Reduce device temperature to $T_C = -10^{\circ} \pm 2^{\circ}\text{C}$ with bias cycled and maintain at that temperature for a minimum of 5 hours duration.
 - (3) With the cycled bias maintained, allow T_C to go to room temperature (by removal from cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_C shall not exceed $+35^{\circ}\text{C}$ during this period.
 - (4) Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.

- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7, 8, 9, 10, and 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically to other device types on this specification, then the other device types may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 5 tests.
- c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 5 or equivalent, shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 5 or equivalent.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration = 1000 hours except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

- c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross referenced in 6.6 herein with the manufacturer's symbol or FSCM number.

4.7 Programming procedure for circuit A. The programming characteristics in table IVA and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7A and the programming characteristics in table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.
- c. Apply V_{PL} voltage to V_{CC} .
- d. Bring the \overline{CE}_x inputs high and the CE_x inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.
- e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.
- f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH} .
- g. After a delay equal to or greater than t_{D1} apply only one pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
- h. Lower V_{CC} to V_{PL} following a delay to t_{D2} from programming enable pulse applied to an output.
- i. Enable the PROM for verification by applying V_{IL} to CE_x and V_{IH} to CE_x .
- j. Apply V_{PHV} to V_{CC} and verify bit is programmed.
- k. Repeat steps a through j for all other bits to be programmed in the PROM.
- l. If any bit does not verify as programmed, it shall be considered a programming reject.

TABLE III. Group A inspection for device type 01.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage.
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL STD-883 method	Cases												Test limits		Unit								
			1	2	3	4	5	6	7	8	9	10	11	12	13	14		15	16	17	18	Measured terminal	Min	Max	
1 T _C = +25°C	VIC		A6	A5	A4	A3	A0	A1	A2	CE1	GND	CE2	O4	O3	O2	O1	A9	A8	A7	V _{CC}					
			1	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	4.5 V	-1.5	V												
			2	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			3	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			4	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			5	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			6	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			7	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			8	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			9	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			10	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
			11	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA											
12	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA			
VOL		J007	13	5/9/	9/	9/	9/	9/	18/9/	10.8 V			18/	18/	16 mA		18/9/	9/	9/						
			14																						
			15																						
			16																						
			17																						
			18																						
			19																						
			20																						
IIL		J009	17	10.5 V	0.5 V	0.5 V	0.5 V	0.5 V	10.5 V	10.5 V															
			18																						
			19																						
			20																						
			21																						
			22																						
			23																						
			24																						
I1H1		J010	29	15.5 V	5.5 V	5.5 V	5.5 V	5.5 V	15.5 V	15.5 V															
			30																						
			31																						
			32																						
			33																						
			34																						
			35																						
			36																						
			37																						
			38																						
I1H2 I1J/			40																						
			41																						
ICEX			42																						
			43																						
			44																						
			45																						
ICC		J005	45	GND	GND	GND	GND	GND	V _{CC}																
			46																						
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and VIC tests are omitted.		46																						
			47																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and VIC tests are omitted.		48																						
			49																						
7 T _C = +25°C	Functional tests		50																						
			51																						

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
 Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
 inputs not designated are high ≥ 4.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL STD-883 Case method	Cases V ₁ , Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Test limits		Unit	
																						Measured terminal	Min		Max
8				A6	A5	A4	A3	A0	A1	A2	CE1	GND	CE2	O4	O3	O2	O1	A9	A8	A7	V _{CC}				
	9	tPLH1	47		2/	2/	2/	2/	2/	2/	2/	GND	GND	4/	4/	4/	4/	2/	2/	2/	2/	2/	185	17/	ns
		tPHL1	48		2/	2/	2/	2/	2/	2/	2/	GND	GND					2/	2/	2/	2/	2/	185		
		tPLH2	49		3/	3/	3/	3/	3/	3/	3/			3/				3/	3/	3/	3/	3/	140		
10	tPHL2	50		3/	3/	3/	3/	3/	3/	3/			3/					3/	3/	3/	3/	140			
10	Same tests, terminal conditions, and limits as subgroup 7, except T _C = +125°C and -55°C.																								
11	Same tests, terminal conditions, and limits as subgroup 9, except T _C = -55°C.																								

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 - Continued.
 Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
 Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
				A6	A5	A4	A3	A0	A1	A2	GND	04	03	02	01	A9	A8	A7	VCC	Measured terminal	Min	Max	Unit
8	Same tests, terminal conditions, and limits as for subgroup 7, except $T_C = +125^\circ\text{C}$ and $T_C = -55^\circ\text{C}$.																						
9	t_{pLH1}	See Fig. 6	45	2/	2/	2/	2/	2/	2/	2/	GND	4/	4/	4/	4/	2/	2/	2/	2/	2/	Outputs	85	ns
				2/	2/	2/	2/	2/	2/	GND	4/	4/	4/	4/	2/	2/	2/	2/	2/	2/	2/	2/	Outputs
10	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = +125^\circ\text{C}$.																						
11	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55^\circ\text{C}$.																						

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see 3.2.2). All bits shall be tested. Terminal conditions shall be as follows:

- a. Inputs: H = 3.0 V, L = 0.0 V.
- b. Outputs:
H > 1.0 V and L < 1.0 V.
- c. The functional tests shall be performed with $V_{CC} = 4.5$ and $V_{CC} = 5.5$ V.

2/ GALPAT (PROGRAMMED PROM)

This program will test all bits in the array, the addressing and interaction between bits for ac performance t_{PLH1} . Each bit in the pattern is fixed by being programmed with a "H" and "L".

Description:

1. Word 0 is read.
2. Word 1 is read.
3. Word 0 is read.
4. Word 2 is read.
5. Word 0 is read.
6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 1023 is reached, then increments to the next word and reads back and forth as in steps 1 through 6 shall include all words.
7. Pass execution time = $(n^2 + n) \times$ cycle time. N = 1024.
8. The GALPAT tests shall be performed with $V_{CC} = 4.5$ and 5.5 V.

3/ SEQUENTIAL TEST (PROGRAMMED PROM)

This program will test all bits in the array for t_{PHL2} and t_{PLH2} .

Description

1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
2. Each 0 is addressed. Enable line is pulled HI to LO and LO to HI. t_{PHL2} and t_{PLH2} are read.
3. Word 1 is addressed. Same enable sequence as above.
4. The reading procedure continues until word 1023 is reached.
5. Pass execution time = 1024 x cycle time.
6. The sequential tests shall be performed with $V_{CC} = 4.5$ V and 5.5 V.

- 4/ The outputs are loaded per figure 6.
- 5/ For unprogrammed devices (circuit A), apply 11.0 V on pin 1 (A₆) for device types 01 and 03. Apply 11.0 V on pin 1 (A₆) for device type 02 with date codes prior to 8225, and apply 13.0 V on pin 1 (A₆) for device type 02 with date codes after and including 8226.
- 6/ For unprogrammed devices, apply 12.0 V on pin 17 (A₇) for circuit B devices.
- 7/ For unprogrammed 02 devices, apply 10.0 V on pin 17 (A₇), apply 0.5 V on pins 3, 2, 1, 16, 15 (A₄, A₅, A₆, A₈, A₉) and 5.0 V on all other addresses for circuit C.
- 8/ For unprogrammed devices, apply 12.0 V on terminals A₂ and A₉ for circuit D devices.
- 9/ For programmed devices, select an appropriate address to acquire the desired output state. $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
- 10/ For unprogrammed devices, apply 10.5 V on A₂ and A₅ for circuit G devices.
- 11/ For unprogrammed devices, apply 0 V on this pin for circuit G devices.
- 12/ For unprogrammed devices, apply 3 V on this pin for circuit G devices.
- 13/ At the manufacturer's option, this may be performed with $V_{IH} = 5.5$ and test limits of 50 μ A maximum.
- 14/ For unprogrammed 04 devices, apply 10.0 V on pin 17 (A₇), apply 0.5 V on pins 1,2,3,15,16 (A₄, A₅, A₆, A₈, A₉) and 5.0 V on all other addresses for circuit C.
- 15/ The limits shall be as follows:

Device	02 (ns)	04 (ns)
t _{PLH1}	85	55
t _{PHL1}	85	55
t _{PLH2}	40	35
t _{PHL2}	40	35

- 16/ For circuit B devices apply 2.4 V.
- 17/ For circuit B devices, type 01 and 02, t_{PHL1}, t_{PLH1} = 70 ns and t_{PHL2}, t_{PLH2} = 30 ns.
- 18/ I_{OL} = 8 mA for circuit A only.

TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits <u>1/</u>			Unit
		Min	Rec	Max	
Address input voltage <u>2/</u>	V _{IH}	2.4	5.0	5.0	V
	V _{IL}	0.0	0.4	0.5	V
Programming Voltage to V _{CC} low	V _{PH} <u>3/</u>	10.75	11.0	11.25	"
Program verify	V _{PL}	0.0	0.0	1.5	"
Verify voltage	V _{PHV}	---	5.5	---	"
	V _R <u>4/</u>	4.5	---	5.5	"
Programming input low current at V _{PH}	I _{ILP}	---	-300	-600	μA
Programming voltage (V _{CC}) transition time	t _{TLH}	1	5	10	μs
	t _{THL}	1	5	10	"
Programming delay	t _{D1}	10	10	20	"
	t _{D2}	1	5	5	"
Programming pulse width	t _p <u>5/</u>	90	100	110	"
Programming duty cycle	PDC	---	30	60	%
Output voltage	V _{OPE} <u>6/</u>	10.5	10.5	11.0	V
	V _{OPD}	0.0	5.0	5.5	V

During the programming the chip must be disabled for proper operation.

1/ T_C = +25°C.

2/ No inputs should be left open for V_{IH}.

3/ V_{PH} source must be capable of supplying one ampere.

4/ It is recommended that post programming dual verification be made at V_R minimum and V_R maximum.

5/ Note step j in programming procedure.

6/ V_{OPE} source must be capable of supplying 10 mA minimum.

TABLE IVB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Rec	Max	
V _{CC} required during programming	V _{CCP}		11.5	11.75	12.0	V
V _{OUT} current limit during programming	I _{OP}		20	25	30	mA
Output programming voltage	V _{OUT}		10.5	11.0	11.5	V
Pulse width of programming voltage	t _p		9	10	11	μs
Programming delay	t _D		0	1	10	μs
V _{CCP} or V _{OUT} transition time	t _{TLH}	Rise time of V _{CC} or V _{OUT}	1	5	10	V/μs
V _{CCP} current	I _{CCP}		800	1200		mA
Low V _{CC} for verification	V _{CCL}		4.2	4.3	4.4	V
High V _{CC} for verification	V _{CCH}		5.8	6.0	6.2	V
Address input voltage	V _{IH}		2.4	3.0	5.5	V
	V _{IL}		0.0	0.0	0.5	V
Maximum duty cycle during automatic programming of program pin and output pin	D.C.	t _p /t _c	---	25	25	%

1/ T_A = +25°C.

TABLE IVC. Programming characteristics for circuit C.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Rec	Max	
Programming voltage	V_{CCP} <u>1/</u>	$I_{CCP} = 375 \pm 75$ mA Transient or steady-state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_s <u>2/</u>		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	$V_{CCP} = +8.75 \pm .25$ V	300	375	450	mA
Input voltage high level "1"	V_{IH}		2.4		5.5	V
Input voltage low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	$V_{IH} = +5.5$ V			50	μ A
Input current	I_{IL}	$V_{IL} = +0.4$ V			-500	μ A
Output programming voltage	V_{OUT} <u>3/</u>	$I_{OUT} = 200 \pm 20$ mA Transient or steady-state	16	17	18	V
Output programming current	I_{OUT}	$V_{OUT} = +17 \pm 1$ V	180	200	220	mA
Output pulse transition	t_{TLH}		10		50	μ s
CE programming pulse width	t_p		0.3	0.4	0.5	ms
Pulse sequence delay	t_D		10			μ s

1/ Bypass V_{CC} to GND with a 0.01 μ F capacitor to reduce voltage spikes.

2/ V_s is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ± 1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

TABLE IVD. Programming characteristics for circuit D.

Parameter	Symbol	Conditions <u>1/</u>	Limits <u>1/</u>			Unit
			Min	Rec	Max	
V _{CC} required during programming	V _{CCP}		4.75	5.0	5.25	V
Verification V _{CC} read	V _{CCL}	Programming read verify	4.2	4.4	5.0	V
Input voltage high level "1"	V _{IH}	Do not leave inputs open	2.4	5.0	5.0	V
Input voltage low level "0"	V _{IL}	Do not leave inputs open	0	0	0.4	V
Chip enable	CE ₁ , CE ₂	Pin 8 or 10 or both	2.4	5.0	5.0	V
Output programming voltage	V _{OUT}	Applied to output to be programmed	20	20.5	21	V
Output programming current	I _{OUT}	If pulse generator is used, set current limit to the max value			100	mA
Programming voltage transition time	t _{TLH}		0.5	1.0	3.0	μs
Programming pulse width	t _p		50	100	180	μs
Programming duty cycle	D.C.	Maximum duty cycle to maintain T _C < +85°C		20	20	%
Required delay between disabling memory output and application of output programming pulse	t _D		30			ns

1/ Recommended T_C = +25°C; maximum T_C = +85°C.

4.8 Programming procedure for circuit B. The programming characteristics in table IVB and the following procedures shall be used for programming the device:

- Connect the device in the electrical configuration for programming. The waveforms on figure 7B and the programming characteristics of table IVB shall apply to these procedures.
- Apply V_{IH} to CE₁ and the binary address of the PROM word to be programmed. Raise V_{CC} to V_{CCP}.
- After a t_D delay, apply only one V_{OP} to the output to be programmed high. Apply V_{OP} to one output at a time.
- After a t_D delay, a pulse CE₁ to a V_{IL} level for a duration of t_p.
- After t_p and a t_D delay, remove V_{OP} from the programmed output.
- Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OP} pulses to each output to be programmed and pulsing CE₁ to the V_{IL} level, allowing for proper delays between V_{OP} and CE₁.
- Repeat 4.8b through 4.8e for all bits to be programmed.

- h. To verify programming, lower V_{CCP} to V_{CC} . Connect a 10 k Ω resistor between each output and V_{CC} . Apply V_{IL} to CE₁ inputs. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.
- i. If any bit does not verify as programmed, it shall be considered a programming reject.

4.9 Programming procedures for circuit C. The programming characteristics in table IVC and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7C and the programming characteristics of table IVC shall apply to these procedures.
- b. Terminate all device outputs with a 10 k Ω resistor to V_{CC} .
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a t_D delay (10 μ s), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.
- e. After a t_D delay (10 μ s), pulse both CE inputs to logic "0" for a duration of t_p .
- f. After a t_D delay (10 μ s), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 7C.
- h. Repeat steps b through g for all other bits to be programmed.
- i. To verify programming, after t_D (10 μ s) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both CE inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.
- j. If any bit does not verify as programmed it shall be considered a programming reject.

4.10 Programming procedure for circuit D. The programming characteristics in table IVD and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7D and the programming characteristics in table IVD shall apply to these procedures.
- b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- c. Disable the chip by applying V_{IH} to the CE inputs. The CE inputs are TTL compatible.
- d. After a delay of t_D , apply only one V_{OUT} pulse with a duration of t_p to the output selected for programming. The other outputs may be left open or tied to V_{IH} . The outputs shall be programmed one output at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- e. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

- f. Repeat steps b through e for all other bits to be programmed.
- g. Enable the chip by applying V_{IL} to the CE inputs and verify the program.
- h. If any bit does not verify as programmed, it shall be considered a programming reject.

4.11 Programming procedure for circuit G. The programming characteristics on table IVG and the following procedures shall be used for programming:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7G and the programming characteristics of table IVG shall apply to these procedures.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and Enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase V_{CC} from nominal to V_{CCP} (10.5 ± 0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 V/ μ s). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.
- d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ± 0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 V/ μ s). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP} , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 k Ω minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip enable(s) to a low level. This is done with a pulse PWE for 10 μ s. The 10 μ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 V (± 0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.
- g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of step f is to be performed at a V_{CC} level of 4.0 volts (± 0.2 V). V_{OH} , during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.
- h. Repeat steps 4.11b through 4.11f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified..
- i. If any bit does not verify as programmed it shall be considered a programming reject.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE IVG. Programming characteristics for circuit G.

Parameter	Symbol	Conditions	Limits ^{1/}			Unit
			Min	Rec	Max	
V _{CC} required during programming	V _{CCP}		10.0	10.5	11.0	V
I _{CC} during programming	I _{CCP}	V _{CC} = 11 V			750	mA
Required output voltage for programming	V _{OP}		10.0	10.5	11.0	V
Output current while programming	I _{OP}	V _{OUT} = 11 V			20	mA
Rate of voltage change of V _{CC} or output	I _{RR}		1.0		10.0	V/μs
Programming pulse width (Enabled)	PWE		9	10	11	μs
Required V _{CC} for verification	V _{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V _{CC} at V _{CCP}	MDC			25	25	%
Address set-up time	T ₁		100			ns
V _{CCP} set-up time	T ₂	^{2/}	5			μs
V _{CCP} hold time	T ₅		100			ns
V _{OP} set-up time	T ₃		100			ns
V _{OP} hold time	T ₄		100			ns

^{1/} T_A = +25°C.

^{2/} V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP}.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. Requirement for programming the device, including processing option. The device may be programmed pre- or post-burn-in, if applicable.
- i. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND-	- - - - -	Ground zero voltage potential.
V _{IN} -	- - - - -	Voltage level at an input terminal
V _{IC} -	- - - - -	Input clamp voltage
I _{IN} -	- - - - -	Current flowing into an input terminal

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>	<u>Circuit designator</u>	<u>Fusible links</u>	<u>Symbol/FSCM number</u>
01	54S572/National Semiconductor	G	TiW	CCXP/27014
01 <u>1/</u>	7642/Harris Semiconductor	A	NiCr	CDWO/34371
01	53S440/Monolithic Memories	B	TiW	CECD/50364
01 <u>1/</u>	82S136/Sigmetics Corporation	C	NiCr	CDKB/18324
01	93452/Fairchild Semiconductor	D	NiCr	CFJ/07263
02	7643/Harris Semiconductor	A	NiCr	---
02	53S441/Monolithic Memories	B	TiW	---
02,04	82S137A/Sigmetics Corporation	C	NiCr	---
02	93453/Fairchild Semiconductor	D	NiCr	---
02	54S573/National Semiconductor	G	TiW/W	---
03 <u>1/</u>	7644/Harris Semiconductor	A	NiCr	---

1/ This generic-industry type is no longer manufactured.

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0974)