

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 256 BIT, SCHOTTKY, BIPOLAR,
PROGRAMMABLE READ-ONLY MEMORY (PROM),
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, programmable read-only memory (PROM) microcircuits which employ thin film nichrome (NiCr) resistors, tungsten (W) or titanium-tungsten (TiW) as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead material and finishes are provided for each type and are reflected in the complete part number. A special test requirement is included in this specification to screen against devices which may contain excess moisture in the package materials or internal atmosphere (see freeze-out test of 4.3d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01, 03	32 word/8 bits per word PROM with open collector
02, 04	32 word/8 bits per word PROM with tri-state output.

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range	-65°C to 150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}): 1/	
Case E	30°C/W
Case F	45°C/W
Output voltage applied	-0.5 V dc to +V _{CC}
Output sink current	100 mA
Maximum power dissipation (P _D) 2/	739 mW dc
Maximum junction temperature (T _J) 3/	+175°C

1/ Heat sinking is recommended to reduce the junction temperature.

2/ Must withstand the added P_D due to short circuit (e.g., I_{OS}) test.

3/ Maximum junction temperatures shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage range - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) - - - - -	2.0 V dc
Maximum low-level input voltage (V_{IL}) - - - - -	0.8 V dc
Normalized fanout (each output) - - - - -	16 mA
Case operating temperature range (T_C) - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and standards. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the acquiring activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the device shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Device type	Limits		Units
				Min	Max	
High-level output voltage	V_{OH}	$V_{IL} = 0.8\text{ V}$ $V_{CC} = 4.5\text{ V}$ $I_{OH} = -2\text{ mA}$ $V_{IH} = 2.0\text{ V}$	02, 04	2.4		V
Low-level output voltage	V_{OL}	$V_{IL} = 0.8\text{ V}$ $V_{CC} = 4.5\text{ V}$ $I_{OL} = 16\text{ mA}, V_{IH} = 2.0\text{ V}$	01, 02 03, 04		0.5	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\text{ V}$ $T_C = 25^{\circ}\text{C}$ $I_{IN} = -10\text{ mA}$	01, 02 03, 04		-1.5	V
Maximum collector cut-off current	I_{CEX}	$V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.2\text{ V}$	01, 03		100	μA
High-impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.2\text{ V}$	02, 04		100	μA
High-impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5\text{ V}$ $V_{OL} = 0.5\text{ V}$	02, 04		-100	μA
High-level input current	I_{IH1}	$V_{CC} = 5.5\text{ V}, V_{IN} = 5.5\text{ V}$	01, 02 03, 04		50	μA
	I_{IH2}	$V_{CC} = 5.5\text{ V}, V_{IN} = 4.5\text{ V}$ Special program pin	01, 02 03, 04		100	μA
Low-level input current	I_{IL}	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.5\text{ V}$	01, 02 03, 04	-1.0	-250	μA
Short circuit output current	I_{OS}	$V_{CC} = 5.5\text{ V}$ $\underline{2/}$ $V_O = 0.0\text{ V}$	02, 04	-10	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5\text{ V}, V_{IN} = 0$ Outputs open	01, 02 03, 04		130	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Units
				Min	Max	
Propagation delay time, high-to-low level logic, address to output	t _{PHL1}	V _{CC} = 4.5 V and 5.5 V C _L = 30 pF See figure 5	01, 02		80	ns
			03, 04		35	ns
Propagation delay time, low-to-high level logic, address to output	t _{PLH1}		01, 02		80	ns
			03, 04		35	ns
Propagation delay time, high-to-low level logic, enable to output	t _{PHL2}		01, 02		50	ns
			03, 04		25	ns
Propagation delay time, low-to-high level logic, enable to output	t _{PLH2}		01, 02		50	ns
			03, 04		25	ns

1/ Complete terminal conditions shall be specified on table III.

2/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

3.2.3 Functional block diagrams. The functional block diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Processing options. Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical tests (method 5004)	I	I
Final electrical tests (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*, 8
Final electrical tests (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9
Group A electrical tests (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B electrical tests (method 5005, subgroup 5)	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical tests (method 5005)	None	1, 2, 3, 7, 8
Group D end-point electrical tests (method 5005)	1, 2, 3, 7, 8	1, 2, 3, 7, 8

NOTES:

1. (*) Indicates PDA applies to subgroup 1 and 7 (see 4.3c).
2. Any and all subgroups may be combined when using high-speed testers.
3. Subgroup 7 and 8 shall consist of verifying the pattern specified.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4). Qualification data for subgroups 7, 8, 9, 10, and 11 shall be by attributes only.

4.2.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in (method 1015 of MIL-STD-883). Test condition D or E, using the circuit shown on figure 4, or equivalent.
- b. Interim and final electrical tests shall be as specified in table II; the interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. Freeze-out test. This test shall be conducted as a 100 percent screen on all class S devices having nichrome as the fusible link. Within no more than 24 hours after completion of burn-in and prior to final electrical test, all devices containing nichrome resistors as the fusing link shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned at 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical tests shall be completed within 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:
 - (1) Connect devices in electrical configuration of figure 6, or in the burn-in configuration of figure 4 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - (2) Reduce device temperature to $T_C = -10^\circ\text{C} \pm 2^\circ\text{C}$ with the bias cycled and maintain at that temperature for a minimum of 5 hours.
 - (3) With the cycled bias maintained, allow T_C to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5 hour cold soak. T_C shall not exceed 35°C during this period.
 - (4) Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.3c.
- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail in all 3 subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1.c.) shall be included in the subgroup 5 tests.
- b. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4, or equivalent, shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration - 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c.) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross referenced herein (see 6.5) with the manufacturer's symbol or FSCM number.

4.7 Programming procedure for circuit A. The programming characteristics on table IVA and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7A and the programming characteristics of table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.
- c. Apply V_{PL} voltage to V_{CC} .
- d. Bring the \overline{CE}_x inputs high and the CE_x inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.
- e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.
- f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH} .
- g. After a delay equal to or greater than t_{D1} apply only one pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
- h. Lower V_{CC} to V_{PL} following a delay of t_{D2} from programming enable pulse applied to an output.
- i. Enable the PROM for verification by applying V_{IL} to \overline{CE}_x and V_{IH} to CE_x .
- j. Apply V_{PHV} to V_{CC} and verify bit is programmed.
- k. Repeat steps a through j for all other bits to be programmed in the PROM.
- l. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

4.8 Programming procedure for circuit B. The programming characteristics on table IVB and the following procedures shall be used for programming the devices:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7B and the programming characteristics of table IVB shall apply to these procedures.
- b. Raise V_{CC} to 5.5 volts.
- c. Address the PROM with binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the \overline{CE} input. \overline{CE} input is TTL compatible.

- e. Apply the V_{pp} pulse to the \overline{CE} pin. In order to insure that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the output pin's programming pulse by T_{D2} (see figure 7B).
- f. Apply the V_{OUT} pulse with duration of t_D to the output selected for programming (see table IVB). The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- h. Repeat steps (b) through (g) for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the \overline{CE} input and verify the program.
 Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.0$ V and 0.2 mA at $V_{CC} = 7.0$ V at $T_C = 25^\circ$ C.
- j. For classes S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

4.9 Programming procedures for circuit C. The programming characteristics on table IVC and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7C and the programming characteristics of table IVC shall apply to these procedures.
- b. Terminate all device outputs with a 10 k Ω resistor to V_{CC} .
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a t_D delay (10 μ s), apply V_{OUT} to the output to be programmed. Program one output at a time.
- e. After a t_D delay (10 μ s), pulse \overline{CE} input to logic "0" for a duration of t_p .
- f. After a t_D delay (10 μ s), remove the V_{OUT} pulse from the programmed output. Note that the PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay to t_D between pulses as shown on figure 7C.
- h. Repeat steps (b) through (g) for all other bits to be programmed.
- i. To verify programming, after t_D (10 μ s) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to the \overline{CE} input. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.
- j. For classes S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

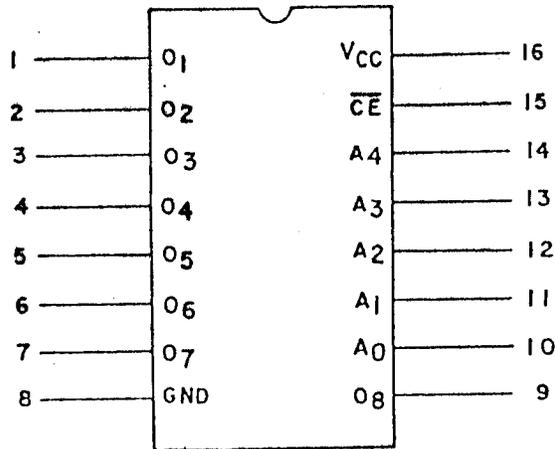


FIGURE 1. Terminal connections.

Word No.	Address						Data							
	\overline{CE}	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈
NA	L	X	X	X	X	X	5/	5/	5/	5/	5/	5/	5/	5/
NA	H	X	X	X	X	X	OC							

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be high for circuits A and B, and shall be low for circuits C and G.

FIGURE 2. Truth table (unprogrammed).

Circuits A and B

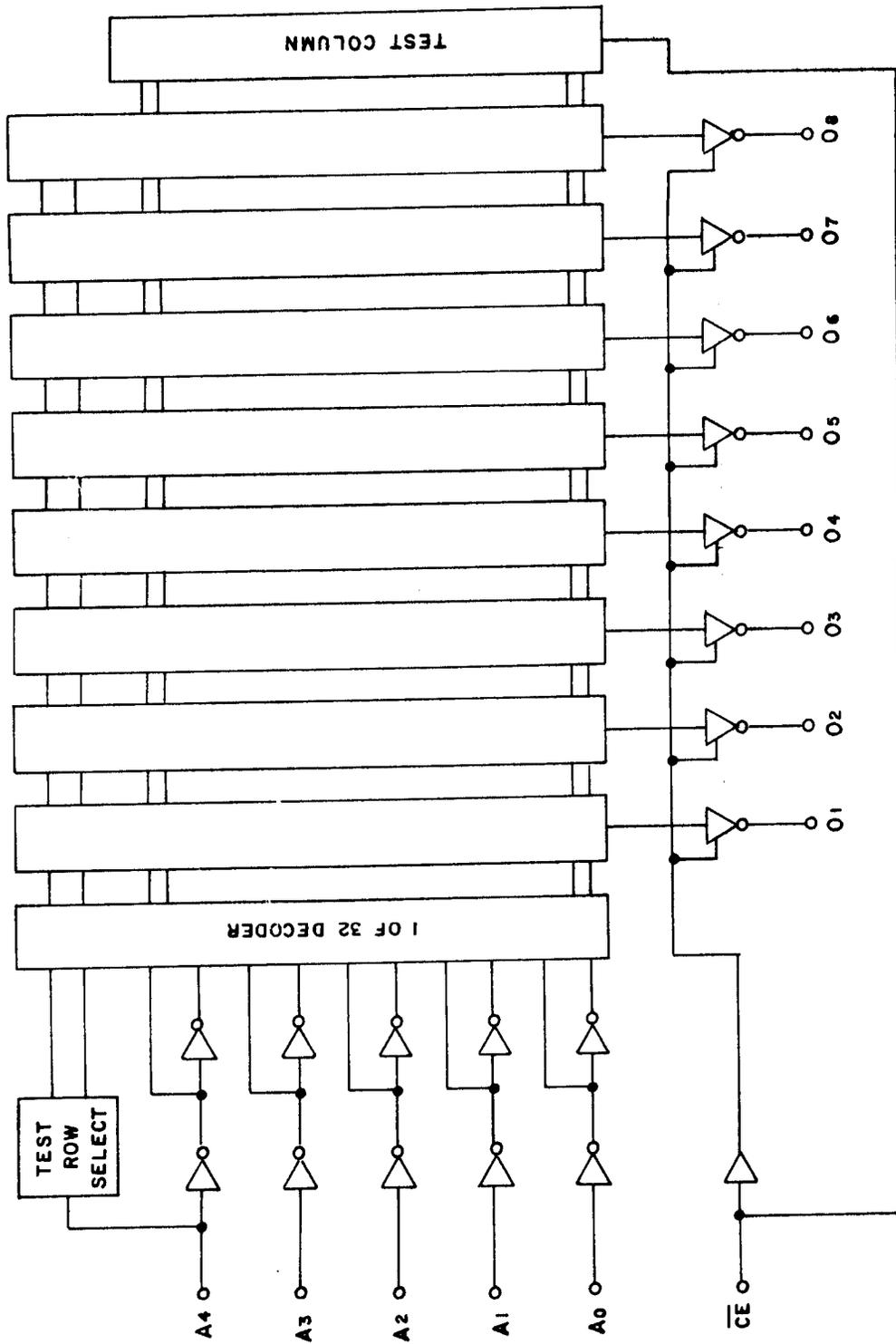


FIGURE 3. Logic diagram.

Circuit C

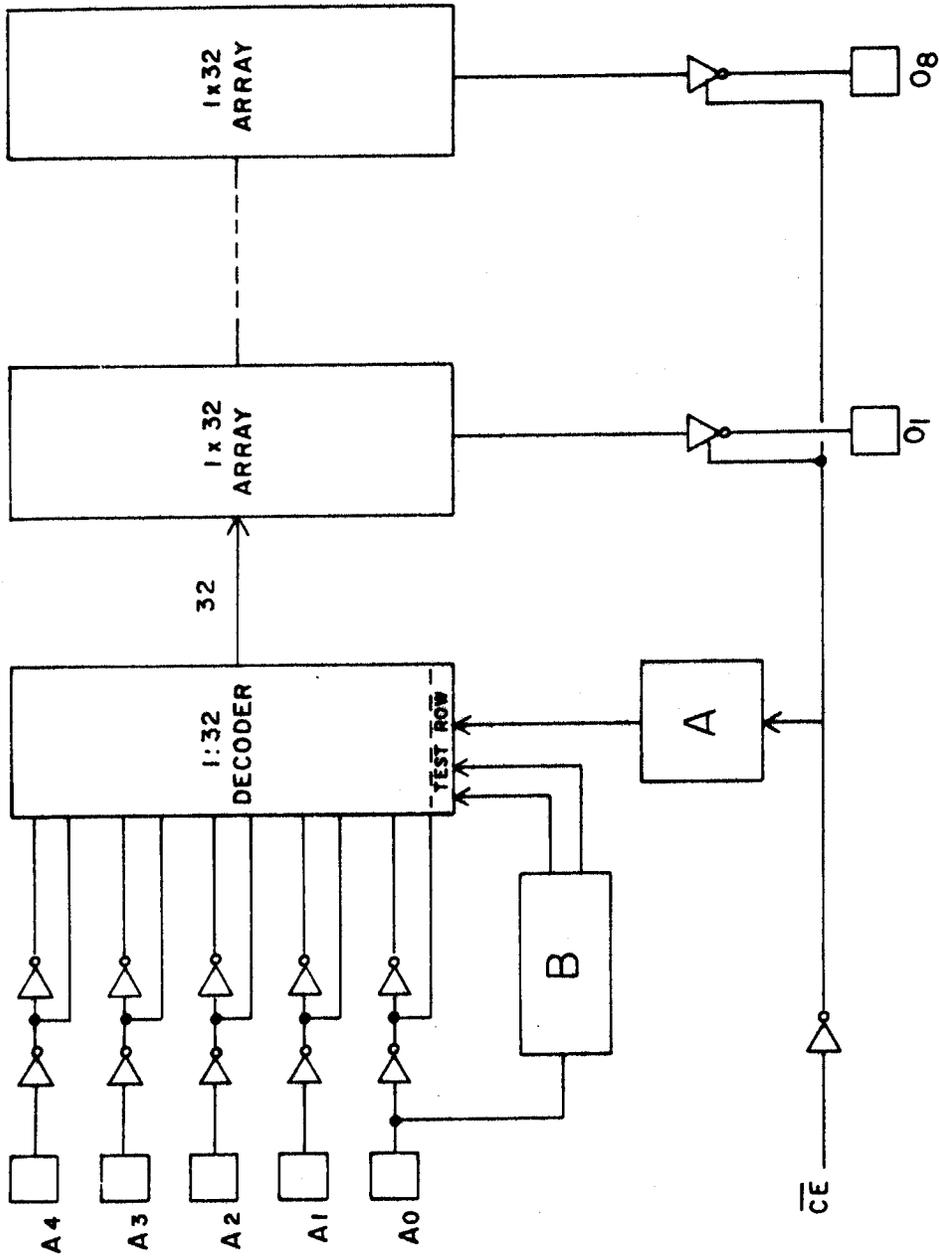


FIGURE 3. Logic diagram - Continued.

Circuit G

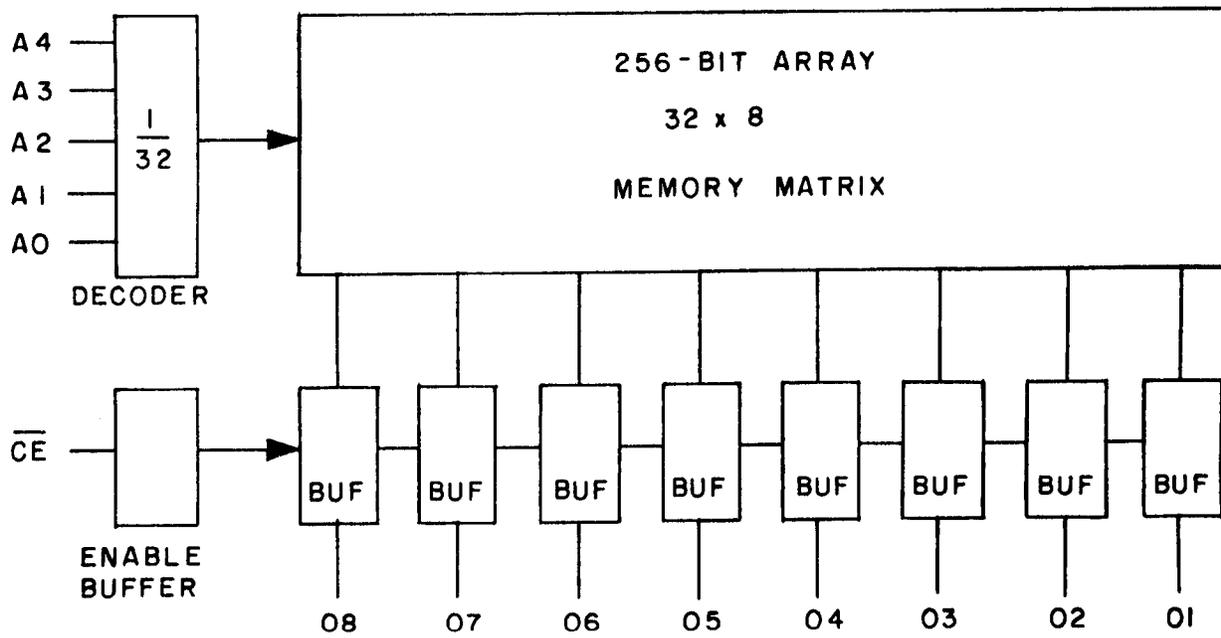
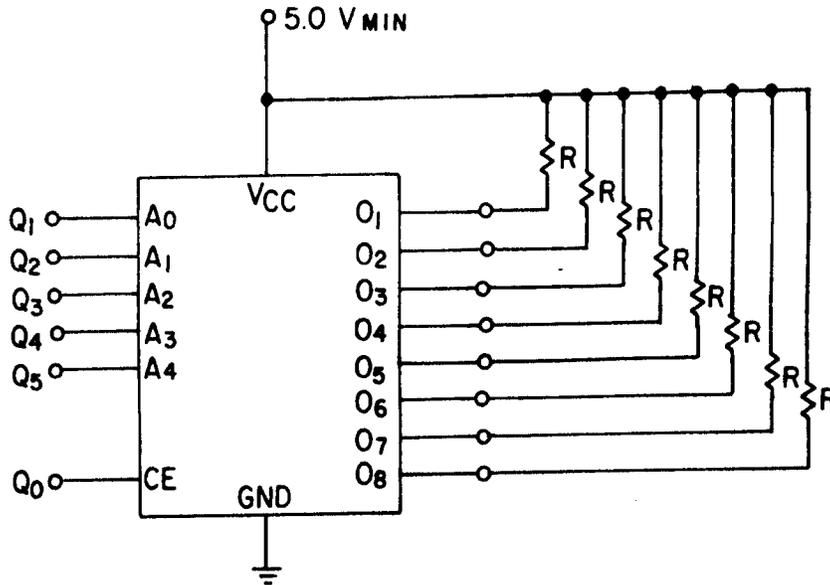


FIGURE 3. Logic diagram - Continued.

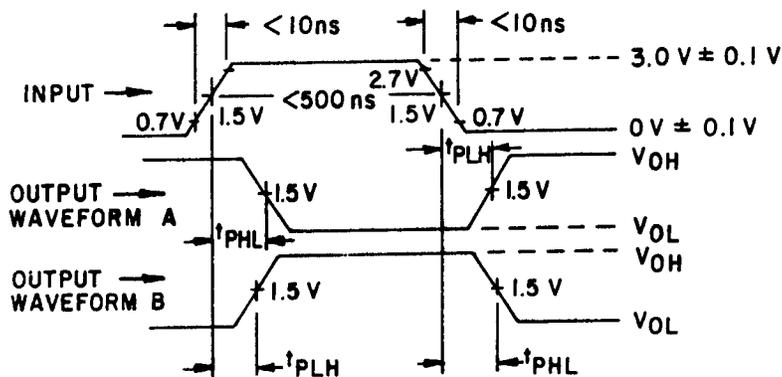
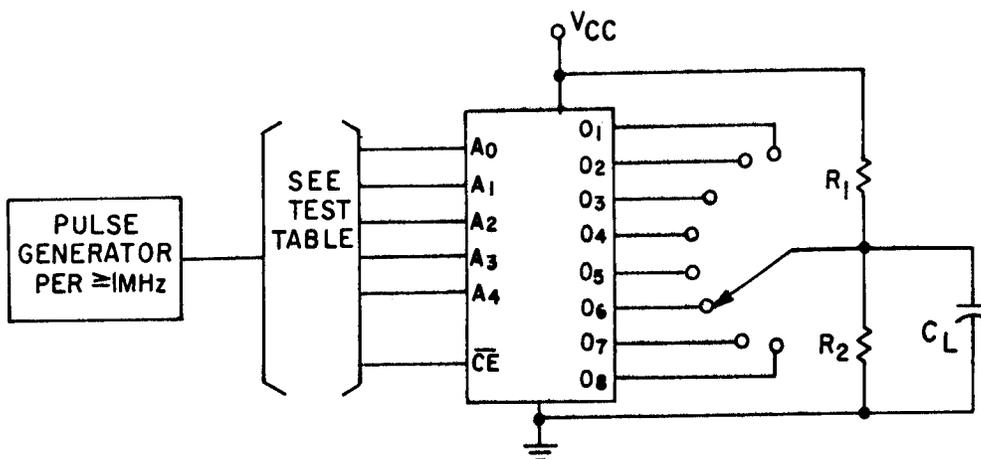


NOTES:

1. $R = 330\Omega \pm 5\%$. ($R = 560\Omega \pm 5\%$ for circuit B).
All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum;
50% $\pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency
Q_0	$f_0 = 100$ kHz minimum
Q_1	$f_1 = 1/2 f_0$
Q_2	$f_2 = 1/2 f_1$
Q_3	$f_3 = 1/2 f_2$
Q_4	$f_4 = 1/2 f_3$
Q_5	$f_5 = 1/2 f_4$

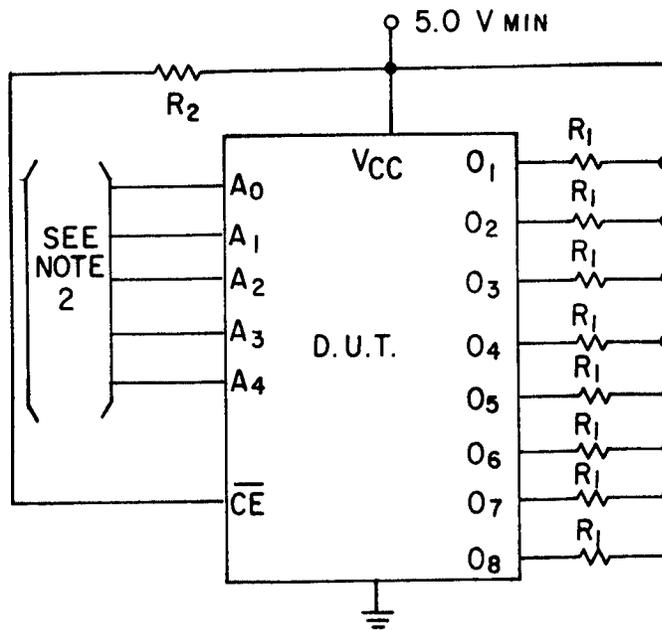
FIGURE 4. Burn-in and life test circuit.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance;
 $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

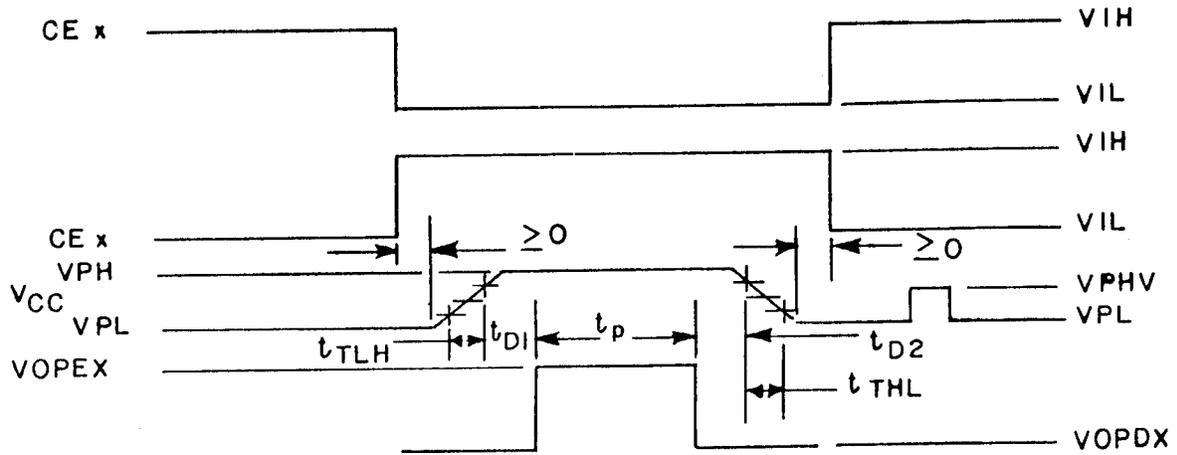
FIGURE 5. Switching time test circuit.



NOTES:

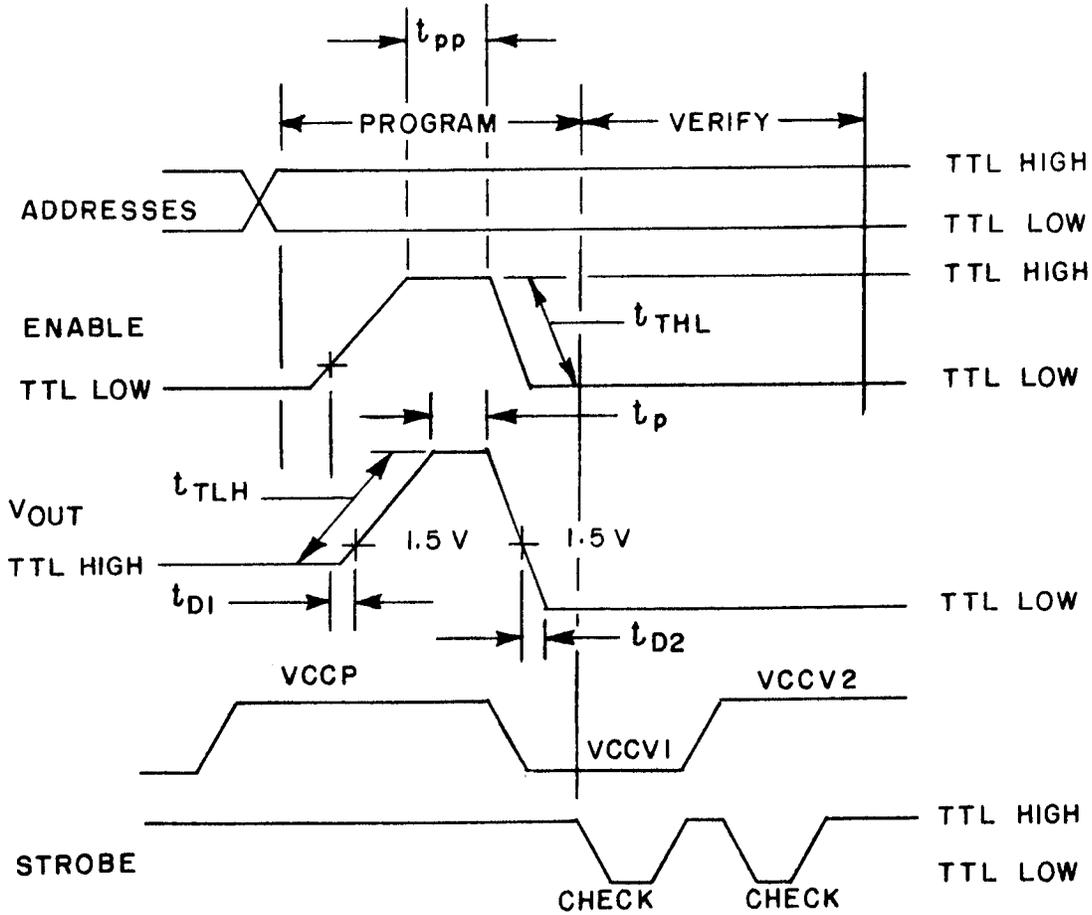
1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
3. Burn-in circuit may be used to perform this test (see 4.3d). All address inputs shall be either high, low or open.
4. For the freeze-out test, all address inputs shall be either high, low or open.

FIGURE 6. Freeze-out test bias configuration.



NOTE: All other waveform characteristics shall be as specified in table IVA.

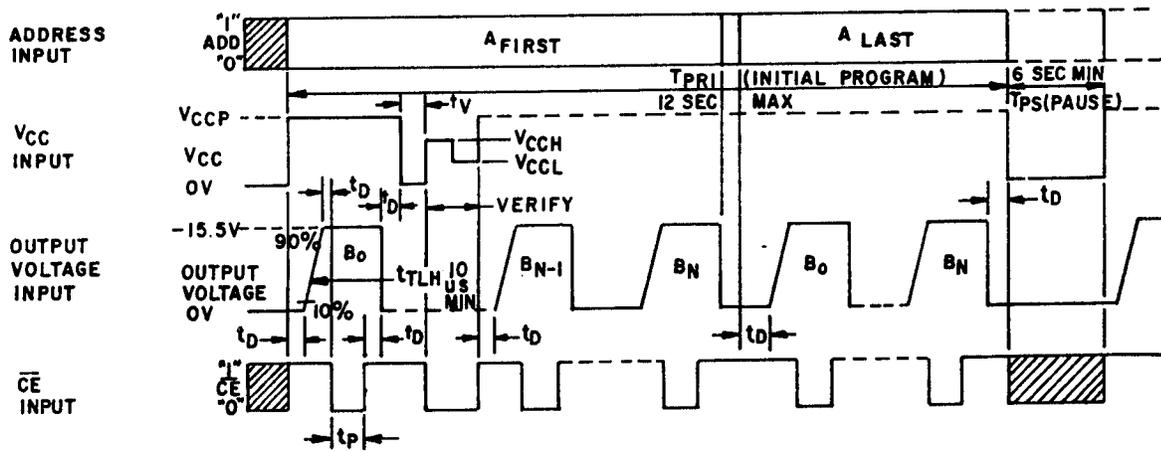
FIGURE 7A. Typical programming voltage waveforms during programming for circuit A.



NOTES:

1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check respectively.
2. All other waveform characteristics shall be as specified in table IV B.

FIGURE 7B. Typical programming voltage waveforms during programming for circuit B.



NOTE: All other waveform characteristics shall be as specified in table IV C.

FIGURE 7C. Typical programming voltage waveforms during programming for circuit C.

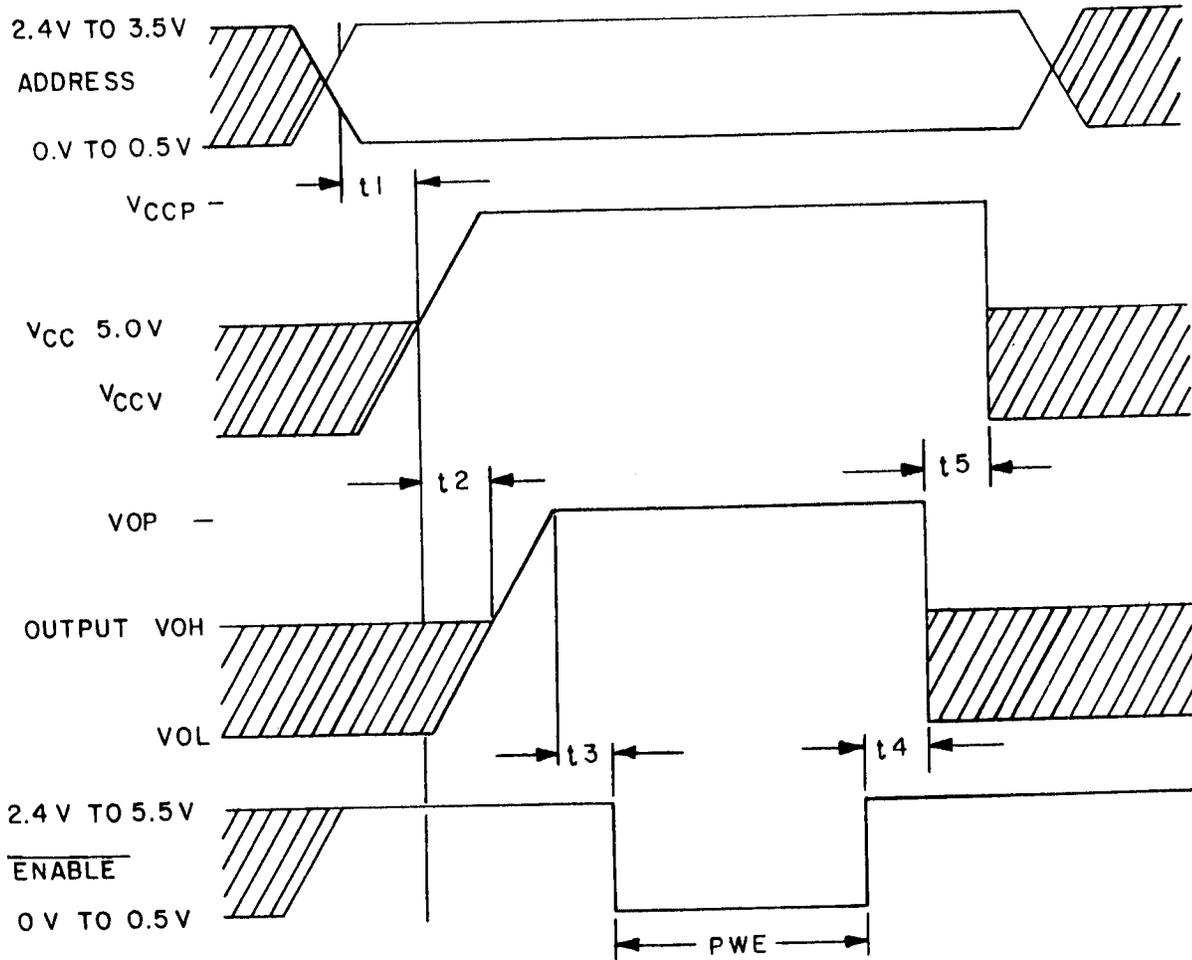


FIGURE 7D. Programming voltage waveforms during programming for circuit G.

TABLE III. Group A Inspection for device type 01 and 03.
Terminal conditions (Outputs not designated are open or resistive coupled to ground or voltage). (Inputs not designated are high ≥ 2.0 V or low ≤ 0.8 V).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				01	02	03	04	05	06	07	08	A0	A1	A2	A3	A4	CE	VCC	Min		Max					
1 $T_C = 25^\circ C$	V_{IC}		1										-10 mA	-10 mA	-10 mA					A0	-1.5		V			
			2																		A1	"		"		
			3																		A2	"		"		
			4																		A3	"		"		
			5																		A4	"		"		
			6																		CE	"		"		
	V_{OL}		3007	7	16 mA									$1/2/3/$	$1/3/$	$1/3/$	$1/3/$	$1/2/3/$	0.5 V		01	0.5		"		
				8																		02	"		"	
				9																			03	"		"
				10			16 mA																04	"		"
				11				16 mA															05	"		"
				12					16 mA														06	"		"
				13																			07	"		"
				14																			08	"		"
I_{IL}		3009	15										0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	5.5 V	A0	-1.0	-250	μA			
			16																		A1	"	"	"		
			17																			A2	"	"	"	
			18																			A3	"	"	"	
			20																			CE	"	"	"	
I_{IH1}		3010	21										5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		A0	50		"			
			22																		A1	"	"	"		
			23																			A2	"	"	"	
			24																			A3	"	"	"	
			25																			A4	"	"	"	
I_{IH2}			26																	CE	100		"			
I_{GEX}			27	5.2 V																	01	"	"	"		
			28																			02	"	"	"	
			29			5.2 V																03	"	"	"	
			30				5.2 V															04	"	"	"	
			31					5.2 V														05	"	"	"	
			32							5.2 V												06	"	"	"	
			33								5.2 V											07	"	"	"	
34									5.2 V										08	"	"	"				
I_{CC}			35																	VCC	130		mA			
2	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = 125^\circ C$ and V_{IC} tests are omitted.																									
3	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = -55^\circ C$ and V_{IC} tests are omitted.																									

See footnotes at end of device type 02.

TABLE III. Group A Inspection for device type 01 and 03 - Continued.
 Terminal conditions (Outputs not designated are open or resistive coupled to ground or voltage). (Inputs not designated are high ≥ 2.0 V or low ≤ 0.8 V).

Subgroup	Symbol	MIL-STD-883C, E, F method no.	Cases test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit								
				01	02	03	04	05	06	07	08	A0	A1	A2	A3	A4	CE	VCC	Min		Max										
7 T _C = 25°C	Functional test	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	01	6/ 36	6/ 36	ns							
				6/ 36	6/ 36	6/ 36	02	6/ 36	6/ 36	ns																					
				6/ 36	6/ 36	6/ 36	6/ 36	03	6/ 36	6/ 36	ns																				
				6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	04	6/ 36	6/ 36	ns																			
				6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	05	6/ 36	6/ 36	ns																			
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = 125°C and -55°C.	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	06	6/ 36	6/ 36	ns							
				6/ 36	6/ 36	6/ 36	6/ 36	07	6/ 36	6/ 36	ns																				
				6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	08	6/ 36	6/ 36	ns																			
				6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	ns																		
				6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	6/ 36	ns																	
9 T _C = 25°C	tpHL1	GALPAT Fig. 5	37	7/ 37	8/ 37	8/ 37	8/ 37	ns																							
				8/ 37	8/ 37	8/ 37	8/ 37	8/ 37	8/ 37	8/ 37	8/ 37	ns																			
				9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	9/ 37	ns																	
				10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	10/ 37	ns																	
10	tpLH1	GALPAT Fig. 5	38	8/ 38	8/ 38	8/ 38	ns																								
				9/ 38	9/ 38	9/ 38	9/ 38	9/ 38	9/ 38	9/ 38	9/ 38	9/ 38	ns																		
				10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	10/ 38	ns																
				11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	11/ 38	ns																
11	tpLH2	Sequential Fig. 5	39	10/ 39	10/ 39	10/ 39	ns																								
				11/ 39	11/ 39	11/ 39	11/ 39	11/ 39	11/ 39	11/ 39	11/ 39	11/ 39	ns																		
				12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	12/ 39	ns																
				13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	13/ 39	ns																

See footnotes at end of device type 02.

Terminal conditions (Outputs not designated are open or resistive coupled to ground or voltage). (Inputs not designated are high ≥ 2.0 V or low ≤ 0.8 V).

Subgroup	Symbol	MIL-STD-883 E,F method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				01	02	03	04	05	06	07	08	A0	A1	A2	A3	A4	CE	VCC	Min		Max					
1 T _C = 25°C	V _{IC}		1																		A0		-1.5	V		
			2																			A1		"	"	
			3																			A2		"	"	
			4																			A3		"	"	
			5																			A4		"	"	
			6																			CE		"	"	
	V _{OL}	3007		7	16 mA																	01		0.5	"	
				8																			02		"	"
				9																			03		"	"
				10																			04		"	"
				11																			05		"	"
				12																			06		"	"
				13																			07		"	"
				14																			08		"	"
V _{OH}	3006		15	-2.0 mA																	01		2.4	"		
			16																			02		"	"	
			17																			03		"	"	
			18																			04		"	"	
			19																			05		"	"	
			20																			06		"	"	
I _{IL}	3009		21																		07		"	"		
			22																			08		"	"	
			23																			A0		-1.0	-250	
			24																			A1		"	"	
			25																			A2		"	"	
			26																			A3		"	"	
I _{IH1}	3010		27																		A4		"	"		
			28																		CE		"	"		
			29																		A0		50	"		
			30																		A1		"	"		
			31																		A2		"	"		
			32																			A3		"	"	
I _{IH2}			33																		A4		"	"		
			34																		CE		100	"		
			35																			01		+100	"	
			36																			02		"	"	
			37																			03		"	"	
			38																			04		"	"	
I _{OHZ}			39																		05		"	"		
			40																			06		"	"	
			41																			07		"	"	
			42																			08		"	"	
			43																							
			44																							

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 and 04 - Continued.
Terminal conditions (Outputs not designated are open or resistive coupled to ground or voltage). (Inputs not designated are high > 2.0 V or low < 0.8 V).

Subgroup	Symbol	MIL-STD-883 E, F method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit		
				01	02	03	04	05	06	07	08	A0	A1	A2	A3	A4	CE	VCC	Min		Max				
1 T _C = 25°C	IOLZ		43	0.5 V							GND								5.5 V	5-5 V	01	-100	μA		
			44	0.5 V								"										02	"	"	
			45	0.5 V									"										03	"	"
			46	0.5 V									"										04	"	"
			47	0.5 V									"										05	"	"
2	I _{CC}	3005	51								"										V _{CC}	130	mA		
			52	GND																					
			53	GND																					
7 T _C = 25°C	Functional tests	6/	60	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/	01	-10	"		
			54																			02	"	"	
			55																			03	"	"	
			56																			04	"	"	
			57																			05	"	"	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = 125°C and T _C = -55°C.		58																		06	"	"		
			59																			07	"	"	
																						08	"	"	
9 T _C = 25°C	t _{PHL1}	GALPAT Fig. 5	61	Z/	Z/	Z/	Z/	Z/	Z/	Z/	GND	Z/	8/	8/	8/	8/	8/	8/	8/	8/	Outputs	9/	ns		
			62	"	"	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	8/	"	"	9/	"
			63	"	"	"	"	"	"	"	"	"	"	"	10/	10/	10/	10/	10/	10/	10/	"	"	9/	"
			64	"	"	"	"	"	"	"	"	"	"	"	10/	10/	10/	10/	10/	10/	10/	"	"	9/	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = 125°C.																								
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																								

NOTES:

- 1/ For programmed devices, select an appropriate address to acquire the desired output state, $V_{IL} = 0.8 \text{ V}$, $V_{IH} = 2.0 \text{ V}$.
- 2/ For unprogrammed devices, apply 11.0 V on pins 10(A₀) and 14(A₄) for circuit A devices.
- 3/ For unprogrammed 02 devices (V_{OL} test), apply 0 V to pins 10(A₀) through 14(A₄) for circuit G.
- 4/ For unprogrammed devices, apply 12.0 V on pin 14(A₄) for circuit B devices.
- 5/ This test may, at the manufacturer's option, be performed with $V_{IH} = 5.5 \text{ V}$ (Pin 15) and test limit of 50 μA maximum.
- 6/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see 3.2.2). All bits shall be tested. Terminal conditions shall be as follows:
- Inputs: $H = 3.0 \text{ V}$, $L = 0.0 \text{ V}$.
 - Outputs: Output voltage shall be: $H \geq 1.0 \text{ V}$ and $L < 1.0 \text{ V}$.
 - The functional tests shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.
- 7/ The outputs are loaded per figure 5.
- 8/ GALPAT (PROGRAMMED PROM)
This program will test all bits in the array, the addressing and interaction between bits for AC performance, t_{PHL1} and t_{PLH1} . Each bit in the pattern is fixed by being programmed with a "H" or "L".

Description

- Word 0 is read.
- Word 1 is read.
- Word 0 is read.
- Word 2 is read.
- Word 0 is read.
- The reading procedure continues back and forth between word 0 and the next higher numbered word until word 255 is reached, then increments to the next word and reads back and forth as in steps 1 through 6 and shall include all words.
- Pass execution time = $(n^2 + n) \times \text{cycle time}$, $n = 256$.
- The GALPAT tests shall be performed with $V_{CC} = 4.5 \text{ V}$ and 5.5 V .

9/

Device	t_{PHL1}	t_{PLH1}	t_{PHL2}	t_{PLH2}
01,02	80 ns	80 ns	50 ns	50 ns
03,04	35 ns	35 ns	25 ns	25 ns

NOTES - Continued:

10/ SEQUENTIAL TEST (PROGRAMMED PROM)

This program will test all bits in the array for t_{PHL2} and t_{PLH2} .

Description

1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
2. Word 0 is addressed. Enable line is pulled high to low and low to high, t_{PHL2} and t_{PLH2} are read.
3. Word 1 is addressed. Same enable sequence as above.
4. The reading procedure continues until word 255 is reached.
5. Pass execution time = 256 X cycle time.
6. The sequential tests shall be performed with $V_{CC} = 4.5$ V and 5.5 V.

11/ For unprogrammed 01, 02 devices (with date codes before 8601), apply 10.0 V to pin 10(A₀), apply 0.5 V to pin 11(A₁), and apply 5.0 V to all other addresses for circuit C.

12/ For unprogrammed 02 devices (V_{OH} test), apply 0 V to pins 10(A₀) through 13(A₃), and 11.5 V to pin 14(A₄) for circuit G.

13/ For unprogrammed devices 01, 02 (with date codes of 8601 or later), 03 and 04, apply 10.0 V to pin 10(A₀), 0.5 V to pins 12, 13, 14 (A₂, A₃, A₄) and 5.0 V to all other addresses for circuit C.

TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits <u>1/</u>			Unit
		Min	Recommended	Max	
Address input voltage <u>2/</u>	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.5	V V
Programming Voltage to V_{CC} low	V_{PH} <u>3/</u>	10.75	11.0	11.25	V
Program verify	V_{PL}	0.0	0.0	1.5	V
Verify voltage	V_{PHV} V_R <u>4/</u>	---	5.5	---	V
Programming input low current at V_{PH}	I_{ILP}	---	-300	-600	μA
Programming voltage (V_{CC}) transition time	t_{TLH} t_{THL}	1 1	5 5	10 10	μs μs
Programming delay	t_{D1} t_{D2}	10 1	10 5	20 5	μs μs
Programming pulse width	t_p <u>5/</u>	90	100	110	μs
Programming duty cycle	PDC <u>6/</u>	---	30	60	%
Output voltage Enable	V_{OPE} <u>7/</u>	10.5	10.5	11.0	V
Output voltage Disable	V_{OPD}	0.0	5.0	5.5	V

During the programming the chip must be disabled for proper operation.

1/ $T_C = 25^\circ C$.

2/ No inputs should be left open for V_{IH} .

3/ V_{PH} source must be capable of supplying one ampere.

4/ It is recommended that post programming dual verification be made at V_R min and V_R max.

5/ Note step j in programming procedure.

6/ Programming Duty Cycle applies to DIPs only.

7/ V_{OPE} source must be capable of supplying 10 mA minimum.

TABLE IVB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Recom- mended	Max	
Current into output during programming before the fuse has programmed	I_{OUT1}	$V_{CC} = 5.5 \text{ V}$ $V_{OUT} = 9.0 \text{ V}$ $V_{OUT} = 25 \text{ V}$		0.1 35		mA mA
Current into output during programming after the fuse has programmed	I_{OUT2}	$V_{OUT} = 20 \text{ V}$ $V_{CC} = 5.50 \text{ V}$		3		mA
Rise time of program pulse applied to the data out from 10% to 90%	t_{TLH}		50	60	70	μs
Chip enable (\overline{CE}) pin pulse width	t_{pp}	Chip disabled $V_{CC} = 5.5 \text{ V}$	80	95	110	μs
Pulse width of programming voltage	t_p	Chip disabled $V_{CC} = 5.5 \text{ V}$	1		40	μs
Fall time of the pulse applied to the CE from 90% to 10%	t_{THL}		50		1000	ns
Required time delay between disabling memory output and application of output programming pulse	t_{D1}	Measured at 1.5 V levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	t_{D2}	Measured at 1.5 V levels	100			ns
V_{CC} required during programming	V_{CCP}		5.40	5.50	5.60	V
Output current required during verification	I_{OLV1}	$T_C = 25^\circ\text{C}$ $V_{CC} = 4.20 \text{ V}$ chip enabled	11	12	13	mA
Output current required during verification	I_{OLV2}	$T_C = 25^\circ\text{C}$ $V_{CC} = 6.0 \text{ V}$ chip enabled	0.19	0.2	0.21	mA
Maximum duty cycle during automatic programming of enable and output pin	DC	T_p/T_C			25	%
Required programming voltage on the output pin	V_{OUT}		20	20	26	V
Required current limit of the power supply feeding the output during programming	I_L	$V_{OUT} = 25 \text{ V}$ $V_{CC} = 5.50 \text{ V}$	150			mA

1/ $T_C = 25^\circ\text{C}$.

TABLE IVC. Programming characteristics for circuit C.

Parameter	Symbol	Conditions	Limits			Unit
			Min	Recom- mended	Max	
Programming voltage to V_{CC}	V_{CCP} <u>1/</u>	$I_{CCP} = 375 \pm 75$ mA; transient or steady state	9.5	10.0	10.5	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S <u>2/</u>		0.9	1.0	1.1	V
Programming supply current	I_{CCP}	$V_{CCP} = +8.75 \pm .25$ V	200	250	300	mA
Input voltage high level "1"	V_{IH}		2.4		5.5	V
Input voltage low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	$V_{IH} = +5.5$ V			50	μ A
Input current	I_{IL}	$V_{IL} = +0.4$ V			-500	μ A
Output programming voltage	V_{OUT} <u>3/</u>	$I_{OUT} = 65 \pm 3$ mA transient or steady state	15.0	15.5	16.0	V
Output programming current	I_{OUT}	$V_{OUT} = +17$ V ± 1 V	62	65	68	mA
Programming voltage transition time	t_{TLH}		10		50	μ s
CE programming pulse width	t_p		300	400	500	μ s
Pulse sequence delay	t_D		10			μ s
Programming duty cycle	$\frac{t_{PR}}{t_{PR}+t_{PS}}$				50	%

1/ Bypass V_{CC} to GND with a 0.01 μ F capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ± 1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

TABLE IVG. Programming characteristics for circuit G.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Recom- mended	Max	
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	$V_{CC} = 11$ V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	$V_{OUT} = 11$ V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/ μ s
Programming pulse width (Enabled)	PWE		9	10	11	μ s
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	t_1		100			ns
V_{CCP} set-up time	t_2	<u>2/</u>	5			μ s
V_{CCP} hold time	t_5		100			ns
V_{OP} set-up time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ $T_C = 25^\circ\text{C}$.

2/ V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP} .

4.10 Programming procedure for circuit G. The programming characteristics on table IVG and the following procedures shall be used for programming:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7D and the programming characteristics of table IVG shall apply to these procedures.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase V_{CC} from nominal to V_{CCP} (10.5 ± 0.5 V) with a slew rate limit of I_{PR} (1.0 to 10.0 v/ μ s). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.
- d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ± 0.5 V). Limit the slew rate to I_{PR} (1.0 to 10.0 v/ μ s). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP} , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kilohms minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip Enable(s) to a low level. This is done with a pulse PWE for 10 μ s. The 10 μ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 (± 0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.
- g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of step f is to be performed at a V_{CC} level of 4.0 volts (± 0.2 V). V_{OH} , during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.
- h. Repeat steps b through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.
- i. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. Requirement for programming the device, including processing option.
- i. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal).
V _{IN}	- - - - -	Voltage level at an input terminal.
V _{IC}	- - - - -	Input clamp voltage.
I _{IN}	- - - - -	Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of pre-programmed devices.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type/manufacturer</u>	<u>Circuit designator</u>	<u>Fusible link</u>	<u>Symbol/FSCM number</u>
01	7602/Harris Semiconductor	A	NiCr	CDWO/34371
01	5330/Monolithic Memories	B	NiCr	CECD/50364
02	DM54S288/National Semiconductor	G	TiW/W	CCXP/27014
02	7603/Harris Semiconductor	A	NiCr	-----
02	5331/Monolithic Memories	B	NiCr	-----
01, 03	82S23A/Signetics Corporation	C	NiCr	CDKB/18324
02, 04	83S123A/Signetics Corporation	C	NiCr	-----

6.6 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17

Review activities:
 Army - AR, MI
 Navy - OS, SH, TD
 Air Force - 11, 19, 95, 99
 DLA - ES

User activities:
 Army - SM
 Navy - AS, CG, MC

Preparing activity:
 Air Force - 17

Agent:
 DLA - ES

(Project 5962-0858)