

Thermal resistance, junction-to-case (θ_{JC}) ^{1/} :	
Cases J, K, and Y- - - - -	30°C/W
Cases X and Z- - - - -	36°C/W
Output voltage - - - - -	-0.5 V dc to +V _{CC}
Output sink current- - - - -	100 mA
Maximum power dissipation (P _D) ^{2/} - - - - -	1.02 W
Maximum junction temperature (T _J)- - - - -	175°C

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage - - - - -	2.0 V dc
Maximum low-level input voltage- - - - -	0.8 V dc
Normalized fanout (each output)- - - - -	8 mA ^{3/}
Case operating temperature range - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.2 Truth table.

^{1/} Heat sinking is recommended to reduce the junction temperature.

^{2/} Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

^{3/} 16 mA for circuit F devices.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/2/</u>	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2 mA	02,03,05	2.4	---	V
Low-level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8 mA <u>3/</u>	A11	---	0.5	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -10 mA, T _C = 25°C	A11	---	-1.5	V
Maximum collector cut-off current	I _{CEX}	V _{CC} = 5.5 V, V _O = 5.2 V	01,04	---	100	μA
High-impedance (off-state) output high current	I _{OHZ}	V _{CC} = 5.5 V, V _O = 5.2 V	02,03,05	---	100	μA
High-impedance (off-state) output low current	I _{OLZ}	V _{CC} = 5.5 V, V _O = 0.5 V	02,03,05		-100	μA
High-level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	A11	---	50	μA
	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 4.5 V, special programming pin	A11	---	100	μA
Low-level input current	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.5 V	A11	-1.0	-250	μA
	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.5 V, for CE ₃ and CE ₄	01,02	-1.0	-1000	μA
Short circuit output current	I _{OS}	V _{CC} = 5.5 V, V _O = 0.0 V <u>4/</u>	02,03,05	-10	-100	mA
Supply current	I _{CC}	V _{CC} = 5.5 V, V _{IN} = 0, outputs = open	01,02,03	---	185	mA
			04,05	---	155	mA
Propagation delay time, high-to-low level logic, address to output	t _{PHL1}	V _{CC} = 4.5 V and 5.5 V, C _L = 30 pF (see figure 7)	01,02,03	---	90	ns
			04,05	---	80	ns
Propagation delay time, low-to-high level logic, address to output	t _{PLH1}		01,02,03	---	90	ns
			04,05	---	80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/2/	Device type	Limits		Unit
				Min	Max	
Propagation delay time, high-to-low level logic, enable to output	tPHL2	V _{CC} = 4.5 V and 5.5 V, C _L = 30 pF (see figure 7)	01,02,03	---	50	ns
			04,05	---	40	ns
Propagation delay time, low-to-high level logic, enable to output	tPLH2		01,02,03	---	50	ns
			04,05		40	ns

1/ Complete terminal conditions shall be as specified on table III.

2/ For device type 03, the fusing pins FE₁ and FE₂ may be grounded or floating during operation.

3/ I_{OL} = 16 mA for circuit F devices.

4/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)		
	Class S devices	Class B devices	Class C devices
Interim electrical tests (pre burn-in) (method 5004)	1	1	None
Final electrical tests (method 5004) for unprogrammed devices	1*,2,3,7*,8	1*,2,3,7*,8	1
Final electrical tests (method 5004) for programmed devices	1*,2,3,7*,8,9,10,11	1*,2,3,7*,8,9	1,7,9
Group A electrical tests (method 5005)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11
Group B electrical tests (method 5005, subgroup 5)	1,2,3,7,8,9,10,11	N/A	N/A
Group C end-point electrical tests (method 5005)	N/A	1,2,3,7,8	1,2,3,7
Group D end-point electrical tests (method 5005)	1,2,3,7,8	1,2,3,7,8	1,2,3,7

NOTES:

- * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
- Any or all subgroups may be combined when using high-speed testers.
- Subgroups 7 and 8 shall consist of verifying the pattern specified.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 4. When required in group A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 5.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics of table I apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be as indicated by the subgroups shown in table II and, where applicable, by the altered item drawing. The subgroup tests shall be as specified in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container.

3.7 Processing options. Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspections. The following additional criteria shall apply:

- a. Interim and final electrical tests shall be as specified in table II; the interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- b. Burn-in test (method 1015 of MIL-STD-883, test condition D or E), using the circuit shown on figure 6 or equivalent.

- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. The freeze-out test shall be conducted as a 100-percent screen on all class S devices having nichrome as the fusible link. Within no more than 24 hours after completion of burn-in and prior to the final electrical test, all devices having nichrome as the fusing link shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned with at least 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical tests shall be completed within 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:
- Step 1. Connect devices in the electrical configuration of figure 9 or in the burn-in configuration of figure 6 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - Step 2. Reduce device temperature to $T_A = -10^\circ\text{C} \pm 2^\circ\text{C}$ with bias cycled and maintain at that temperature for a minimum of 5 hours.
 - Step 3. With the cycled bias maintained, allow T_A to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_A shall not exceed 35°C during this period.
 - Step 4. Remove bias and subject all devices to subgroup 1 final electrical tests to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.
- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 through 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

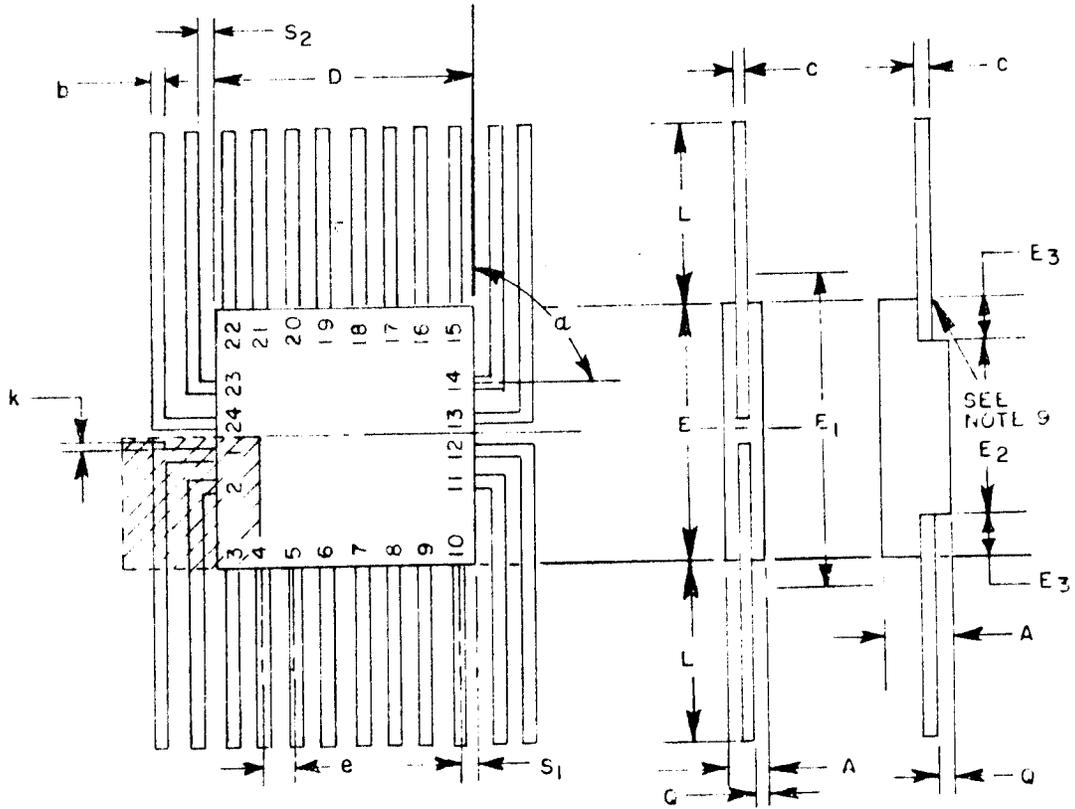
- a. Electrical tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy the programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowed.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein. Class S devices selected for testing in subgroup 5, table IIa of method 5005 of MIL-STD-883, shall be programmed in accordance with 3.2.2.
- b. Steady state life test for class S devices shall be in accordance with subgroup 5, table IIa of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 6 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883, test condition D or E), using the circuit shown on figure 6 or equivalent.
 - (1) $T_A = 125^{\circ}\text{C}$ minimum.
 - (2) Test duration = 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. For qualification inspection, at least 25 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.



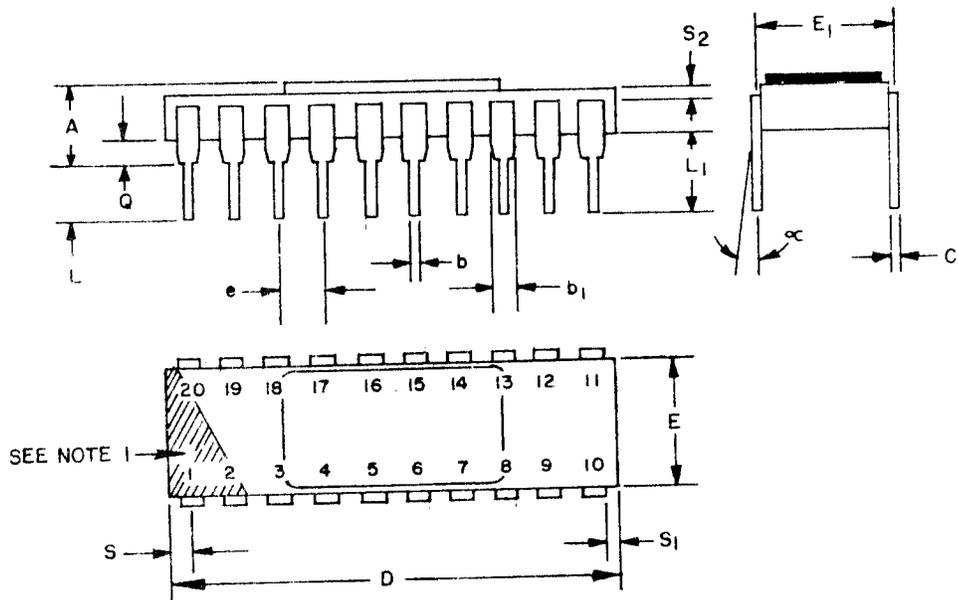
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.045	.090	1.14	2.29	
b	.015	.019	.38	.48	5
c	.003	.006	.08	.15	5
D	---	.400	---	10.16	3
E	.340	.385	8.64	9.78	
E ₁	---	.400	---	10.16	3
E ₂	.125	---	3.18	---	
E ₃	.030	---	.76	---	14
e	.050 BSC		1.27 BSC		4,6
k	.008	.015	.20	.38	10
L	.250	.370	6.35	9.40	
Q	.010	.040	.25	1.02	2
S ₁	.005	---	.13	---	7,8
S ₂	.005	---	.13	---	11
α	30°	90°	30°	90°	12,13

FIGURE 1. Case outline X (24-lead, 3/8" x 3/8").

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within $\pm .005$ (.13 mm) of its exact longitudinal position relative to pins 1 and 24.
5. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Twenty-two spaces.
7. Applies to all four corners (leads number 3, 10, 15, and 22).
8. Dimension S_1 may be .000 (.00 mm) if leads number 3, 10, 15, and 22 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body (see 40.3 of appendix C, MIL-M-38510).
9. Optional configuration; if this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.
11. Applies to leads number 2, 11, 14 and 23.
12. Lead configuration is optional within dimension E except dimensions b and c apply (see 40.2 of appendix C, MIL-M-38510).
13. Applies to leads number 1, 2, 11, 12, 13, 14, 23, and 24.
14. Applies to all edges.

FIGURE 1. Case outline x (24-lead, 3/8" x 3/8") - Continued.

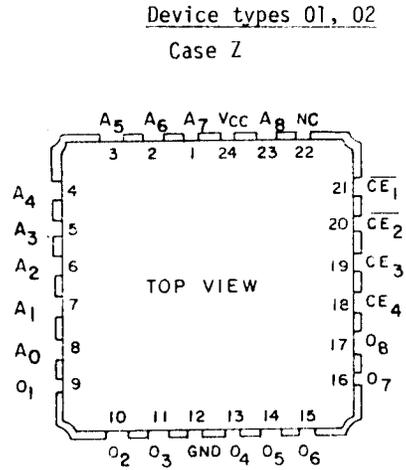
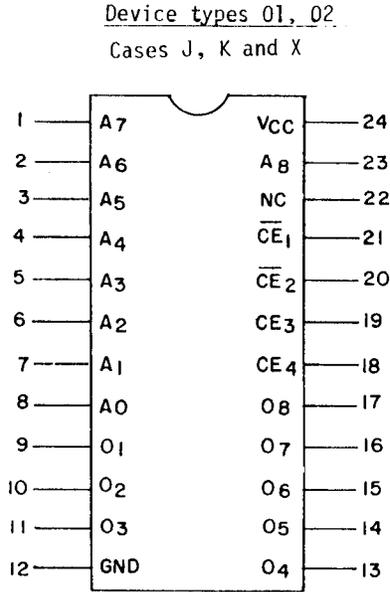


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	---	.175	---	4.44	
b	.016	.020	.41	.51	11,8
b ₁	.040	.060	1.02	1.52	8,2
C	.008	.012	.20	.30	11,8
D	.970	1.010	24.64	25.65	4
E	.280	.300	7.11	7.62	4
E ₁	.290	.320	7.37	8.13	7
e	.090	.110	2.29	2.79	5,9
L	.125	.180	3.18	4.58	
L ₁	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
S	---	.098	---	2.49	6
S ₁	.005	---	.13	---	6
S ₂	.005	---	.13	---	8
α	0°	15°	0°	15°	

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b₁ may be .020 (.51 mm) for leads number 1, 10, 11, and 20 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corners (leads number 1, 10, 11, and 20) (see 40.5 of appendix C, MIL-M-38510).
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads (see 40.4 of appendix C, MIL-M-38510).
8. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Eighteen spaces.
10. No organic or polymeric materials shall be molded to the bottom of the package.
11. Applies to all leads.

FIGURE 2. Case outline Y (20-lead, 5/16" x 1.0").



OPTION A WITH ACTIVE TERMINALS
ON PLANE 1.

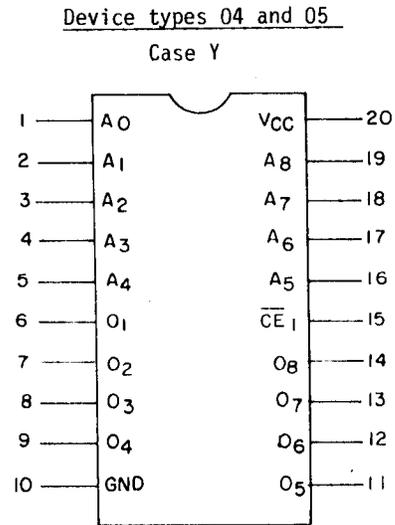
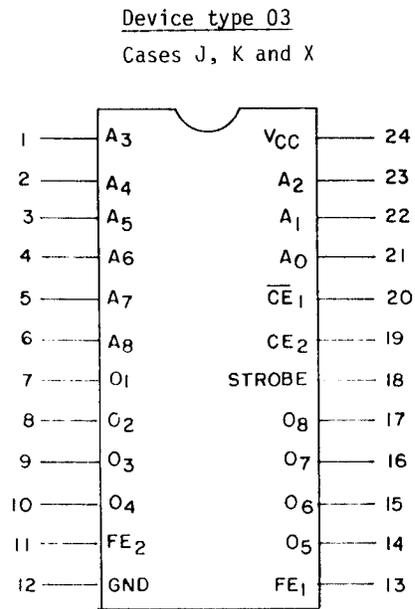


FIGURE 3. Terminal connections.

Device types 01 and 02

WORD NO.	ENABLE				ADDRESS									DATA							
	\overline{CE}_1	\overline{CE}_2	CE_3	CE_4	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈
NA	L	L	L	L	X	X	X	X	X	X	X	X	X	OC							
NA	H	L	L	L	X	X	X	X	X	X	X	X	X	OC							
NA	L	H	L	L	X	X	X	X	X	X	X	X	X	OC							
NA	H	H	L	L	X	X	X	X	X	X	X	X	X	OC							
NA	L	L	H	L	X	X	X	X	X	X	X	X	X	OC							
NA	H	L	H	L	X	X	X	X	X	X	X	X	X	OC							
NA	L	H	H	L	X	X	X	X	X	X	X	X	X	OC							
NA	H	H	H	L	X	X	X	X	X	X	X	X	X	OC							
NA	L	L	L	H	X	X	X	X	X	X	X	X	X	OC							
NA	H	L	L	H	X	X	X	X	X	X	X	X	X	OC							
NA	L	H	L	H	X	X	X	X	X	X	X	X	X	OC							
NA	H	H	L	H	X	X	X	X	X	X	X	X	X	OC							
NA	L	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	L	H	H	X	X	X	X	X	X	X	X	X	OC							
NA	L	H	H	H	X	X	X	X	X	X	X	X	X	OC							
NA	H	H	H	H	X	X	X	X	X	X	X	X	X	OC							

Device type 03

WORD NO.	ENABLE			ADDRESS									DATA							
	\overline{CE}_1	CE_2	STROBE	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈
NA	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	X	X	X	X	X	X	X	X	X	Last data is latched							

Device types 04 and 05

WORD NO.	ENABLE	ADDRESS										DATA							
	CE_1	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	
NA	H	X	X	X	X	X	X	X	X	X	OC								
NA	L	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/	

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. The outputs for an unprogrammed device shall be high for circuits A, B, D, and F, and low for circuits C and G.

FIGURE 4. Truth table (unprogrammed).

LOGIC CIRCUIT B
 (Device types 01, 02, 04, & 05) and
 LOGIC CIRCUIT F
 (Device type 05)

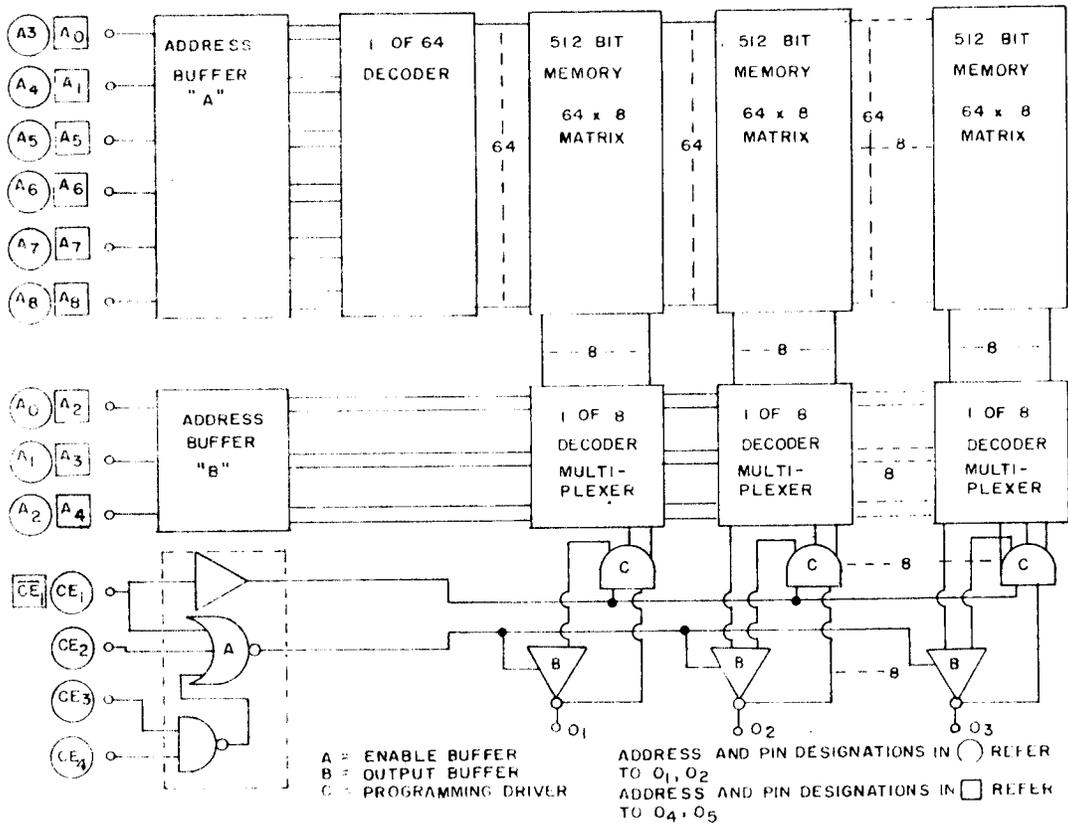


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT C
(Device types 01 and 02)

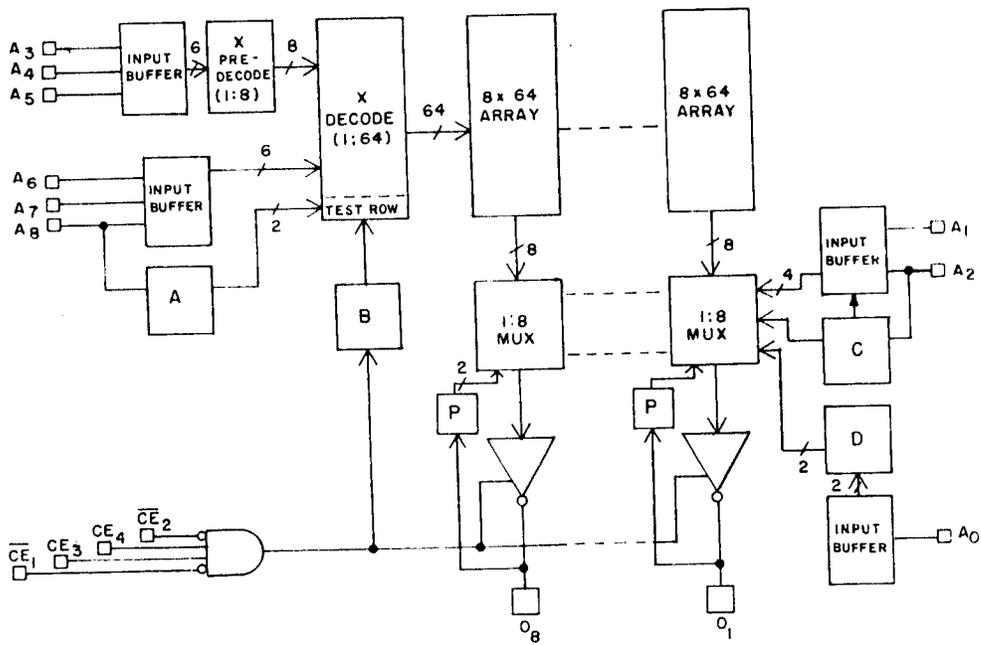


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT C
(Device type 03)

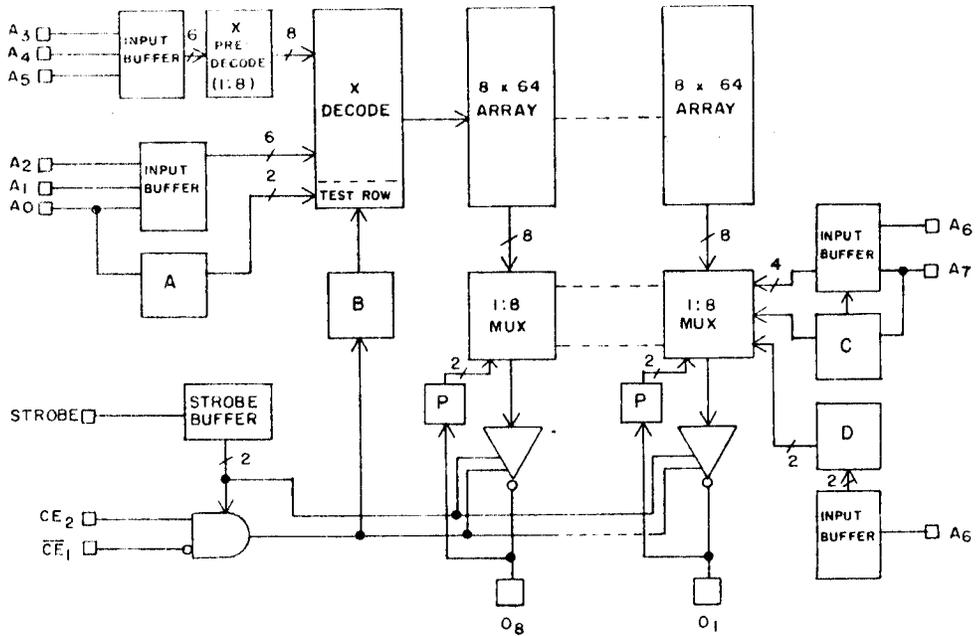


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT D
(Device types 01 and 02)

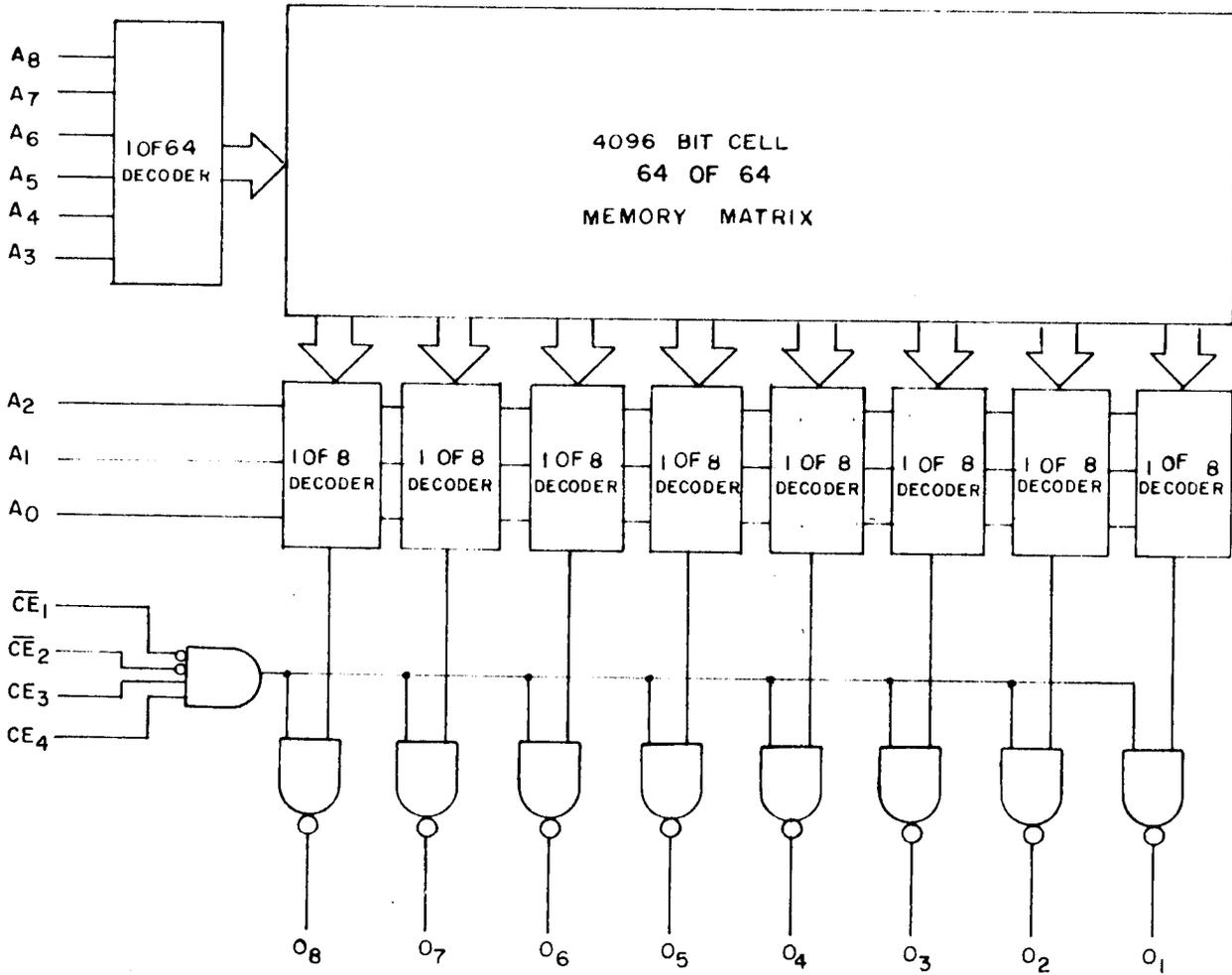


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device type 01)

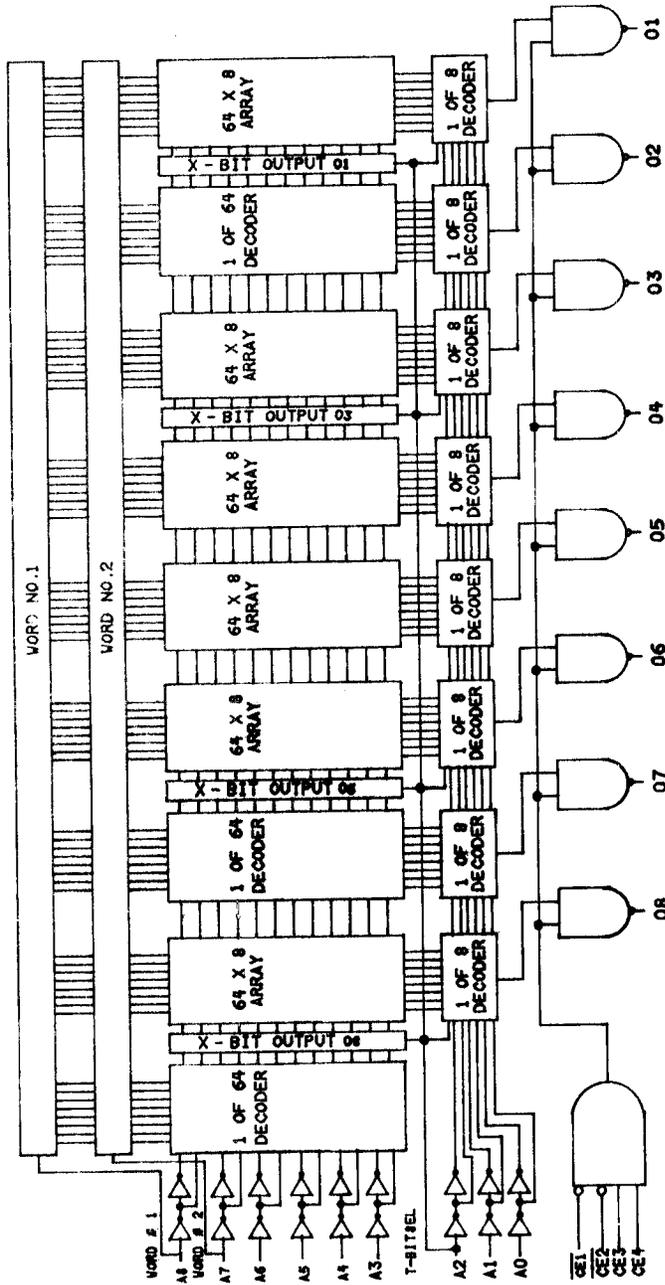


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device type 02)

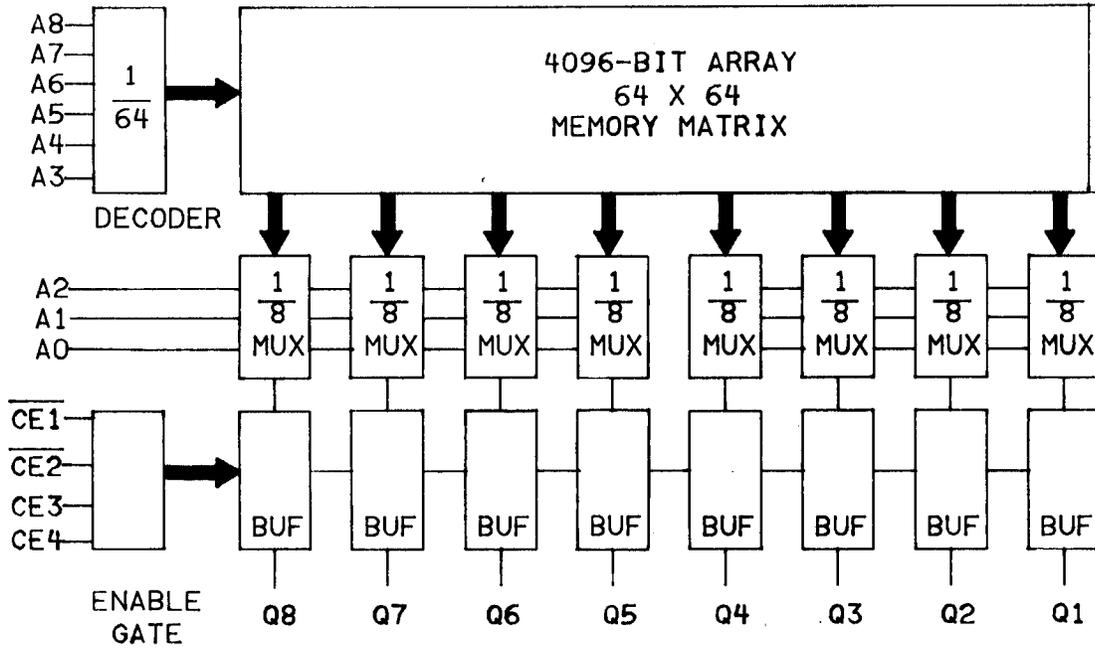


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device types 04 and 05)

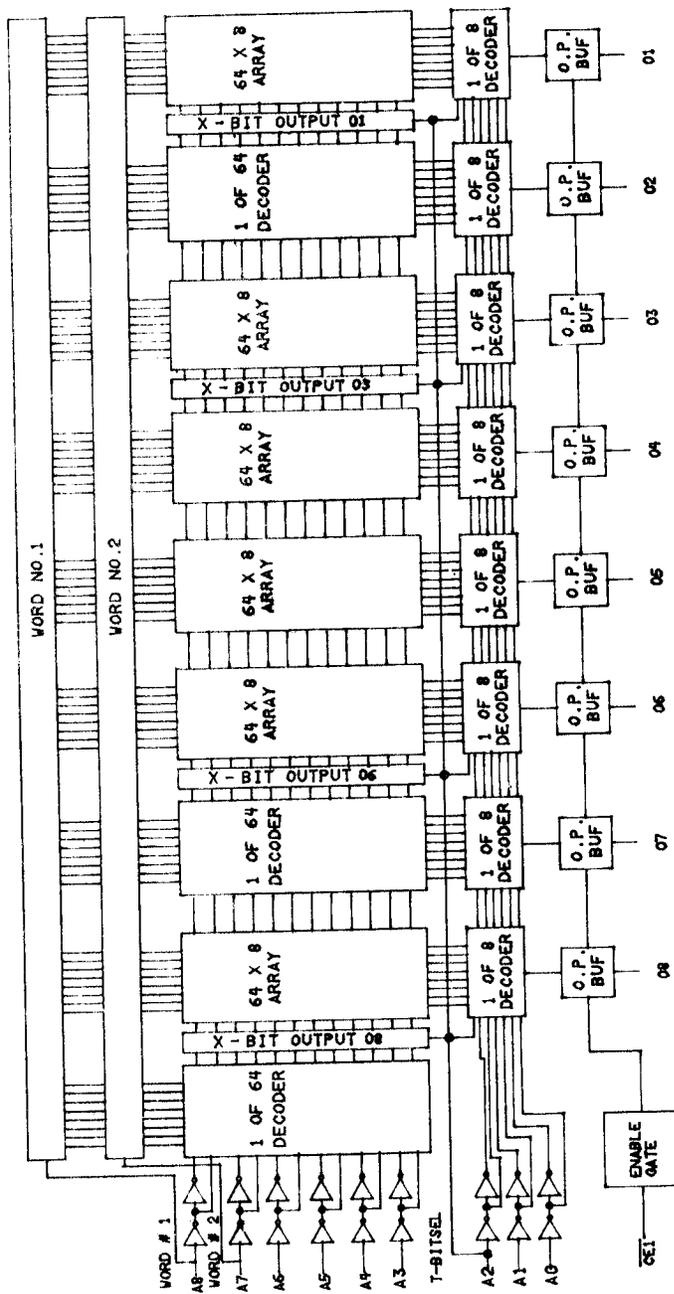
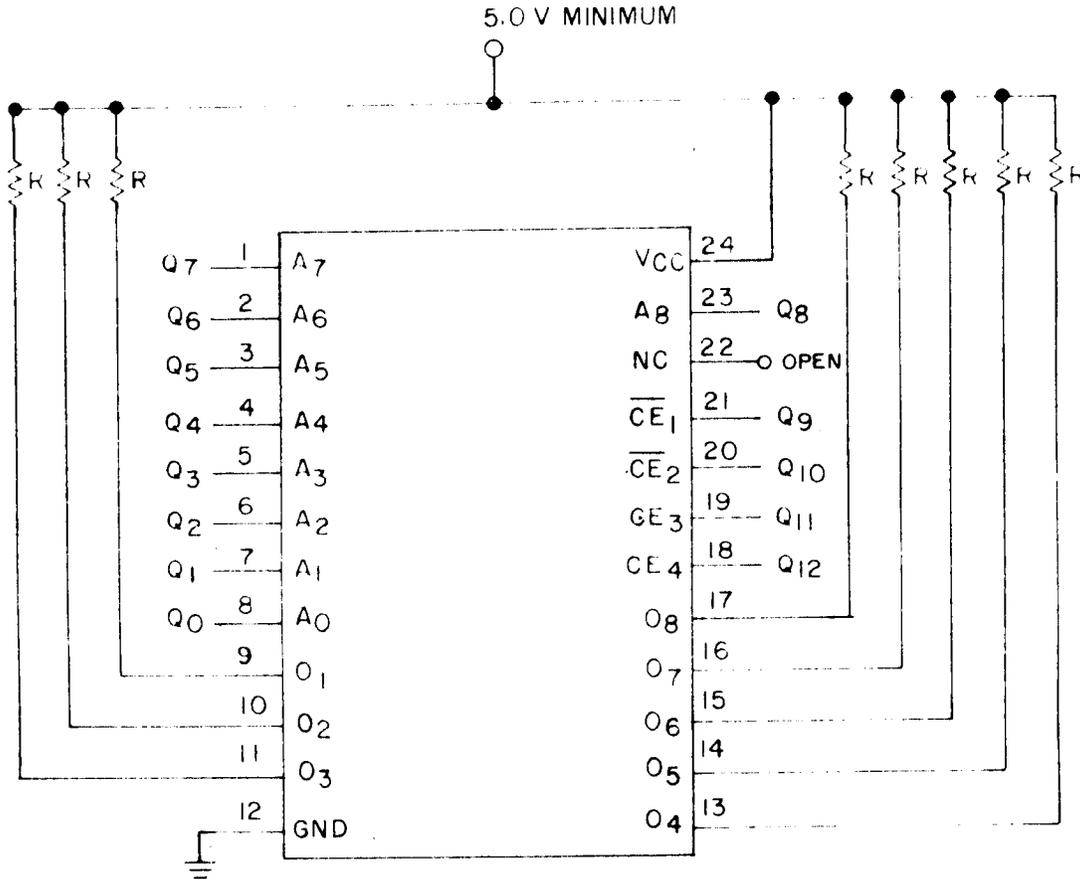


FIGURE 5. Logic diagrams - Continued.

Device types 01 and 02.



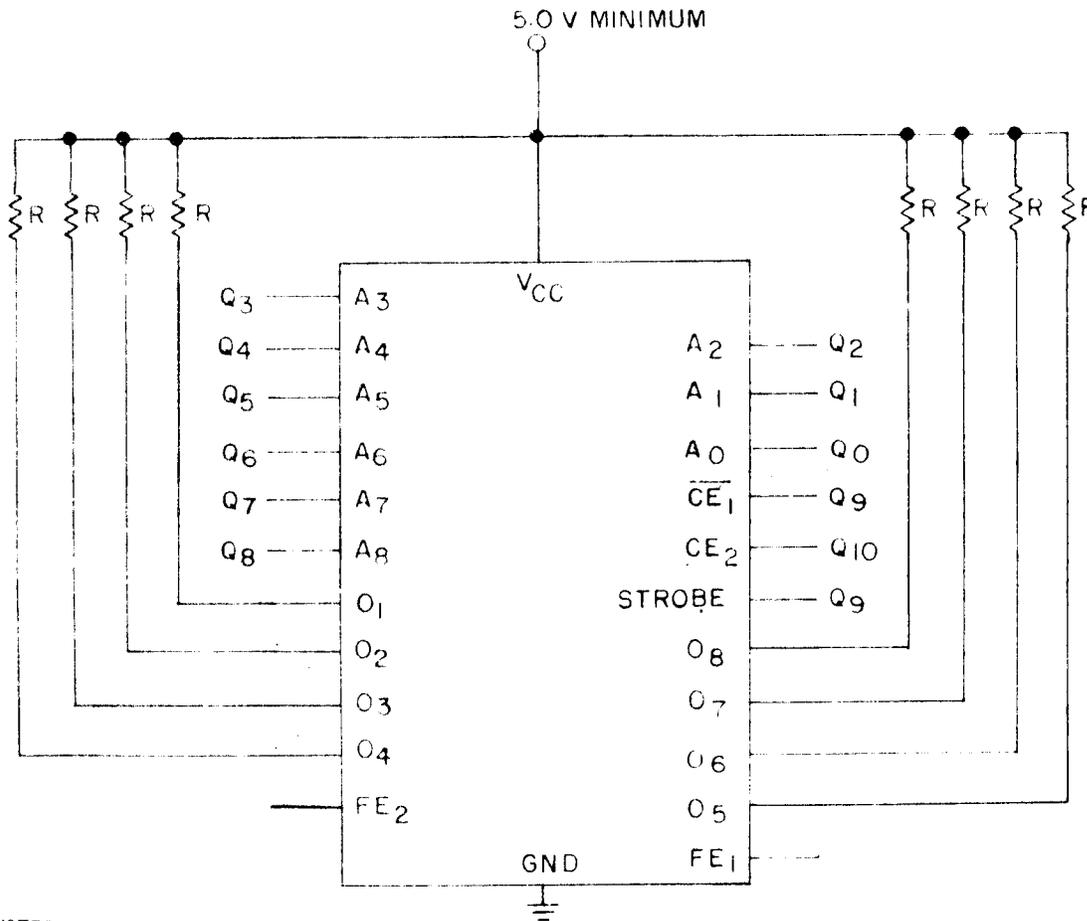
NOTES:

1. $R = 560\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
3. All pulse generators have the following characteristics: $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle; and input frequencies as follows:

Input	Frequency ($\pm 50\%$)
Q_0	$f_0 = 100$ kHz min.
Q_1	$f_1 = 1/2 f_0$
Q_2	$f_2 = 1/2 f_1$
Q_3	$f_3 = 1/2 f_2$
Q_4	$f_4 = 1/2 f_3$
Q_5	$f_5 = 1/2 f_4$
Q_6	$f_6 = 1/2 f_5$
Q_7	$f_7 = 1/2 f_6$
Q_8	$f_8 = 1/2 f_7$
Q_9	$f_9 = 1/2 f_8$
Q_{10}	$f_{10} = 1/2 f_9$
Q_{11}	$f_{11} = 1/2 f_{10}$
Q_{12}	$f_{12} = 1/2 f_{11}$

FIGURE 6. Burn-in and steady state life test circuit.

Device type 03

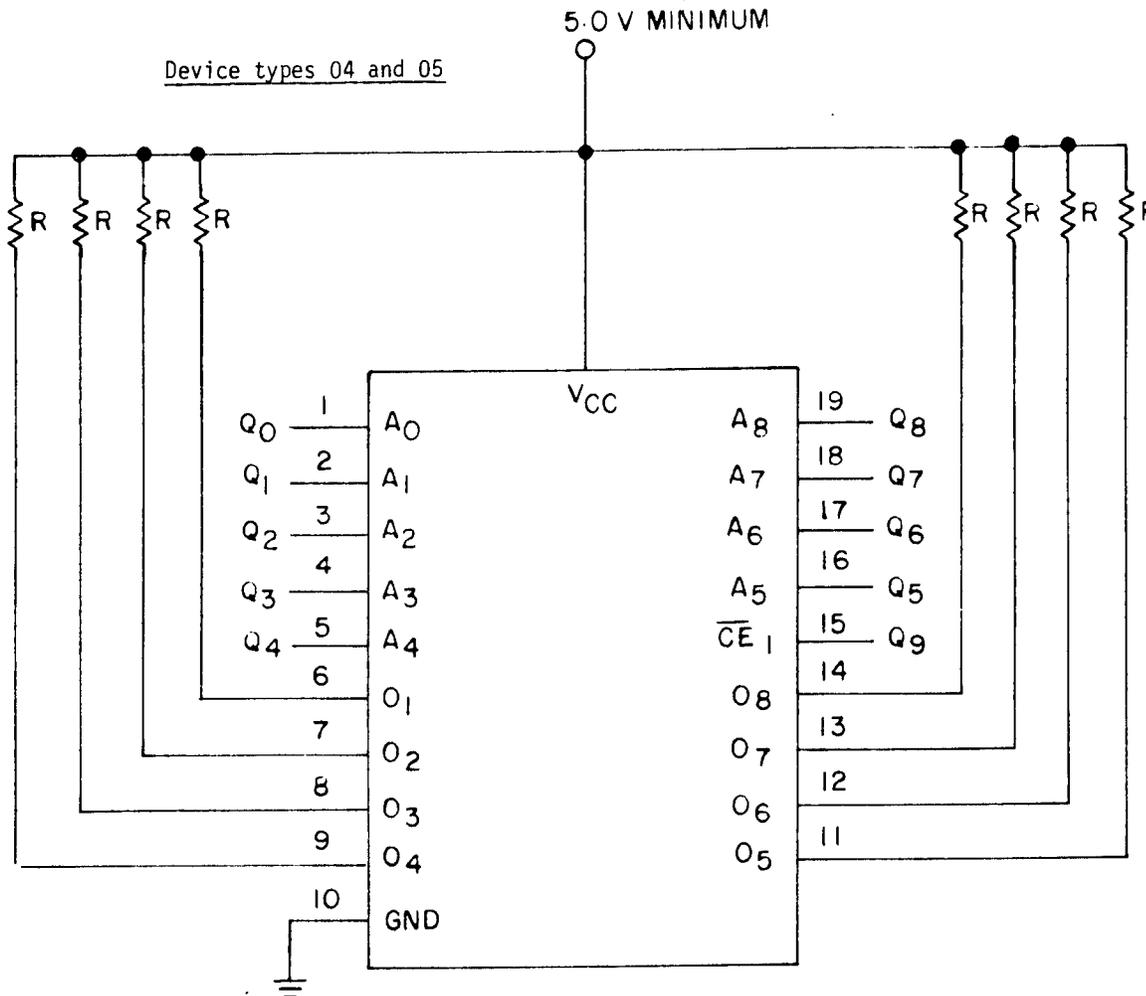


NOTES:

1. $R = 560\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle and frequencies as specified in note 5.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. FE_1 and FE_2 should be GND or open.
5. Input frequencies are as follows:

Input	Frequency ($\pm 50\%$)
Q_0	$f_0 = 100$ kHz min.
Q_1	$f_1 = 1/2 f_0$
Q_2	$f_2 = 1/2 f_1$
Q_3	$f_3 = 1/2 f_2$
Q_4	$f_4 = 1/2 f_3$
Q_5	$f_5 = 1/2 f_4$
Q_6	$f_6 = 1/2 f_5$
Q_7	$f_7 = 1/2 f_6$
Q_8	$f_8 = 1/2 f_7$
Q_9	$f_9 = 1/2 f_8$
Q_{10}	$f_{10} = 1/2 f_9$

FIGURE 6. Burn-in and steady state life test circuit - Continued.

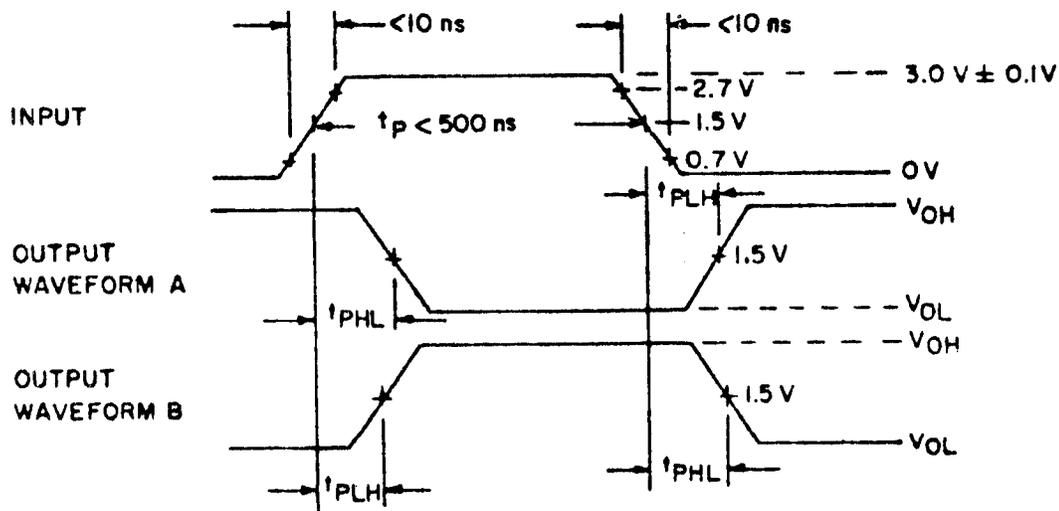
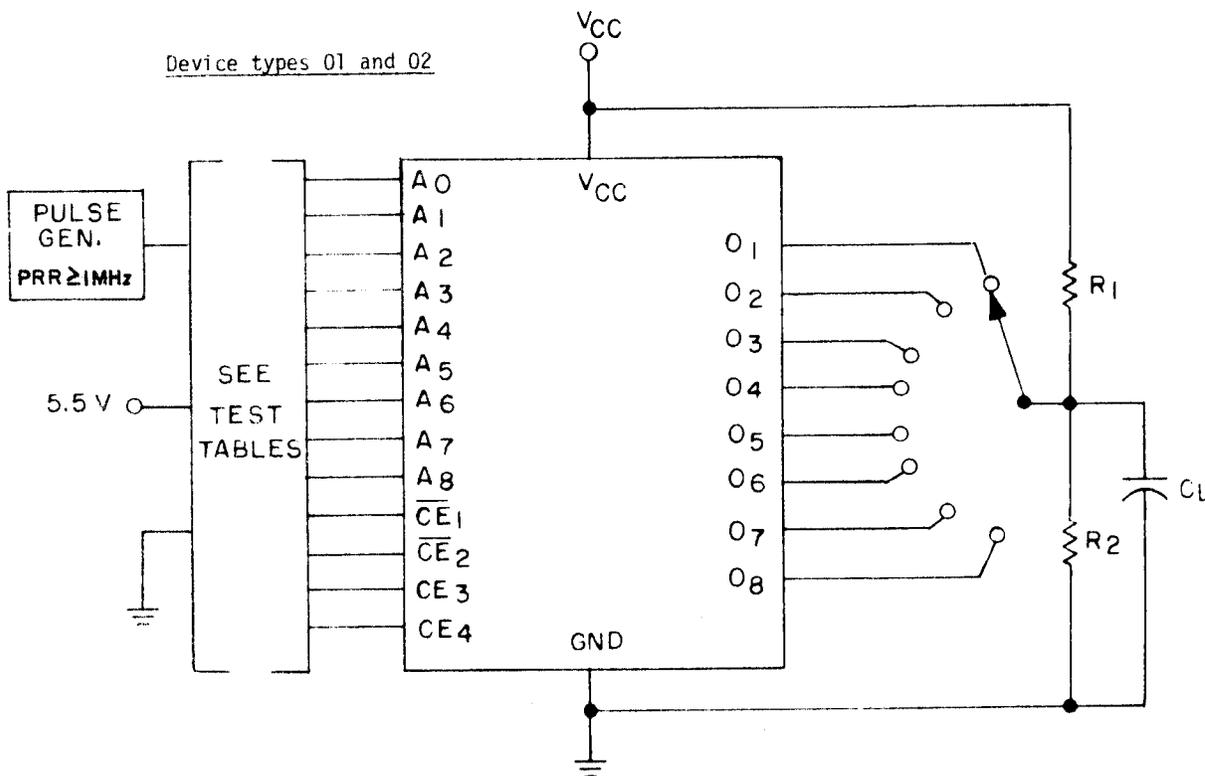


NOTES:

1. $R = 560\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency ($\pm 50\%$)
Q_0	$f_0 = 100$ kHz min.
Q_1	$f_1 = 1/2 f_0$
Q_2	$f_2 = 1/2 f_1$
Q_3	$f_3 = 1/2 f_2$
Q_4	$f_4 = 1/2 f_3$
Q_5	$f_5 = 1/2 f_4$
Q_6	$f_6 = 1/2 f_5$
Q_7	$f_7 = 1/2 f_6$
Q_8	$f_8 = 1/2 f_7$
Q_9	$f_9 = 1/2 f_8$
Q_{10}	$f_{10} = 1/2 f_9$
Q_{11}	$f_{11} = 1/2 f_{10}$
Q_{12}	$f_{12} = 1/2 f_{11}$

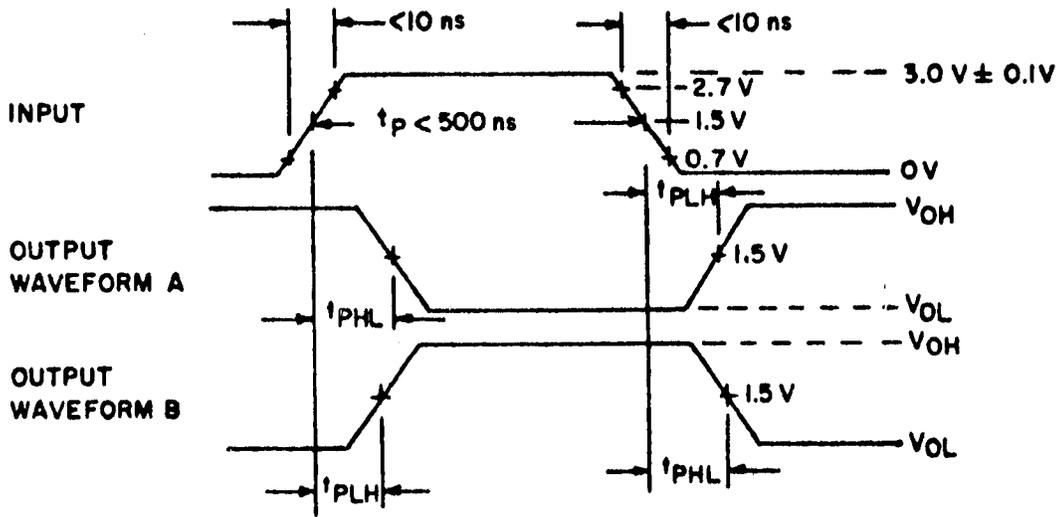
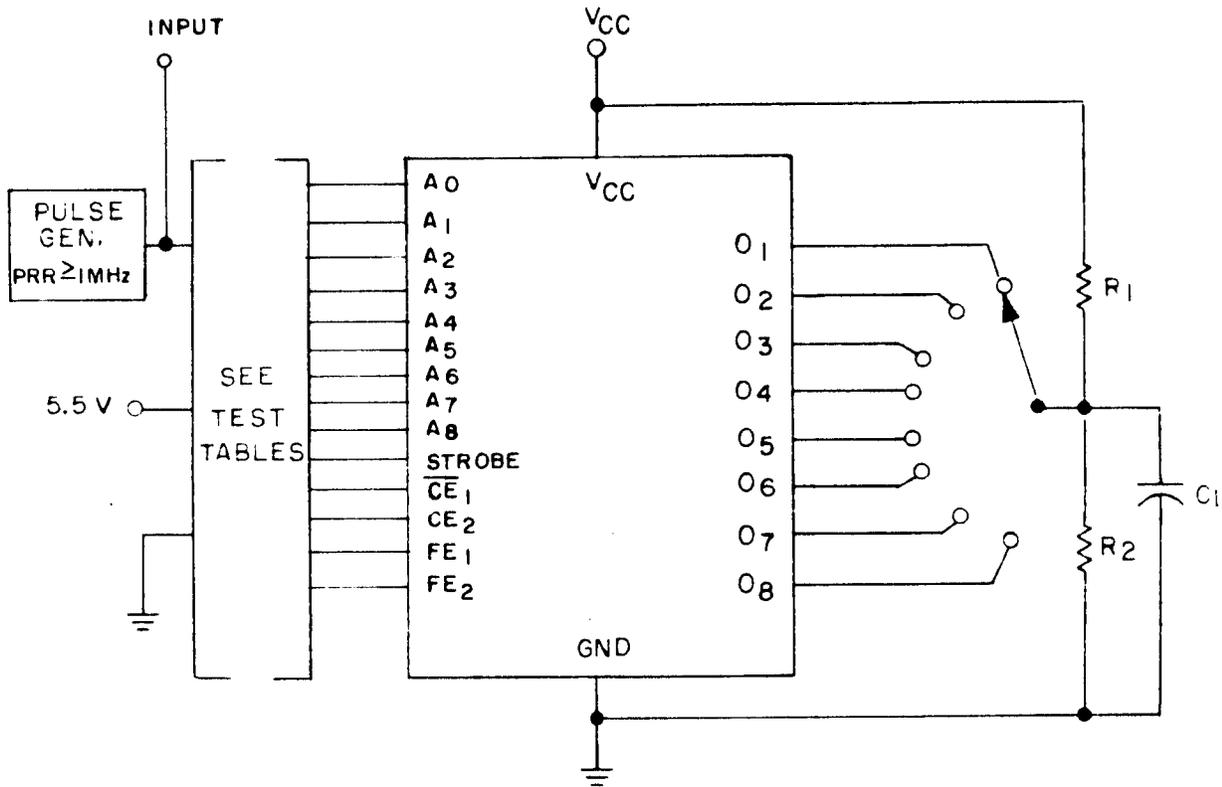
FIGURE 6. Burn-in and steady state life test circuit - Continued.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

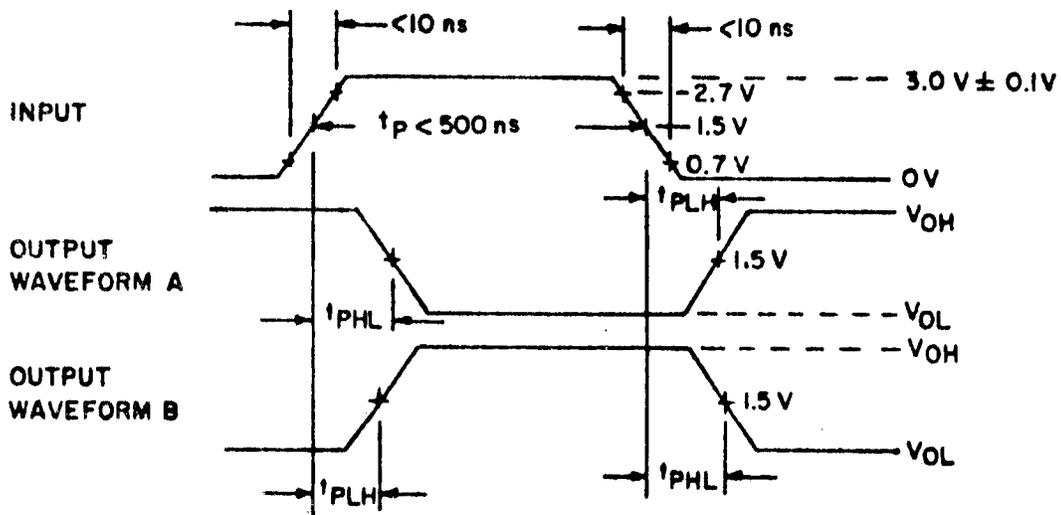
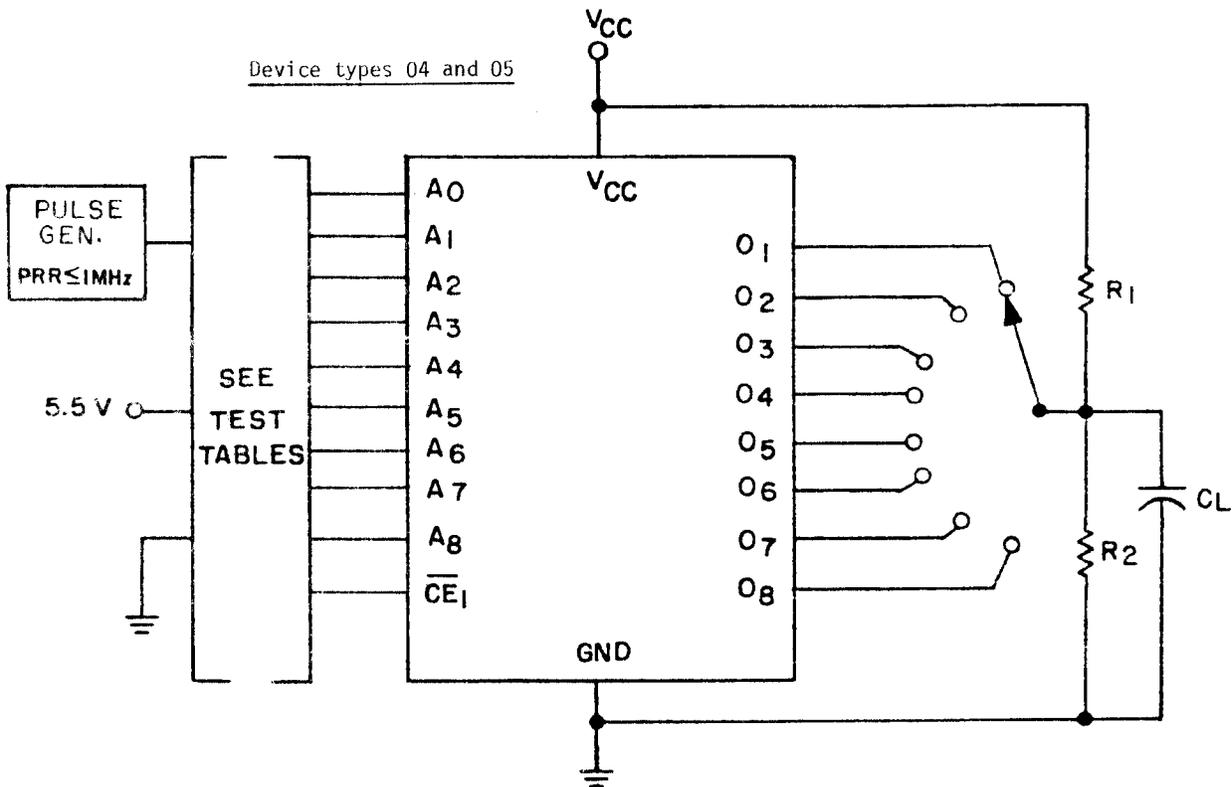
FIGURE 7. Switching time test circuit.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

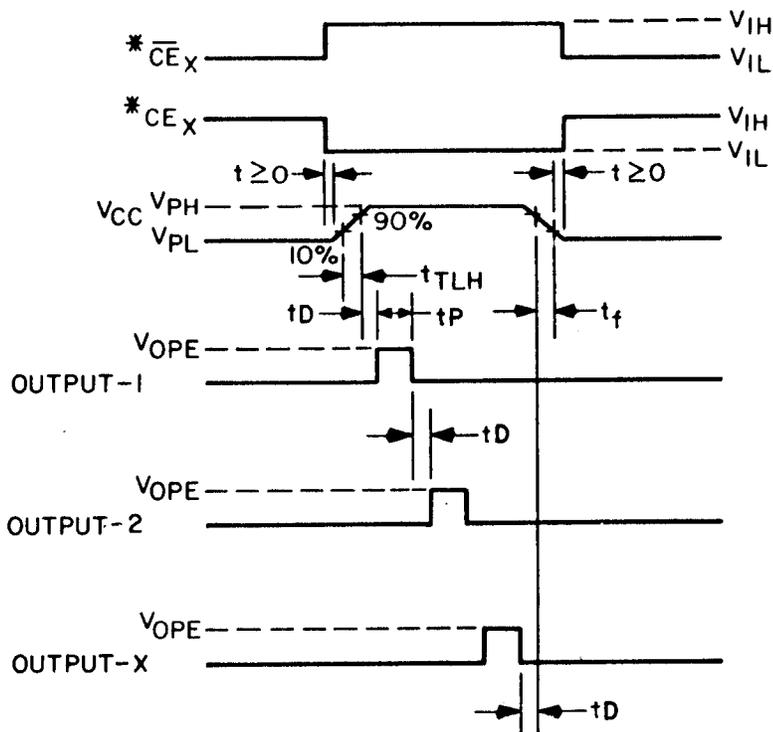
FIGURE 7. Switching time test circuit - Continued.



NOTES:

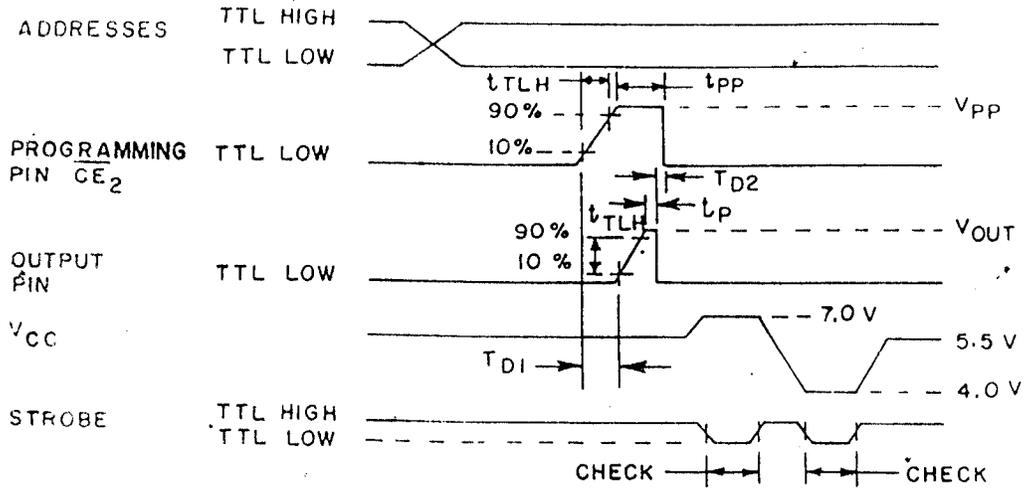
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

FIGURE 7. Switching time test circuit - Continued.



- NOTES:
1. (*) Disregard for devices with no chip enable inputs.
 2. All other waveform characteristics shall be as specified in table IVA.

FIGURE 8a. Programming voltage waveforms during programming for circuit A.

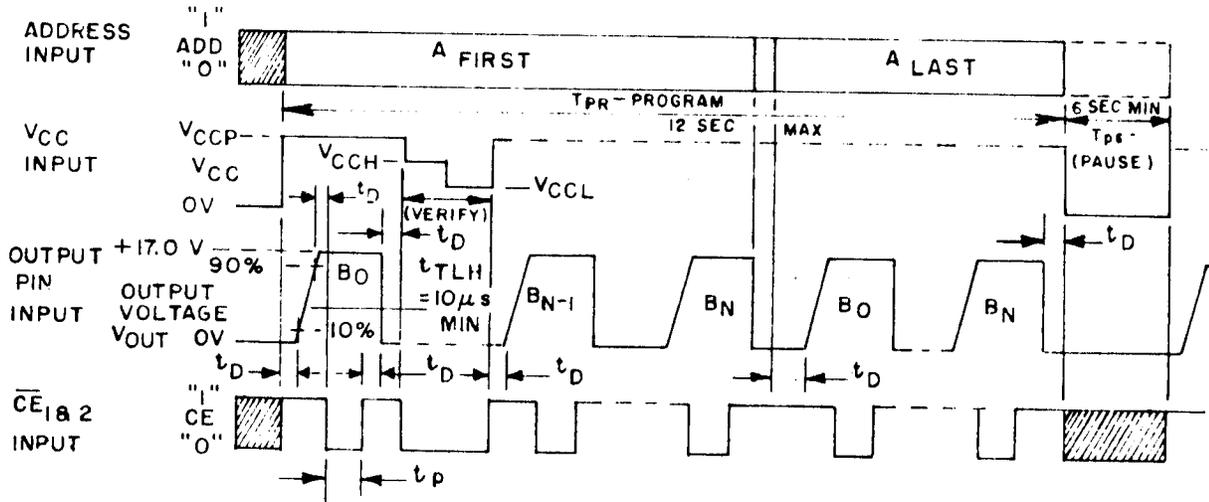


NOTES:

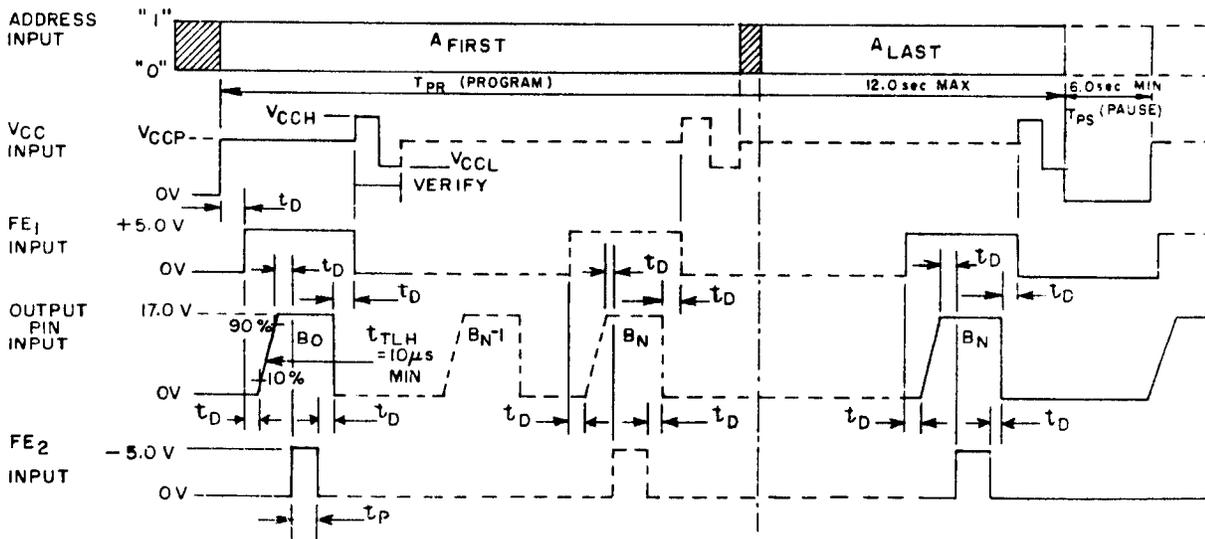
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in IVB.
3. CE_1 is the programming pin for device types 04 and 05.

FIGURE 8b. Programming voltage waveforms during programming for circuit B.

Device types 01 and 02

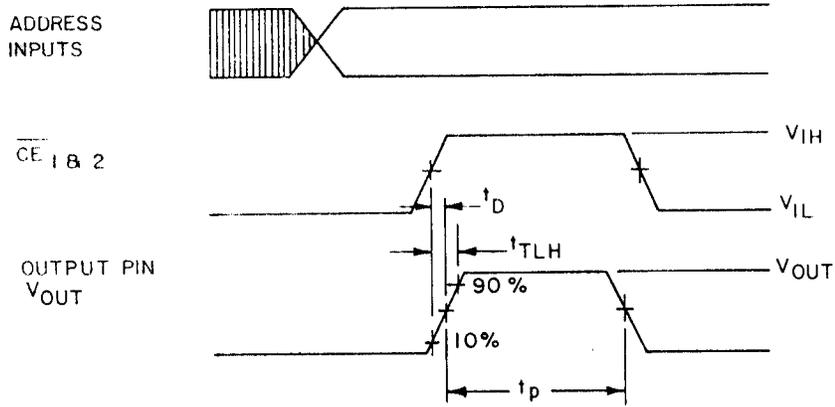


Device type 03



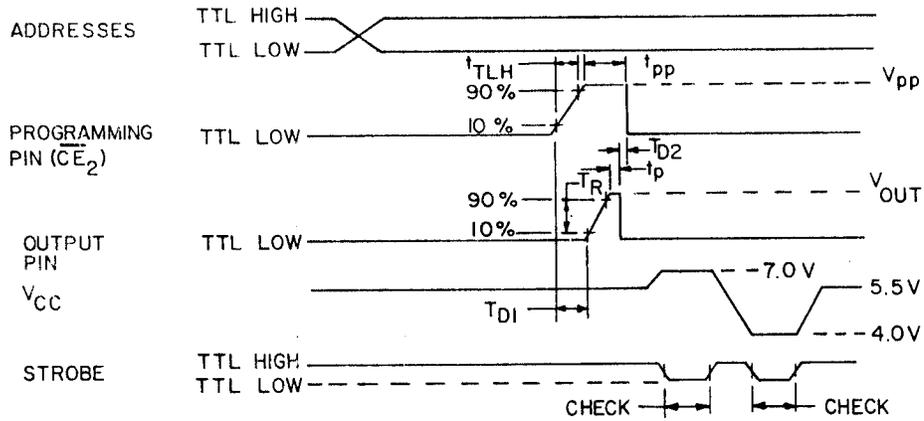
NOTE: All other waveform characteristics shall be as specified in tabel IVC.

FIGURE 8c. Programming voltage waveforms during programming for circuit C.



NOTE: All other waveform characteristics shall be as specified in table IV.D.

FIGURE 8d. Programming voltage waveforms during programming for circuit D.



NOTES:

1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IV.F.

FIGURE 8e. Programming voltage waveforms during programming for circuit F.

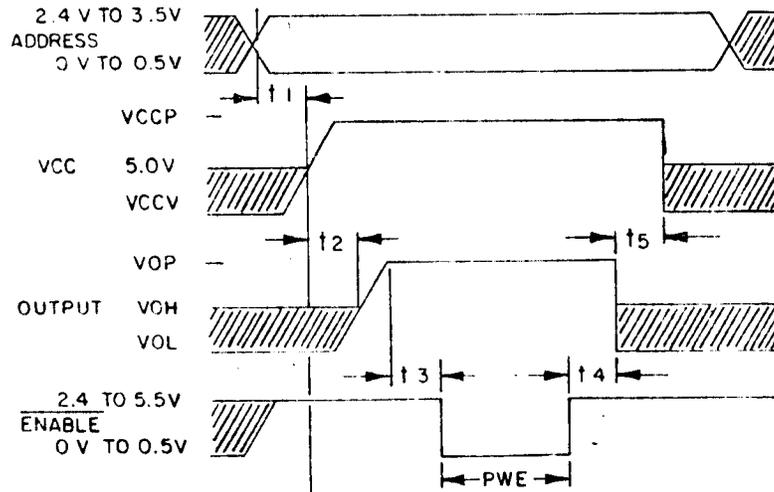
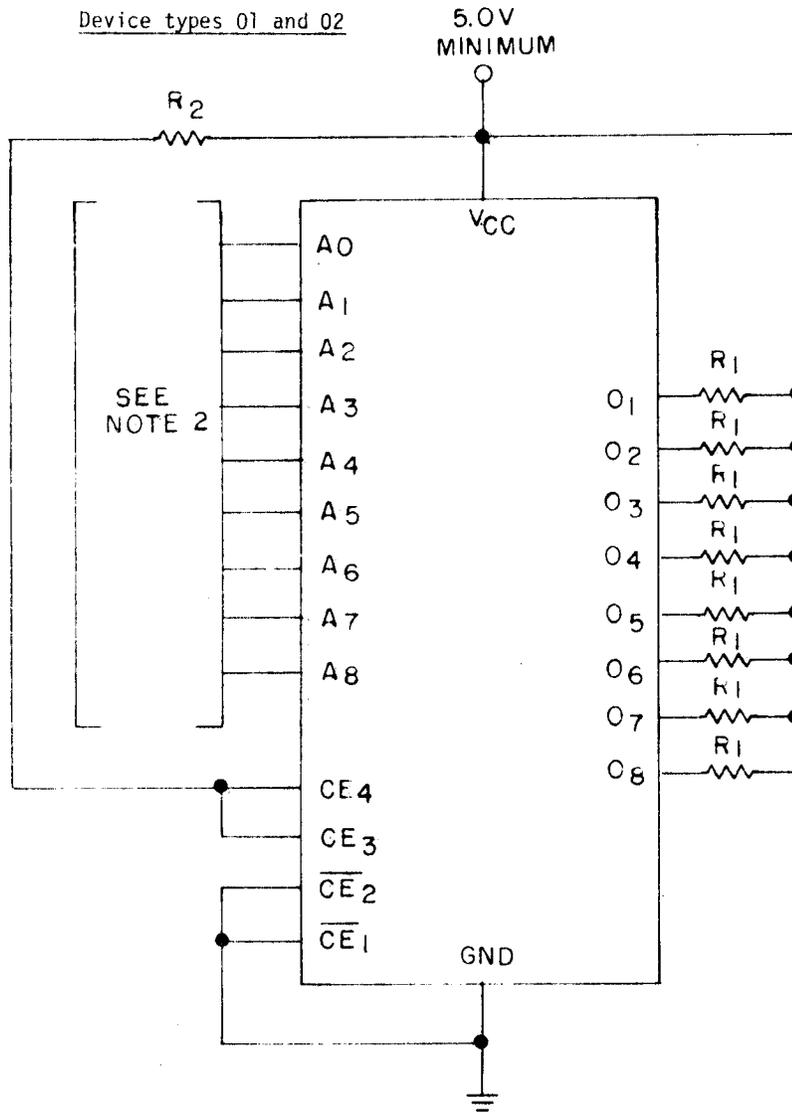


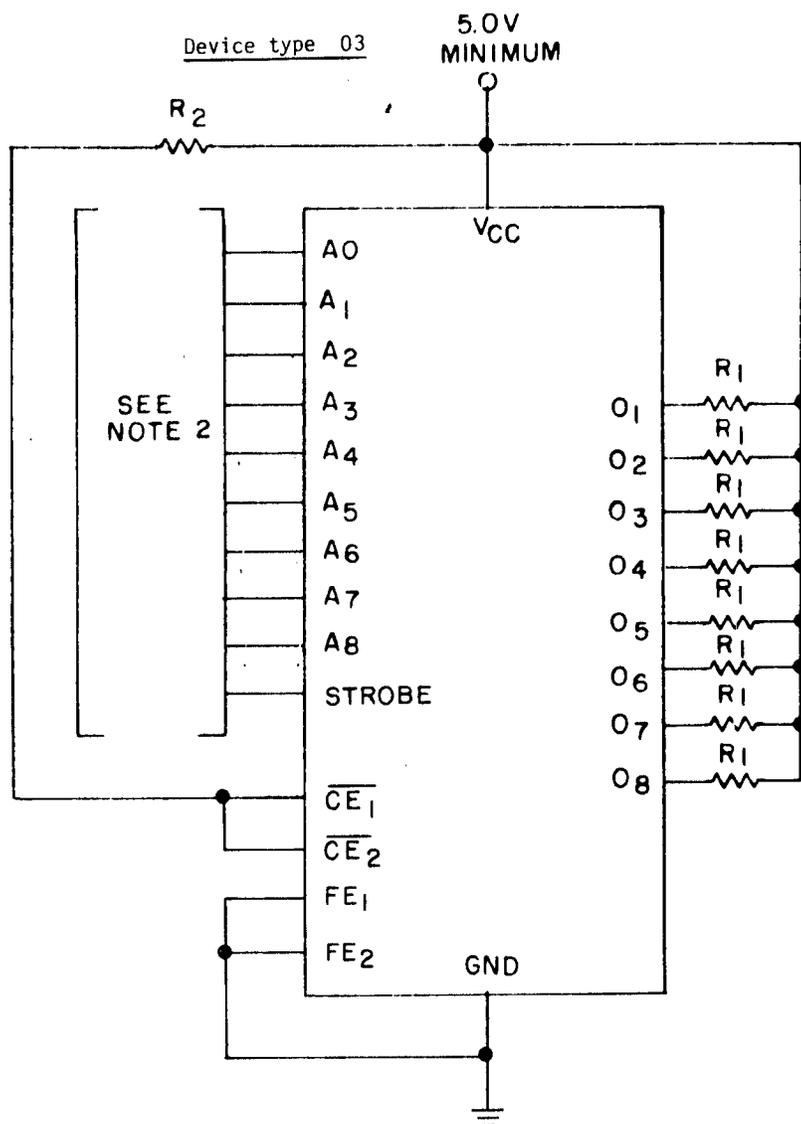
FIGURE 8j. Programming voltage waveforms during programming for circuit G.



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test. (see 4.2d).

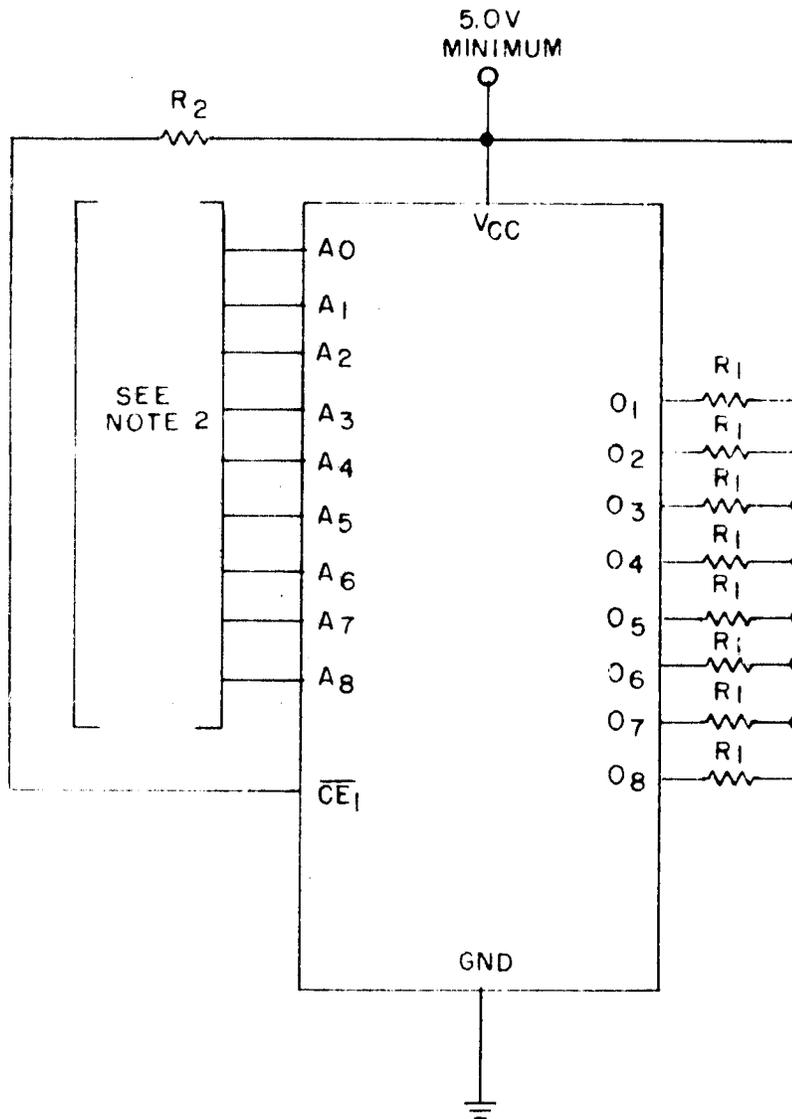
FIGURE 9. Freeze-out test bias configuration.



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test. (See 4.2d.)

FIGURE 9. Freeze-out test bias configuration - Continued.



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test. (See 4.2d.)

FIGURE 9. Freeze-out test bias configuration - Continued.

TABLE III. Group A inspection for device type 04.
Terminal conditions: Outputs not designated are open or resistive coupled to GND or V_{CC}. Inputs not designated may be high >2.0 V, low <0.6 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Case V								Measured terminal								Test limits		Unit																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		19	20	Min	Max																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
T _C = 25°C	V _{IC}	N/A	1	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	A33	A34	A35	A36	A37	A38	A39	A40	A41	A42	A43	A44	A45	A46	A47	A48	A49	A50	A51	A52	A53	A54	A55	A56	A57	A58	A59	A60	A61	A62	A63	A64	A65	A66	A67	A68	A69	A70	A71	A72	A73	A74	A75	A76	A77	A78	A79	A80	A81	A82	A83	A84	A85	A86	A87	A88	A89	A90	A91	A92	A93	A94	A95	A96	A97	A98	A99	A100	A101	A102	A103	A104	A105	A106	A107	A108	A109	A110	A111	A112	A113	A114	A115	A116	A117	A118	A119	A120	A121	A122	A123	A124	A125	A126	A127	A128	A129	A130	A131	A132	A133	A134	A135	A136	A137	A138	A139	A140	A141	A142	A143	A144	A145	A146	A147	A148	A149	A150	A151	A152	A153	A154	A155	A156	A157	A158	A159	A160	A161	A162	A163	A164	A165	A166	A167	A168	A169	A170	A171	A172	A173	A174	A175	A176	A177	A178	A179	A180	A181	A182	A183	A184	A185	A186	A187	A188	A189	A190	A191	A192	A193	A194	A195	A196	A197	A198	A199	A200	A201	A202	A203	A204	A205	A206	A207	A208	A209	A210	A211	A212	A213	A214	A215	A216	A217	A218	A219	A220	A221	A222	A223	A224	A225	A226	A227	A228	A229	A230	A231	A232	A233	A234	A235	A236	A237	A238	A239	A240	A241	A242	A243	A244	A245	A246	A247	A248	A249	A250	A251	A252	A253	A254	A255	A256	A257	A258	A259	A260	A261	A262	A263	A264	A265	A266	A267	A268	A269	A270	A271	A272	A273	A274	A275	A276	A277	A278	A279	A280	A281	A282	A283	A284	A285	A286	A287	A288	A289	A290	A291	A292	A293	A294	A295	A296	A297	A298	A299	A300	A301	A302	A303	A304	A305	A306	A307	A308	A309	A310	A311	A312	A313	A314	A315	A316	A317	A318	A319	A320	A321	A322	A323	A324	A325	A326	A327	A328	A329	A330	A331	A332	A333	A334	A335	A336	A337	A338	A339	A340	A341	A342	A343	A344	A345	A346	A347	A348	A349	A350	A351	A352	A353	A354	A355	A356	A357	A358	A359	A360	A361	A362	A363	A364	A365	A366	A367	A368	A369	A370	A371	A372	A373	A374	A375	A376	A377	A378	A379	A380	A381	A382	A383	A384	A385	A386	A387	A388	A389	A390	A391	A392	A393	A394	A395	A396	A397	A398	A399	A400	A401	A402	A403	A404	A405	A406	A407	A408	A409	A410	A411	A412	A413	A414	A415	A416	A417	A418	A419	A420	A421	A422	A423	A424	A425	A426	A427	A428	A429	A430	A431	A432	A433	A434	A435	A436	A437	A438	A439	A440	A441	A442	A443	A444	A445	A446	A447	A448	A449	A450	A451	A452	A453	A454	A455	A456	A457	A458	A459	A460	A461	A462	A463	A464	A465	A466	A467	A468	A469	A470	A471	A472	A473	A474	A475	A476	A477	A478	A479	A480	A481	A482	A483	A484	A485	A486	A487	A488	A489	A490	A491	A492	A493	A494	A495	A496	A497	A498	A499	A500	A501	A502	A503	A504	A505	A506	A507	A508	A509	A510	A511	A512	A513	A514	A515	A516	A517	A518	A519	A520	A521	A522	A523	A524	A525	A526	A527	A528	A529	A530	A531	A532	A533	A534	A535	A536	A537	A538	A539	A540	A541	A542	A543	A544	A545	A546	A547	A548	A549	A550	A551	A552	A553	A554	A555	A556	A557	A558	A559	A560	A561	A562	A563	A564	A565	A566	A567	A568	A569	A570	A571	A572	A573	A574	A575	A576	A577	A578	A579	A580	A581	A582	A583	A584	A585	A586	A587	A588	A589	A590	A591	A592	A593	A594	A595	A596	A597	A598	A599	A600	A601	A602	A603	A604	A605	A606	A607	A608	A609	A610	A611	A612	A613	A614	A615	A616	A617	A618	A619	A620	A621	A622	A623	A624	A625	A626	A627	A628	A629	A630	A631	A632	A633	A634	A635	A636	A637	A638	A639	A640	A641	A642	A643	A644	A645	A646	A647	A648	A649	A650	A651	A652	A653	A654	A655	A656	A657	A658	A659	A660	A661	A662	A663	A664	A665	A666	A667	A668	A669	A670	A671	A672	A673	A674	A675	A676	A677	A678	A679	A680	A681	A682	A683	A684	A685	A686	A687	A688	A689	A690	A691	A692	A693	A694	A695	A696	A697	A698	A699	A700	A701	A702	A703	A704	A705	A706	A707	A708	A709	A710	A711	A712	A713	A714	A715	A716	A717	A718	A719	A720	A721	A722	A723	A724	A725	A726	A727	A728	A729	A730	A731	A732	A733	A734	A735	A736	A737	A738	A739	A740	A741	A742	A743	A744	A745	A746	A747	A748	A749	A750	A751	A752	A753	A754	A755	A756	A757	A758	A759	A760	A761	A762	A763	A764	A765	A766	A767	A768	A769	A770	A771	A772	A773	A774	A775	A776	A777	A778	A779	A780	A781	A782	A783	A784	A785	A786	A787	A788	A789	A790	A791	A792	A793	A794	A795	A796	A797	A798	A799	A800	A801	A802	A803	A804	A805	A806	A807	A808	A809	A810	A811	A812	A813	A814	A815	A816	A817	A818	A819	A820	A821	A822	A823	A824	A825	A826	A827	A828	A829	A830	A831	A832	A833	A834	A835	A836	A837	A838	A839	A840	A841	A842	A843	A844	A845	A846	A847	A848	A849	A850	A851	A852	A853	A854	A855	A856	A857	A858	A859	A860	A861	A862	A863	A864	A865	A866	A867	A868	A869	A870	A871	A872	A873	A874	A875	A876	A877	A878	A879	A880	A881	A882	A883	A884	A885	A886	A887	A888	A889	A890	A891	A892	A893	A894	A895	A896	A897	A898	A899	A900	A901	A902	A903	A904	A905	A906	A907	A908	A909	A910	A911	A912	A913	A914	A915	A916	A917	A918	A919	A920	A921	A922	A923	A924	A925	A926	A927	A928	A929	A930	A931	A932	A933	A934	A935	A936	A937	A938	A939	A940	A941	A942	A943	A944	A945	A946	A947	A948	A949	A950	A951	A952	A953	A954	A955	A956	A957	A958	A959	A960	A961	A962	A963	A964	A965	A966	A967	A968	A969	A970	A971	A972	A973	A974	A975	A976	A977	A978	A979	A980	A981	A982	A983	A984	A985	A986	A987	A988	A989	A990	A991	A992	A993	A994	A995	A996	A997	A998	A999	A1000	A1001	A1002	A1003	A1004	A1005	A1006	A1007	A1008	A1009	A1010	A1011	A1012	A1013	A1014	A1015	A1016	A1017	A1018	A1019	A1020	A1021	A1022	A1023	A1024	A1025	A1026	A1027	A1028	A1029	A1030	A1031	A1032	A1033	A1034	A1035	A1036	A1037	A1038	A1039	A1040	A1041	A1042	A1043	A1044	A1045	A1046	A1047	A1048	A1049	A1050	A1051	A1052	A1053	A1054	A1055	A1056	A1057	A1058	A1059	A1060	A1061	A1062	A1063	A1064	A1065	A1066	A1067	A1068	A1069	A1070	A1071	A1072	A1073	A1074	A1075	A1076	A1077	A1078	A1079	A1080	A1081	A1082	A1083	A1084	A1085	A1086	A1087	A1088	A1089	A1090	A1091	A1092	A1093	A1094	A1095	A1096	A1097	A1098	A1099	A1100	A1101	A1102	A1103	A1104	A1105	A1106	A1107	A1108	A1109	A1110	A1111	A1112	A1113	A1114	A1115	A1116	A1117	A1118	A1119	A1120	A1121	A1122	A1123	A1124	A1125	A1126	A1127	A1128	A1129	A1130	A1131	A1132	A1133	A1134	A1135	A1136	A1137	A1138	A1139	A1140	A1141	A1142	A1143	A1144	A1145	A1146	A1147	A1148	A1149	A1150	A1151	A1152	A1153	A1154	A1155	A1156	A1157	A1158	A1159	A1160	A1161	A1162	A1163	A1164	A1165	A1166	A1167	A1168	A1169	A1170	A1171	A1172	A1173	A1174	A1175	A1176	A1177	A1178	A1179	A1180	A1181	A1182	A1183	A1184	A1185	A1186	A1187	A1188	A1189	A1190	A1191	A1192	A1193	A1194	A1195	A1196	A1197	A1198	A1199	A1200	A1201	A1202	A1203	A1204	A1205	A1206	A1207	A1208	A1209	A1210	A1211	A1212	A1213	A1214	A1215	A1216	A1217	A1218	A1219	A1220	A1221	A1222	A1223	A1224	A1225	A1226	A1227	A1228	A1229	A1230	A1231	A1232	A1233	A1234	A1235	A1236	A1237	A1238	A1239	A1240	A1241	A1242	A1243	A1244	A1245	A1246	A1247	A1248	A1249	A1250	A1251	A1252	A1253	A1254	A1255	A1256	A1257	A1258	A1259	A1260	A1261	A1262	A1263	A1264	A1265	A1266	A1267	A1268	A1269	A1270	A1271	A1272	A1273	A1274	A1275	A1276	A1277	A1278	A1279	A1280	A1281	A1282	A1283	A1284	A1285	A1286	A1287	A1288	A1289	A1290	A1291	A1292	A1293	A1294	A1295	A1296	A129

- 1/ For unprogrammed devices, select an appropriate address to acquire the desired output state.
- 2/ For unprogrammed devices (circuit D), apply 12.0 V on pin 8 (A₀) and pin 1 (A₇).
- 3/ For unprogrammed device types 01 and 02 (circuit B), apply 12.0 V on pin 2 (A₆); for unprogrammed device types 04 and 05 (circuit B), apply 12.0 V on pin 2 (A₁).
- 4/ For unprogrammed devices (circuit A), apply 11.0 V on pin 23 (A₈).
- 5/ CE₄ and CE₃ may be "GND" or "2.4 V".
- 6/ The functional test shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. Terminal conditions shall be as follows:
 - a. Inputs: H = 3.0 V, L = 0.0 V.
 - b. Outputs: Output voltage shall be either:
 - (1) H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator, or
 - (2) H \geq 1.0 V and L < 1.0 V when using a high-speed checker single comparator.
- 7/ GALPAT (PROGRAMMED PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PLH1} and t_{PHL1}. Each bit in the pattern is fixed by being programmed with an "H" or "L". The GALPAT tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:

- Step 1. Word 0 is read.
- Step 2. Word 1 is read.
- Step 3. Word 0 is read.
- Step 4. Word 2 is read.
- Step 5. Word 0 is read.
- Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 511 is reached, then increments to the next word and reads back and forth as in Step 1 through Step 6 and shall include all words.
- Step 7. Pass execution time = (n² + n) x cycle time. n = 512.

- 8/ SEQUENTIAL (PROGRAMMED PROM). This program will test all bits in the array for t_{PHL2} and t_{PLH2}. The sequential tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:

- Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
- Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t_{PHL2} and t_{PLH2} are read.
- Step 3. Word 1 is addressed. Same enable sequence as above.
- Step 4. The reading procedure continues until word 511 is reached.
- Step 5. Pass execution time = 512 x cycle time.

- 9/ The outputs are loaded per figure 7.
- 10/ For unprogrammed device types 01 and 02 (circuit C), apply 10.0 V on pin 23 (A₈); 0.5 V on pin 2 (A₆); and 5.0 V on all other address pins. For unprogrammed device type 03 (circuit C), apply 10.0 V on pin 6 (A₈); 0.5 V on pin 22 (A₁); and 5.0 V on all other address pins.
- 11/ For unprogrammed devices (circuit F), apply 12.0 V on pin 3 (A₂) and 0.0 V on pin 4 (A₃).
- 12/ I_{OL} = 8 mA for circuit B devices; I_{OL} = 16 mA for circuit F devices.

- 13/ For unprogrammed device types 01, 02, 04, and 05 (circuit G) select an appropriate address to obtain the desired output state.
- 14/ For programmed device type 02 (circuit G) apply 4.5 V to pin 24; 10.5 V to pin 1; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3 and 2; and 0.0 V to pins 21, 20, 12, and 5.
- 15/ For unprogrammed device type 01 (circuit G) apply 10.5 V to pins 6 and 1; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, 3, and 2; 0.0 V to pins 21, 20, 12, and 5.
- 16/ For programmed device type 02 (circuit G) apply 10.5 V to pin 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3, and 2; 0.0 V to pins 21, 20, 5, and 12.
- 17/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 6 and 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, and 2; 2.0 V to pin 3; 0.0 V to pins 21, 20, 12, and 5.
- 18/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 1 and 6; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, 3 and 2; 0.0 V to pins 5, 12, 20, and 21.
- 19/ For programmed device type 04 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.
- 20/ For programmed device type 05 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.
- 21/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 17 and 3; 4.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.
- 22/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 3 and 17; 5.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.
- 23/ At the manufacturer's option, this may be prepared with $V_{IH} = 5.5$ and test limits of 50 μA maximum.
- 24/ At the manufacturer's option, this may be performed with $V_{IO} = 0.5$ V and test limits of -1 μA minimum to -250 μA maximum.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Subgroup 2 shall be omitted for devices in package Z.
- c. For moisture resistance and salt atmosphere of subgroups 3 and 5, omit initial conditioning for devices in package Z.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as specified herein.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

TABLE IVA. Programming characteristics for circuit A.

Characteristic	Symbol	Limits 1/			Unit
		Min	Recommended	Max	
Address input voltage 2/	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
V_{CC} required during programming	V_{PH}	12.0	12.0	12.5	V
	V_{PL}	4.5	4.5	5.5	V
Programming input low current	I_{ILP}	---	-300	-600	μ A
Programming voltage transition time	t_{TLH}	1	1	10	μ s
	t_{THL}	1	1	10	μ s
Programming delay	t_D	10	10	100	μ s
Programming pulse width	t_p	90	100	110	μ s
Programming duty cycle	D.C.	---	50	90	%
Output voltage Enable 3/ Disable 4/	V_{OPE}	10.5	10.5	11.0	V
	V_{OPD}	4.5	5.0	5.5	V
Output voltage enable current	I_{OPE}	---	---	10	mA

1/ $T_A = 25^\circ\text{C}$.

2/ Address and chip enable shall not be left open for V_{IH} .

3/ V_{OPE} supply shall be capable of sourcing 10 mA.

4/ Disable condition can be met with output open circuit.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross referenced in 6.6 herein with the manufacturer's symbol or FSCM number.

4.7 Programming procedures for circuit A. The waveforms on figure 8a, the programming characteristics of table IVA, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- c. Disable the chip by applying V_{IH} to the \overline{CE}_1 and \overline{CE}_2 inputs and V_{IL} to the CE_3 and CE_4 inputs. The CE inputs are TTL compatible.
- d. Disable the programming circuitry by applying V_{OPD} to the outputs of the PROM.
- e. Raise V_{CC} to V_{PH} as specified on the waveforms on figure 8a.
- f. After a delay of t_D , apply only one V_{OPE} pulse with duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{PH} level by applying V_{OPE} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 8a.
- h. Repeat 4.7b through 4.7g for all other bits to be programmed.
- i. Lower V_{CC} to 4.5 volts following a delay of t_D from the last programming pulse applied to an output.
- j. Enable the chip by applying V_{IL} to the \overline{CE}_1 and \overline{CE}_2 inputs and V_{IH} to the CE_3 and CE_4 inputs and verify the program.
- k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.7b through 4.7i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.8 Programming procedures for circuit B. The waveforms on figure 8b, the programming characteristics of table IVB, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Raise V_{CC} to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the \overline{CE}_1 and \overline{CE}_2 and V_{IL} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IH} to the CE input (device types 04 and 05). The CE input is TTL compatible.
- e. Apply the V_{PP} pulse to the programming pin \overline{CE}_2 (device types 01 and 02) or CE (device types 04 and 05). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by t_{D1} and leave after the output pin's programming pulse by t_{D2} (see figure 8b).
- f. Apply only one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

TABLE IVB. Programming characteristics for circuit B.

Characteristic	Symbol	Conditions	Limits 1/			Unit
			Min	Recom- mended	Max	
V _{CC} required during programming	V _{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t _{TLH}		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V _{pp}		32.5	33	33.5	V
Output programming voltage	V _{OUT}		25.5	26	26.5	V
Programming pin pulse width (CE ₂) 2/	t _{pp}	Chip disabled, V _{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t _p	Chip disabled, V _{CC} = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I _L	V _{pp} = 33 V, V _{OUT} = 26 V, V _{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T _{D1}	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T _{D2}	Measured at 10% levels	100			ns
Output current during verification	I _{OLV1}	Chip enabled, V _{CC} = 4.0 V	11	12	13	mA
	I _{OLV2}	Chip enabled, V _{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V _{IH}		2.4	5.0	5.5	V
	V _{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t _p /t _c			25	%

1/ T_A = 25°C.2/ CE₁ is the programming pin for device types 04 and 05.

- g. Other bits in the same word may be programmed sequentially by applying V_{DD} pulses to each output to be programmed.
- h. Repeat 4.8c through 4.8g for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the \overline{CE}_1 and \overline{CE}_2 and V_{IH} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IL} to the \overline{CE} inputs (device types 04 and 05) and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.0$ V and 0.2 mA at $V_{CC} = 7.0$ V at $T_A = 25^\circ\text{C}$.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.8c through 4.8i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.9 Programming procedures for circuit C. The waveforms on figure 8c, the programming characteristics of table IVc, and the following procedures shall apply:

4.9.1 Device types 01 and 02.

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all device outputs with a 10-k Ω resistor to V_{CC} . Apply $\overline{CE}_1 = V_{IH}$, $\overline{CE}_2 = V_{IL}$, $CE_3 = V_{IH}$, and $CE_4 = V_{IH}$.
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a t_D delay (10 μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.
- e. After a t_D delay (10 μs), pulse CE_1 input to logic "0" for a duration of t_p .
- f. After a t_D delay (10 μs), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 8c.
- h. Repeat 4.9.1c through 4.9.1g for all other bits to be programmed.
- i. To verify programming after a t_D (10 μs) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both \overline{CE}_1 and \overline{CE}_2 inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.9.1c through 4.9.1i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.9.2 Device type 03.

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all device outputs with a 10-k Ω resistor to V_{CC} . Apply $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IH}$, and $\text{strobe} = V_{IH}$.
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .

TABLE IVC. Programming characteristics for circuit C.

Characteristic	Symbol	Conditions	Limits			Unit
			Min	Recom- mended	Max	
Programming voltage to V_{CC}	V_{CCP1} 1/	$I_{CCP} = 375 \pm 75$ mA, transient or steady state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_s 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	$V_{CCP} = 8.75 \pm .25$ V	300		450	mA
Input voltage, high level "1"	V_{IH}		2.4		5.5	V
Input voltage, low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	$V_{IH} = 5.5$ V			50	μ A
Input current	I_{IL}	$V_{IL} = 0.4$ V			-500	μ A
Output programming voltage	V_{OUT} 3/	$I_{OUT} = 200 \pm 20$ mA, transient or steady state	16	17	18	V
Output programming current	I_{OUT}	$V_{OUT} = 17 \pm 1$ V	180	200	220	mA
Programming voltage transition time	t_{TLH} 1		10		50	μ s
\overline{CE} programming pulse width	t_p		300	400	500	μ s
Pulse sequence delay	t_D		10			μ s

- 1/ Bypass V_{CC} to GND with a 0.01μ F capacitor to reduce voltage spikes.
- 2/ V_s is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
- 3/ Care should be taken to insure the 17 ± 1 output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

- d. After a t_D delay (10 μ s), apply to FE₁ (pin 13) a voltage source of +5.0 \pm 0.5 V, with 10 mA sourcing current capability.
- e. After a t_D delay (10 μ s), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.
- f. After a t_D delay (10 μ s), raise FE₂ (pin 11) from GND to +5.0 \pm 0.5 V for 1 ms, and return to GND.
- g. After a t_D delay (10 μ s), remove the V_{OUT} pulse from the programmed output.
- h. Programming a fuse will cause the output to go to a high level logic in the verify mode. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay to t_D between pulses as shown on figure 8c.
- i. Repeat 4.9.2c through 4.9.2h for all other bits to be programmed.
- j. To verify programming after a t_D (10 μ s) delay, return FE₁ to GND. Raise V_{CC} to V_{CCH}. The programmed output should remain in the high state. Again lower V_{CC} to V_{CCL} and verify that the programmed output remains in the high state.
- k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.9.2c through 4.9.2i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.10 Programming procedures for circuit D. The waveforms on figure 8d, the programming characteristics of table IVD, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- c. Disable the chip by applying V_{IH} to the \overline{CE}_1 and \overline{CE}_2 inputs and V_{IL} to the CE₃ and CE₄ inputs. The chip enable input is TTL compatible.
- d. After a delay of t_D , apply only one V_{OUT} pulse with a duration of t_p to the output selected for programming. The other outputs may be left open or tied to V_{IH}. The outputs shall be programmed one output at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- e. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- f. Repeat 4.10b through 4.10e for all other bits to be programmed.
- g. Enable the chip by applying V_{IL} to the \overline{CE}_1 and \overline{CE}_2 inputs and V_{IH} to the CE₃ and CE₄ inputs and verify the program.
- h. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.10b through 4.10g one time only. Bits which fail to program the second time shall be considered programming rejects.

TABLE IVD. Programming characteristics for circuit D.

Characteristic	Symbol	Conditions <u>1/</u>	Limits			Unit
			Min	Recom- mended	Max	
V _{CC} required during programming	V _{CCP}		4.75	5.0	5.25	V
Verification V _{CC} read	V _{CCL}	Programming read verify	4.2	4.4	5.0	V
Input voltage, high level "1"	V _{IH}	Do not leave inputs open	2.4	5.0	5.0	V
Input voltage, low level "0"	V _{IL}	Do not leave inputs open	0	0	0.4	V
Output programming voltage	V _{OUT}	Applied to output to be programmed	20	20.5	21	V
Output programming current	I _{OUT}	If pulse generator is used, set current limit to the maximum value			100	mA
Programming voltage transition time	t _{T LH}		0.5	1.0	3.0	μs
Programming pulse width	t _p		50	100	180	μs
Programming duty cycle	D.C.	Maximum duty cycle to maintain T _A < 85°C		20	20	%
Required delay between disabling memory output and application of output programming pulse	t _D		30			ns

1/ T_A = 25°C (recommended); T_A = 85°C (maximum).

4.11 Programming procedures for circuit F. The waveforms on figure 8b, the programming characteristics of table IVE, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Raise V_{CC} to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the \overline{CE} inputs and V_{IL} to the CE inputs. The chip enable inputs are TTL compatible.
- e. Apply the V_{pp} pulse to the programming pin \overline{CE}_2 . In order to insure that the output transistor is off before increasing voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the programming pin's programming pulse by T_{D2} (see figure 8b).
- f. Apply only one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- h. Repeat 4.11c through 4.11g for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the \overline{CE} inputs and V_{IH} to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.0$ V and 0.2 mA at $V_{CC} = 7.0$ V at $T_A = 25^\circ\text{C}$.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.11c through 4.11i one time only. Bits which fail to program the second time shall be considered programming rejects.

TABLE IVE. Programming characteristics for circuit F.

Characteristic	Symbol	Conditions	Limits			Unit
			Min	Recom- mended	Max	
V _{CC} required during programming	V _{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t _{TLH}		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V _{pp}		32.5	33	33.5	V
Output programming voltage	V _{OUT}		25.5	26	26.5	V
Programming pin pulse width (CE)	t _{pp}	Chip disabled, V _{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t _p	Chip disabled, V _{CC} = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I _L	V _{pp} = 33 V, V _{OUT} = 26 V, V _{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T _{D1}	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T _{D2}	Measured at 10% levels	100			ns
Output current during verification	I _{OLV1}	Chip enabled, V _{CC} = 4.0 V	11	12	13	mA
	I _{OLV2}	Chip enabled, V _{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V _{IH}		2.4	5.0	5.5	V
	V _{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t _p /t _c			25	%

∓/ T_A = 25°C.

4.12 Programming procedure for circuit G. The programming characteristics on table IV G and the following procedures shall be used for programming:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 8G and the programming characteristics of table IVG shall apply to these procedures.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase V_{CC} from nominal to V_{CCP} (10.5 ± 0.5 V) with a slew rate limit of I_{PR} (1.0 to 10.0 v/ μ s). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.
- d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ± 0.5 V). Limit the slew rate to I_{PR} (1.0 to 10.0 v/ μ s). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP} , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kilohms minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip Enable(s) to a low level. This is done with a pulse PWE for 10 μ s. The 10 μ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 (± 0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.
- g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of Step f. is to be performed at a V_{CC} level of 4.0 volts (± 0.2 V). V_{OH} , during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.
- h. Repeat steps 4.12b thru 4.12f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.
- i. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.12b through 4.12f, one time only. Bits which fail to program the second time shall be considered programming rejects.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE IVG. Programming characteristics for circuit G.

Characteristic	Symbol	Conditions	Limits 1/			Unit
			Min	Recom- mended	Max	
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	$V_{CC} = 11$ V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	$V_{OUT} = 11$ V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/ μ s
Programming pulse width (Enabled)	PWE		9	10	11	μ s
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	t_1		100			ns
V_{CCP} set-up time	t_2	2/	5			μ s
V_{CCP} hold time	t_5		100			ns
V_{OP} set-up time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ $T_A = 25^\circ\text{C}$.

2/ V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP} .

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- i. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal).
I _{IN}	- - - - -	Current flowing into an input terminal.
V _{IC}	- - - - -	Input clamp voltage.
V _{IN}	- - - - -	Voltage level at an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

MIL-M-38510/208C

<u>Military device type</u>	<u>Generic-industry type/manufacturer</u>	<u>Circuit designator</u>	<u>Fusible link</u>	<u>Symbol/FSCM no.</u>
01	7640/Harris Corporation	A	NiCr	CDW0/34371
01	5340-1/Monolithic Memories, Inc.	B	NiCr	CECD/50364
01	82S140/Signetics Corporation	C	NiCr	CDKB/18324
01	93438/Fairchild Corporation	D	NiCr	CFJ/07263
01	54S475/National Semiconductor	G	TiW	CCXP/27014
02	7641/Harris Corporation	A	NiCr	---
02	5341-1/Monolithic Memories, Inc.	B	NiCr	---
02	82S141/Signetics Corporation	C	NiCr	---
02	93448/Fairchild Corporation	D	NiCr	---
02	54S474/National Semiconductor	G	TiW	---
03	82S115/Signetics Corporation	C	NiCr	---
04	5348-1/Monolithic Memories, Inc.	B	NiCr	---
04	54S473/National Semiconductor	G	TiW	---
05	5349-1/Monolithic Memories, Inc.	B	NiCr	---
05	29621/Raytheon Company	F	NiCr	CRP/07933
05	54S472/National Semiconductor	G	TiW	---

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17
 (Project 5962-0528)

Review activities:
 Army - AR, MI
 Navy - OS, SH
 Air Force - 11, 19, 85, 99
 DLA - ES

User activities:
 Army - SM
 Navy - AS, CG, MC

Agent:
 DLA - ES