

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 8192-BIT SCHOTTKY,
 BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome (NiCr) resistors, zapped vertical emitter, tungsten (W), titanium-tungsten (TiW), or platinum silicide as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the part number. A special test requirement is included in this specification to screen against devices which may contain excess moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Circuit</u>	<u>Access times (ns)</u>
01	2048 word/4 bits per word PROM with uncommitted collector	125
02, 08, 10	2048 word/4 bits per word PROM with active pullup and a third high-impedance state output	125, 90, 55
03	1024 word/8 bits per word PROM with uncommitted collector	90
04, 09	1024 word/8 bits per word PROM with active pullup and a third high-impedance state output	90, 55
05	1024 word/8 bits per word PROM with active pullup and a third high-impedance state output	90
06	1024 word/8 bits per word PROM with uncommitted collector	90

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
J	D-3 (24-lead, 1/2" x 1 1/4") dual-in-line package
K	F-6 (24-lead, 3/8" x 5/3") flat package
V	O-6 (18-lead, 1/4" x 15/15") dual-in-line package
X	See figure 1 (18-lead, 3/8" x 3/8") flat package

1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.5 V to +7.0 V
Input voltage range	- - - - -	-1.5 V at -10 mA to +5.5 V
Storage temperature range	- - - - -	-65°C to +150°C

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}) 1/- - - - -	2/
Output voltage - - - - -	-0.5 V to +V _{CC}
Output sink current- - - - -	100 mA
Maximum power dissipation (P_D) 3/:	
Device types 01, 02, 08, and 10- - - - -	950 mW
Device types 03, 04, 05, 06, and 09- - - - -	1.1 W
Maximum junction temperature (T_J)- - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 V minimum to 5.5 V maximum
Minimum high-level input voltage (V_{IH}) - - - - -	2.0 V
Maximum low-level input voltage (V_{IL})- - - - -	0.8 V
Normalized fanout (each output):	
Device types 01, 02, 08, and 10- - - - -	12 mA 4/
Device types 03, 04, 05, 06, and 09- - - - -	8 mA 4/
Case operating temperature range (T_C)- - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

- 1/ Heat sinking is recommended to reduce the junction temperature.
- 2/ Case outlines J and V - - - - - 40°C/W maximum
Case outline K- - - - - 60°C/W maximum
Case outline X- - - - - 35°C/W maximum
- 3/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).
- 4/ 16 mA for circuits B, D, and F devices.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth tables.

3.2.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in group A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Functional block diagrams. The functional block diagrams shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics of table I apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be as indicated by the subgroups shown in table II and, where applicable, by the altered item drawing. The subgroup tests shall be as specified in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Interim and final electrical tests shall be as specified in table II; the interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- b. Burn-in test (method 1015 of MIL-STD-883), using the circuits shown on figure 5 or equivalent.
 - (1) Test condition D or E.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u>	Device	Limits		
				Min	Max	
High-level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$ $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	02,04, 05,08, 09,10	2.4		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$ <u>2/</u> $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	01,02, 08,10		0.5	V
		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$ <u>2/</u>	03,04, 05,06, 09			
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -10 \text{ mA}$ $T_C = +25^\circ\text{C}$	A11		-1.5	V
Maximum collector cut-off current	I_{CEX}	$V_{CC} = 5.5 \text{ V}$, $V_O = 5.2 \text{ V}$	01,03, 06		100	μA
High-impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5 \text{ V}$, $V_O = 5.2 \text{ V}$	02,04, 05,08, 09,10		100	μA
High-impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.5 \text{ V}$	02,04, 05,08, 09,10		-100	μA
High-level input current	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	A11		50	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 4.5 \text{ V}$, special programming pin	03,04, 06,09		100	μA
Low-level input current	I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$	A11	-1.0	-250	μA
Short-circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.0 \text{ V}$ <u>3/</u> $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	02,04, 05,08, 09,10	-15	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$, outputs = open	01,02		170	mA
			03,04, 05,06, 08,09, 10		185	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u>	Device type	Limits		Unit
				Min	Max	
Propagation delay time, high-to-low level logic, address to output	t _{PHL1}	V _{CC} = 4.5 V and 5.5 V, C _L = 30 pF (see figure 8)	08		90	ns
			01,02		125	
			03,04,		90	
			05,06			
			09,10		55	
Propagation delay time, low-to-high level logic, address to output	t _{PLH1}		08		90	ns
			01,02		125	
			03,04,		90	
			05,06			
			09,10		55	
Propagation delay time, high-to-low level logic, enable to output	t _{PHL2}		08		50	ns
			01,02		60	
			03,04,		50	
			05,06			
			09,10		30	
Propagation delay time, low-to-high level logic, enable to output	t _{PLH2}		08		50	ns
			01,02		60	
			03,04,		50	
			05,06			
			09,10		30	

1/ Complete terminal conditions shall be as specified in table III.

2/ I_{OL} = 16 mA for circuits B, D, and F devices.

3/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	<u>1/</u>	<u>2/</u> <u>3/</u>
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical tests (method 5004) for unprogrammed devices	1*,2,3,7*,8	1*,2,3,7*,8
Final electrical tests (method 5004) for programmed devices	1*,2,3,7*,8,9,10,11	1*,2,3,7*,8,9
Group A electrical tests (method 5005)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11
Group B electrical tests (method 5005, subgroup 5)	1,2,3,7,8,9,10,11	N/A
Group C end-point electrical tests (method 5005)	N/A	1,2,3,7,8
Group D end-point electrical tests (method 5005)	1,2,3,7,8	1,2,3,7,8

1/ * indicates PDA applies to subgroups 1 and 7 (see 4.2c).

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

- d. The freeze-out test shall be conducted as a 100-percent screen on all class S devices having nichrome or platinum silicide as the fusing link. Within no more than 24 hours after completion of burn-in and prior to the final electrical tests, all devices having nichrome or platinum silicide as the fusing link (see 3.7.1 and 3.7.2) shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the +125°C burn-in exposure, devices shall be conditioned at +125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the +25°C final electrical tests shall be completed within 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:
- Step 1. Connect devices in the electrical configuration of figure 7 or in the burn-in configuration of figure 5 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - Step 2. Reduce device temperature to $T_C = -10^\circ\text{C} \pm 2^\circ\text{C}$ with bias cycled and maintain at that temperature for a minimum of 5 hours.
 - Step 3. With the cycled bias maintained, allow T_C to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_C shall not exceed +35°C during this period.
 - Step 4. Remove bias and subject all devices to subgroup 1 final electrical tests to establish continuity of the fusible links and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.
- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 through 11 shall be attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically (i.e., same die, process, and package) to other device types on this specification, then the other device types may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510, and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy the programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowed.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 5 tests.
- b. Steady-state life tests for class S devices shall be in accordance with subgroup 5, table IIa of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 5 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life tests (method 1005 of MIL-STD-883, test condition D or E), using the circuits shown on figure 5 or equivalent.
 - (1) $T_A = +125^{\circ}\text{C}$ minimum.
 - (2) Test duration = 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

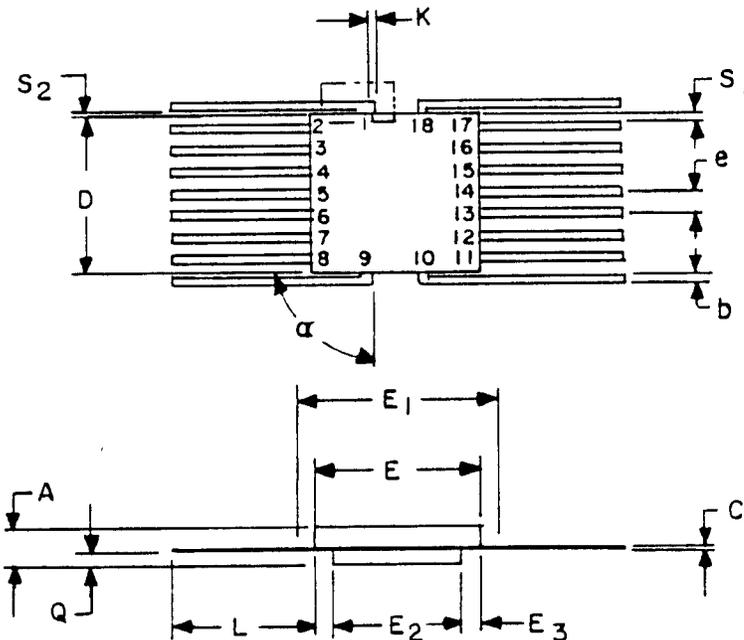
4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedures identification. The programming procedures to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross-referenced in 6.6 herein with the manufacturer's symbol or CAGE number.

Text continues on page 48.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.045	.085	1.14	2.16	
b	.015	.020	.38	.51	5
C	.003	.006	.08	.15	5
D	.340	.380	8.64	9.65	
E	.340	.380	8.64	9.65	
E ₁		.400		10.37	3
E ₂	.260	.290	6.60	7.37	
E ₃	.025		.63		
e	.050 BSC		1.27 BSC		4,6
K	.008	.015	.20	.38	9
L	.250	.330	6.35	8.38	
Q	.010	.040	.25	1.02	2
S ₁	.005		.13		7,8
S ₂	.004		.10		10
α	30°	90°	30°	90°	



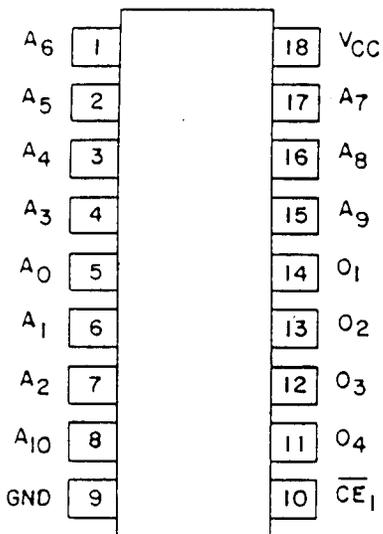
NOTES:

1. Index area: A tab (dim. K) is used to identify pin one.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within ± 0.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 18.
5. All leads-increase may limit by .003 (0.08 mm) measured at the center of the flat, when finish A is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads no. 2, 8, 11, and 17).
8. Dimension S₁ may be .000 (0.00 mm) if leads are brazed to the metallized ceramic body (see appendix C of MIL-M-38510).
9. Optional, see note 1. If pin one identification mark is used in addition to this tab the minimum limit of dimension K does not apply.
10. Applies to leads no. 1, 9, 10, and 18.

FIGURE 1. Case outline X (18-lead, .375 inch X .375 inch).

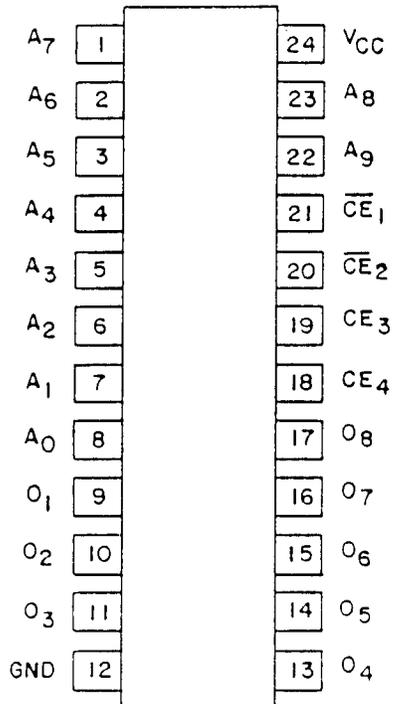
Device types 01, 02, 08 and 10

Case V



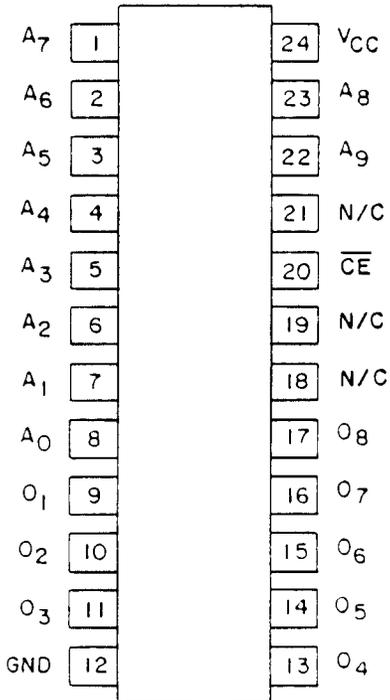
Device types 03, 04 and 09

Cases J and K



Device types 05 and 06

Cases J and K



Device types 01, 02 and 08

Case X

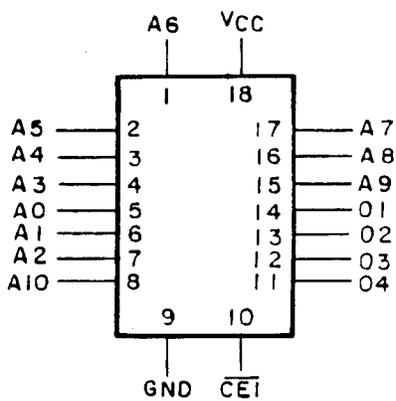


FIGURE 2. Terminal connections.

Device types 01, 02, 08 and 10 (see notes 1, 2 and 3)

Word no.	Enable	Address											Data			
	\overline{CE}_1	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄
NA	L	X	X	X	X	X	X	X	X	X	X	X	See note 5			
NA	H	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC

Device types 03, 04 and 09 (see notes 1, 2, 3 and 4)

Word no.	Enable				Address										Data								
	\overline{CE}_1	\overline{CE}_2	CE ₃	CE ₄	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	
NA	L	L	H	H	X	X	X	X	X	X	X	X	X	X	See note 5								
NA	L	H	H	H	X	X	X	X	X	X	X	X	X	X	OC	OC							
NA	H	L	H	H	X	X	X	X	X	X	X	X	X	X	OC	OC							
NA	H	H	L	H	X	X	X	X	X	X	X	X	X	X	OC	OC							
NA	H	H	L	L	X	X	X	X	X	X	X	X	X	X	OC	OC							

Device types 05 and 06 (see notes 1, 2 and 3)

Word no.	Enable	Address										Data							
	\overline{CE}	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈
NA	L	X	X	X	X	X	X	X	X	X	X	See note 5							
NA	H	X	X	X	X	X	X	X	X	X	X	OC							

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with both enable inputs at low level.
5. The outputs for an unprogrammed device shall be high for circuits, A, B (device types 03 and 04), and F, and shall be low for circuits B (device types 01, 02, and 08), C, D, E and G.

FIGURE 3. Truth tables (unprogrammed).

Device types 01, 02 and 08 (Circuit B)

Device types 01 and 02 (Circuit A)

Device type 02 (Circuit F)

Device types 03 and 04 (Circuit E)

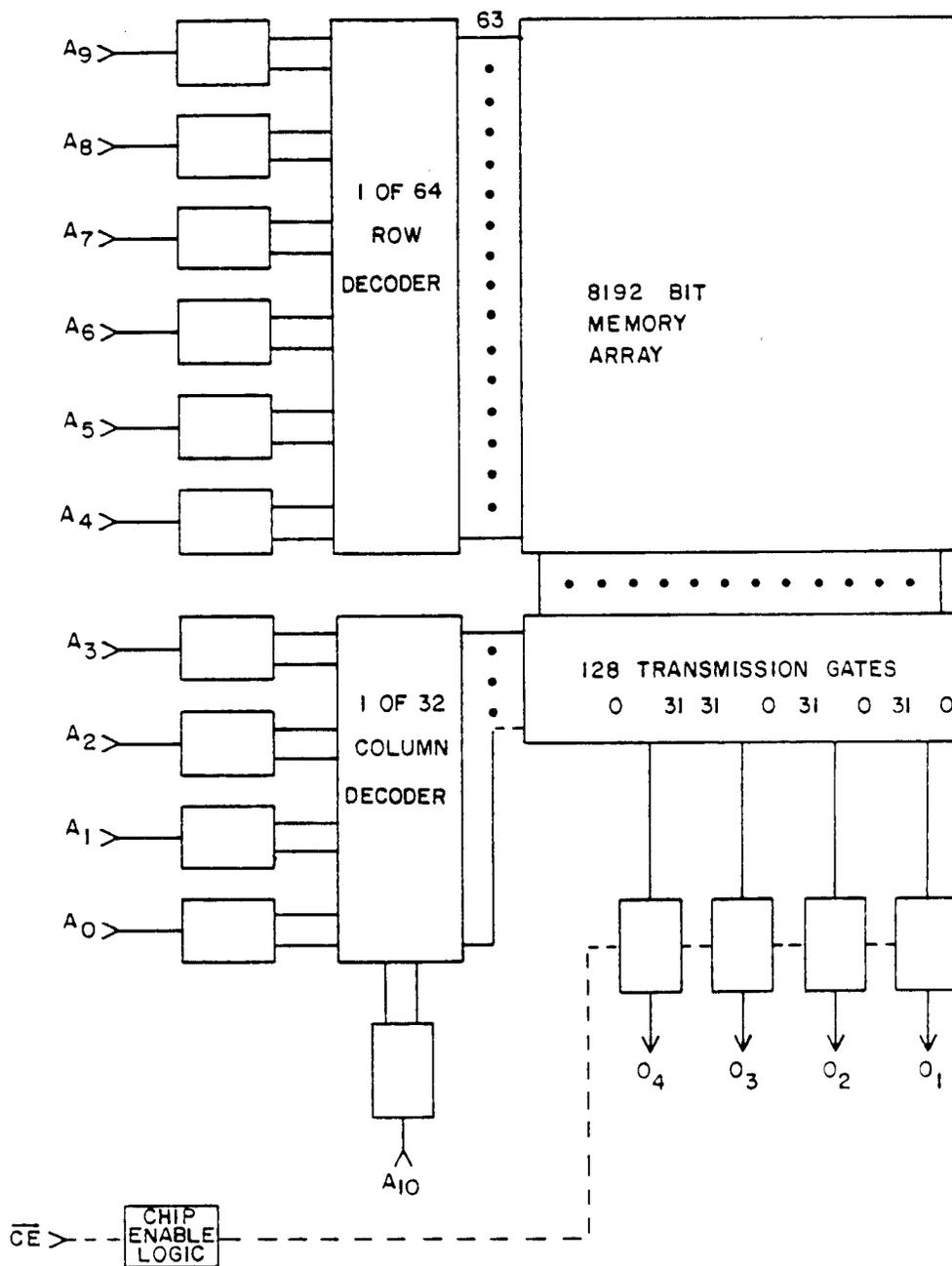


FIGURE 4. Functional block diagrams.

Device types 01, 02 and 10

Circuit C

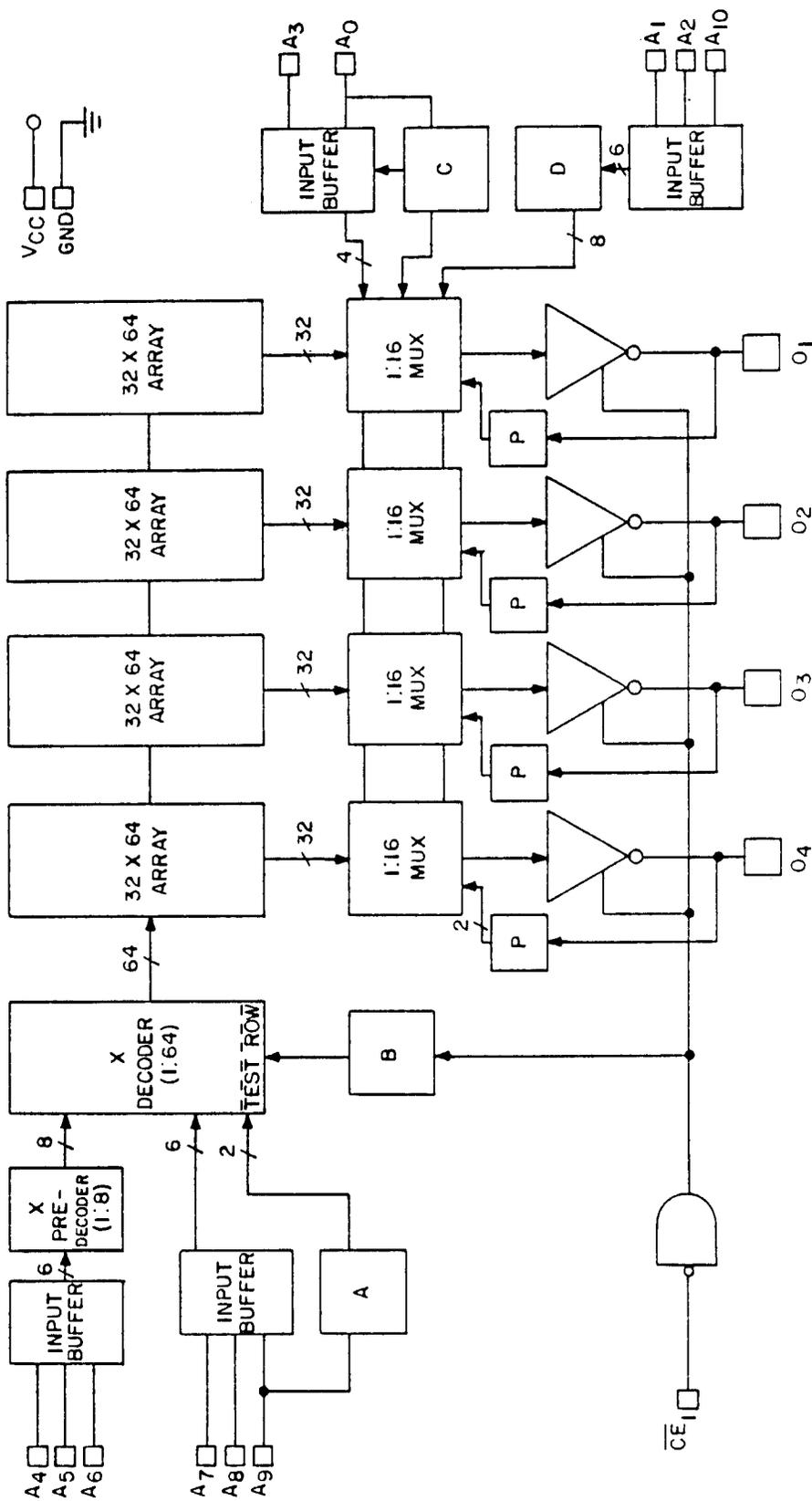


FIGURE 4. Functional block diagrams - Continued.

Device types 03 and 04

Circuit A

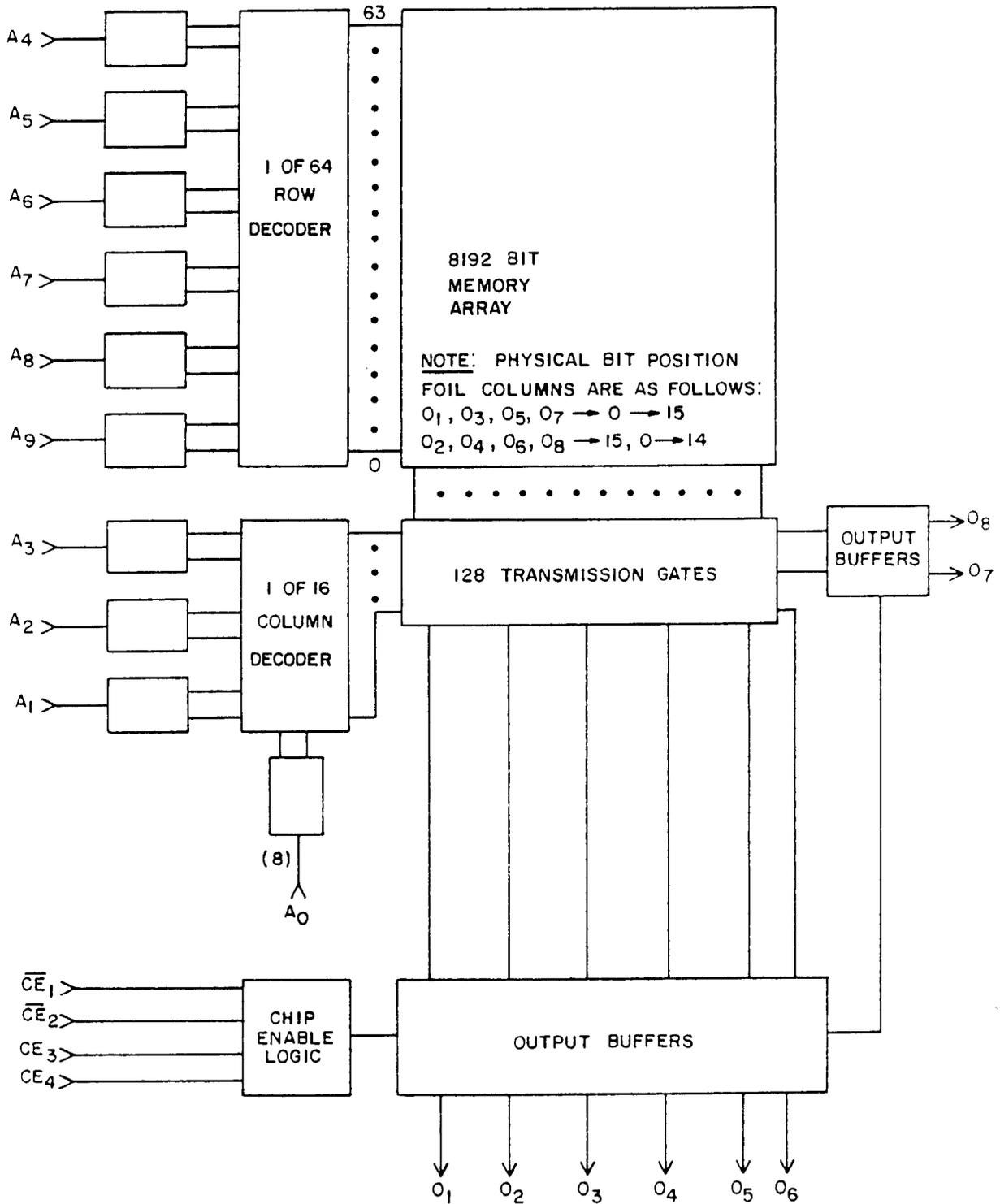
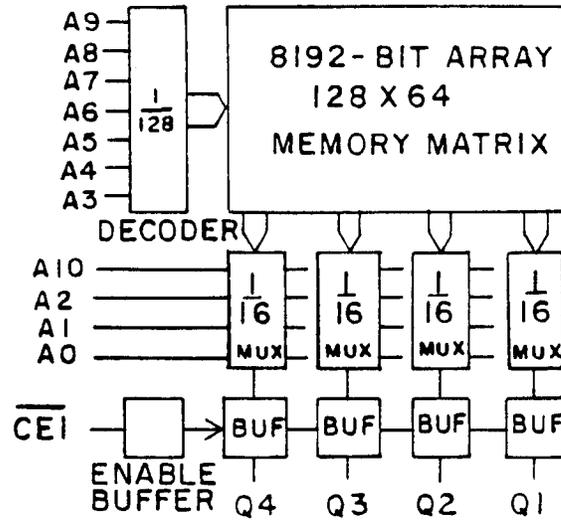


FIGURE 4. Functional block diagrams - Continued.

Device types 01 and 02

Circuit G



Device types 03 and 04

Circuit G

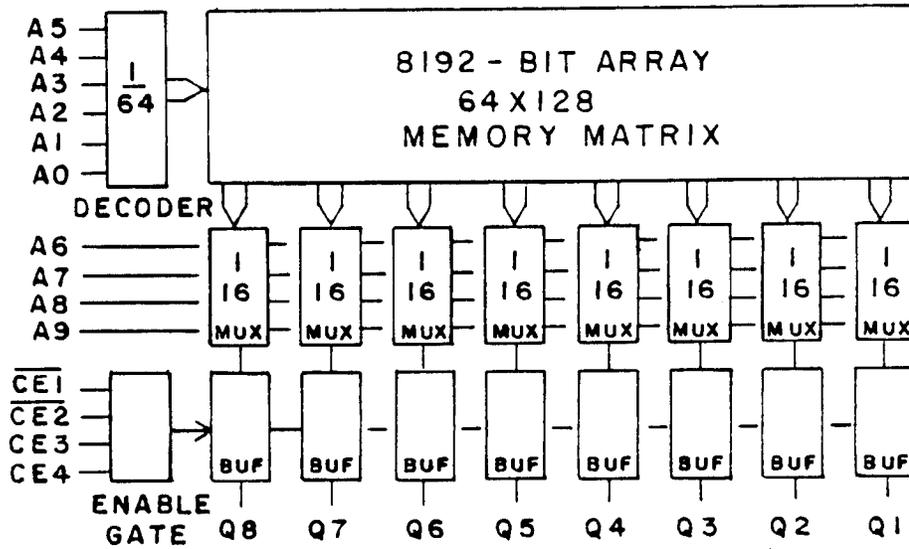


FIGURE 4. Functional block diagrams - Continued.

Device type 04

Circuit F

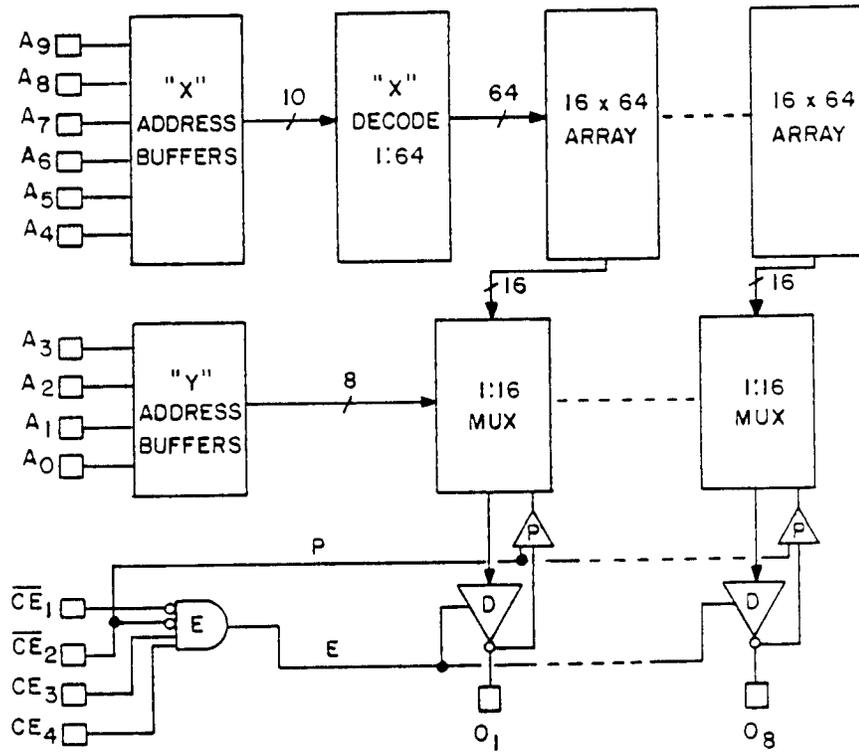


FIGURE 4. Functional block diagrams - Continued.

Device types 03, 04, 05, and 09

Circuit C

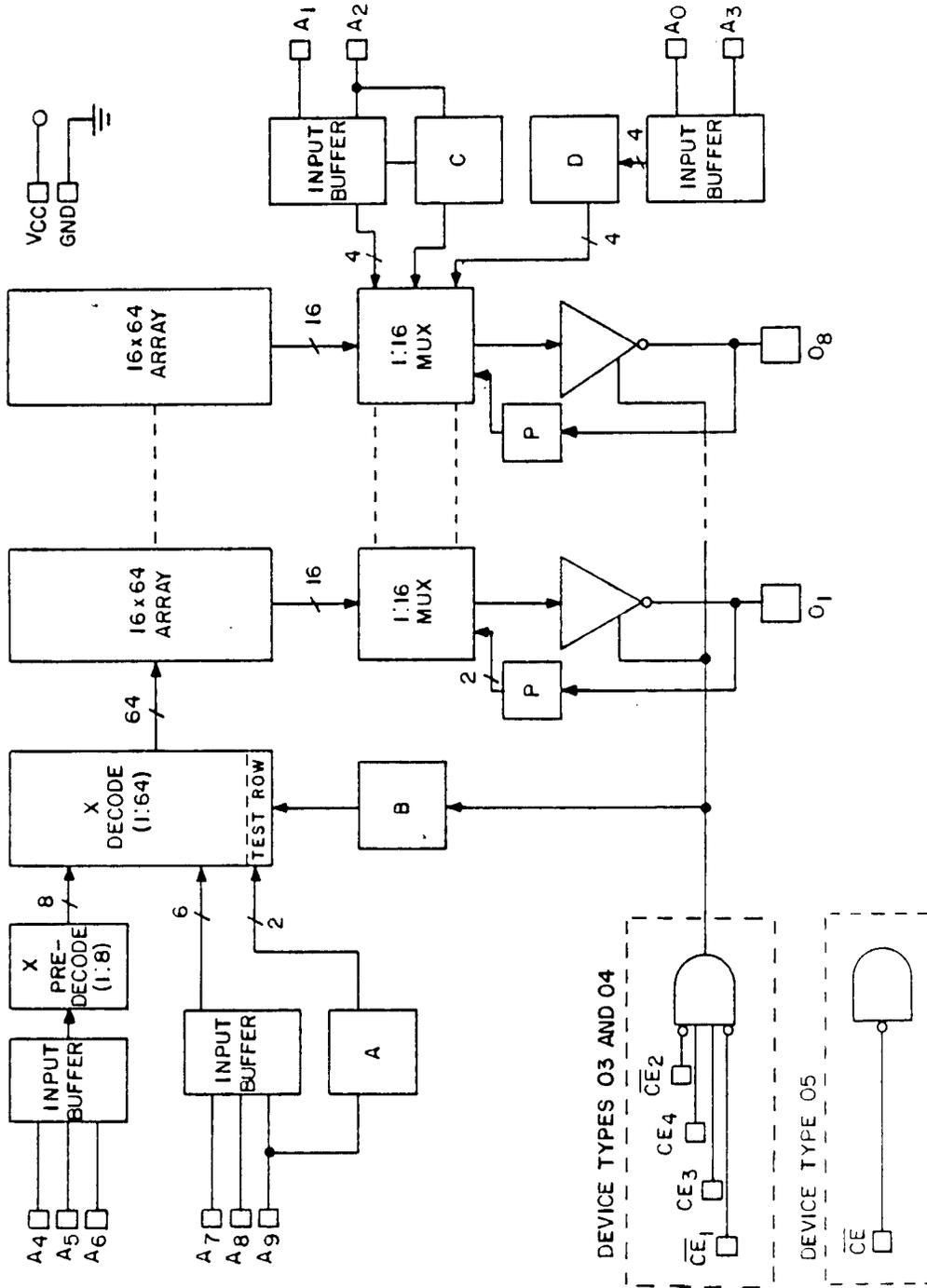


FIGURE 4. Functional block diagrams - Continued.

Device types 03, 04, 05, 06 and 09

Circuits B and D

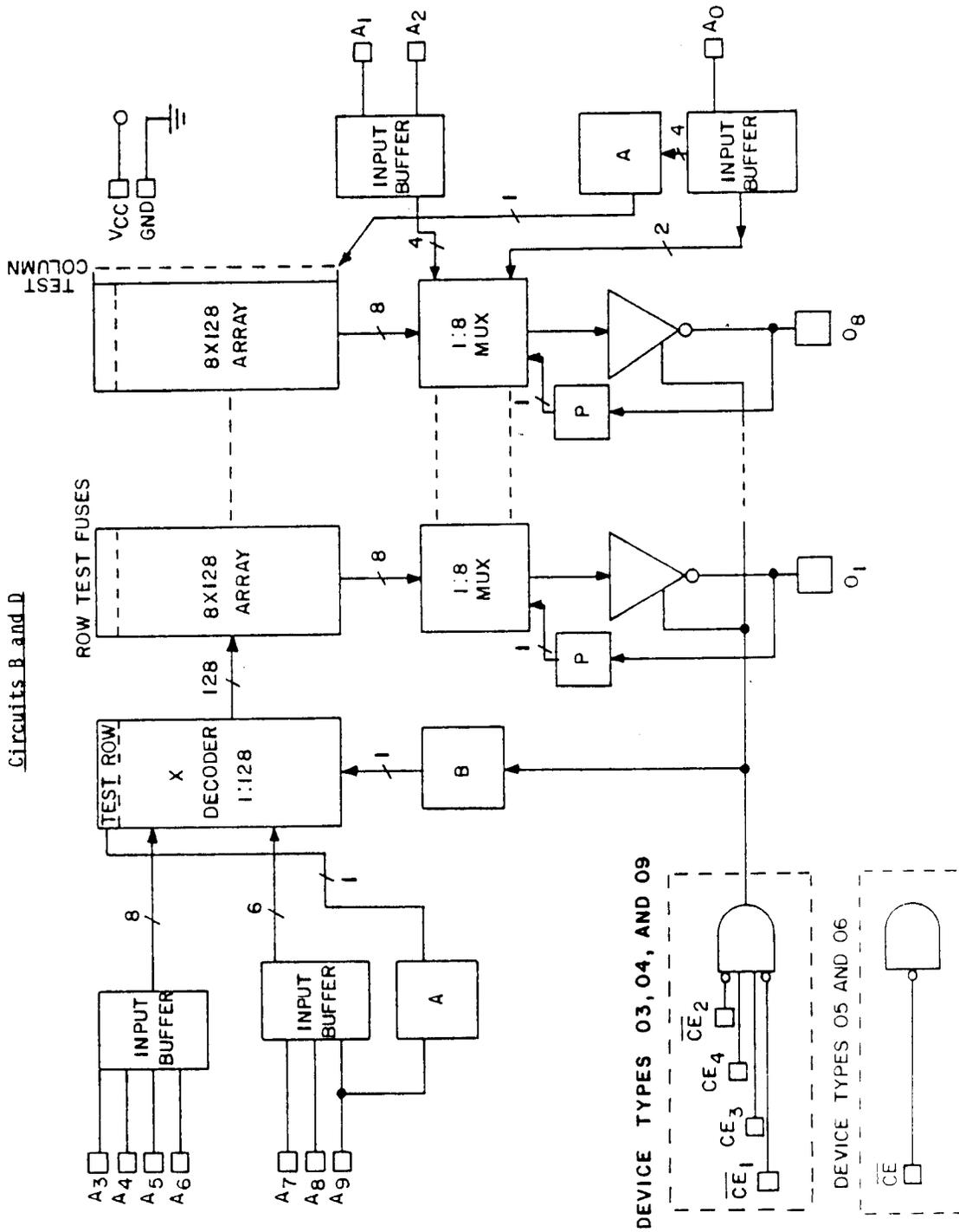
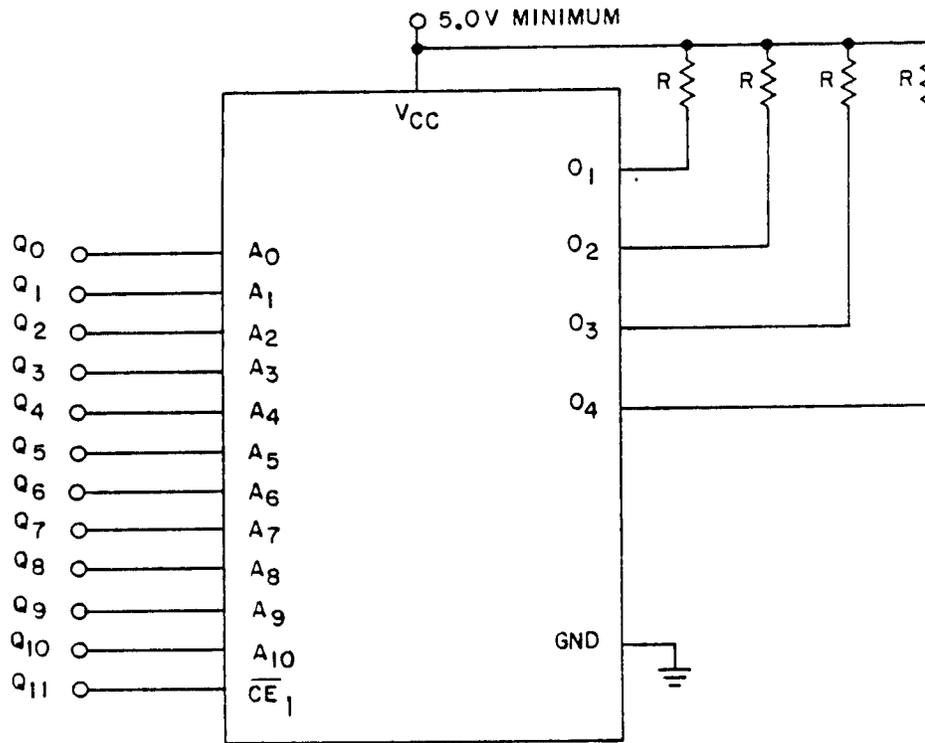


FIGURE 4. Functional block diagrams - Continued.

Device types 01, 02, 08 and 10



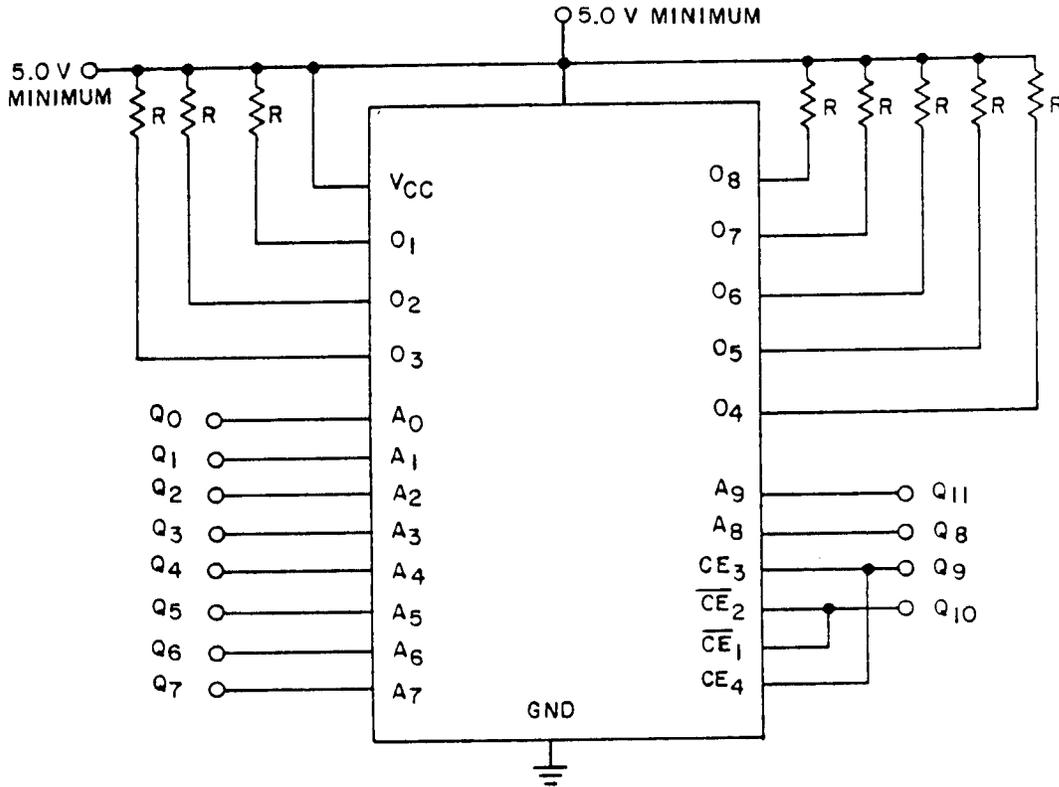
NOTES:

1. $R = 360\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5 \text{ V min to } 0.8 \text{ V max}$; $V_{IH} = 2.0 \text{ V min to } 5.5 \text{ V max}$; 50% $\pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency $\pm 50\%$
Q0	F0 = 100 kHz min
Q1	F1 = 1/2 F0
Q2	F2 = 1/2 F1
Q3	F3 = 1/2 F2
Q4	F4 = 1/2 F3
Q5	F5 = 1/2 F4
Q6	F6 = 1/2 F5
Q7	F7 = 1/2 F6
Q8	F8 = 1/2 F7
Q9	F9 = 1/2 F8
Q10	F10 = 1/2 F9
Q11	F11 = 1/2 F10

FIGURE 5. Burn-in and steady-state life test circuit.

Device types 03, 04 and 09



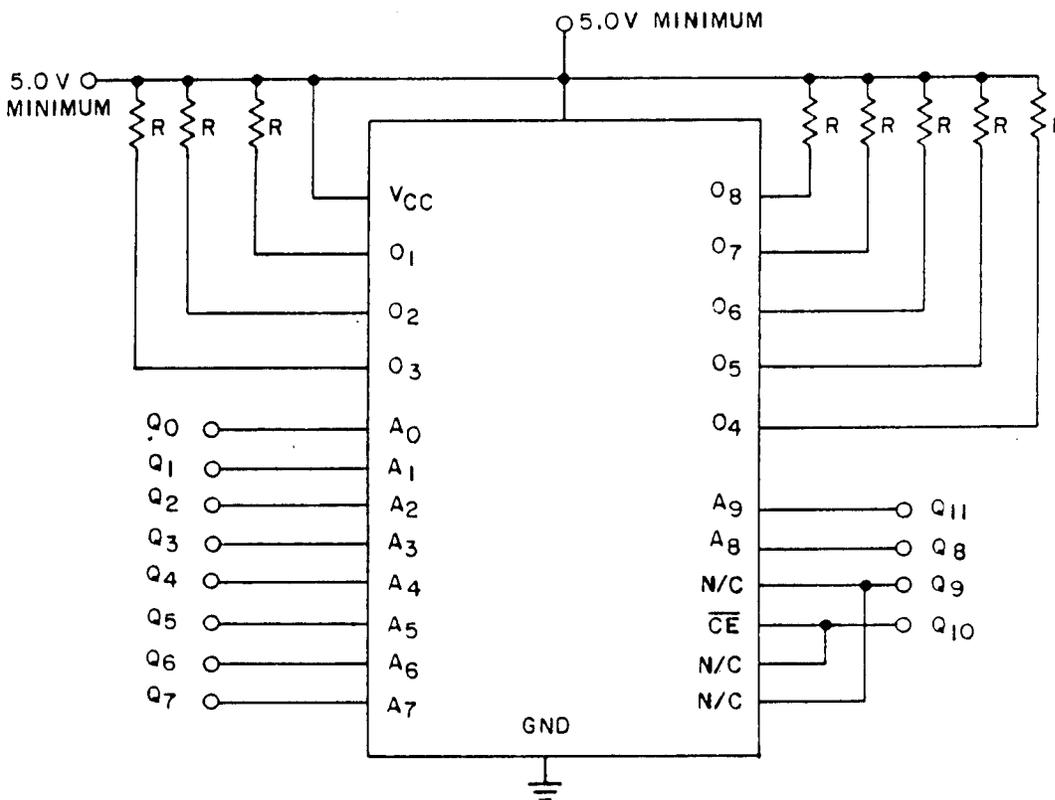
NOTES:

1. $R = 560\Omega \pm 5\%$ ($R = 300\Omega \pm 5\%$ for circuit F, $R = 270\Omega \pm 5\%$ for circuit D devices). All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5\text{ V minimum to } 0.8\text{ V maximum}$; $V_{IH} = 2.0\text{ V minimum to } 5.5\text{ V maximum}$; $50\% \pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

<u>Input</u>	<u>Frequency $\pm 50\%$</u>
O0	F0 = 100 kHz min
O1	F1 = 1/2 F0
O2	F2 = 1/2 F1
O3	F3 = 1/2 F2
O4	F4 = 1/2 F3
O5	F5 = 1/2 F4
O6	F6 = 1/2 F5
O7	F7 = 1/2 F6
O8	F8 = 1/2 F7
O9	F9 = 1/2 F8
O10	F10 = 1/2 F9
O11	F11 = 1/2 F10

FIGURE 5. Burn-in and steady-state life test circuit - Continued.

Device types 05 and 06

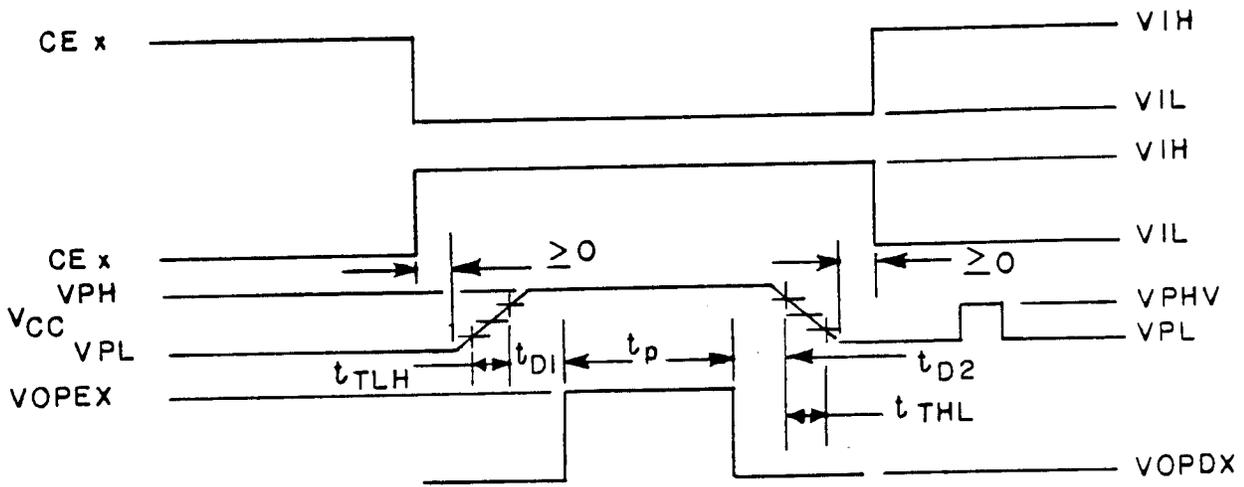


NOTES:

1. $R = 560\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

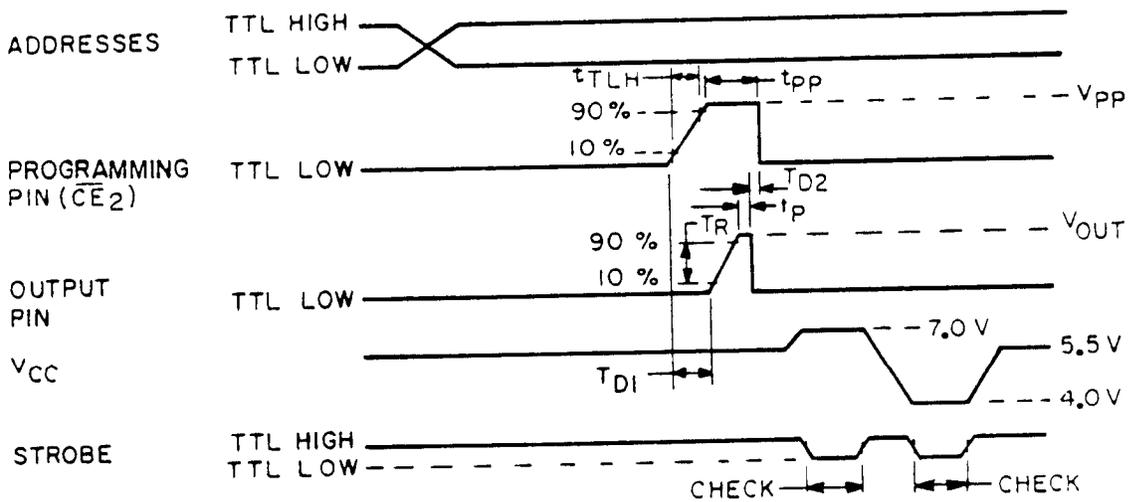
<u>Input</u>	<u>Frequency $\pm 50\%$</u>
Q0	F0 = 100 kHz min
Q1	F1 = 1/2 F0
Q2	F2 = 1/2 F1
Q3	F3 = 1/2 F2
Q4	F4 = 1/2 F3
Q5	F5 = 1/2 F4
Q6	F6 = 1/2 F5
Q7	F7 = 1/2 F6
Q8	F8 = 1/2 F7
Q9	F9 = 1/2 F8
Q10	F10 = 1/2 F9
Q11	F11 = 1/2 F10

FIGURE 5. Burn-in and steady-state life test circuit - Continued.



NOTE: All other waveform characteristics shall be as specified in table IVA.

FIGURE 6A. Programming voltage waveforms during programming for circuit A.



NOTES:

1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVB.

FIGURE 6B. Programming voltage waveforms during programming for circuit B (Device types 03 and 04).

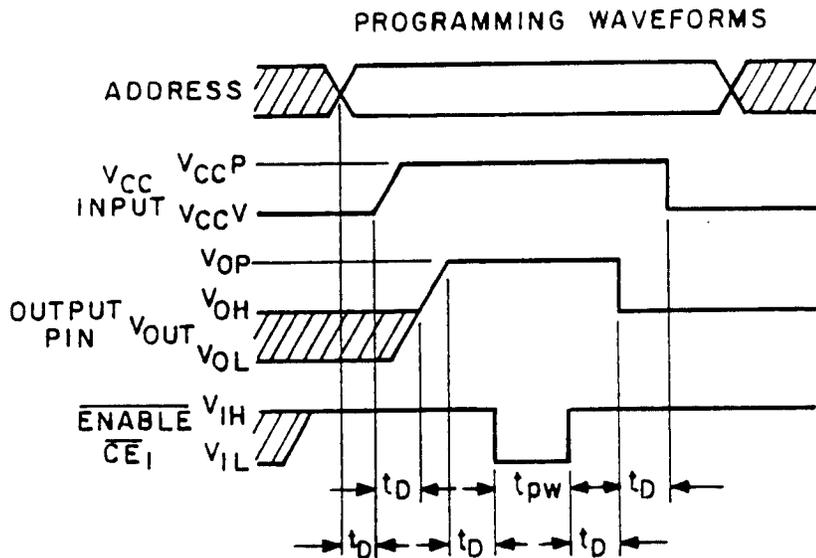
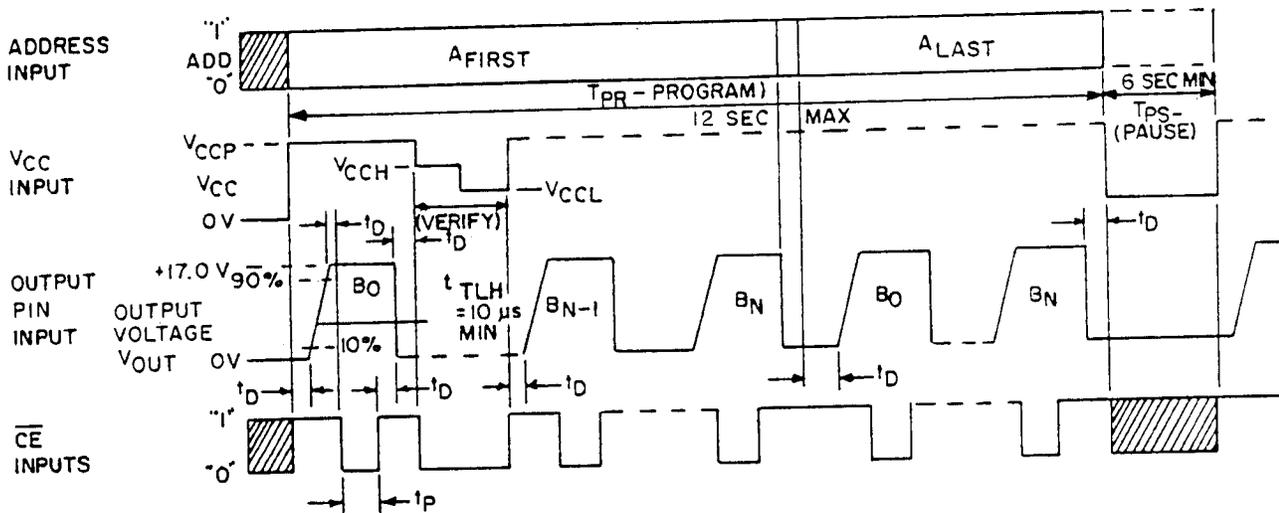
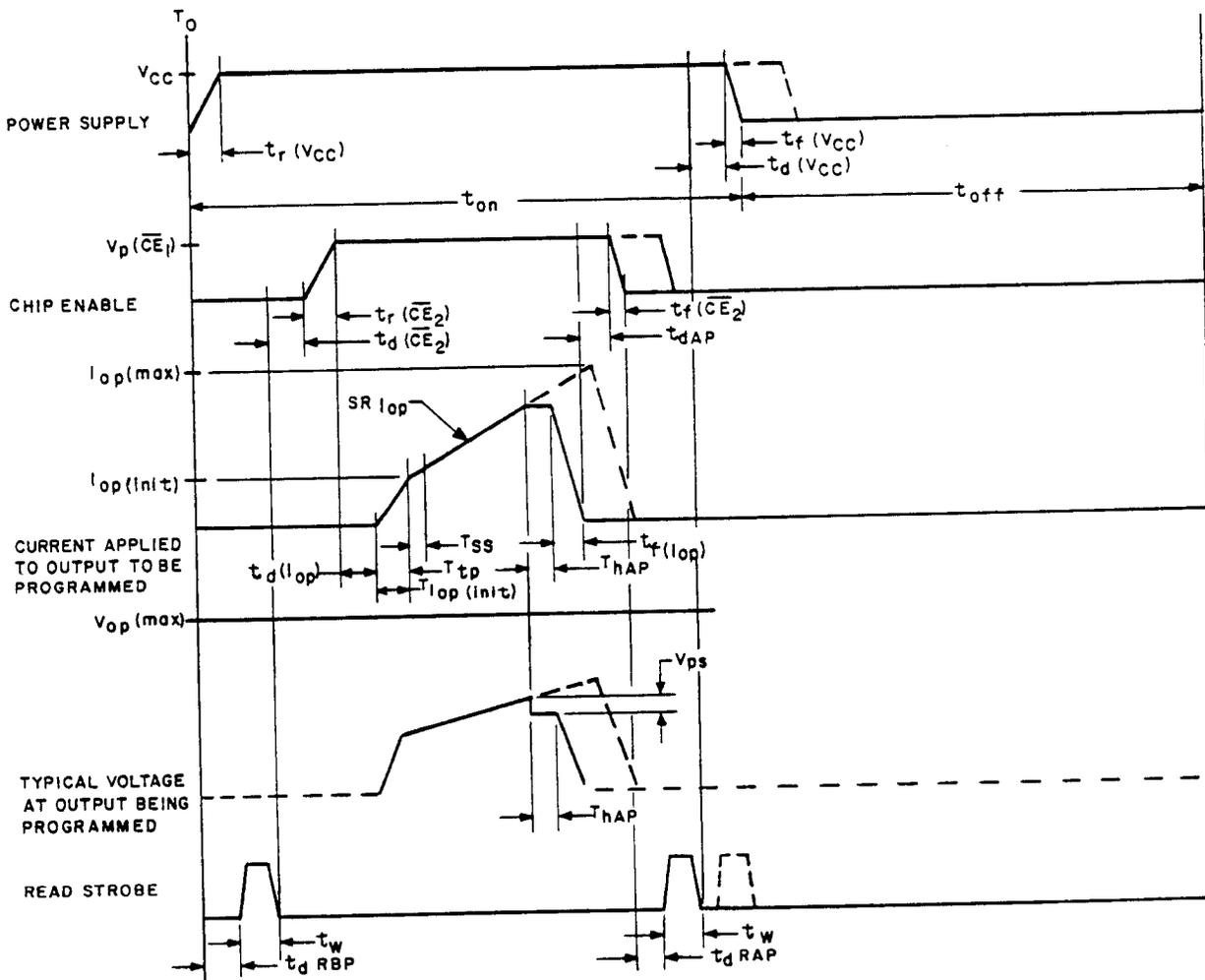


FIGURE 6B. Programming voltage waveforms during programming for circuit B (Device types 01, 02 and 08) - Continued.



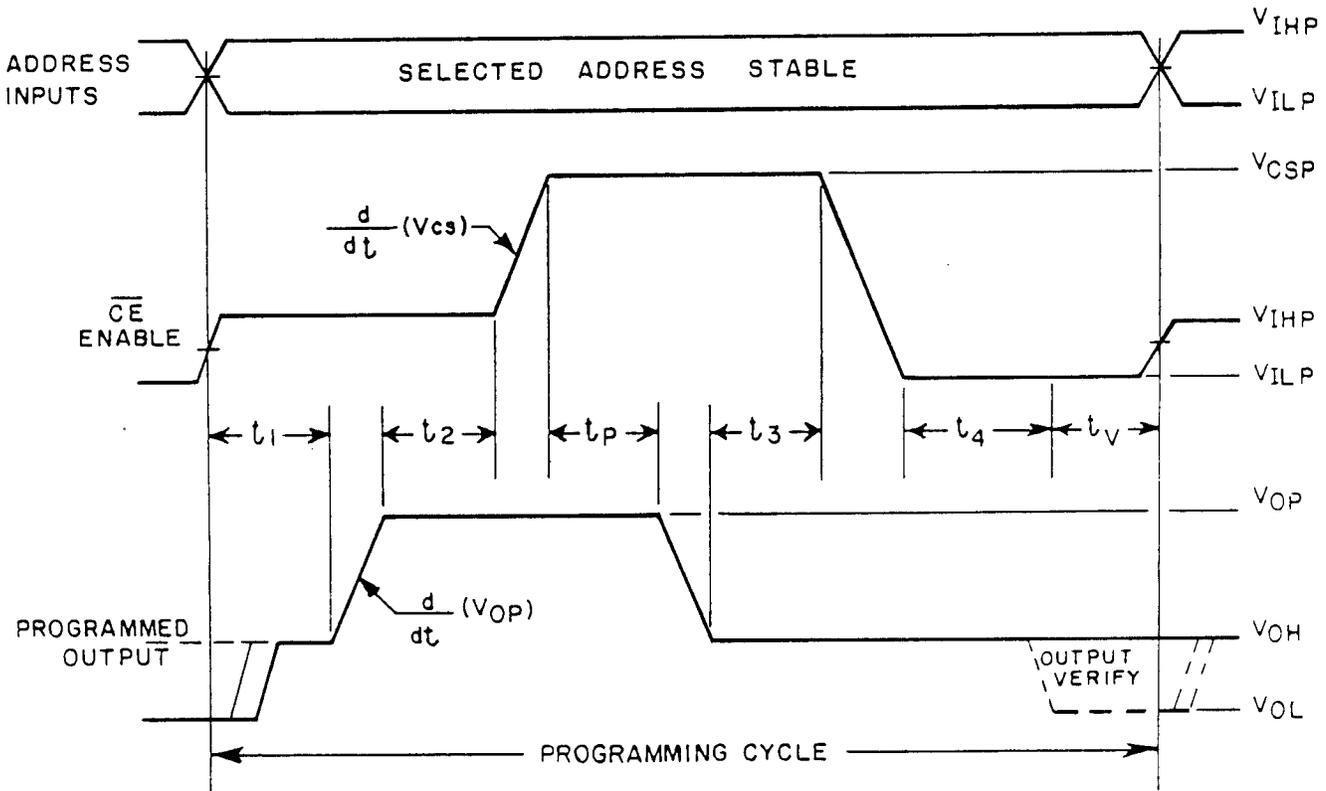
NOTE: All other waveform characteristics shall be as specified in table IVC.

FIGURE 6C. Programming voltage waveforms during programming for circuit C.



NOTE: All other waveform characteristics shall be as specified in table IVD.

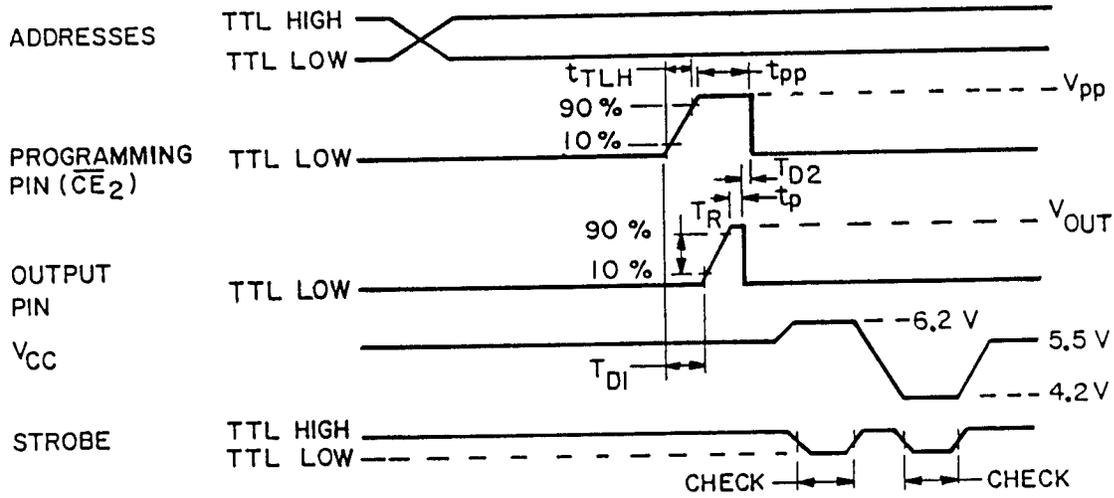
FIGURE 6D. Programming voltage waveforms during programming for circuit D.



NOTES:

1. All delays between edges are specified from completion of the first edge, not midpoints.
2. Delays t_1 , t_2 , t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μ s are recommended to minimize heating during programming.
3. During t_V the output being programmed is switched to the load R and verified.
4. Outputs not being programmed are connected to V_{ONP} through a resistor which provides output current limiting.
5. All other waveform characteristics shall be as specified in table IVE.

FIGURE 6E. Programming voltage waveforms during programming for circuit E.



NOTES:

1. Output load is 0.2 mA and 12 mA during 6.2 V and 4.2 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVF.

FIGURE 6F. Programming voltage waveforms during programming for circuit F.

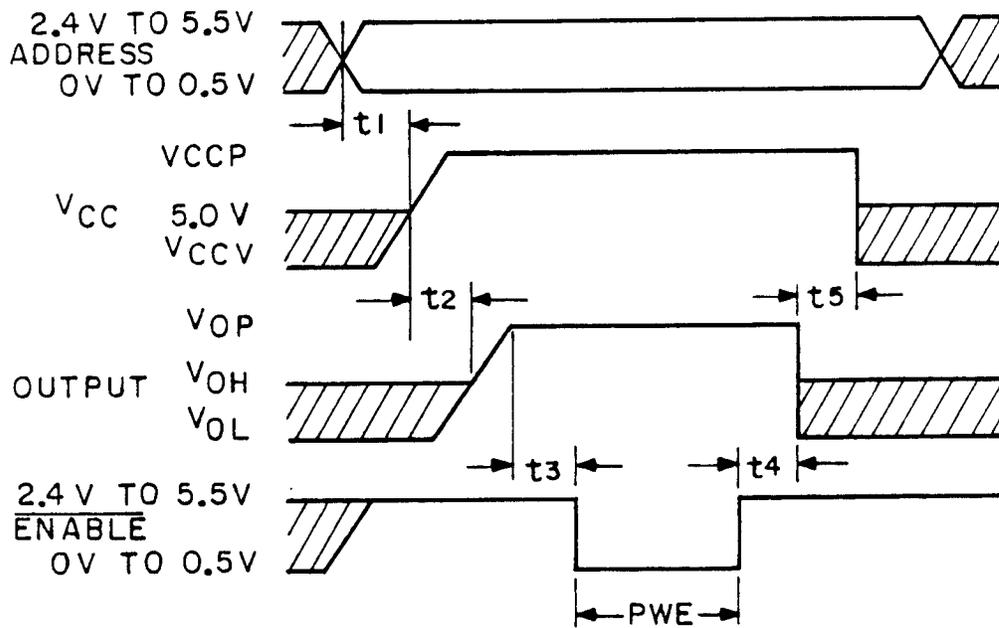
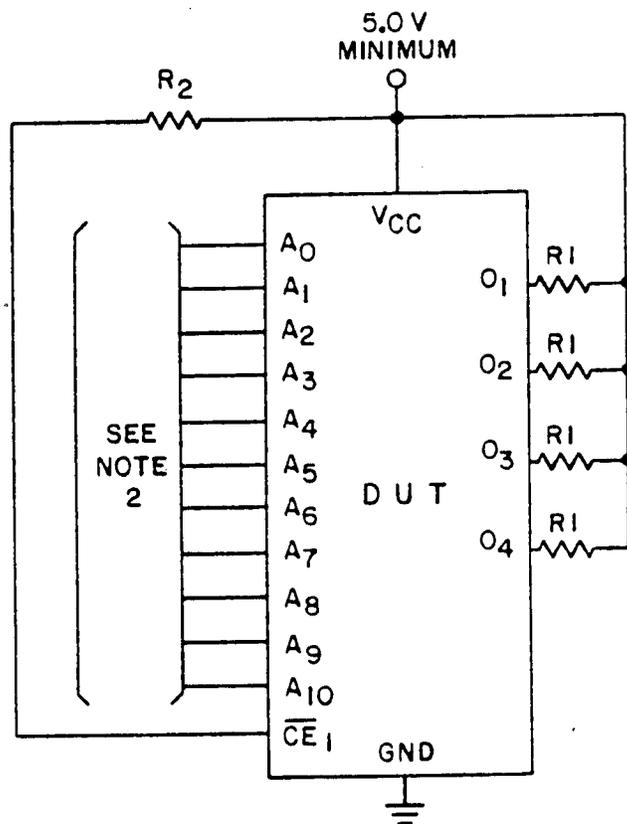


FIGURE 6G. Programming voltage waveforms during programming for circuit G.

Device types 01, 02, 08 and 10

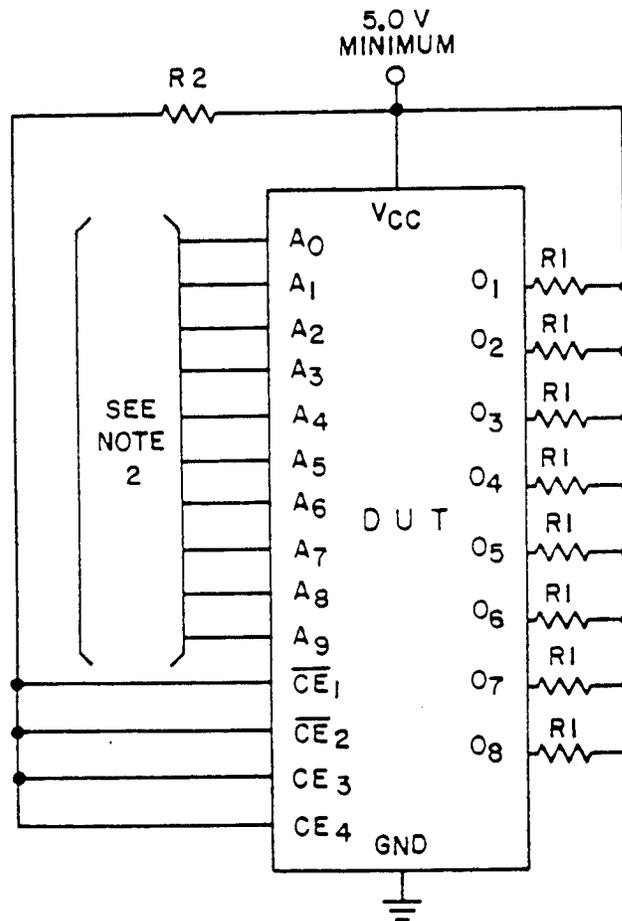


NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test (see 4.2d).

FIGURE 7. Freeze-out test bias configurations.

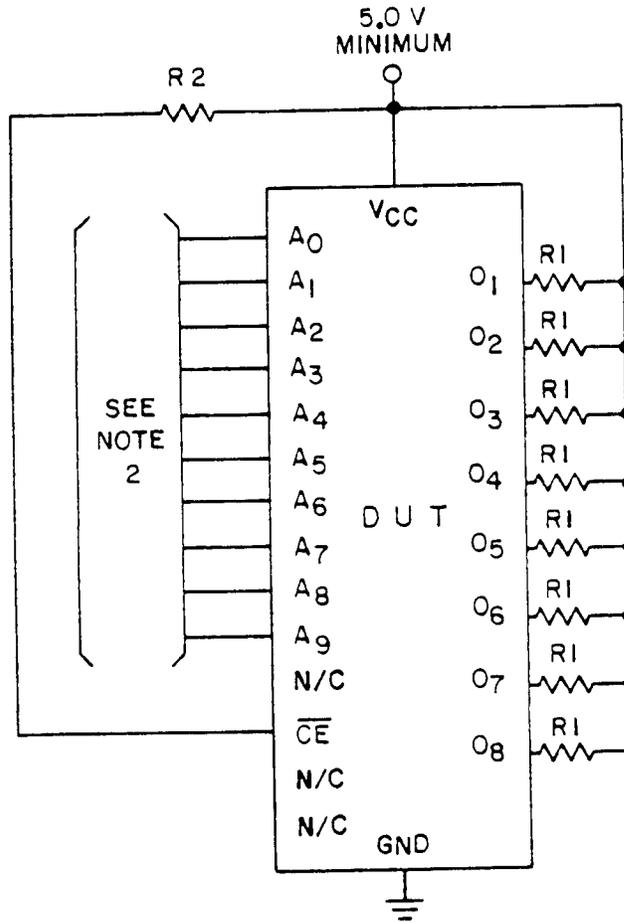
Device types 03, 04 and 09



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test (see 4.2d).

FIGURE 7. Freeze-out test bias configurations - Continued.

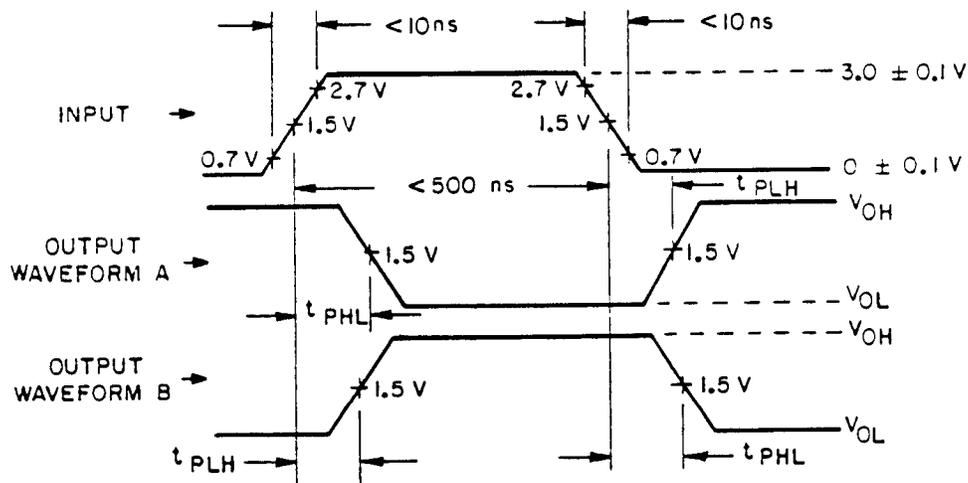
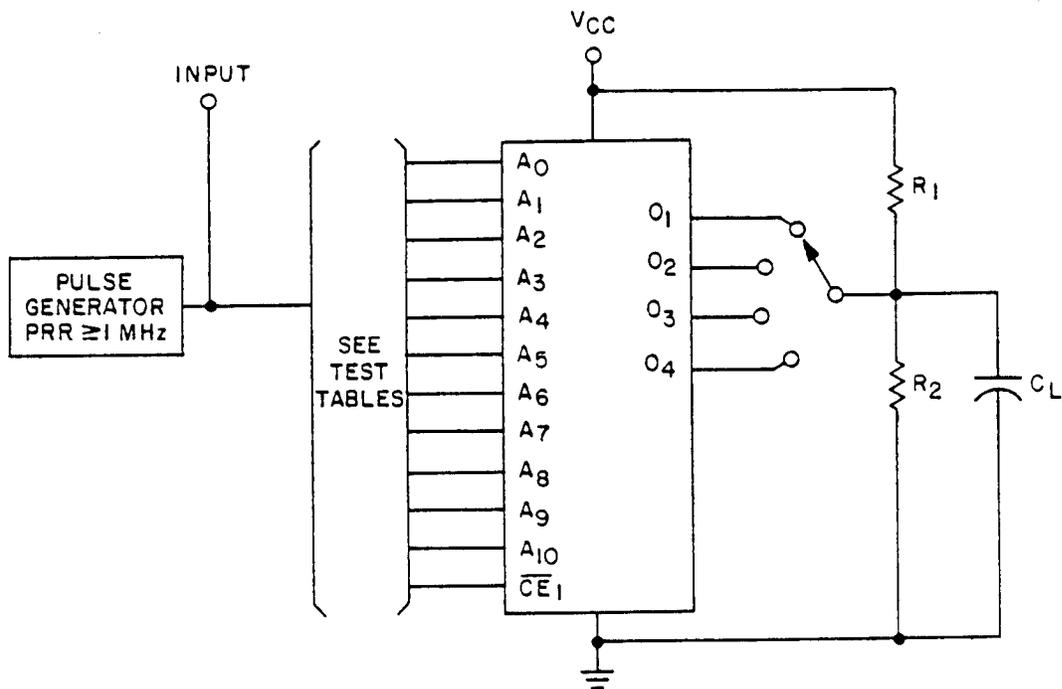
Device types 05 and 06

NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low, or open.
3. $R_2 = 1 \text{ k}\Omega \pm 5\%$.
4. Burn-in circuit may be used to perform this test (see 4.2d).

FIGURE 7. Freeze-out test bias configurations - Continued.

Device types 01, 02, 08 and 10

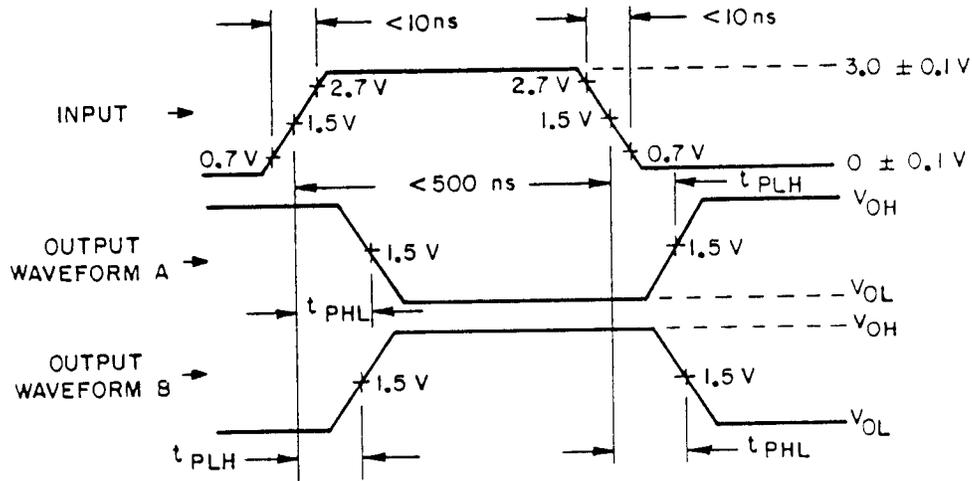
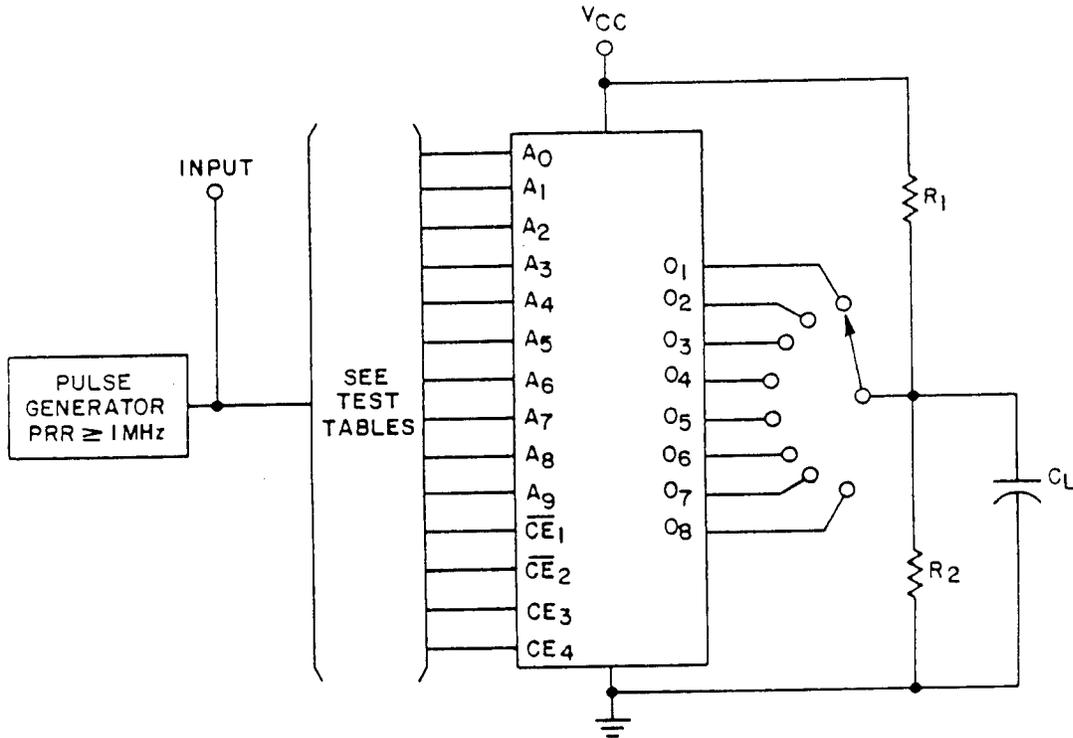


NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance; R₁ = 330Ω ±25% and R₂ = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 8. Switching time test circuits.

Device types 03, 04 and 09

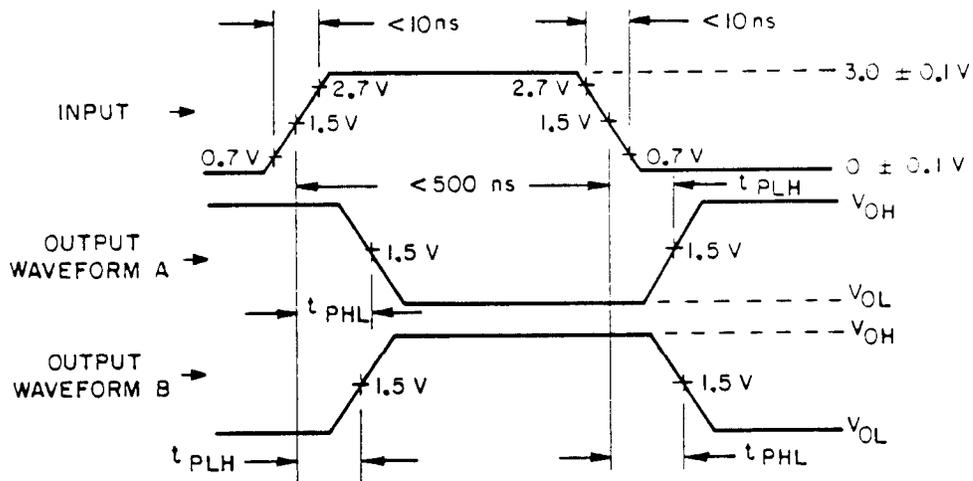
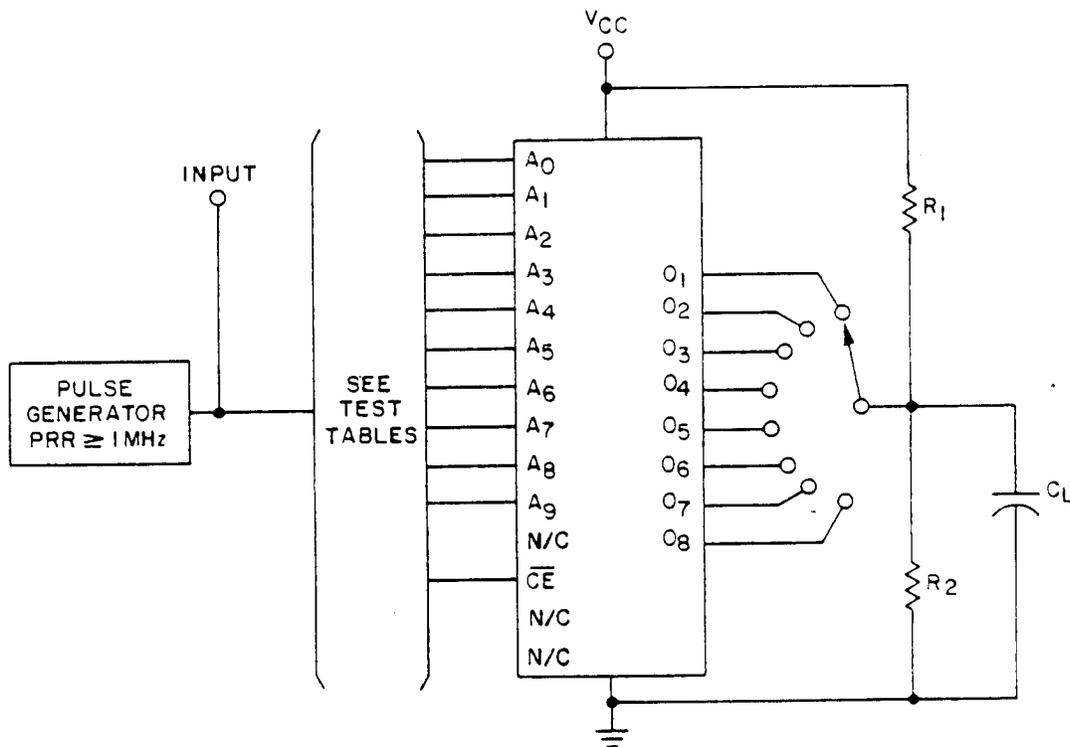


NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30$ pF minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

FIGURE 8. Switching time test circuits - Continued.

Device types 05 and 06



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 30\text{ pF}$ minimum, including jig and probe capacitance; $R_1 = 330\Omega \pm 25\%$ and $R_2 = 680\Omega \pm 20\%$.
3. Outputs may be under load simultaneously.

FIGURE 8. Switching time test circuits - Continued.

TABLE III. Group A inspection for device types 02, 08, and 10 - Continued.

Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage, inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases V.X test no.	Terminal													Test Limits		Unit																																																								
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18																																																					
1 $T_C = +25^\circ C$	105	3011	54	A6	A4	A3	A0	A1	A2	A10	GND	EE1	04	03	02	01	A9	A8	A7	VCC	Meas. Terminal	Min	Max																																																				
			55	11/10/11/11/9/10/	1/	1/	1/13/	1/	1/	1/10/	GND	0.5 V	GND	GND	GND	11/9/	1/13/	1/	15-5 V	04	-15	-100	mA																																																				
			56	"12/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"																																																		
			57	"12/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"																																																		
2	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = +125^\circ C$ and V _{IC} tests are omitted.																																																																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = -55^\circ C$ and V _{IC} tests are omitted.																																																																										
7 $T_C = +25^\circ C$	Functional tests	4/	58	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs																																																			
																									Outputs																																																		
8	tpHL1	GALPAT IFig. 8	59	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	Outputs																																																		
																										tpLH1	GALPAT IFig. 8	60	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/																								
																																																				tpHL2	Sequen-tial IFig. 8	61	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/
Same tests, terminal conditions, and limits as for subgroup 7, except $T_C = +125^\circ C$ and $T_C = -55^\circ C$.																																																																											
10	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = +125^\circ C$.																																																																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55^\circ C$.																																																																										

See footnotes at end of table.

TABLE 111. Group A Inspection for device type 03 - Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are High, 2.0 V, Low, 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases (U, K, test no.)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Test limits		Unit							
				A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	A9	A8	VCC	Measured terminal	Min		Max						
1 T _C = +25°C	V _{CEX}		55														15.2 V	5.2 V	5.2 V		0.5 V	0.5 V	5.5 V	5.5 V				U5		100	μA						
			56																																		
			57																																		
			58																	5.2 V																	
2	V _{CC}	J005	59	GND					GND	GND	GND	GND	GND	GND	GND		VCC		185	mA																	
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and V _{IC} tests are omitted.																																				
4	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																																				
7 T _C = +25°C	Functional tests		60	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/				
8 T _C = +25°C	E _{PHL} E _{PHL} E _{PHL2} E _{PHL2}	GALPAT Fig. 8 GALPAT Fig. 8 Sequen- tial Fig. 8 Sequen- tial Fig. 8	61	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/			
			62	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	
			63	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/
			64	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																																				
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																																				

See footnotes at end of table.

TABLE III. Group A Inspection for device types D4 and D9 - Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ± 2.0 V, low ± 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J.K.	Terminal conditions												Measured terminal	Test limits		Unit																								
				1	2	3	4	5	6	7	8	9	10	11	12		13	14		15	16	17	18	19	20	21	22	23	24	Min	Max												
TC = +25°C	I _{HH}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	50		μA											
																					5.5 V	5.5 V			5.5 V																		
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																							5.5 V	5.5 V			5.5 V																
																							5.5 V	5.5 V			5.5 V																
																							5.5 V	5.5 V			5.5 V																
																							5.5 V	5.5 V			5.5 V																
																							5.5 V	5.5 V			5.5 V																
																				5.5 V	5.5 V			5.5 V																			
TC = +25°C	I _{OL}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	100													
																					5.5 V	5.5 V			5.5 V																		
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
TC = +25°C	I _{OL}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	100													
																					5.5 V	5.5 V			5.5 V																		
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
TC = +25°C	I _{OL}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	100													
																					5.5 V	5.5 V			5.5 V																		
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
TC = +25°C	I _{OL}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	100													
																					5.5 V	5.5 V			5.5 V																		
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
																						5.5 V	5.5 V			5.5 V																	
TC = +25°C	I _{OL}	3010	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	Ag	VCC	CE4	CE3	CE1	Ag	100													

TABLE III. Group A Inspection for device types D4 and D9 - Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or r voltage; inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	MIL-STD-883 method	Test J,K no.	Terminal conditions														Measured Terminal	Test Limits		Unit									
			1	2	3	4	5	6	7	8	9	10	11	12	13	14		15	16		17	18	19	20	21	22	23	24	
			A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE4	CE3	CE2	CE1	A9	A8	VCC	Min	Max	
9 T _C = +25°C	tpHL1	IGALPAT FIG. 8	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/	5.5 V	5.5 V	GND	GND	5/	5/	5/	Outputs	100/100	ns
	tpLH1	IGALPAT FIG. 8	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/	5.5 V	5.5 V	GND	GND	5/	5/	5/	-	190/155	-
	tpHL2	Sequence FIG. 8	7/	7/	7/	7/	7/	7/	7/	7/	6/	6/	6/	GND	6/	6/	6/	6/	6/	7/	7/	7/	7/	7/	7/	7/	-	150/130	-
	tpLH2	Sequence FIG. 8	7/	7/	7/	7/	7/	7/	7/	7/	6/	6/	6/	GND	6/	6/	6/	6/	6/	7/	7/	7/	7/	7/	7/	7/	-	150/130	-
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																												
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																												

See footnotes at end of table.

TABLE III. Group A Inspection for device Type 05 - Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 J, K method	(Cases U, K, test no.)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured Terminal	Test Limits	Unit						
				A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	M/C	M/C	M/C	EE	VCC	A9	A8				VCC	M/n	Max			
1 $T_C = +25^\circ\text{C}$	tPHZ		50 51 52 53 54 55 56 57									5.2 V	5.2 V	5.2 V	GND								5.5 V					O1	100	μA						
														5.2 V	5.2 V															O2						
																			5.2 V												O3					
																					5.2 V										O4					
																						5.2 V									O5					
																							5.2 V								O6					
																								5.2 V							O7					
2	tOLZ		58 59 60 61 62 63 64 65									0.5 V	0.5 V	0.5 V														O1	-100							
																													O2							
																														O3						
																														O4						
																															O5					
																															O6					
																															O7					
3	tOS	3011	66 67 68 69 70 71 72 73		1/	1/	1/	1/	1/	1/	1/	1/	GND	GND	GND								0.5 V		1/9/13/	1/		O1	-15							
																														O2						
																														O3						
																														O4						
																														O5						
																														O6						
																															O7					
7 $T_C = +25^\circ\text{C}$	tFunc-tional tests		74	GND	GND	GND	GND							GND	GND	GND	GND	GND	GND																	
8 $T_C = +25^\circ\text{C}$	tPHL1 tPHL2 tPLH1 tPLH2	GALPAT FIG. 8 GALPAT FIG. 8 Sequen- tial FIG. 8 Sequen- tial FIG. 8	76 77 78 79	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	GND	GND																					
10	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = +125^\circ\text{C}$.			GND	GND	GND	GND							GND	GND	GND	GND	GND	GND																	
11	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55^\circ\text{C}$.			GND	GND	GND	GND							GND	GND	GND	GND	GND	GND																	

See footnotes at end of Table.

- 1/ For programmed devices, select an appropriate address to acquire the desired output state.
- 2/ For unprogrammed device types 01 and 02 (circuit A), apply 10.0 V on pin 1 (A₆); and for unprogrammed device types 03 and 04, apply 10.0 V on pin 1 (A₇) (circuit A).
- 3/ I_{OL} = 12 mA for circuits A, C, E, and G devices; I_{OL} = 16 mA for circuits B, D, and F devices.
- 4/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. Terminal conditions shall be as follows:
 - a. Inputs: H = 3.0 V, L = 0.0 V.
 - b. Outputs: Output voltage shall be either:
 - (1) H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator, or
 - (2) H \geq 1.0 V and L < 1.0 V when using a high-speed checker single comparator.
- 5/ GALPAT (PROGRAMMED PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PHL1} and t_{PLH1}. Each bit in the pattern is fixed by being programmed with an "H" or "L". The GALPAT tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

Description:

- Step 1. Word 0 is read.
 - Step 2. Word 1 is read.
 - Step 3. Word 0 is read.
 - Step 4. Word 2 is read.
 - Step 5. Word 0 is read.
 - Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 1023 or 2047 (as applicable) is reached, then increments to the next word and reads back and forth as in Step 1 through Step 6 and shall include all words.
 - Step 7. Pass execution time = (n² + n) x cycle time. n = 1024 or 2048 (as applicable).
- 6/ The outputs are loaded per figure 8.
 - 7/ SEQUENTIAL (PROGRAMMED PROM). This program will test all bits in the array for t_{PHL2} and t_{PLH2}. The sequential tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

Description:

- Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
- Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t_{PHL2} and t_{PLH2} are read.
- Step 3. Word 1 is addressed. Same enable sequence as above.
- Step 4. The reading procedure continues until word 1023 or 2047 (as applicable) is reached.
- Step 5. Pass execution times 1024 or 2048 (as applicable) x cycle time.

8/

Device type	t _{PHL1} (ns)	t _{PLH1} (ns)	t _{PHL2} (ns)	t _{PLH2} (ns)
01, 02	125	125	60	60
03, 04, 05, 06	90	90	50	50
Circuit F	90	90	50	50
Circuit B device 08	55	55	30	30
09	55	55	30	30
10	55	55	30	30

- 9/ For unprogrammed devices (circuit C), apply 10.0 V on pin 15 (A₉), 0.5 V on pin 2 (A₅) and 5.0 V to all other address pins for device types 02 and 10; device types 04 and 09, apply 10 V on pin 8 (A₀) and 5.0 V on pins 7, 6, 5, 4, 3 (A₁, A₂, A₃, A₄, A₅); device type 05, apply 10 V on pin 22 (A₉), 0.5 V on pins 8, 7, 6, 5 (A₀, A₁, A₂, A₃) and 5.0 V to all other address pins. For unprogrammed devices (circuit F) apply 12.0 V on pin 5 (A₀) for device types 02 and 08.
- 10/ For unprogrammed devices (circuit G), apply 10.5 V to pins 1 and 8 (A₆ and A₁₀), apply 0.0 V to pin 2 (A₅) and apply 3.0 V to all other address pins for device types 01 and 02; apply 10.5 V to pin 3 (A₅), apply 0.0 V to pins 2 and 8 (A₆ and A₀), and apply 3.0 V to all other address pins for device types 03 and 04.
- 11/ For unprogrammed devices, apply 12.0 V on pin 1 (A₆) for device types 02 and 08 (circuit B).
- 12/ For unprogrammed devices (circuit G), apply 10.5 V on pins 1 and 8 (A₆ and A₁₀), apply 0.0 V to pin 3 (A₄) and apply 3.0 V to all other address pins for device type 02, apply 10.5 V to pin 3 (A₅), apply 0.0 V to pin 8 (A₀) and apply 3.0 V to all other address pins for device type 04.
- 13/ For unprogrammed device type 02 (with date codes before 9501), apply 10.0 V on pin 5 (A₀); 0.5 V on pin 16 (A₉), and 5.0 V on all other address pins; and for unprogrammed device type 04 (with date codes before 9501) (circuit C), apply 10.0 V on pin 22 (A₉) and 5.0 V on all other address pins.
- 14/ For circuit B, device type 08, apply 2.4 V.
- 15/ For unprogrammed devices (circuit B), apply 12.0 V on pins 22 and 1 (A₉ and A₇) for device types 03 and 04.
- 16/ At the manufacturer's option, this may be performed with V_{IN} = 5.5 V and test limits of 50 μA maximum.
- 17/ For unprogrammed devices (circuit F) apply 12.0 V on pin 6 (A₂) and all other inputs at 0 V for device type 04.
- 19/ I_{OL} = 8 mA for circuits A, B, C, D, E, and G devices; I_{OL} = 16 mA for circuit F devices.
- 19/ For unprogrammed devices (circuit D), apply 12.0 V on pins 8 and 22 (A₀ and A₉), select an appropriate address to acquire the desired output state.
- 20/ For unprogrammed device type 03 (circuit E), apply 13.0 V on pin 4 (A₄) and pin 8 (A₀); and for unprogrammed device type 04 (circuit E), apply 13.0 V on pin 8 (A₀).

4.7 Programming procedures for circuit A. The programming characteristics of table IVA and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6A and the programming characteristics of table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.
- c. Apply V_{PL} voltage to V_{CC} .
- d. Bring the \overline{CE}_x inputs high and the CE_x inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.
- e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.
- f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH} .
- g. After a delay equal to or greater than t_{D1} , apply only one pulse with amplitude of V_{OPF} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
- h. Lower V_{CC} to V_{PL} following a delay of t_{D2} from programming enable pulse applied to an output.
- i. Enable the PROM for verification by applying V_{IL} to \overline{CE}_x and V_{IH} to CE_x .
- j. Apply V_{PHV} to V_{CC} and verify bit is programmed.
- k. Repeat 4.7a through 4.7j for all other bits to be programmed in the PROM.
- l. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVA. Programming characteristics for circuit A. 1/

Characteristic	Symbol	Limits <u>2/</u>			Unit
		Min	Recommended	Max	
Address input voltage <u>3/</u>	V _{IH}	2.4	5.0	5.0	V
	V _{IL}	0.0	0.4	0.5	V
Programming	V _{PH} <u>4/</u>	10.75	11.0	11.25	V
Voltage to V _{CC} low	V _{PL}	0.0	0.0	1.5	V
Program verify	V _{PHV}		5.5		V
Verify voltage	V _R <u>5/</u>	4.5		5.5	V
Programming input low current at V _{PH}	I _{ILP}		-300	-600	μA
Programming voltage (V _{CC}) transition time	t _{TLH}	1	5	10	μs
	t _{THL}	1	5	10	μs
Programming delay	t _{D1}	10	10	20	μs
	t _{D2}	1	5	5	μs
Programming pulse width	t _p <u>6/</u>	90	100	110	μs
Programming duty cycle	PDC		30	60	%
Output voltage, enable	V _{0PE} <u>7/</u>	10.5	10.5	11.0	V
Output voltage, disable	V _{0PD}	0.0	5.0	5.5	V

1/ During the programming, the chip must be disabled for proper operation.

2/ T_C = +25°C.

3/ No inputs should be left open for V_{IH}.

4/ V_{PH} source must be capable of supplying one ampere.

5/ It is recommended that post programming dual verification be made at V_R min and V_R max.

6/ Note 4.7j in programming procedure.

7/ V_{0PE} source must be capable of supplying 10 mA minimum.

4.8 Programming procedures for circuit B, device types 03 and 04. The waveforms on figure 6B, the programming characteristics of table IVB, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Raise V_{CC} to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the \overline{CE} inputs and V_{IL} to the CE inputs. The chip enable inputs are TTL compatible.
- e. Apply the V_{pp} pulse to the programming pin (CE_2). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the output pin's programming pulse by T_{D2} (see figure 6B).
- f. Apply only one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- h. Repeat 4.8c through 4.8g for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the \overline{CE} inputs and V_{IH} to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.0$ V and 0.2 mA at $V_{CC} = 7.0$ V at $T_C = +25^\circ\text{C}$.
- j. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVB. Programming characteristics for circuit B, device types 03 and 04.

Characteristic	Symbol	Conditions	Limits ^{1/}			Unit
			Min	Recommended	Max	
V _{CC} required during programming	V _{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t _{TLH}		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V _{pp}		32.5	33	33.5	V
Output programming voltage	V _{OUT}		25.5	26	26.5	V
Programming pin pulse width (CE ₂)	t _{pp}	Chip disabled, V _{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t _p	Chip disabled, V _{CC} = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I _L	V _{pp} = 33 V, V _{OUT} = 26 V, V _{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T _{D1}	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T _{D2}	Measured at 10% levels	100			ns
Output current during verification	I _{OLV1}	Chip enabled, V _{CC} = 4.0 V	11	12	13	mA
	I _{OLV2}	Chip enabled, V _{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V _{IH}		2.4	5.0	5.5	V
	V _{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t _p /t _c			25	%

^{1/} T_C = +25°C.

4.8.1 Programming procedures for circuit B, device types 01, 02, and 08. The waveforms on figure 6B (device types 01, 02, and 08), the programming characteristics of table IVB (device types 01, 02, and 08), and the following shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Apply V_{IH} to \overline{CE}_1 and the binary address of the PROM word to be programmed. Raise V_{CC} to V_{CCP} .
- c. After a t_D delay, apply only one V_{OP} to the output to be programmed high. Apply V_{OP} to one output at a time.
- d. After a t_D delay, a pulse \overline{CE}_1 to a V_{IL} level for a duration of t_p .
- e. After a t_p and a t_D delay, remove V_{OP} from the programmed output.
- f. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OP} pulses to each output to be programmed and pulsing \overline{CE}_1 to the V_{IL} level, allowing for proper delays between V_{OP} and \overline{CE}_1 .
- g. Repeat 4.8.1b through 4.8.1e for all bits to be programmed.
- h. To verify programming, lower V_{CCP} to V_{CC} . Connect a 10-k Ω resistor between each output and V_{CC} . Apply V_{IL} to \overline{CE}_1 input. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.
- i. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVB. Programming characteristics for circuit B, device types 01, 02, and 08.

Characteristic	Symbol	Conditions	Limits ^{1/}			Unit
			Min	Recommended	Max	
V _{CC} required during programming	V _{CCP}		11.5	11.75	12.0	V
V _{OUT} current limit during programming	I _{OP}		20	25	30	mA
Output programming voltage	V _{OUT}		10.5	11.0	11.5	V
Pulse width of programming voltage	t _p		9	10	11	μs
Programming delay	t _D		0	1	10	μs
V _{CCP} or V _{OUT} transition time	t _{TLH}	Rise time of V _{CC} or V _{OUT}	1	5	10	V/μs
V _{CCP} current	I _{CCP}		800	900	1000	mA
Low V _{CC} for verification	V _{CCL}		4.2	4.3	4.4	V
High V _{CC} for verification	V _{CCH}		5.8	6.0	6.2	V
Address input voltage	V _{IH}		2.4	3.0	5.5	V
	V _{IL}		0.0	0.0	0.5	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t _p /t _c		25	25	%

^{1/} T_C = +25°C.

4.9 Programming procedures for circuit C. The waveforms on figure 6C, the programming characteristics of table IVC, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all device outputs with a 10-k Ω resistor to V_{CC} . Apply V_{IH} to the \overline{CE} inputs and V_{IL} to the CE inputs.
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a t_D delay (10 μ s), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.
- e. After a t_D delay (10 μ s), pulse \overline{CE} input to logic "0" for a duration of t_p .
- f. After a t_D delay (10 μ s), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 6C.
- h. Repeat 4.9c through 4.9g for all other bits to be programmed.
- i. To verify programming after t_D (10 μ s) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to \overline{CE} inputs and logic "1" level to CE inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.
- j. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVC. Programming characteristics for circuit C.

Characteristic	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
Programming voltage	V_{CCP} 1/	$I_{CCP} = 375 \pm 75$ mA, transient or steady state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	$V_{CCP} = 8.75 \pm .25$ V	300	350	400	mA
Input voltage high level "1"	V_{IH}		2.4		5.5	V
Input voltage low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	$V_{IH} = 5.5$ V			50	μ A
Input current	I_{IL}	$V_{IL} = 0.4$ V			-500	μ A
Output programming voltage	V_{OUT} 3/	$I_{OUT} = 200 \pm 20$ mA, transient or steady state	16	17	18	V
Output programming current	I_{OUT}	$V_{OUT} = 17 \pm 1$ V	180	200	220	mA
Programming voltage transition time	t_{TLH}		10		50	μ s
CE programming pulse width	t_p		0.3	0.4	0.5	ms
Pulse sequence delay	t_D		10			μ s
Programming duty cycle	t_{PR} $t_{PR} + t_{PS}$				50	%

1/ Bypass V_{CC} to GND with a 0.01- μ F capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 \pm 1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4.10 Programming procedures for circuit D. The programming characteristics on table IVD and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 5D and the programming characteristics of table IVD shall apply to these procedures.
- b. Select the word to be programmed by applying the appropriate voltages to the address pins as well as the required voltages to chip enable pins to select the device.
- c. Apply the proper power, $V_{CC} = 6.5 \text{ V}$, $GND = 0 \text{ V}$.
- d. Verify that the bit to be programmed is in the "0" logic state.
- e. Enable the chip for programming by application of the chip enable voltage, $V_p(CE) = 21.0 \text{ V}$, CE_2 , CE_3 and CE_4 should be left high, and CE_1 should remain low.
- f. Apply I_{op} programming current ramp to the output to be programmed. The other outputs shall be left open. Only one output may be programmed at a time. During the rise of the current ramp, the required current will be achieved to program the junction. As programming occurs, a drop in voltage can be sensed at the output of the device. Upon detection of V_{ps} , the current shall be held for t_{hap} and then shut off.
- g. Verify that the programmed bit is in the "1" logic state. Lower $V_p(CE_1)$ to 0 V and read the output. Note that the PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- h. Lower V_{CC} to 0 V. The power supply duty cycle shall be equal to or less than 50 percent.
- i. If the bit verifies as not having been programmed at $V_{CC} = 6.5 \text{ V}$, repeat the programming ramp sequence up to 15 times until the bit is programmed. If after 16 programming attempts, the bit does not program, the device shall be considered a reject.
- j. If the bit verifies as having been programmed at $V_{CC} = 6.5 \text{ V}$, one of the following two conditions shall be followed:
 - (1) If the current required to program was less than $I_{op(max)}$, proceed to 4.10 k.
 - (2) If the current required to program was equal to or greater than $I_{op(max)}$, the device shall be considered a reject and no further attempts at programming other bits shall be attempted.
- k. Repeat 4.10a through 4.10j for all other bits to be programmed.
- l. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IV.D. Programming characteristics for circuit D.

Characteristic	Symbol	Conditions <u>1/</u>	Limits			Unit
			Min	Recommended	Max	
Address input voltage	V _{IH}	Don't leave inputs open	2.4	5.0	5.0	V
	V _{IL}		0	0	0.4	
Chip enable programming voltage	V _{P(CE)}	$\overline{CE}_1 = V_{IL}$ $CE_3 = CE_4 = V_{IH}$ $V_{P(CE)} = \overline{CE}_2$	20.5	21.0	21.5	V
Programming voltage limit	V _{OP(max)}	Programming current ramp voltage limit	24	25	26	V
Power supply	V _{CC}		6.3	6.5	6.7	V
Power supply current	I _{CC}				250	mA
Chip enable current	I _{CE}				150	mA
Initial value of programming current ramp	I _{OP(INIT)}		19	20	21	mA
Maximum value of programming current ramp	I _{OP(max)}		155	160	165	mA
Programming current ramp (linear slew rate)	SRI _{OP}		0.9	1.0	1.1	mA/μs
V _{CC} pulse rise time	t _r (V _{CC})		0.2	2.0		μs
V _{CC} pulse fall time	t _f (V _{CC})		0.2	2.0		μs
Chip enable rise time	t _r (\overline{CE}_2)		3.0	4.0		μs
Chip enable fall time	t _f (\overline{CE}_2)		0.2	4.0		μs
Programming current ramp fall time	t _f (I _{OP})			0.1	0.2	μs
Hold time after programming	t _{hap}		1.4	1.5	1.6	μs
Time to reach I _{OP} initial	t _{IOP}		0.5	1.0	2.0	μs
Delay to start V _{ps} sense	t _{ds}		2.0	3.0	4.0	μs

See footnote at end of table.

TABLE IVD. Programming characteristics for circuit D - Continued.

Characteristic	Symbol	Conditions <u>1/</u>	Limits			Unit
			Min	Recommended	Max	
Delay to chip enable pulse	t_{dce}			1.0		μs
Delay to programming ramp	$t_d(I_{OP})$		2.0	3.0	10	μs
Delay after programming to CE ₁	t_{dRAP}		2.0	3.0	10	μs
Delay to read after programming	t_{dRAP}	Programming verification	2.0	3.0		μs
Delay to V _{CC} off	$t_D(V_{CC})$			1.0		μs
Delay to read before programming	t_{dRBP}	Initial check	2.0	3.0		μs
Width to read compare strobe	t_w			1.0		μs
Voltage change at programming	V_{ps}	Typical 2.0 V	0.7	2.0		V
Time to program bit	t_{tp}	V_{ps} sensing circuit will automatically adjust this time				
Duty cycle power		Maximum duty cycle to maintain $T_C < +85^\circ C$		50		%
Case temperature	T_C		25	85		$^\circ C$

1/ $T_C = +25^\circ C$.

4.11 Programming procedures for circuit E. The waveforms on figure 6E, the programming characteristics of table IV E, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all outputs with a 300-ohm resistor to V_{ONP} . Apply V_{IHP} to the \overline{CE}_2 , CE_3 , and CE_4 inputs and V_{ILP} to the \overline{CE}_1 inputs.
- c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP} .
- d. After a delay of t_1 , apply only one V_{OP} pulse with a duration of t_p , t_2 , and $d(V_{OP})/dt$ to the output selected for programming. After a delay of t_2 and $d(V_{OP})/dt$, pulse \overline{CE}_2 from V_{IHP} to V_{CEP} for the duration of t_p , $2d(V_{CE})/dt$, and t_3 ; \overline{CE}_2 is then to go to the V_{ILP} level.
- e. To verify programming after \overline{CE}_1 has been set to V_{ILP} , lower V_{CC} to V_{CCL} after a delay of t_4 . The programmed output should remain in the logic "1" state.
- f. The outputs should be programmed one output at a time since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Repeat 4.11c through 4.11f for all other bits to be programmed.
- h. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVE. Programming characteristics for circuit E.

Characteristic	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
V _{CC} required during programming	V _{CCP}		5.0		5.5	V
High-level input voltage during programming	V _{IHP}		2.4		5.5	V
Low-level input voltage during programming	V _{ILP}		0.0		0.45	V
Chip enable voltage during programming	V _{CEP}	\overline{CE}_1 pin	14.5		15.5	V
Output voltage during programming	V _{OP}		19.5		20.5	V
Voltage on outputs not to be programmed	V _{ONP}		0		V _{CCP} + 0.3	V
Current on outputs not to be programmed	I _{ONP}				20	mA
Rate of output voltage change	$\frac{d(V_{OP})}{dt}$		20		250	V/ μ s
Rate of chip enable voltage change	$\frac{d(V_{CE})}{dt}$	\overline{CE}_1 pin	100		1000	V/ μ s
Programming period	t _p		50		100	μ s
V _{CC} during programming verification	V _{CCL}		4.5		5.0	μ s

4.12 Programming procedures for circuit F. The waveforms on figure 6F, the programming characteristics of table IVF, and the following procedures shall apply:

- a. Connect the device in the electrical configuration for programming.
- b. Raise V_{CC} to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the \overline{CE} inputs and V_{IL} to the \overline{CE} inputs. The chip enable inputs are TTL compatible.
- e. Apply the V_{pp} pulse to the programming pin (\overline{CE}_2). In order to insure that the output transistor is off before increasing voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the programming pin's programming pulse by T_{D2} (see figure 6F).
- f. Apply only one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- h. Repeat 4.12c through 4.12g for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the \overline{CE} inputs and V_{IH} to the \overline{CE} inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.2$ V and 0.2 mA at $V_{CC} = 6.2$ V at $T_C = +25^\circ\text{C}$.
- j. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVF. Programming characteristics for circuit F.

Characteristic	Symbol	Conditions	Limits ^{1/}			Unit
			Min	Recommended	Max	
V _{CC} required during programming	V _{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t _{TLH}		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V _{pp}		32.5	33	33.5	V
Output programming voltage	V _{OUT}		25.5	26	26.5	V
Programming pin pulse width (CE)	t _{pp}	Chip disabled, V _{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t _p	Chip disabled, V _{CC} = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I _L	V _{pp} = 33 V, V _{OUT} = 26 V, V _{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T _{D1}	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T _{D2}	Measured at 10% levels	100			ns
Output current during verification	I _{OLV1}	Chip enabled, V _{CC} = 4.2 V	11	12	13	mA
	I _{OLV2}	Chip enabled, V _{CC} = 6.2 V	0.19	0.2	0.21	mA
Address input voltage	V _{IH}		2.4	5.0	5.5	V
	V _{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t _p /t _c			25	%

^{1/} T_C = +25°C.

4.13 Programming procedures for circuit G. The programming characteristics of table IVG and the following procedures shall be used for programming:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6G and the programming characteristics of table IVG shall apply to these procedures.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip enable inputs. Note that address and enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase V_{CC} from nominal to V_{CCP} (10.5 ± 0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 V/ μ s). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.
- d. Select the output where a logical high is desired by raising that output voltage to V_{QP} (10.5 ± 0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 V/ μ s). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP} , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 k Ω minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip enables to low level. This is done with a pulse PWE for 10 μ s. The 10 μ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 V (± 0.25 V). The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.
- g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of step f is to be performed at a V_{CC} level of 4.0 volts (± 0.2 V). V_{OH} , during the 4-volt verification, must be at least 2.0 volts. The 4-volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.
- h. Repeat 4.13b through 4.13f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperature. After all selected bits are programmed, the entire contents of the memory should be verified.
- i. For classes S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVG. Programming characteristics for circuit G.

Characteristic	Symbol	Conditions	Limits ^{1/}			Unit
			Min	Recommended	Max	
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	$V_{CC} = 11$ V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	$V_{OUT} = 11$ V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/ μ s
Programming pulse width (enabled)	P_{WE}		9	10	11	μ s
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	M_{DC}			25	25	%
Address setup time	t_1		100			ns
V_{CCP} setup time	t_2	^{2/}	5			μ s
V_{CCP} hold time	t_5		100			ns
V_{OP} setup time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

^{1/} $T_C = +25^\circ\text{C}$.

^{2/} V_{CCP} setup time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP} .

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- i. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

- GND - - - - - Electrical ground (common terminal).
- I_{IN} - - - - - Current flowing into an input terminal.
- V_{IC} - - - - - Input clamp voltage.
- V_{IN} - - - - - Voltage level at an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type/manufacturer</u>	<u>Circuit designator</u>	<u>Fusible link</u>	<u>Symbol/CAGE number</u>
01	7684/Harris Corporation	A	NiCr	CDWD/34371
01	77S184/National Semiconductor	G	TiW	CCXP/27014
01	82S184/Signetics Corporation	C	NiCr	CDKB/18324
02	7685/Harris Corporation	A	NiCr	---
02	77S185/National Semiconductor	G	TiW/W	---
02,10	82S185A/Signetics Corporation	C	NiCr	---
02,08	29651/Raytheon Company	F	NiCr	CRP/07933
03	77S180/National Semiconductor	G	TiW	---
03	7680/Harris Corporation	A	NiCr	---
03	82S180/Signetics Corporation	C	NiCr	---
03	93Z450/Fairchild Corporation	D	ZVE*	CFJ/07263
03	27S180/Advanced Micro Devices, Inc.	E	Platinum silicide	CDWN/34335
04	77S181/National Semiconductor	G	TiW/W	---
04	7681/Harris Corporation	A	NiCr	---
04,09	82S181A/Signetics Corporation	C	NiCr	---
04,09	93Z451/Fairchild Corporation	D	ZVE*	---
04	27S181/Advanced Micro Devices, Inc.	E	Platinum silicide	---
04	29631/Raytheon Company	F	NiCr	---
05	82S2708/Signetics Corporation	C	NiCr	---
05	93Z461/Fairchild Corporation	D	ZVE*	---
06	93Z460/Fairchild Corporation	D	ZVE*	---
02,08	53S841/Monolithic Memories, Inc.	B	TiW	---

* Zapped vertical emitter.

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17

Preparing activity:
Air Force - 17

Agent:
DLA - ES

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

(Project 5962-0885)

User activities:

Army - SM
Navy - AS, CG, MC