

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR,  
TTL, LOW POWER, FLIP-FLOPS

MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, low power, bistable logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	R-S master-slave flip-flop
02	J-K master-slave flip-flop
03	Dual J-K master-slave flip-flop
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
A	F-1 (14-lead, 1/4" x 1/4"), flat package
B	F-3 (14-lead, 3/16" x 1/4"), flat package
C	D-1 (14-lead, 1/4" x 3/4"), dual-in-line package
D	F-2 (14-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	0 V dc to 8.0 V dc
Input voltage range- - - - -	0 V dc to 6.0 V dc
Storage temperature range- - - - -	-65°C to +150°C
Maximum power dissipation in accordance with flip-flop ( $P_D$ ) 1/ - - - - -	11 mW
Lead temperature (soldering, 10 seconds) -	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ): Cases A, B, C, and D - - - - -	(See MIL-M-38510, appendix C)
Junction temperature ( $T_J$ ) 2/ - - - - -	+175°C

1/ Must withstand the added  $P_D$  due to short-circuit conditions (e.g.,  $I_{OS}$ ) at one output for 5 seconds duration.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STU-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

#### 1.4 Recommended operating conditions.

Supply voltage ( $V_{CC}$ ) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage ( $V_{IH}$ ) - -	2.0 V dc
Maximum low-level input voltage ( $V_{IL}$ ) - - -	0.7 V dc, except clock input of types 01, 02, 03, and 04
Maximum low-level clock input voltage - - -	0.6 V dc (types 01, 02, 03, and 04)
Normalized fanout (each output) <u>3</u> / - - -	10 maximum
Width of clock pulse - - - - -	> 200 ns
Width of preset pulse - - - - -	> 100 ns
Width of clear pulse - - - - -	> 100 ns
Input set-up time:	
Device types 02, 03, and 04 - - - - -	> Clock pulse width, minimum 100 ns, minimum when R, S input data is complementary
Device type 01 - - - - -	> Clock pulse width, minimum when R, S input data is not complementary
Device type 05 - - - - -	50 ns, minimum
Input hold time - - - - -	10 ns, minimum
Case operating temperature range - - - - -	-55°C to +125°C

## 2. APPLICABLE DOCUMENTS

### 2.1 Government documents.

2.1.1 Specifications and standards. The following specification and standard, form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

#### SPECIFICATION

##### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

##### STANDARD

##### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3/ The device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type					Limits		Unit
			01	02	03	04	05	Min	Max	
High-level output voltage	$V_{OH}$	$V_{IN} = 0.7\text{ V}$ $V_{CC} = 4.5\text{ V}$ $I_{OH} = -100\text{ }\mu\text{A}$						2.4		V
Low-level input voltage	$V_{OL}$	$I_{OL} = 2\text{ mA}$ $V_{CC} = 4.5\text{ V}$						0.3		V
Low-level input current	$I_{IL1}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.3\text{ V}$	S R	J K	J K	J K		-43	-140	$\mu\text{A}$
Low-level input current	$I_{IL2}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.3\text{ V}$	Clock Preset Clear	Clock Preset Clear	Clock Preset Clear			-1/	-360	$\mu\text{A}$
Low-level input current	$I_{IL3}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.3\text{ V}$				Clock Clear		-172	-560	$\mu\text{A}$
Low-level input current	$I_{IL4}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.3\text{ V}$					D Preset	-60	-180	$\mu\text{A}$
Low-level input current	$I_{IL5}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.3\text{ V}$					Clock Clear	-120	-360	$\mu\text{A}$
High-level input current	$I_{IH1}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 2.4\text{ V}$	S R	J K	J K	J K	D		10	$\mu\text{A}$
High-level input current	$I_{IH2}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V}$	S R	J K	J K	J K	D		100	$\mu\text{A}$
High-level input current	$I_{IH3}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 2.4\text{ V}$	Clear Preset	Clear Preset	Clear Preset	Clear Preset	Clock Preset		20	$\mu\text{A}$
High-level input current	$I_{IH4}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V}$	Clear Preset Clock	Clear Preset Clock	Clock Clear	Preset	Clock Clear		200	$\mu\text{A}$
High-level input current	$I_{IH5}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 2.4\text{ V}$					Clear		30	$\mu\text{A}$
High-level input current	$I_{IH6}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V}$					Clear		300	$\mu\text{A}$
High-level input current	$I_{IH7}$	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 2.4\text{ V}$					Clear		40	$\mu\text{A}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type					Limits		Unit
			01	02	03	04	05	Min	Max	
High-level input current	I <sub>IH8</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 5.5 V				Clock Clear			400	μA
High-level input current	I <sub>IH9</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 2.4 V				Clock		0	-400	μA
High-level input current	I <sub>IH10</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 2.4 V	Clock	Clock	Clock			0	-200	μA
Short-circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 <sup>2/</sup>						-3	-15	mA
Supply current per flip-flop	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN(clock)</sub> = 0	Types 01, 02, 03, and 04				1.90		mA	
			Type 05				1.50		mA	
Maximum clock frequency	f <sub>MAX</sub> <sup>3/</sup>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 4 kΩ					2.5			MHz
Propagation delay to a high level (clear or preset to output)	t <sub>PLH</sub>						10	125		ns
Propagation delay to a low level (clear or preset to output)	t <sub>PHL</sub>		V <sub>IN(clock)</sub> = 2.4 V				10	200		ns
Propagation delay to a high level (clock to output)	t <sub>PLH</sub>		V <sub>IN(clock)</sub> = 0 V, types 01, 02 03, and 04				10	250		ns
Propagation delay to a low level (clock to output)	t <sub>PHL</sub>						10	125		ns
							10	200		ns

1/ Not more than one output should be shorted at a time.

2/ f<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one half of the input frequency.

3/ For device types 01 and 03.

I<sub>IL2</sub> = -120 μA, for device type 02I<sub>IL2</sub> = -105 μA.

3.2.1 Case outlines. The case outlines shall be as specified in 1.2.3.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables and logic diagrams. The truth tables and logic diagrams shall be as specified on figure 2.

3.2.4 Schematic circuits. Schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS) as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained by the agent activity and will be available upon request.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004)	1*,2,3, 9,10,11	1*,2,3, 9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,8, 9,10,11
Group B test requirements (method 5005)	1,2,3,7,8, 9,10,11	N/A
Group C end point electrical parameters (method 5005)	N/A	1,2,3
Group D end point electrical parameters (method 5005)	1,2,3	1,2,3

\*PDA applies to subgroup 1 (see 4.3c).

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 17 (see MIL-M-38510, appendix E).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition D or E, using the circuits shown on figure 4, or equivalent.
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical test requirements shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
  - (1) Test condition D or E, using the circuits shown on figure 4, or equivalent.
  - (2)  $T_A = +125^\circ\text{C}$  minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

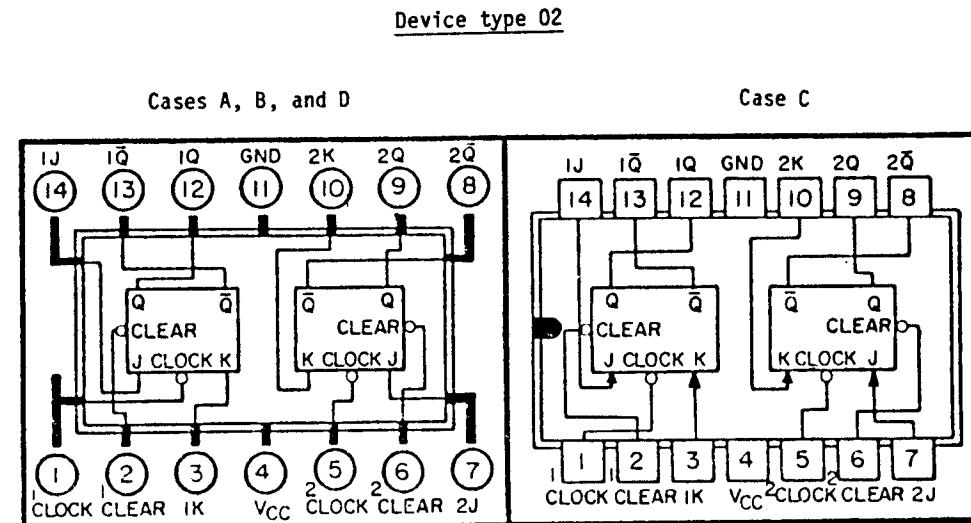
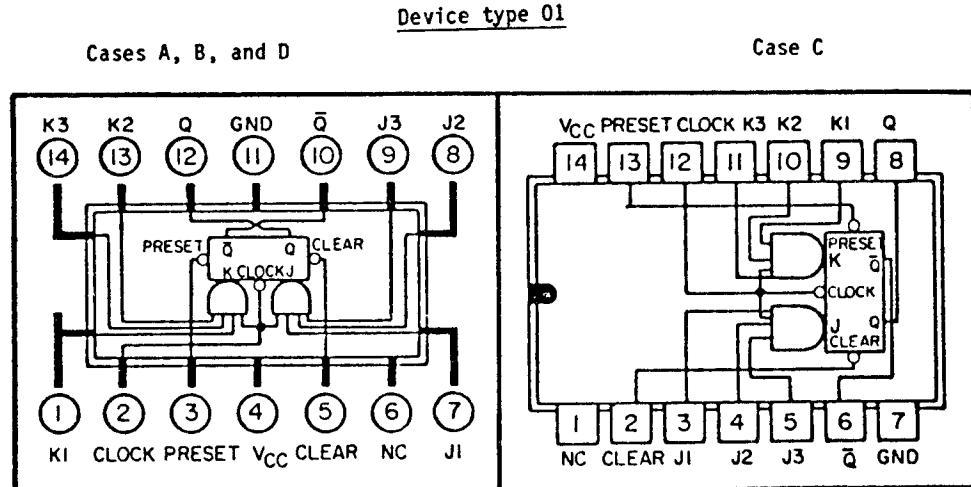
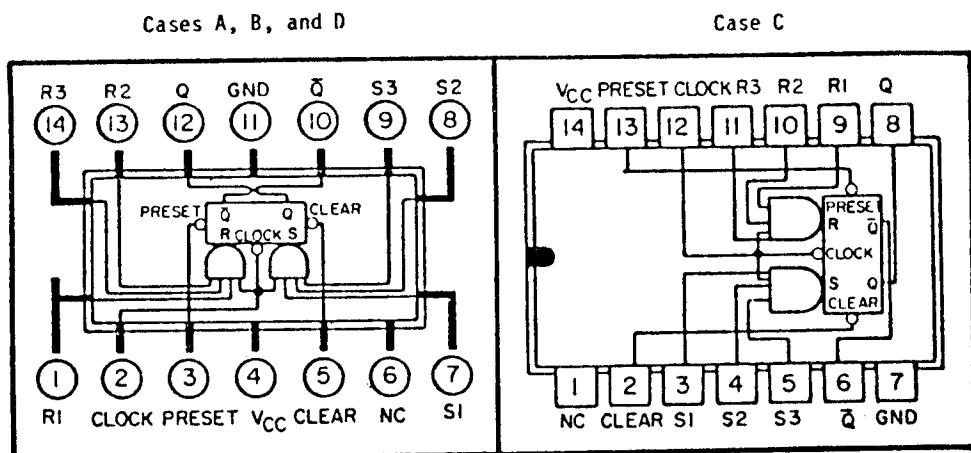
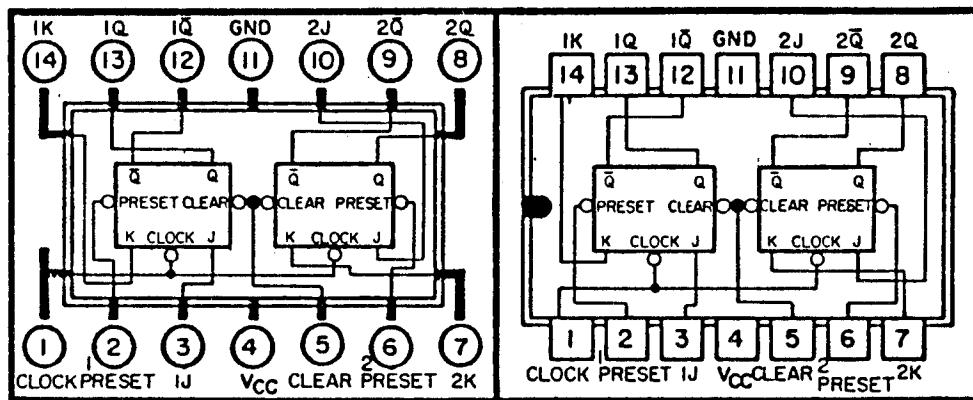


FIGURE 1. Terminal connections.

Cases A, B, and D

Case C



Cases A, B, and D

Case C

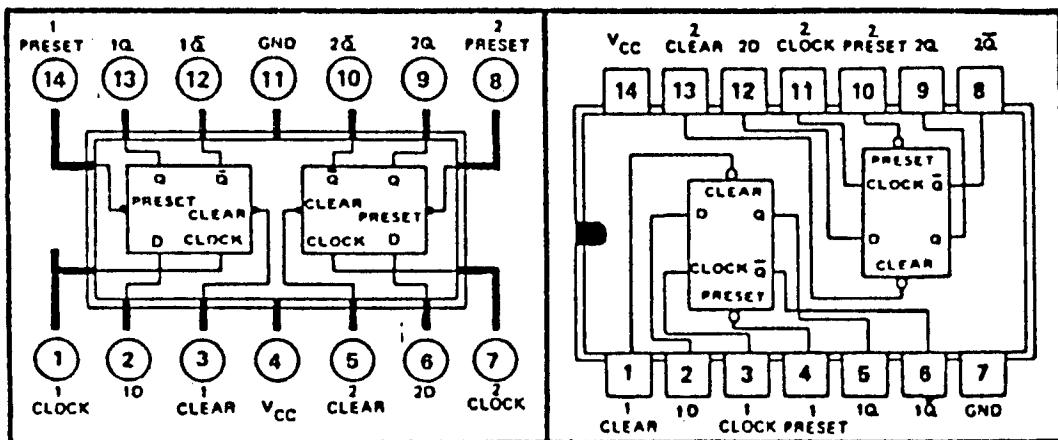


FIGURE 1. Terminal connections - Continued.

Positive logic: Low input to preset sets Q to high-level  
 Low input to clear sets Q to low-level  
 Preset and clear are independent of clock

Truth table		
$t_n$		$t_{n+1}$
R	S	Q
L	L	$Q_n$
L	H	H
H	L	L
H	H	Indeterminate

NOTES: 1.  $J = J_1 \quad J_2 \quad J_3$   
 2.  $K = K_1 \quad K_2 \quad K_3$   
 3.  $t_n$  = Bit time before clock pulse.  
 4.  $t_{n+1}$  = Bit time after clock pulse.

Truth table		
$t_n$		$t_{n+1}$
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\bar{Q}_n$

#### Device type 01.

Positive logic: Low input to preset sets Q to high-level  
 Low input to clear set Q to low-level  
 Preset and clear are independent of clock

NOTES: 1.  $R = R_1 \quad R_2 \quad R_3$   
 2.  $S = S_1 \quad S_2 \quad S_3$   
 3.  $t_n$  = Bit time before clock pulse.  
 4.  $t_{n+1}$  = Bit time after clock pulse.

#### Device type 02.

#### Description for device types 01 and 02

These flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation as controlled by the clock pulse is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.

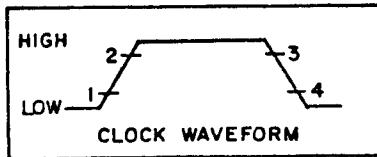


FIGURE 2. Truth tables and device descriptions.

Truth table each flip-flop		
$t_n$	$t_{n+1}$	
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Positive logic: Low input to present sets Q to high-level  
 Low input to clear sets Q to low-level  
 Preset and clear are independent of clock

NOTES: 1.  $t_n$  = Bit time before clock pulse.  
 2.  $t_{n+1}$  = Bit time after clock pulse.

Truth table each flip-flop		
$t_n$	$t_{n+1}$	
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\bar{Q}_n$

#### Device type 04

Positive logic: Low input to clear sets Q to low-level  
 Clear is independent of clock

NOTES: 1.  $t_n$  = Bit time before clock pulse.  
 2.  $t_{n+1}$  = Bit time after clock pulse.

#### Device type 03

#### Description for device types 03 and 04

These flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation as controlled by the clock pulse is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.

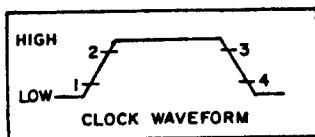


FIGURE 2. Truth tables and device descriptions - Continued.

Truth table each flip-flop		
$t_n$	$t_{n+1}$	
Input	Output	Output
D	Q	$\bar{Q}$
L	L	H
H	H	L

Positive logic: Low input to preset sets Q to high-level  
 Low input to clear sets Q to low-level  
 Clear and preset are independent of clock

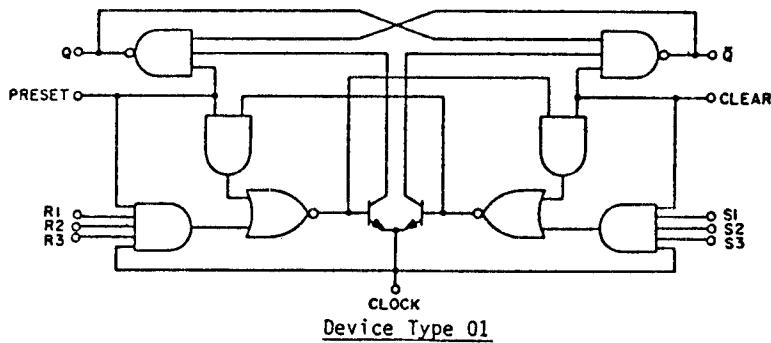
NOTES: 1.  $t_n$  = Bit time before clock pulse.  
 2.  $t_{n+1}$  = Bit time after clock pulse.

#### Device type 05

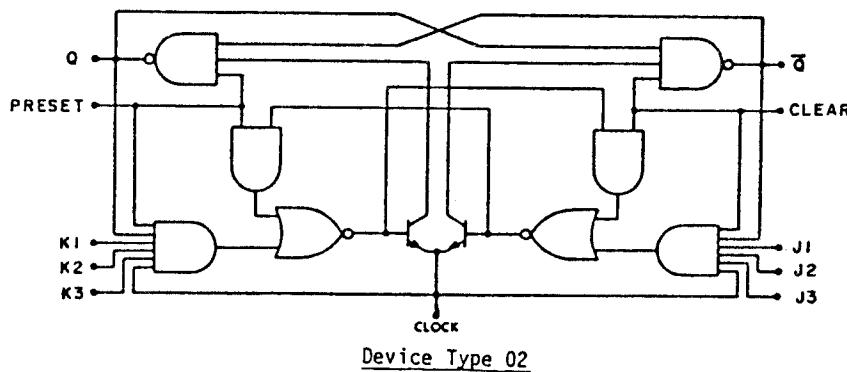
#### Description for device type 05.

Input information is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

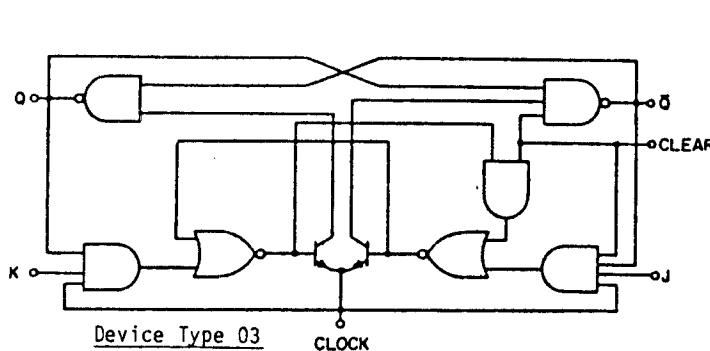
FIGURE 2. Truth tables and device descriptions - Continued.



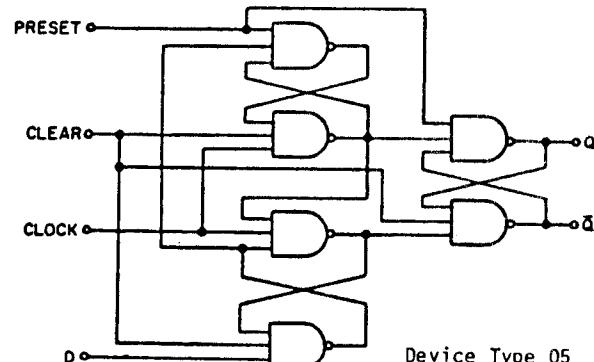
Device Type 01



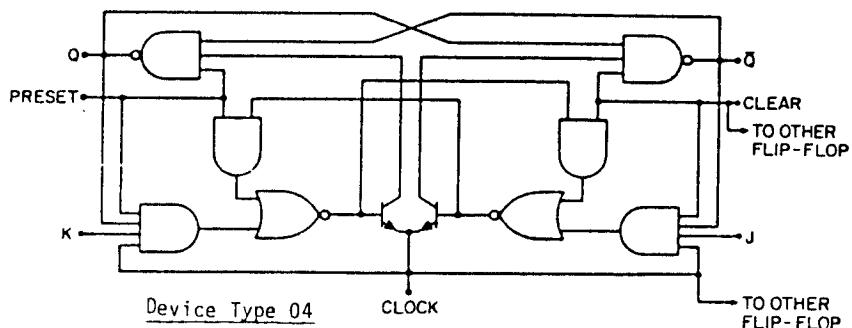
Device Type 02



Device Type 03



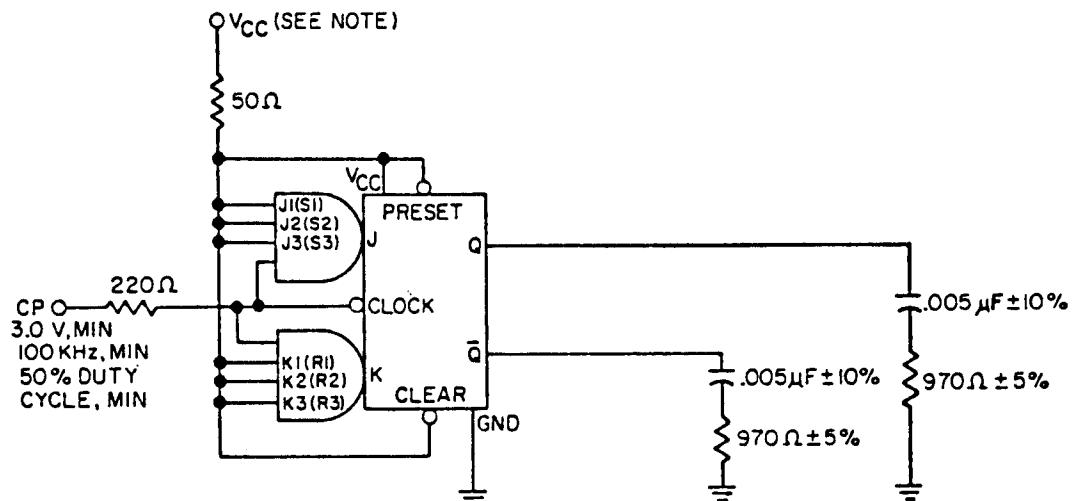
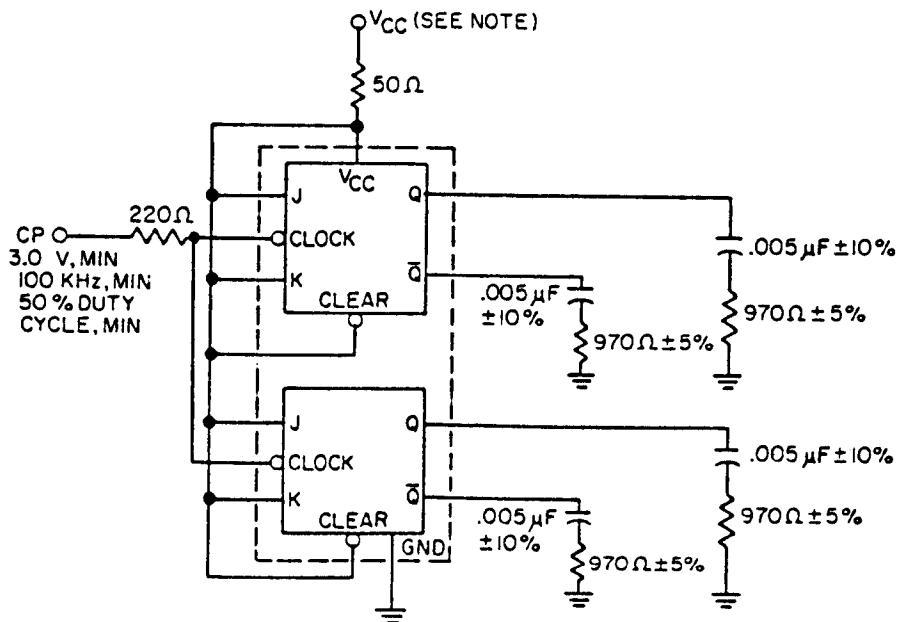
Device Type 05



Device Type 04

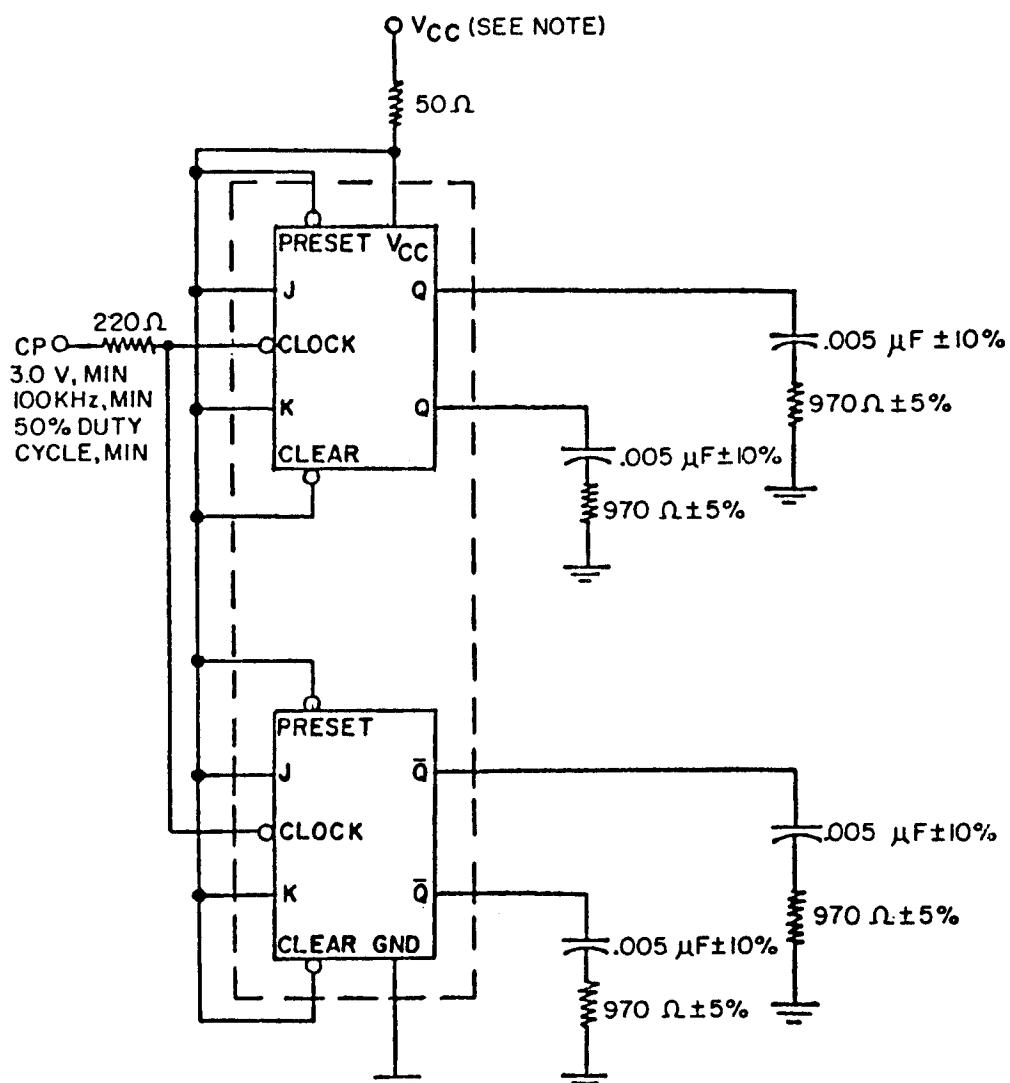
TO OTHER  
FLIP-FLOP

FIGURE 3. Logic diagram for device types 01, 02, 03, 04, and 05.

Device types 01 and 02Device type 03

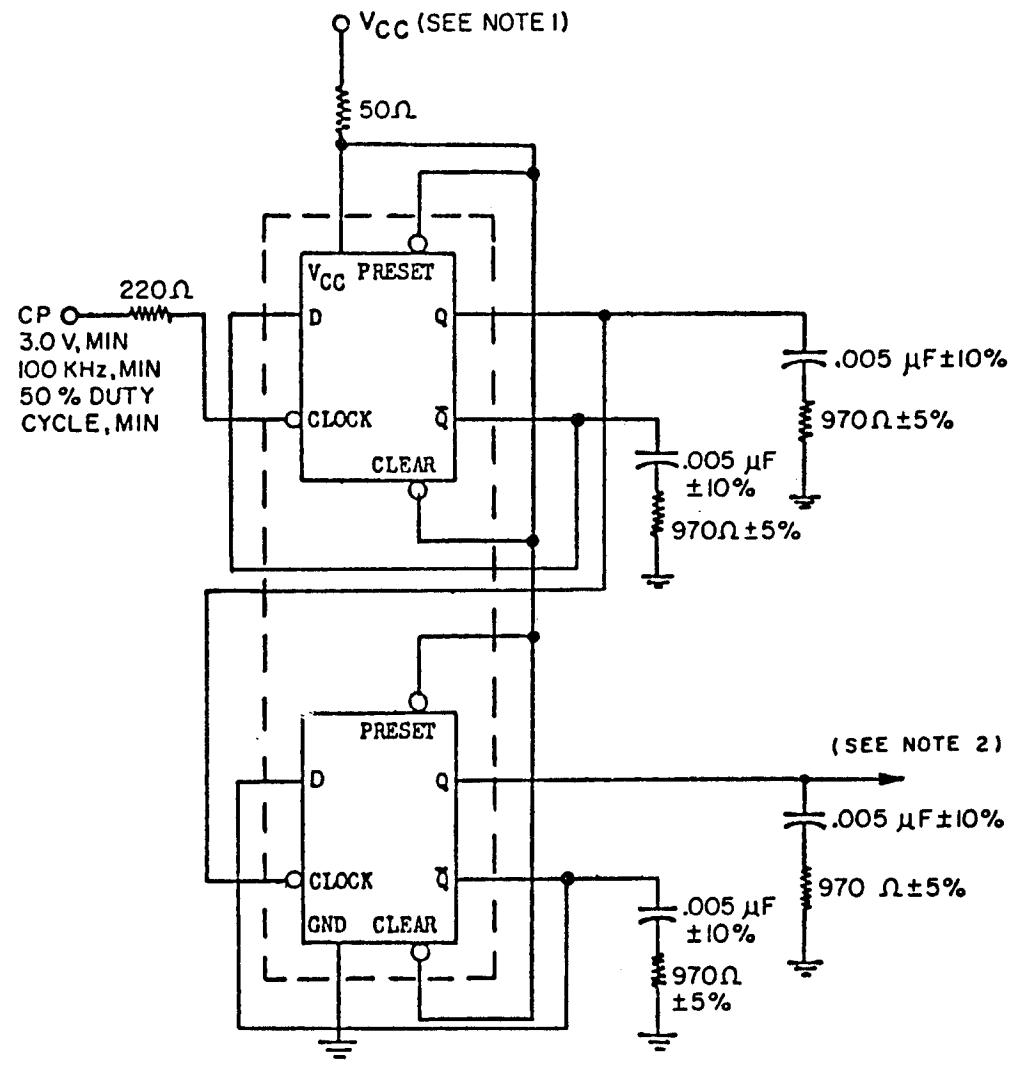
NOTE:  $V_{CC}$  = 5 volts, minimum, at the device terminals.

FIGURE 4. Burn-in and life test circuits.



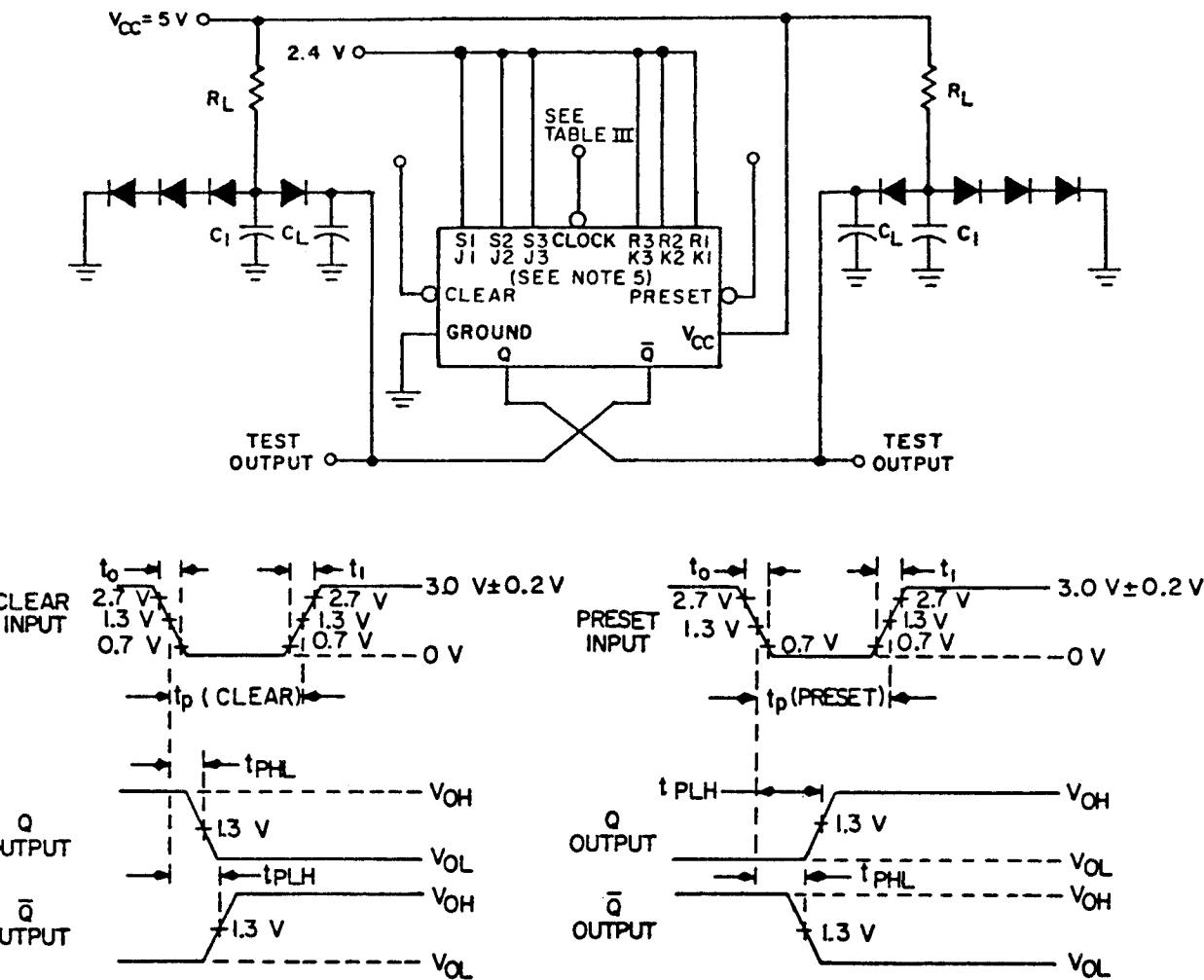
NOTE:  $V_{CC}$  = 5 volts, minimum, at the device terminals.

FIGURE 4. Burn-in and life test circuits - Continued.



1.  $V_{CC} = 5$  volts, minimum, at the device terminals.
2. To other devices when testing in series.

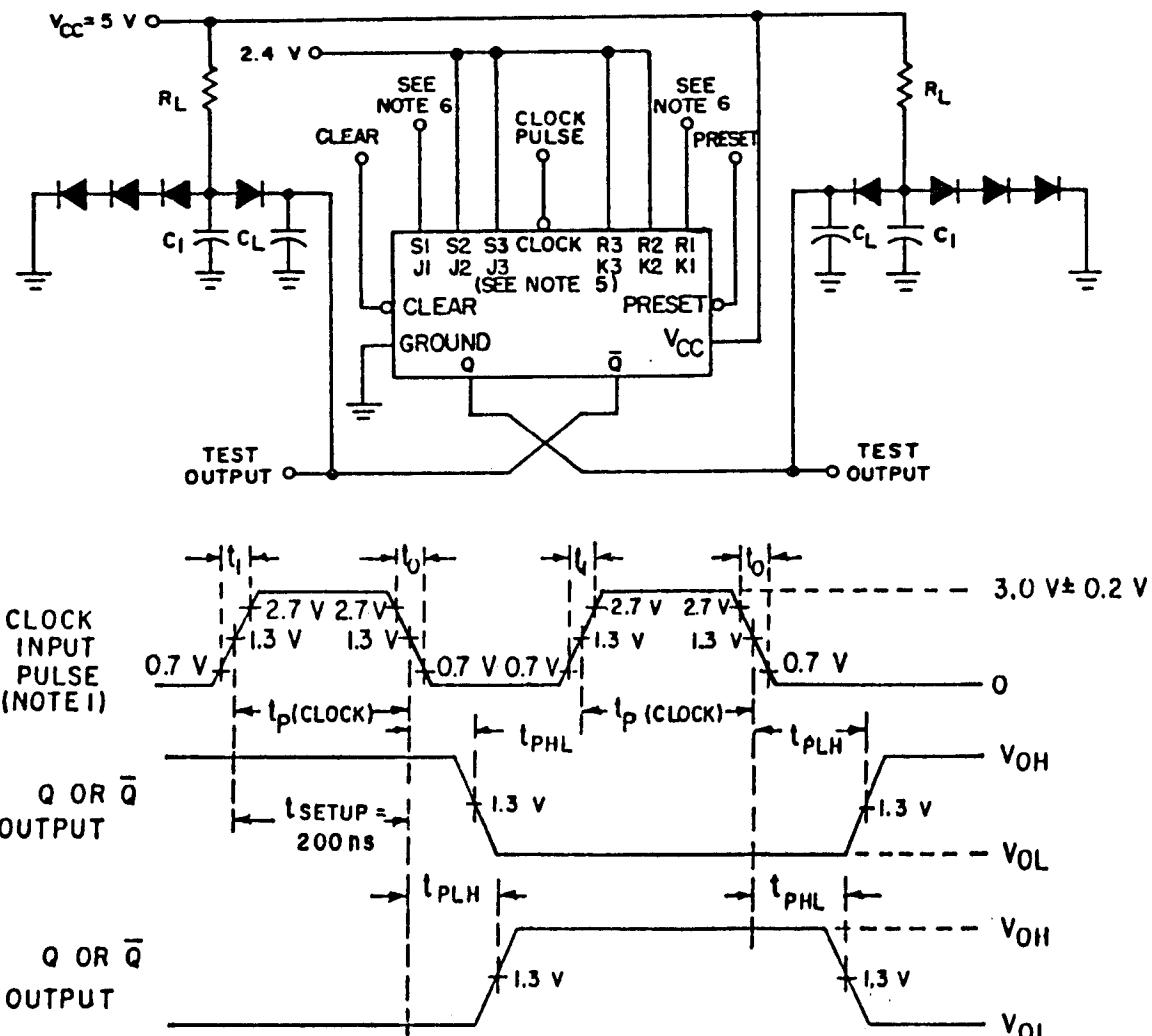
FIGURE 4. Burn-in and life test circuits - Continued.



## NOTES:

1. Clear or preset input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p$  (clear) =  $t_p$  (preset) = 100 ns, PRR = 0.5 MHz and  $Z_{out} \approx 50 \Omega$ .
2.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
3.  $R_L = 4 \text{ k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.
4. All diodes are 1N916 or equivalent.
5. R and S inputs apply for device type 01, J and K inputs apply for device type 02.
6. When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see Table III).1

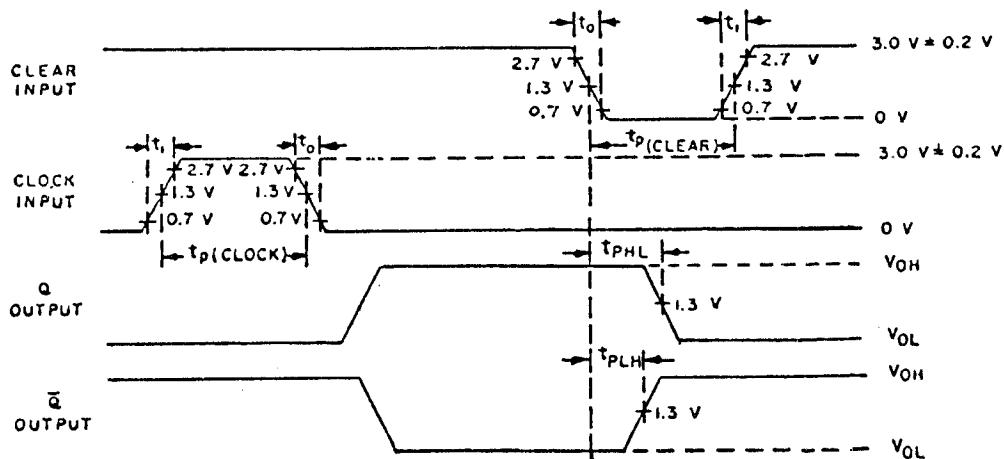
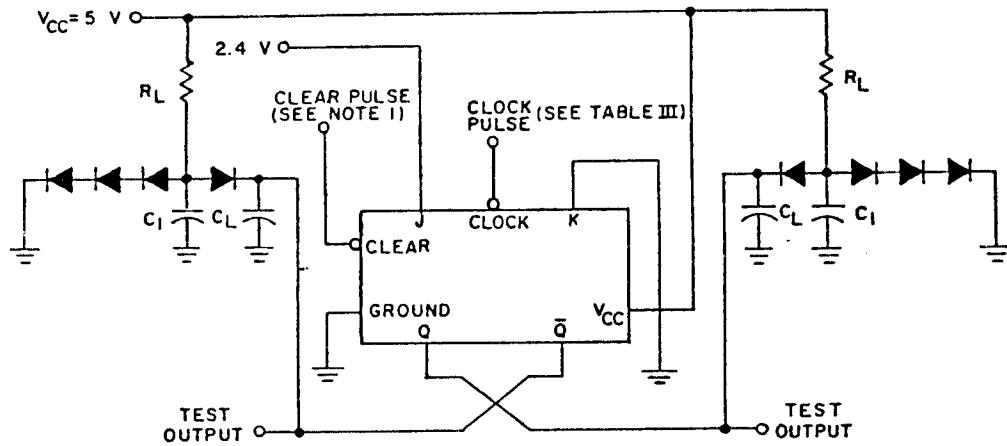
FIGURE 5. Clear and preset switching test circuit for device type 01 and 02.



## NOTES:

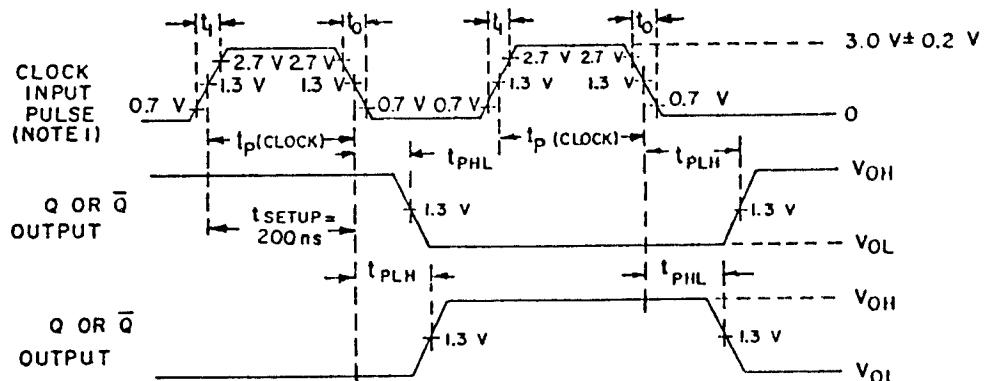
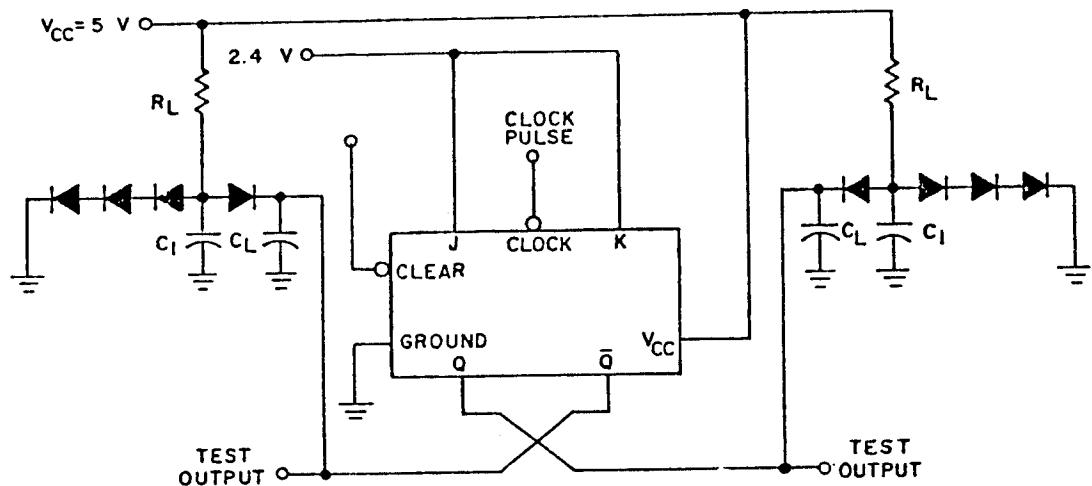
1. Clock input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p = 200 \text{ ns}$ , and PRR = 0.5 MHz.  
when testing  $F_{max}$ , PRR = see table III.
2. All diodes are 1N916 or equivalent.
3.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
4.  $R_L = 4\text{k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.
5. R and S inputs apply for device type 01, J and K inputs apply for device type 02.
6. RI input is connected to Q output, SI input is connected to  $\bar{Q}$  output. J1 and K1 inputs are connected to 2.4 V.

FIGURE 6. Synchronous switching test circuit for devices types 01 and 02.

**NOTES:**

1. Clear input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p(\text{clear}) = 100 \text{ ns}$ , PRR = 0.5 MHz and  $Z_{out} = 50\Omega$ .
2.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
3.  $R_L = 4 \text{ k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.
4. All diodes are 1N916 or equivalent.
5. Clock input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ ,  $t_p(\text{clock}) \geq 200 \text{ ns}$ , PRR = 0.5 MHz.

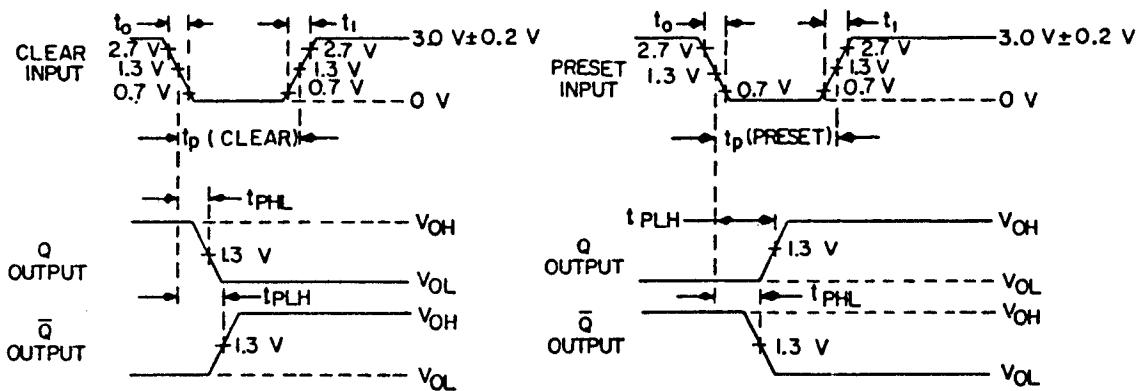
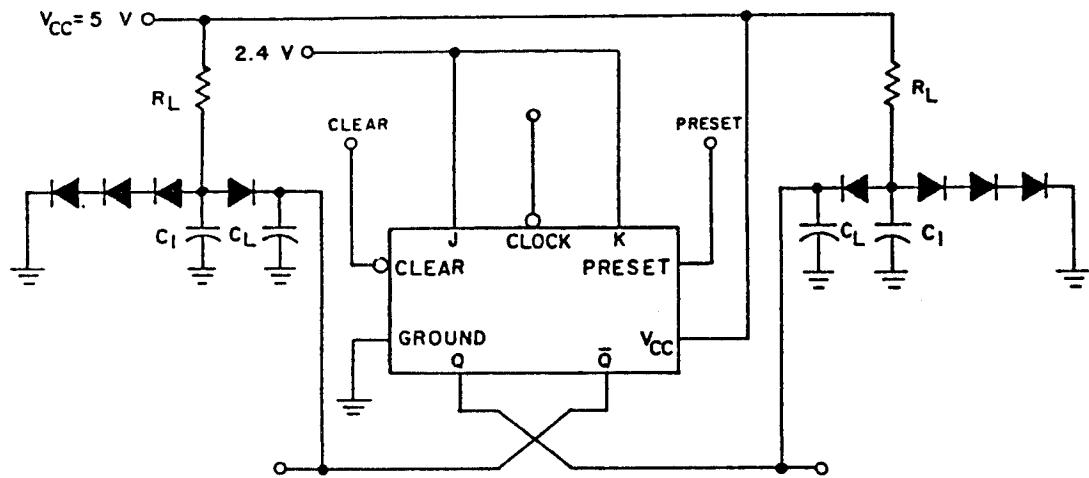
FIGURE 7. Clear switching test circuit for device type 03.



## NOTES:

1. Clock input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_P = 200 \text{ ns}$ , and  $PRR = 0.5 \text{ MHz}$ , when testing  $F_{max}$ ,  $PRR = \text{see table III}$ .
2. All diodes are 1N916 or equivalent.
3.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
4.  $R_L = 4 \text{ k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.

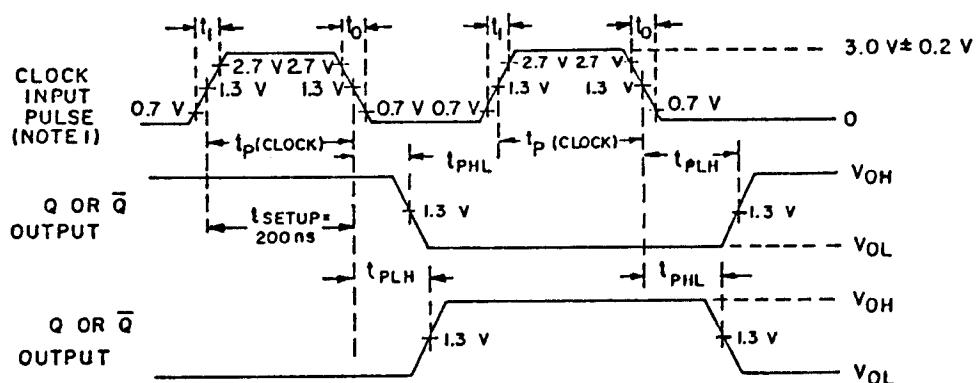
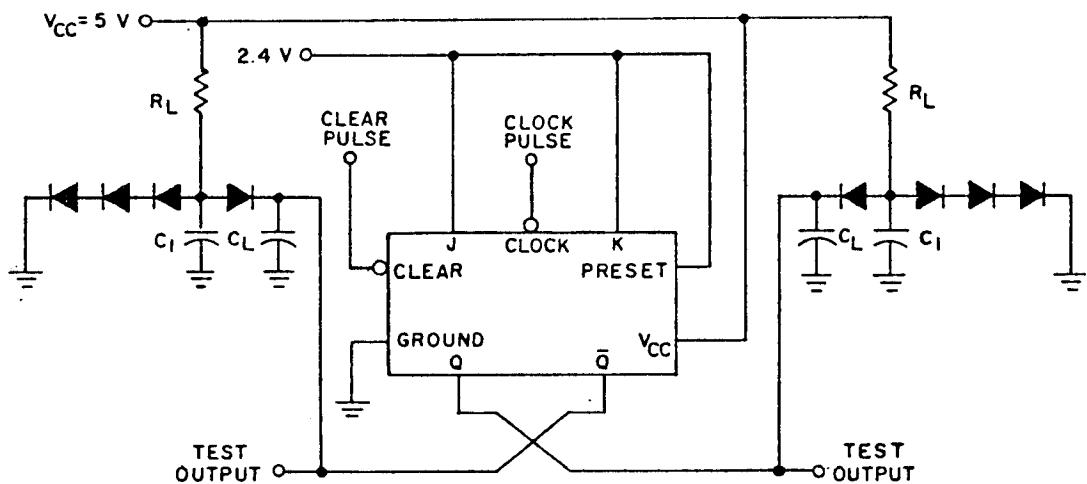
FIGURE 8 Synchronous switching test circuit for device type 03.



## NOTES:

1. Clear or preset input pulse characteristics:  $V_{gen} = 3.0 \text{ V}$   
 $\pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p (\text{Clear}) = t_p (\text{clear}) =$   
 $t_p (\text{preset}) = 100 \text{ ns}$ , PRR = 0.5 MHz and  $Z_{out} \approx 50\Omega$
2.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
3.  $R_L = 4 \text{ k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.
4. All diodes are 1N916 or equivalent.
5. When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see table III).

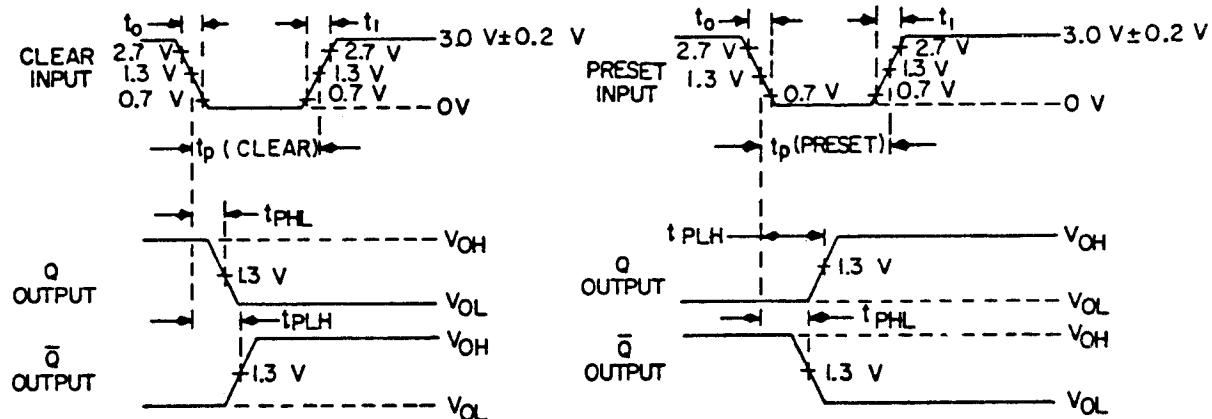
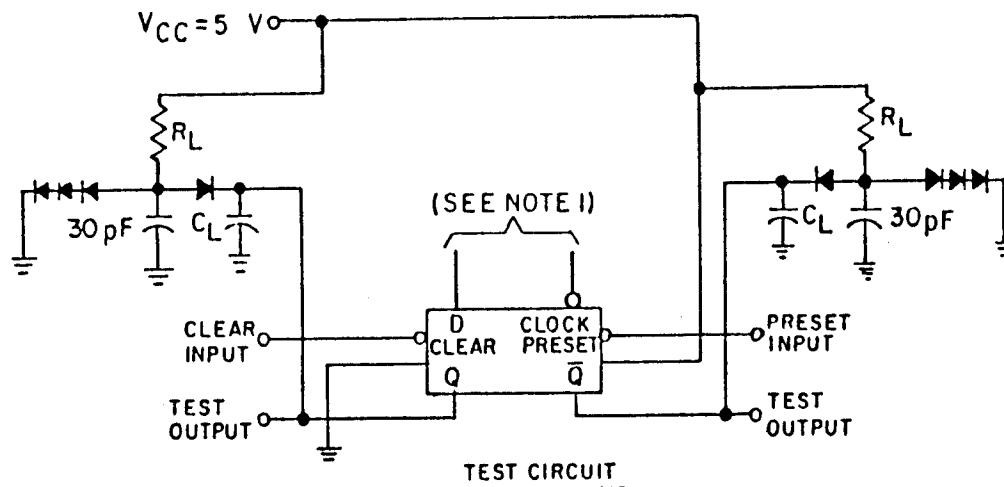
FIGURE 9. Clear and preset switching test circuit for device type 04.



## NOTES:

1. Clock input pulse characteristics:  $V_{gen} = 3.0 \text{ V} \pm 0.2\text{V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_p = 200 \text{ ns}$ , and  $\text{PRR} = 0.5 \text{ MHz}$ , when testing  $F_{max}$ ,  $\text{PRR} = \text{see table III}$ .
2. All diodes are 1N916 or equivalent.
3.  $C_L = 50 \text{ pF}$  minimum and includes probe and jig capacitance.
4.  $R_L = 4 \text{ k}\Omega \pm 5\%$  and  $C_1 = 30 \text{ pF}$  minimum.

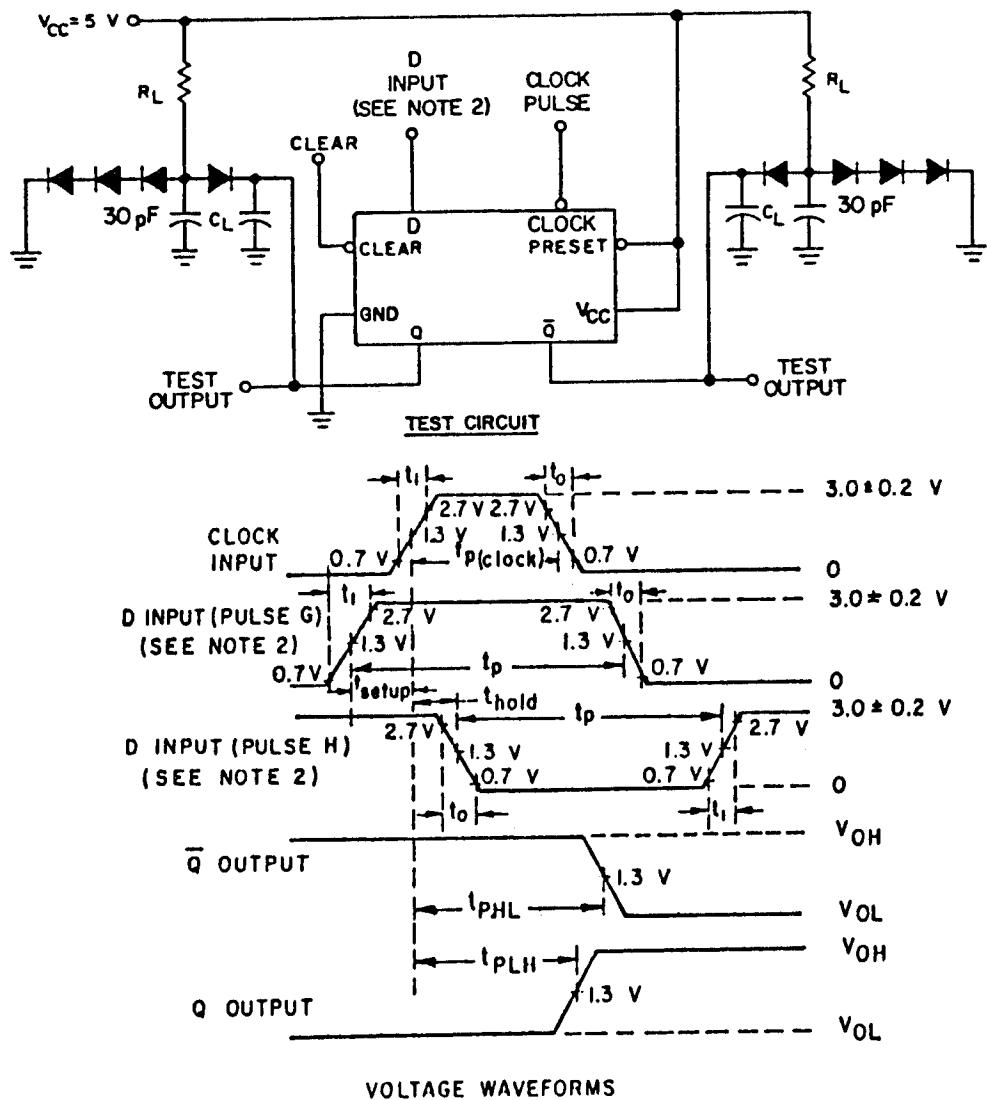
FIGURE 10. Synchronous switching test circuit for device type 04.



## NOTES:

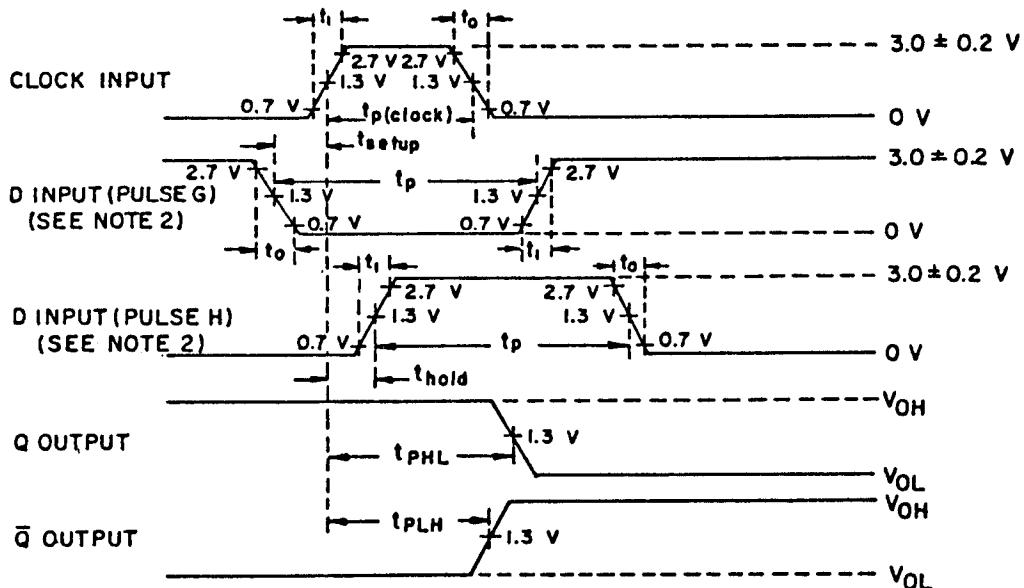
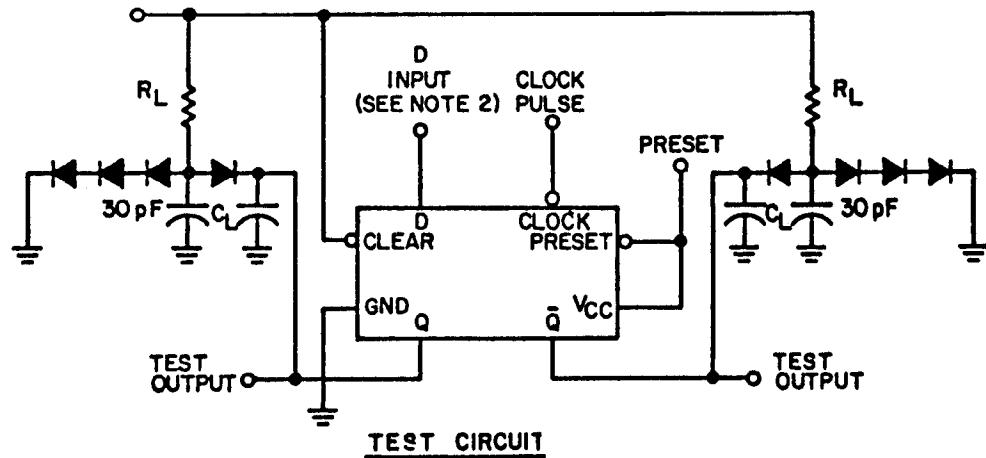
1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
2. All diodes are 1N916 or equivalent.
3. Clear or preset input pulse characteristics:  $V_{gen} = 3.0 \pm 0.2$  V,  $t_0 = 15$  ns,  $t_p = 100$  ns, PRR = 0.5 MHz.
4.  $C_L = 50$  pF minimum and includes probe and jig capacitance.
5.  $R_L = 4$  kΩ ± 5%.
6. When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see Table III).

FIGURE 11. Clear and preset switching test circuit and waveforms for device type 05.

**NOTES:**

1. Clock input pulse has the following characteristics:  
 $V_{gen} = 3.0 \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p = 200 \text{ ns}$ ,  
 and PRR = 0.5 MHz.  
 When testing  $F_{max}$ , PRR = see table III.
2. D input (pulse G) has the following characteristics:  
 $V_{gen} 3.0 \pm 0.2 \text{ V}$ ,  $t_0 = 15 \text{ ns}$ ,  $t_{\text{setup}} = 50 \text{ ns}$ ,  $t_1 = 15 \text{ ns}$ ,  
 $t_p = 100 \text{ ns}$ , and PRR is 50% of the clock PRR.
3. All diodes are 1N916 or equivalent.
4.  $C_L = 50 \text{ pf}$  Minimum and includes probe and jig capacitance.
5.  $R_L = 4k\Omega \pm 5\%$ .

FIGURE 12. Synchronous switching test circuit for device type 05.

**NOTES:**

1. Clock input pulse has the following characteristics:  $V_{gen} = 3.0 \pm 0.2$  V,  
 $t_0 = 15$  ns,  $t_p = 200$  ns, and PRR = 0.5 MHz. When testing  $F_{max}$ ,  
 PRR see table III.
2. D input (pulse G) has the following characteristics:  $V_{gen} = 3.0 \pm 0.2$  V,  
 $t_0 = 15$  ns,  $t_{setup} = 50$  ns,  $t_1 = 15$  ns,  $t_p = 100$  ns, and PRR is 50%  
 of the clock PRR. D input (pulse H) has the following characteristics:  
 $V_{gen} = 3.0 \pm 0.2$  V,  $t_0 = 15$  ns,  $t_{hold} = 0$  ns,  $t_1 = 15$  ns,  $t_p = 80$  ns  
 and PRR is 50% of the clock PRR.
3. All diodes are IN916 or equivalent.
4.  $C_L = 50$  pF minimum and includes probe and jig capacitance.
5.  $R_L = 4$  kΩ ± 5%.

FIGURE 13. Synchronous switching test circuit for device type 05.

TABLE III. Group A Inspection for device type 01. 1/

Subgroup	Symbol	Cases A, B, 0 MIL- STD-883 Method	Test no.	Case no.			Measured Terminal			Test Limits			Unit				
				R <sub>I</sub>	Clock	Preset	V <sub>CC</sub>	Clear	NC	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	Q	R <sub>2</sub>	R <sub>3</sub>	Min	Max
T <sub>C</sub> = 25°C	V <sub>OH</sub>	3006	1	0.7 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	2.4	Y
			2	2.0 V	A	4.5 V	4.5 V	4.5 V	0.7 V	0.7 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.4	Y
			3	4.5 V	A	4.5 V	0.7 V	-	2.0 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	-
			4	4.5 V	A	4.5 V	2.0 V	-	0.7 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	-
T <sub>C</sub> = -25°C	V <sub>OL</sub>	3007	5	2.0 V	A	4.5 V	-	4.5 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	0.3
			6	0.7 V	A	4.5 V	-	4.5 V	2.0 V	2.0 V	2 mA	2 mA	2 mA	2 mA	2 mA	2 mA	-
			7	4.5 V	A	4.5 V	0.7 V	-	2.0 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	-
			8	4.5 V	A	4.5 V	2.0 V	-	0.7 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	-
T <sub>C</sub> = 100°C	V <sub>IL1</sub>	3009	9	-	-	5.5 V	B	-	0.3 V	-	-	-	-	-	-	-	-
			10	-	-	-	-	-	4.5 V	0.3 V	-	-	-	-	-	-	-
			11	-	-	-	-	-	-	4.5 V	0.3 V	-	-	-	-	-	-
			12	0.3 V	-	-	B	-	-	-	-	-	-	-	-	-	-
			13	4.5 V	-	-	-	-	-	-	-	-	-	-	-	-	-
			14	-	-	-	-	-	-	-	-	-	-	-	-	-	-
T <sub>C</sub> = 100°C	V <sub>IL2</sub>	1010	15	-	0.3 V	-	-	-	8	-	-	-	-	-	-	-	-
			16	-	0.3 V	-	-	-	0.3 V	-	-	-	-	-	-	-	-
			17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
			18	-	-	-	-	-	-	-	-	-	-	-	-	-	-
T <sub>C</sub> = 100°C	V <sub>OH1</sub>	1010	19	GND	-	-	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
			20	GND	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			21	2.4 V	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			22	GND	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			23	2.4 V	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			24	GND	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
T <sub>C</sub> = 100°C	V <sub>OH2</sub>	1010	25	-	-	-	-	GND	-	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V
			26	-	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			27	5.5 V	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			28	GND	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			29	5.5 V	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
			30	GND	-	-	-	GND	-	GND	GND	GND	GND	GND	GND	GND	GND
T <sub>C</sub> = 100°C	V <sub>IL3</sub>	1010	31	GND	-	2.4 V	-	2.4 V	-	GND	GND	GND	GND	GND	GND	GND	GND
			32	GND	-	2.4 V	-	2.4 V	-	GND	GND	GND	GND	GND	GND	GND	GND
T <sub>C</sub> = 100°C	V <sub>IL4</sub>	1010	33	GND	-	5.5 V	-	5.5 V	-	GND	GND	GND	GND	GND	GND	GND	GND
			34	GND	-	5.5 V	GND	-	GND	GND	GND	GND	GND	GND	GND	GND	GND
			35	5.5 V	-	5.5 V	GND	-	GND	GND	GND	GND	GND	GND	GND	GND	GND
			36	GND	-	5.5 V	GND	-	GND	GND	GND	GND	GND	GND	GND	GND	GND
T <sub>C</sub> = 100°C	V <sub>IL10</sub>	1010	37	-	2.4 V	GND	-	GND	-	-	-	-	-	-	-	-	-
			38	-	2.4 V	GND	-	GND	-	-	-	-	-	-	-	-	-
T <sub>C</sub> = 100°C	V <sub>IL5</sub>	3011	39	4.5 V	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
			40	4.5 V	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
T <sub>C</sub> = 100°C	V <sub>CC</sub>	3005	41	Ckt A	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
			42	Ckt B	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
			43	Ckt A	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V
			44	Ckt B	GND	-	GND	-	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V

2 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = +125°C.3 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = -55°C.

See footnotes at end of device type 01.

TABLE III. Group A Inspection for device 01 - Continued. 1/  
2/

Subgroup	Symbol	Cases A, B, D Case C	MIL- STD-883J method	Test no.	R <sub>1</sub>	Clock	Preset	V <sub>CC</sub>	Clear	NC	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	Q	GND	Q	R <sub>2</sub>	R <sub>3</sub>	Measured terminal	Test limits	Unit
T <sub>C</sub> = +25°C				43	A	A	A	4.5 V	B		A	A	A	H	L	A	A	A	All outputs	H or L as shown 3/	
T <sub>C</sub> = 4/				44	B	B	B		A		B	B	B	L	H	L	L	L			
				45	A	A	A				B	B	B	L	H	L	L	L			
				46	A	A	A				A	A	A	L	H	L	L	L			
				47	B	B	B				B	B	B	L	H	L	L	L			
				48	A	A	A				B	B	B	L	H	L	L	L			
				49	B	B	B				A	A	A	L	H	L	L	L			
				50	A	A	A				B	B	B	L	H	L	L	L			
				51	B	B	B				A	A	A	L	H	L	L	L			
				52	A	A	A				B	B	B	L	H	L	L	L			
				53	B	B	B				A	A	A	L	H	L	L	L			
				54	A	A	A				B	B	B	L	H	L	L	L			
				55	B	B	B				A	A	A	L	H	L	L	L			
				56	A	A	A				B	B	B	L	H	L	L	L			
				57	B	B	B				A	A	A	L	H	L	L	L			
				58	A	A	A				B	B	B	L	H	L	L	L			
				59	A	A	A				B	B	B	L	H	L	L	L			

8 2/ 4/ Same tests, terminal conditions, and limits as for subgroup 7, except T<sub>C</sub> = +125°C and -55°C.

T <sub>C</sub> = +25°C	f <sub>MAX</sub>	f <sub>MIN</sub>	(Fig. 6)	60	0	IN	5.0 V	5.0 V	8	C	2.4 V	2.4 V	OUT	GND	OUT	2.4 V	2.4 V	OUT	2.4 V	2.4 V	Hz
t <sub>PL-H</sub>	1003	1(Fig. 5)	*62 CKT A	"	2.4 V	J	"	IN	J		"	"	OUT	OUT	"	"	"	"	"	"	
			*62 CKT B	"					J												
			*63 CKT A	"					IN	J											
			*63 CKT B	"					IN	J											
			64 CKT A	"					GND	J											
			64 CKT B	"					IN	J											
			65 CKT A	"					IN	J											
			65 CKT B	"					IN	J											
			66 CKT A	"					IN	J											
			66 CKT B	"					IN	J											
			67 CKT A	"					5.0 V	J											
			67 CKT B	"					5.0 V	J											
			68 CKT A	"					5.0 V	J											
			68 CKT B	"					5.0 V	J											
			69 CKT A	"					5.0 V	J											
			69 CKT B	"					5.0 V	J											

See footnotes at end of device type 01.



TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	ML-STD-883 method	Cases A, B, D		Cases C		Cases 1, 2		Cases 3		Cases 4		Cases 5		Cases 6		Cases 7		Cases 8		Cases 9		Cases 10		Cases 11		Cases 12		Cases 13		Cases 14		Measured terminal		Test limits		Unit
			Test no.	K1	Clock	Preset	V <sub>CC</sub>	Clear	NC	J1	J2	J3	Q	GND	Q	K2	X <sub>3</sub>	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max						
T <sub>C</sub> = +25°C	I <sub>OH</sub>	3006	1	0.7 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	-100 μA	0.7 V	0.7 V	0.7 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0					
		2	2.0 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	-100 μA	2.0 V	2.0 V	2.0 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0						
		3	4.5 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	-100 μA	4.5 V	4.5 V	4.5 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0						
		4	4.5 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	-100 μA	4.5 V	4.5 V	4.5 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0	2.4 V	0						
	I <sub>OL</sub>	3007	5	2.0 V	A	4.5 V	4	4.5 V	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	2 mA	2 mA	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0				
		6	0.7 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	2 mA	2 mA	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0					
		7	4.5 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	2 mA	2 mA	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0					
		8	4.5 V	A	4.5 V	4.5 V	4.5 V	2.0 V	2.0 V	2.0 V	0.7 V	0.7 V	2 mA	2 mA	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0	2 mA	0					
	I <sub>IL1</sub>	3009	9	*	*	*	5.5 V	B	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J1 -43 -140 uA			
		10	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J2 -43 -140 uA			
		11	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J3 -43 -140 uA			
		12	0.3 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J4 -43 -140 uA			
		13	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J5 -43 -140 uA			
		14	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	J6 -43 -140 uA			
	I <sub>IL2</sub>	15	*	0.3 V	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Clock -105 -360 uA			
		16	*	0.3 V	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Clock -105 -360 uA			
		17	*	0.3 V	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Clock -105 -360 uA			
		18	*	0.3 V	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Clock -105 -360 uA			
	I <sub>IH1</sub>	3010	19	*	GND	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J1 10 uA				
		20	*	GND	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J2 10 uA				
		21	*	2.4 V	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J3 10 uA				
		22	*	GND	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J4 10 uA				
		23	*	GND	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J5 10 uA				
		24	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J6 10 uA				
	I <sub>IH2</sub>	25	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J1 100 uA				
		26	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J2 100 uA				
		27	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J3 100 uA				
		28	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J4 100 uA				
		29	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J5 100 uA				
		30	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	J6 100 uA				
	I <sub>IH3</sub>	31	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clear Preset 20 uA				
		32	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	2.4 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clear Preset 20 uA				
	I <sub>IH4</sub>	33	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Preset 200 uA				
		34	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Preset 200 uA				
		35	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Preset 200 uA				
		36	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Preset 200 uA				
	I <sub>HD10</sub>	37	*	2.4 V	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clock 0 -200 uA				
		38	*	2.4 V	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clock 0 -200 uA					
	I <sub>OS</sub>	39	4.5 V	GND	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Q -3 -15 mA					
		40	4.5 V	GND	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Q -3 -15 mA					
	I <sub>CC</sub>	3005	41 CKT A	GND	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V <sub>CC</sub> 1.44 V					
		41 CKT B	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V <sub>CC</sub> 1.44 V					
		42 CKT A	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V <sub>CC</sub> 1.44 V					
		42 CKT B	*	*	*	*	*	*	*	*	*	*	*	*	*	*	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V <sub>CC</sub> 1.44 V					

See footnotes at end of device type 02.

2 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = +125°C.3 Same tests, terminal conditions and limits as for subgroup 1, except T<sub>C</sub> = -55°C.

TABLE III. Group A inspection for device 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases	A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits	Unit
			Case no.	Test no.	K <sub>1</sub>	Clock	Preset	V <sub>CC</sub>	Clear	NC	J <sub>1</sub>	J <sub>2</sub>	J <sub>3</sub>	Q	GND	0	K <sub>2</sub>	K <sub>3</sub>	Min	Max	H or L as shown 3/
7 T <sub>C</sub> = +25°C 2/ 4/			43	B	A	B	A	4.5 V	B	B	B	B	B	L	3/	8	B	All outputs	"	"	
			44	B	A	B	A							H	3/	8	A	"	"	"	
			45	B	A	B	A							H	3/	8	A	"	"	"	
			46	B	A	B	A							H	3/	8	A	"	"	"	
			47	B	A	B	A							H	3/	8	A	"	"	"	
			48	A	B	A	B							H	3/	8	A	"	"	"	
			49	B	A	B	A							H	3/	8	A	"	"	"	
			50	B	A	B	A							H	3/	8	A	"	"	"	
			51	B	A	B	A							H	3/	8	A	"	"	"	
			52	B	A	B	A							H	3/	8	A	"	"	"	
			53	B	A	B	A							H	3/	8	A	"	"	"	
			54	B	A	B	A							H	3/	8	A	"	"	"	
			55	B	A	B	A							H	3/	8	A	"	"	"	
			56	B	A	B	A							H	3/	8	A	"	"	"	
			57	B	A	B	A							H	3/	8	A	"	"	"	
			58	B	A	B	A							H	3/	8	A	"	"	"	
			59	B	A	B	A							H	3/	8	A	"	"	"	
			60	B	A	B	A							H	3/	8	A	"	"	"	
			61	B	A	B	A							H	3/	8	A	"	"	"	
			62	B	A	B	A							H	3/	8	A	"	"	"	
			63	B	A	B	A							H	3/	8	A	"	"	"	
			64	B	A	B	A							H	3/	8	A	"	"	"	
			65	B	A	B	A							H	3/	8	A	"	"	"	
			66	B	A	B	A							H	3/	8	A	"	"	"	
			67	B	A	B	A							H	3/	8	A	"	"	"	
			68	B	A	B	A							H	3/	8	A	"	"	"	
			69	B	A	B	A							H	3/	8	A	"	"	"	
			70	B	A	B	A							H	3/	8	A	"	"	"	
			71	B	A	B	A							H	3/	8	A	"	"	"	
			72	B	A	B	A							H	3/	8	A	"	"	"	
			73	B	A	B	A							H	3/	8	A	"	"	"	
			74	B	A	B	A							H	3/	8	A	"	"	"	
			75	B	A	B	A							H	3/	8	A	"	"	"	
			76	B	A	B	A							H	3/	8	A	"	"	"	
			77	B	A	B	A							H	3/	8	A	"	"	"	
			78	B	A	B	A							H	3/	8	A	"	"	"	
			79	B	A	B	A							H	3/	8	A	"	"	"	
			80	B	A	B	A							H	3/	8	A	"	"	"	
			81	B	A	B	A							H	3/	8	A	"	"	"	

8 2/3/4 Same tests, terminal conditions, and limits as for subgroup 7, except T<sub>C</sub> = +125°C and -55°C

See footnotes at end of device type 02.

TABLE III. Group A inspection for device 02 - Continued. 1/

Terminal 11/ Terminal 11 conditions (pins not designated may be H > 2.0 V, or L  $\leq$  0.8 V, or open).

2/ Tests shall be performed in sequence;

Output voltages shall be either 120 or 240 V. Minimum and maximum values shall be as follows:

speed checker double comparator; or (b)  $n \geq 1.3$  v. when using a single speed checker double comparator.

about voltages shown are:  $A = -0.1 \text{ V minimum and } B = 0.4 \text{ V maximum.}$

$f_{\text{MAX}}$ , minimum limit specified is the frequency of the input pulse. The output free pulse.

— Be one-half of the input frequency.

\* These tests are performed at device manufacturer's option.

TABLE III  
Group A insulation for devine type 03. 1/

Subgroup	Symbol	Cases A <sub>2</sub> , b, D C <sub>2</sub> , Sc	Measured limits												Test limits terminal	Unit		
			Milli- STD-883j				V <sub>C</sub>				Clock Z <sub>t</sub> Clear 2 <sub>t</sub> J <sub>2</sub>							
			Test no.	Clock 1	Clear 1	K <sub>1</sub>	V <sub>C</sub>	Clock 2	Clear 2	J <sub>2</sub>	Q <sub>2</sub>	Q <sub>0</sub>	K <sub>2</sub>	Q <sub>1</sub>	J <sub>1</sub>	M <sub>H</sub>	M <sub>A</sub>	
T <sub>C</sub> = +25°C	V <sub>UL</sub>	3006	1	A	4.5 V	0.7 V	4.5 V							GND	-100 μA	2.0 V	Q <sub>1</sub>	2.4 V
			2	A	4.5 V	2.0 V									-100 μA	0.7 V	Q <sub>1</sub>	
			3	A	4.5 V	0.7 V	4.5 V								-100 μA	4.5 V	Q <sub>1</sub>	
			4	A	4.5 V	0.7 V									-100 μA	0.7 V	Q <sub>2</sub>	
			5	A	4.5 V	0.7 V									-100 μA	4.5 V	Q <sub>2</sub>	
			6	A	4.5 V	0.7 V									-100 μA	2.0 V	Q <sub>2</sub>	
			7	A	4.5 V	2.0 V									2 mA	0.7 V	Q <sub>1</sub>	0.3 V
			8	A	4.5 V	0.7 V	4.5 V								2 mA	2.0 V	Q <sub>1</sub>	
			9	A	4.5 V	0.7 V									4.5 V		Q <sub>2</sub>	
			10	A	4.5 V	0.7 V											Q <sub>2</sub>	
			11	A	4.5 V	0.7 V												
			12	A	4.5 V	0.7 V												
I <sub>IL1</sub>	3009	13	A	4.5 V	4.5 V	0.3 V	5.5 V							E	0.3 V	J <sub>1</sub>	-43	μA
			14	A	4.5 V	4.5 V	0.3 V							E	0.3 V	J <sub>1</sub>		
			15	A	4.5 V	0.3 V								E	0.3 V	J <sub>2</sub>		
			16	A	4.5 V	0.3 V								E	0.3 V	K <sub>2</sub>		
I <sub>IL2</sub>	3010	17	A	4.5 V	0.3 V	0.3 V								4.5 V	Clear 1	-86		
			18	A	4.5 V	0.3 V	0.3 V							4.5 V	Clock 1	-120		
			19	A	4.5 V	0.3 V	0.3 V							4.5 V	Clear 2	-86		
			20	A	4.5 V	0.3 V	0.3 V							4.5 V	Clock 2	-120		
I <sub>IL3</sub>	3010	21	GND	GND	B	2.4 V									2.4 V	J <sub>1</sub>	10	
			22	GND	GND	B	2.4 V									J <sub>1</sub>		
			23	GND	GND	B	2.4 V									J <sub>2</sub>		
			24	GND	GND	B	2.4 V									K <sub>2</sub>		
I <sub>IL4</sub>	3010	25	GND	GND	B	5.5 V									5.5 V	J <sub>1</sub>	10	
			26	GND	GND	B	5.5 V									J <sub>1</sub>		
			27	GND	GND	B	5.5 V									J <sub>2</sub>		
			28	GND	GND	B	5.5 V									K <sub>2</sub>		
I <sub>IL5</sub>	3010	29	GND	2.4 V											GND	Clear 1	20	
			30	GND	2.4 V											Clear 2	20	
I <sub>IL6</sub>	3010	31	5.5 V	GND	5.5 V										GND	Clock 1	20	
			32	5.5 V	GND	5.5 V										Clock 2	20	
			33	5.5 V	GND	5.5 V										Clear 1	20	
			34	5.5 V	GND	5.5 V										Clear 2	20	
I <sub>IL7</sub>	3010	35	2.4 V	GND	GND										GND	Clock 1	0	
			36	2.4 V	GND	GND										Clock 2	0	
I <sub>CC</sub>	3011	37	2.4 V	A	2.4 V										2.4 V	Q <sub>1</sub>	-3	mA
			38	2.4 V	GND										2.4 V	Q <sub>1</sub>		
			39	2.4 V	GND										2.4 V	Q <sub>2</sub>		
			40	2.4 V	GND										2.4 V	Q <sub>2</sub>		
I <sub>CC</sub>	3011	41	CKT A	F	4.5 V	GND									4.5 V	V <sub>CC</sub>	3.6 V	
			42	CKT B	F	4.5 V	GND								4.5 V	GND	2.88 V	
			43	CKT A	F	4.5 V	GND								4.5 V	GND	3.8 V	
			44	CKT B	F	4.5 V	GND								4.5 V	GND	2.88 V	

2 Same tests, terminal conditions and limits as for subgroup 1, except  $T_C = 125^\circ C$ .

3 Same tests, terminal conditions and limits as for subgroup 1, except  $T_C = -55^\circ C$ .

See footnotes at end of device type 03.

TABLE III. Group A inspection for device 03 - Continued. 1/  
2/

Subgroup	Symbol	MIL- Method S10-8831	Cases	A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits	Unit
			Mil- Case C	no.	Test	Clock 1	Clear 1	K1	V <sub>CC</sub>	Clock 2	Clear 2	J <sub>2</sub>	Q <sub>2</sub>	K <sub>2</sub>	GND	Q <sub>1</sub>	J <sub>1</sub>	U <sub>1</sub>	J <sub>1</sub>	Min	Max
7		$T_C = +25^\circ C$	43	B	B	B	4.5 V	8	B	A	H	J/	L	3/	B	H	3/	A	All outputs	H or L as shown 3/	
2/ 4/			44	A	B	B			B												
			45	B	A	B			B												
			46	B	A	A			B												
			47	A																	
			48	B	A																
			49	B	A																
			50	A																	
			51	B	A	B			B												
			52	A	B	A			B												
			53	B	A	B			B												
			54	A	B	A			B												
			55	B	B	B			B												
			56	B	B	B			B												
			57	A	B	B			B												
			58	B	B	B			B												
			59	A	B	A			A												
			60	B	A	B			A												
			61	A	B	A			A												
			62	B	A	B			A												
			63	B	A	B			A												
			64	A	B	A			A												
			65	B	A	B			B												
			66	B	A	B			B												
			67	A	B	A			A												
			68	B	B	A			B												
			69	B	A	B			A												
			70	A	B	A			B												
			71	B	A	B			A												
			72	B	A	B			B												
			73	A	B	A			A												
			74	B	A	B			B												
			75	A	B	A			A												
			76	B	A	B			B												
			77	B	A	B			A												
			78	B	B	A			B												
			79	A	B	A			A												
			80	A	B	A			B												
			81	B	A	B			A												

8 2/ 4/ Same tests, terminal conditions, and limits as for subgroup 7, except  $T_C = +125^\circ C$  and  $-55^\circ C$ .

See footnotes at end of device type 03.

TABLE III. Group A inspection for device 03 - Continued. 1/

Subgroup	Symbol	Mil-STD-883J method	Cases A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits	Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			
			Test no.	Clock 1	Clear 1	K1	VCC	Clock 2	Clear 2	J2	Q2	K2	GND	Q1	Q1	J1				
$T_C = +25^\circ\text{C}$	$f_{MAX} \leq 5\text{ (Fig. 8)}$		82	IN	B	2.4 V	5.0 V			IN	B	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock/Q1	3	MHz
			83	IN	B	2.4 V				IN	B	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock/Q1	3	n.s.
			84															Clock/Q2	50	n.s.
			85															Clock/Q2	50	n.s.
			3003	*9b CKT A	IN	GND												Clear/Q1	10	ns
			(Fig. 7)	*9b CKT B	IN	GND												Clear/Q1	50	n.s.
				*8b CKT A														Clear/Q2	75	n.s.
				*8b CKT B														Clear Q2	50	n.s.
			tpHL	86 CKT A	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear/Q1	200	n.s.
				88 CKT B	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear/Q1	90	n.s.
				89 CKT A														Clear/Q2	200	n.s.
				89 CKT B														Clear/Q2	90	n.s.
				90 CKT A	IN	J	2.4 V			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock/Q1	150	n.s.
				3003	90 CKT B	J	*											Clock/Q1	150	n.s.
			(Fig. 8)	91 CKT A	*	*	*											Clock/Q1	150	n.s.
				91 CKT B	*	*	*											Clock/Q1	70	n.s.
			tpHL	92 CKT A	*	*	*											Clock1/Q1	75	n.s.
				92 CKT B	*	*	*											Clock1/Q1	50	n.s.
				93 CKT A	*	*	*											Clock1/Q1	75	n.s.
				93 CKT B	*	*	*											Clock1/Q1	50	n.s.
				94 CKT A	*	*	*											Clock2/Q2	75	n.s.
				94 CKT B	*	*	*											Clock2/Q2	50	n.s.
				95 CKT A	*	*	*											Clock2/Q2	75	n.s.
				95 CKT B	*	*	*											Clock2/Q2	50	n.s.
			tpHL	96 CKT A	*	*	*											Clock2/Q2	150	n.s.
				96 CKT B	*	*	*											Clock2/Q2	70	n.s.
				97 CKT A	*	*	*											Clock2/Q2	150	n.s.
				97 CKT B	*	*	*											Clock2/Q2	70	n.s.
				104 CKT A	*	*	*											Clock1/Q1	150	n.s.
$T_C = +125^\circ\text{C}$	$f_{MAX} \leq 5\text{ (Fig. 8)}$		98	IN	B	2.4 V				IN	B	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock1/Q1	2.5	MHz
			99	IN	B	2.4 V				IN	B	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock1/Q1	65	n.s.
			100															Clock1/Q2	125	n.s.
			101															Clock1/Q2	65	n.s.
			tpHL	102 CKT A	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear1/Q1	10	ns
				102 CKT B	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear1/Q1	10	ns
				103 CKT A	*	*	*											Clear2/Q2	250	n.s.
				103 CKT B	*	*	*											Clear2/Q2	250	n.s.
				104 CKT A	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear1/Q1	100	n.s.
				104 CKT B	IN	IN	GND			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clear1/Q1	100	n.s.
				105 CKT A	*	*	*											Clear2/Q2	200	n.s.
				105 CKT B	*	*	*											Clear2/Q2	200	n.s.
				106 CKT A	IN	J	2.4 V			IN	IN	2.4 V	OUT	OUT	2.4 V	OUT	2.4 V	Clock1/Q1	85	n.s.
				106 CKT B	J	*	*											Clock1/Q1	200	n.s.
				3003	107 CKT A	*	*											Clock1/Q1	85	n.s.
			(Fig. 8)	107 CKT B	*	*	*											Clock1/Q1	85	n.s.

See footnotes at end of device type 03.

TABLE III. Group A inspection for device 03 - Continued. 1/

Subgroup	Symbol	MIL-STD-883C method	Cases												Measured terminal	Test limits	Unit
			A, B, 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
10 $T_C = +125^\circ C$	$t_{PLH}$ (Fig. 6)	3003	108 CKT A 108 CKT B 109 CKT A 109 CKT B 110 CKT A 110 CKT B 111 CKT A 111 CKT B	IN IN IN IN IN IN IN IN	J J J J J J J J	2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V	5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V										
	$t_{PHL}$		112 CKT A 112 CKT B 113 CKT A 113 CKT B														
11	Same tests, terminal conditions, and limits as for subgroup 10, except $T_C = -35^\circ C$ .																

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V, E = momentary GND, then open, F = momentary 4.5 V, then GND. J = input pulse  $t_p \geq 100$  ns, PH = 0.5 MHz, VOL = 0 V,  $V_{OH} = 4.5$  V.

1/ Terminal conditions (pins not designated may be H  $\geq$  2.0 V, or L  $\leq$  0.8 V, or open).

2/ Tests shall be performed in sequence.  
3/ Output voltages shall be either: (a) H  $\geq$  2.4 V, minimum and L  $\leq$  0.4 V, maximum when using a high speed checker double comparator; or (b) H  $\geq$  1.5 V and L  $\leq$  1.5 V when using a high speed checker single comparator.

4/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.

5/ MAX minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

\* These tests are performed at device manufacturer's option.

\*\* Test time limit  $\leq 100$  ns.

TABLE III. Group A Inspection for device type 04. 1/

Subgroup	Symbol	Test No.	Cases A, B, D				Cases C				Measured Terminal				Test Limits			
			MIL-STD-883	C	1	2	3	4	5	6	7	8	9	10	11	12	13	
			Method	Test	Clock	[Preset 1]	U1	VCC	Clear	[Preset 2]	K2	Q2	Q1	J2	GND	Q1	K1	
1 TC = +25°C	V <sub>DH</sub>	3006	1	A	4.5 V	2.0 V	4.5 V	4.5 V	-	-	-	-	-	GND	-100 $\mu$ A	0.7 V	Q1 Q2	
			2	A	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	GND	-100 $\mu$ A	2.0 V	Q1 Q2	
			3	A	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	GND	-100 $\mu$ A	4.5 V	Q1 Q2	
			4	A	4.5 V	4.5 V	4.5 V	4.5 V	-	-	-	-	-	GND	-100 $\mu$ A	4.5 V	Q1 Q2	
			5	A	-	-	-	-	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	Q1 Q2
			6	A	-	-	-	-	4.5 V	4.5 V	4.5 V	-	-	-	-	-	-	Q1 Q2
			7	A	-	-	-	-	4.5 V	4.5 V	4.5 V	-	-	-	-	-	-	Q1 Q2
			8	A	-	-	-	-	4.5 V	4.5 V	4.5 V	-	-	-	-	-	-	Q1 Q2
V <sub>OL</sub>	V <sub>OL</sub>	3007	9	-	4.5 V	0.7 V	-	-	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			10	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			11	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			12	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			13	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			14	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			15	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
			16	-	4.5 V	0.7 V	4.5 V	4.5 V	-	-	-	-	-	-	-	2 mA	2.0 V	Q1 Q2
I <sub>IL1</sub>	I <sub>IL1</sub>	3009	17	4.5 V	0.3 V	5.5 V	-	GND	GND	GND	GND	GND	GND	GND	-	E	0.3 V	J1 J2
			18	-	GND	GND	-	-	-	-	-	-	-	-	-	E	0.3 V	J1 J2
			19	-	GND	GND	-	-	-	-	-	-	-	-	-	E	0.3 V	J1 J2
			20	-	GND	GND	-	-	-	-	-	-	-	-	-	E	0.3 V	J1 J2
			21	4.5 V	0.3 V	-	-	-	0.3 V	4.5 V	-	-	-	-	-	4.5 V	Preset 1 Preset 2	-86 -86
			22	4.5 V	0.3 V	-	-	-	0.3 V	4.5 V	-	-	-	-	-	4.5 V	Preset 1 Preset 2	-86 -86
			23	0.3 V	4.5 V	-	B	0.3 V	-	4.5 V	-	-	-	-	-	4.5 V	Clock Clock	-560 -560
			24	0.3 V	4.5 V	-	B	0.3 V	-	4.5 V	-	-	-	-	-	4.5 V	Clear Clear	-172 -172
I <sub>IL2</sub>	I <sub>IL2</sub>	3010	25	GND	3	2.4 V	-	GND	B	GND	B	2.4 V	-	-	-	2.4 V	J1 J2	10 10
			26	GND	4	2.4 V	-	GND	B	GND	B	2.4 V	-	-	-	2.4 V	J1 J2	10 10
			27	GND	5	2.4 V	-	GND	B	GND	B	2.4 V	-	-	-	2.4 V	J1 J2	10 10
			28	GND	6	2.4 V	-	GND	B	GND	B	2.4 V	-	-	-	2.4 V	J1 J2	10 10
			29	B	5.5 V	-	GND	B	GND	B	5.5 V	-	-	-	-	5.5 V	J1 J2	100 100
			30	B	5.5 V	-	GND	B	GND	B	5.5 V	-	-	-	-	5.5 V	J1 J2	100 100
			31	B	5.5 V	-	GND	B	GND	B	5.5 V	-	-	-	-	5.5 V	J1 J2	100 100
			32	B	5.5 V	-	GND	B	GND	B	5.5 V	-	-	-	-	5.5 V	J1 J2	100 100
I <sub>IL3</sub>	I <sub>IL3</sub>	33	-	2.4 V	-	-	-	-	2.4 V	-	-	-	-	-	-	-	-	-
			34	-	2.4 V	-	-	-	2.4 V	-	-	-	-	-	-	-	-	-
			35	-	5.5 V	-	-	-	5.5 V	-	-	-	-	-	-	-	-	-
			36	-	5.5 V	-	-	-	5.5 V	-	-	-	-	-	-	-	-	-
			37	-	GND	GND	-	-	2.4 V	-	-	-	-	-	-	-	-	-
			38	-	GND	GND	-	-	5.5 V	-	-	-	-	-	-	-	-	-
			39	-	2.4 V	-	-	-	GND	-	-	-	-	-	-	-	-	-
			40	-	5.5 V	-	-	-	GND	-	-	-	-	-	-	-	-	-
I <sub>IL4</sub>	I <sub>IL4</sub>	3011	41	4.5 V	GND	4.5 V	-	GND	GND	GND	GND	4.5 V	-	-	-	4.5 V	J1 J2	100 100
			42	-	GND	GND	-	-	-	-	-	-	-	-	-	4.5 V	J1 J2	100 100
			43	-	GND	GND	-	-	-	-	-	-	-	-	-	4.5 V	J1 J2	100 100
			44	-	GND	GND	-	-	-	-	-	-	-	-	-	4.5 V	J1 J2	100 100

See footnotes at end of device type 04.

TABLE III. Group A Inspection for device 04 - Continued. 1/

Subgroup	Symbol	Mil-Std-883C Method	Cases												Measured terminal	Test limits	Unit	
			A	B	C	1	2	3	4	5	6	7	8	9	10	11	12	13
1	I <sub>CC</sub> = +25°C	3005	45 CKT A	GND	4.5 V	GND	5.5 V	GND	4.5 V	GND	4.5 V	GND	GND	GND	GND	V <sub>CC</sub>	3.80 mA	
		45 CKT B			4.5 V												3.88 mA	
		46 CKT A			GND												3.80 mA	
		46 CKT B			GND												2.88 mA	
2 Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = +125°C.																		
3 Same tests, terminal conditions and limits as for subgroup 1, except T <sub>C</sub> = -55°C.																		
7 T <sub>C</sub> = +25°C 2/ 4/	tpLd	47	A	b	A	b	4.5 V	A	b	A	b	A	b	Q40	L 3J	H 3J	A	All outputs as shown 3/
		48	A	b	A	b												
		49	B	b	A	b												
		50	A	b	A	b												
		51	b	b	A	b												
		52	A	b	A	b												
		53	b	b	A	b												
8 2/ 4/	tpLd	54	A	b	A	b												
		55	b	b	A	b												
		56	A	b	A	b												
		57	b	b	A	b												
		58	IN	2.4 V	2.4 V	5.0 V	b		2.4 V	2.4 V	OUT	2.4 V		GND	OUT	OUT	2.4 V	Clock/Q <sub>1</sub>
		59	IN	2.4 V	2.4 V		b		2.4 V	2.4 V	OUT	2.4 V			OUT	OUT	2.4 V	Clock/Q <sub>2</sub>
		60	*	*	*	*	*	*	2.4 V	2.4 V	OUT	2.4 V						MHz
9 T <sub>C</sub> = +25°C 5/	tpLd	61	*	*	*	*	*	*	2.4 V	2.4 V	OUT	2.4 V						*
		62	CKT A	2.4 V	J	2.4 V	*	*	IN	*	*	*	*					
		63	CKT B	*	*	*	*	*	IN	*	*	*	*					
		64	CKT A	*	*	*	*	*	IN	J	2.4 V	*	*					
		64	CKT B	*	*	*	*	*	IN	J	2.4 V	*	*					
		65	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		65	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
66 tpLd	tpLd	66	CKT A	GND	J	2.4 V	*	*	IN	*	*	*	*					
		66	CKT B	*	*	*	*	*	IN	*	*	*	*					
		67	LKT A	*	*	*	*	*	IN	*	*	*	*					
		67	LKT B	*	*	*	*	*	IN	*	*	*	*					
		68	CKT A	*	*	*	*	*	IN	J	2.4 V	*	*					
		68	CKT B	*	*	*	*	*	IN	J	2.4 V	*	*					
		69	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
70 tpLd	tpLd	69	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		70	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		71	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		71	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		72	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		72	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		73	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
74 tpLd	tpLd	73	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		74	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		75	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		75	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		76	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
		76	CKT B	*	*	*	*	*	IN	*	OUT	*	*					
		77	CKT A	*	*	*	*	*	IN	*	OUT	*	*					
See footnotes at end of device type 04.																		

TABLE III. Group A inspection for device 04 - Continued. 1/

Subgroup	Symbol	Cases A,B,D Case C	Test no.	Measured limits										Test limits	Unit			
				1	2	3	4	5	6	7	8	9	10	11	12	13		
MIL-STD-883 method	t <sub>PHL</sub> $T_C = +25^\circ C$	74 CKT A (Fig. 10) 75 CKT A 76 CKT A 77 CKT B 78 CKT A 79 CKT B 80 CKT A 81 CKT B	3003	74 CKT A IN 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V	74 CKT A IN 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V 2.4 V	2.4 V =	5.0 V =	4.5 V =	4.5 V =	4.5 V =	4.5 V =	2.4 V =	2.4 V =	GND	Q <sub>1</sub>	Q <sub>1</sub>		
			10	t <sub>MAX</sub> $T_C = +125^\circ C$	51 (Fig. 10)	78 CKT A 79 CKT B 80 CKT A 81 CKT B	2.4 V 2.4 V 2.4 V 2.4 V	2.4 V 2.4 V 2.4 V 2.4 V	2.4 V =	2.4 V =	OUT	OUT	2.4 V =					
	t <sub>PHL</sub> $T_C = +25^\circ C$	*82 CKT A *82 CKT B *83 CKT A *83 CKT B *84 CKT A *84 CKT B *85 CKT A *85 CKT B	3003 (Fig. 9)	*82 CKT A 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	*82 CKT B 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	J =	J =	J =	J =	J =	J =	J =	J =	OUT	OUT	2.4 V =		
				86 CKT A 86 CKT B 87 CKT A 87 CKT B	86 CKT B 2.4 V IN 2.4 V IN	J =	J =	J =	J =	J =	J =	J =	J =	OUT	OUT	2.4 V =		
	t <sub>PHL</sub>	87 CKT B 88 CKT A 88 CKT B 89 CKT A 89 CKT B		87 CKT B IN 2.4 V IN 2.4 V IN	88 CKT A IN 2.4 V IN 2.4 V IN	=	J =	J =	J =	J =	J =	J =	J =	OUT	OUT	2.4 V =		
				90 CKT A 90 CKT B 91 CKT A 91 CKT B 92 CKT A 92 CKT B 93 CKT A 93 CKT B	90 CKT A 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	J =	J =	J =	J =	J =	J =	J =	J =	GND	Q <sub>1</sub>	Q <sub>1</sub>		
	t <sub>PHL</sub> $T_C = -55^\circ C$	94 CKT A 94 CKT B 95 CKT A 95 CKT B 96 CKT A 96 CKT B 97 CKT A 97 CKT B	3003 (Fig. 10)	94 CKT A 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	94 CKT B 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	J =	J =	J =	J =	J =	J =	J =	J =	OUT	OUT	2.4 V =		
				98 CKT A 98 CKT B 99 CKT A 99 CKT B 100 CKT A 100 CKT B 101 CKT A 101 CKT B	98 CKT B 2.4 V IN 2.4 V IN 2.4 V IN 2.4 V IN	J =	J =	J =	J =	J =	J =	J =	J =	OUT	OUT	2.4 V =		

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V, E = momentary GND, then open,  
 Y = input pulse,  $V_{in} = 0$  V,  $V_{oh} = 4.5$  V.

14 Terminal conditions (pins not designated may be H > 2.0 V, or L < 0.8 V, or open).

2/ Tests shall be performed in sequence.  
 3/ Output voltages shall be either: (a)  $H = 2.4 \text{ V}$ , minimum and  $L = 0.4 \text{ V}$ , maximum when using a high speed checker speed checker double comparator or (b)  $H > 1.5 \text{ V}$  and  $L < 1.5 \text{ V}$  when using a high speed checker

Input voltages shown are:  $A = 2.4 \text{ V minimum}$  and  $B = 0.4 \text{ V maximum}$ . Minimum limit specified is the frequency of the input to be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/

MIL-M-38510/21D

TABLE III. Group A inspection for device 05 - continued. 1/

8.2/3 Same tests, terminal conditions, and limits as for subgroup 7, except  $T_C = +125^\circ\text{C}$  and  $-55^\circ\text{C}$

3

See footnotes at end of device type 05.

TABLE III. Group A Inspection for device 05 - Continued. 1/

Subj group	Symbol	NLL- STD-883	Cases												Measured terminal	Test limits	Unit		
			A	B	D	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Case no.	Test no.	Clock 1	Q1	Clear 1	VCC	Clear 2	D2	Clock 2	Preset 2	Q2	V2	GND	Q1	Q1	Preset 1	
T <sub>C</sub> = +25°C	tPLH	3003 (Fig.12)	86 CKT A	IN	IN(G)	B	5.0 V								GND	OUT	OUT	5.0 V	Clock1/Q1
			86 CKT B	IN	IN(G)	B										OUT	OUT	5.0 V	Clock1/Q1
			87 CKT A																Clock2/Q2
			87 CKT B																Clock2/Q2
	tPLH	3003	88 CKT A	IN	IN(H)	B													Clock1/Q1
			88 CKT B	IN	IN(H)	B												Clock1/Q1	
			89 CKT A															Clock2/Q2	
			89 CKT B															Clock2/Q2	
	tPLH	3003 (Fig.13)	90 CKT A	IN	IN(G)	5.0 V												3	
			90 CKT B	IN	IN(G)	5.0 V												Clock1/Q1	
			91 CKT A															Clock1/Q1	
			91 CKT B															Clock2/Q2	
	tPLH	3003	92 CKT A	IN	IN(H)	5.0 V												3	
			92 CKT B	IN	IN(H)	5.0 V												Clock1/Q1	
			93 CKT A															Clock2/Q2	
			93 CKT B															Clock2/Q2	
T <sub>C</sub> = +125°C	tPLH	3003 (Fig.12)	94	IN	IN(H)	5.0 V												2.5	
			95	IN	IN(G)	5.0 V												MHz	
			96																
			97																
	tPLH	3003 (Fig.11)	98 CKT A																
			98 CKT B																
			99 CKT A																
			99 CKT B																
			100 CKT A																
			100 CKT B																
			101 CKT A																
			101 CKT B																

See footnotes at end of device type 05.

TABLE III. Group A inspection for device 05 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 Method	Cases										Measured terminal				Test limits		Unit
			A	8,	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
10 $T_C = +125^\circ C$	tPHL	3003 (Fig. 11)	102 CKT A	IN	5.0 V									GND	OUT	J	Clear1/Q1	10	200 ns
		102 CKT B	C	3	2	1	14	i3	12	11	10	9	8		OUT	J	Clear1/Q1	10	120
		103 CKT A	Test no.	1	01	Clear 1	V <sub>CC</sub>	Clear 2	D <sub>2</sub>	Clock 2/Preset 2	Q <sub>2</sub>	Q <sub>2</sub>	GND	Q <sub>1</sub>	Preset 1	IN	Preset1/V	-	200
		103 CKT B														IN	Preset1/V	-	120
		104 CKT A														Q <sub>1</sub>	Clock2/Q2	-	200
		104 CKT B														Q <sub>2</sub>	Clock2/Q2	-	120
		105 CKT A														Q <sub>2</sub>	Preset2/V	-	200
		105 CKT B														Q <sub>2</sub>	Preset2/V	-	120
11 tPLH	tPLH	3003 (Fig. 12)	106 CKT A	IN	IN(G)	B	*	B	IN(G)	IN	5.0 V	OUT	OUT	OUT	OUT	5.0 V	Clock1/Q1	150	---
		106 CKT B	IN	IN(G)	B	*	B	IN(G)	IN	5.0 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Clock1/Q1	150	---
		107 CKT A															Clock2/Q2	150	---
		107 CKT B															Clock2/Q2	150	---
		108 CKT A															Clock2/Q2	150	---
		108 CKT B															Clock2/Q2	150	---
		109 CKT A															Clock2/Q2	150	---
		109 CKT B															Clock2/Q2	150	---
12 tPLD	tPLD	3003 (Fig. 13)	110 CKT A	IN	IN(H)	B	*	B	IN(H)	IN	5.0 V	OUT	OUT	OUT	OUT	5.0 V	Clock1/Q1	200	---
		110 CKT B	IN	IN(H)	B	*	B	IN(H)	IN	5.0 V	OUT	OUT	OUT	OUT	OUT	5.0 V	Clock1/Q1	200	---
		111 CKT A															Clock2/Q2	200	---
		111 CKT B															Clock2/Q2	200	---
		112 CKT A															Clock2/Q2	200	---
		112 CKT B															Clock2/Q2	200	---
		113 CKT A															Clock2/Q2	200	---
		113 CKT B															Clock2/Q2	200	---
13 tPHL	tPHL																		

11 Same tests, terminal conditions, and limits as for subgroup 10, except  $T_C = -55^\circ C$ .NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V, J = input pulse  $t_p \geq 100 \text{ ns}$ , PRR = 0.5 MHz,  $V_{OL} = 0 \text{ V}$ ,  $V_{OH} = 4.5 \text{ V}$ .1/ Terminal conditions pins not designated may be H  $\geq 2.0 \text{ V}$ , or L  $\leq 0.8 \text{ V}$ , or open.

2/ Tests shall be performed in sequence.

3/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.

4/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker single comparator; or (b) H  $\geq 1.5 \text{ V}$  and L  $\leq 1.5 \text{ V}$  when using a high speed checker.5/ MAX<sub>1</sub> limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for "JAN" marking.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - - -	Ground (zero voltage potential)
VIN - - - - - - - - - - - - - - -	Voltage level at an input terminal
I <sub>IN</sub> - - - - - - - - - - - - - - -	Current flowing into an input terminal

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3), and case outline A (see 1.2.3). There is no substitute for case outline C. Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	54L71
02	54L72
03	54L73
04	54L78
05	54L74

6.6 Manufacturers' designation. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designation.

Device type	Manufacturer			
	Circuit A Texas Instruments	Circuit B National Semiconductor	Circuit C	Circuit D
01		X		
02		X		
03		X		
04		X		
05		X		

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

## Custodians:

Army - ER

Navy - EC

Air Force - 17

## Preparing activity:

Air Force - 17

## Agent:

DLA - ES

## Review activities:

Army - AR, MI

Navy - OS, SH, TD

Air Force - 11, 19, 85, 99

DLA - ES

(Project 5962-1095)

## User activities:

Army - SM

Navy - CG, MC