

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 32,768 BIT SCHOTTKY, BIPOLAR,
PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome resistors (NiCr), titanium-tungsten (TiW), or zapped vertical emitter as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the part number. A special test requirement is included in this specification to screen against devices which may contain moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

| <u>Device type</u> | <u>Circuit</u> | <u>Access times (ns)</u> |
|--------------------|--|--------------------------|
| 01 | 4096 words/8 bits per word PROM with tri-state outputs | 45 |
| 02 | 4096 words/8 bits per word PROM with tri-state outputs | 85 |

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

| <u>Letter</u> | <u>Case outline (see MIL-M-38510, appendix C)</u> |
|---------------|---|
| J | D-3 (24-lead, 1/2" x 1 1/4"), dual-in-line package |
| 3 | C-4 (28-terminal, .450" x .450"), square chip carrier package |

1.3 Absolute maximum ratings:

| | | |
|--|-----------|-------------------------------|
| Supply voltage range | - - - - - | -0.5 V dc to +7.0 V dc |
| Input voltage range | - - - - - | -0.5 V dc to +5.5 V dc |
| Storage temperature range | - - - - - | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | - - - - - | +300°C |
| Thermal resistance, junction-to-case (θ_{JC}): 1/ | | |
| Case J | - - - - - | 40°C/W |
| Case 3 | - - - - - | 60°C/W |
| Output voltage range | - - - - - | -0.5 V dc to +V _{CC} |
| Output sink current | - - - - - | 100 mA |
| Maximum power dissipation (P _D) 2/- | - - - - - | 1.10 W |
| Maximum junction temperature (T _J) | - - - - - | +175°C |

1/ Heat sinking is recommended to reduce junction temperature.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}.)

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions:

| | |
|---|--------------------------------------|
| Supply voltage - - - - - | 4.5 V dc minimum to 5.5 V dc maximum |
| Minimum high-level input voltage (V_{IH}) - | 2.0 V dc |
| Maximum low-level input voltage (V_{IL}) - | 0.8 V dc |
| Normalized fanout (each output) - - - - | 8 mA 3/ |
| Case operating temperature range - - - - | -55°C to +125°C |

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3/ Circuit C, device 01, and circuit F are 16 mA devices.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new functional block diagram to the qualifying activity for inclusion in this specification. The functional block diagram shall clearly define the row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and shall apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be as specified in table III and, where applicable, the altered item drawing for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance inspection are specified in table II by device class.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the acquisition contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
- b. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions <u>1/</u> | Device type | Limits | | Unit |
|--|-------------------|--|-------------|--------|------|------|
| | | | | Min | Max | |
| High-level output voltage | V _{OH} | V _{CC} = 4.5 V; I _{OH} = -2 mA; V _{IH} = 2.0 V; V _{IL} = 0.8 V | 01, 02 | 2.4 | | V |
| Low-level output voltage | V _{OL} | V _{CC} = 4.5 V; I _{OL} = 8 mA; <u>2/</u> V _{IH} = 2.0 V; V _{IL} = 0.8 V | 01, 02 | | 0.4 | V |
| High-level input voltage | V _{IH} | | 01, 02 | 2.0 | | V |
| Low-level input voltage | V _{IL} | | 01, 02 | | 0.8 | V |
| Input clamp voltage | V _{IC} | V _{CC} = 4.5 V; I _{IN} = -10 mA; T _C = 25°C | 01, 02 | | -1.5 | V |
| High-impedance (off-state) output high current | I _{OHZ} | V _{CC} = 5.5 V; V _O = 2.4 V | 01, 02 | -60 | +60 | μA |
| High-impedance (off-state) output low current | I _{OLZ} | V _{CC} = 5.5 V; V _O = 0.4 V | 01, 02 | -60 | +60 | μA |
| High-level input current | I _{IH} | V _{CC} = 5.5 V; V _{IN} = 5.5 V | 01, 02 | | 50 | μA |
| Low-level input current | I _{IL} | V _{CC} = 5.5 V; V _{IN} = 0.4 V | 01, 02 | | -250 | μA |
| Short circuit output current | I _{OS} | V _{CC} = 5.5 V; V _O = 0.0 V <u>3/</u> | 01, 02 | -12 | -85 | mA |
| Supply current | I _{CC} | V _{CC} = 5.5 V; V _{IN} = 0; outputs = open | 01, 02 | | 190 | mA |
| Address access time | t _{AVQV} | V _{CC} = 4.5 V and 5.5 V (see figure 5) | 01 | | 45 | ns |
| | | | 02 | | 85 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions ^{1/} | Device type | Limits | | Unit |
|---------------------------|-------------------|---|-------------|--------|-----|------|
| | | | | Min | Max | |
| Output-enable access time | t _{ELQV} | V _{CC} = 4.5 V and 5.5 V (see figure 5) | 01 | | 30 | ns |
| | t _{EHQV} | | 02 | | 40 | |
| Output-disable time | t _{EHQZ} | | 01 | | 30 | ns |
| | t _{ELQZ} | | 02 | | 40 | |

^{1/} Complete terminal conditions shall be specified in table III.

^{2/} I_{OL} = 16 mA for device type 01, circuit C.

^{3/} Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (see ^{1/} ^{2/} ^{3/} table III) | |
|---|---|--------------------------|
| | Class S devices | Class B devices |
| Interim electrical parameters (method 5004) | 1 | 1 |
| Final electrical test parameters (method 5004) for programmed devices | 1*,2,3,7*, 9, 10, 11 | 1*,2,3,7*, 9 |
| Final electrical test parameters (method 5004) for unprogrammed devices | 1*,2,3,7*, | 1*,2,3,7* |
| Group A test requirements (method 5005) | 1,2,3,7,8, 9,10,11,12 | 1,2,3,7,8, 9,10,11,12 |
| Group B electrical test parameters (method 5005, subgroup 5) | 1,2,3,7, 9,10,11 | N/A |
| Group C end-point electrical parameters (method 5005) | N/A | 1,2,3,7 |
| Group D end-point electrical parameters (method 5005) | 1,2,3,7 | 1,2,3,7 |

^{1/} * PDA applies to subgroups 1 and 7 (see 4.2c).

^{2/} Any or all subgroups may be combined when using high-speed testers.

^{3/} Subgroup 7 shall consist of verifying the pattern specified.

- d. The freeze-out test shall be conducted as a 100-percent screen on all class S devices having nichrome as the fusing link. Within no more than 24 hours after completion of burn-in and prior to the final electrical test, all devices containing nichrome resistors (see 3.7.1 and 3.7.2) shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned at 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical test parameters shall be completed 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:
- (1) Connect devices in the electrical configuration of figure 7 or in the burn-in configuration of figure 4 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
 - (2) Reduce device temperature to $T_C = -10^\circ\text{C} \pm 2^\circ\text{C}$ with the bias cycled and maintain at that temperature for a minimum of 5 hours.
 - (3) With the cycled bias maintained, allow T_C to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_C shall not exceed 35°C during this period.
 - (4) Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.
- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 through 11 of group A shall be attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device type may be Part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.
- e. Subgroup 12 shall be added to group A inspection requirements for class B devices using a LTPD of 10 and consist of procedures, test conditions and limits specified in table III.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method ~~5005~~ of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1.c.) shall be included in the subgroup 5 tests.
- c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method ~~5005~~ of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

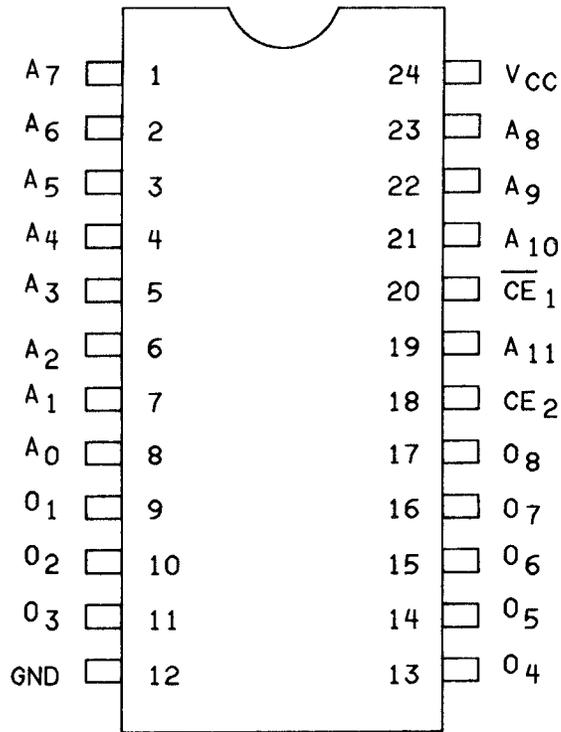
4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method ~~5005~~ of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as specified in 4.5.1 herein.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross-referenced in 6.6 herein with the manufacturer's symbol or CAGE number.

Case J



Case 3

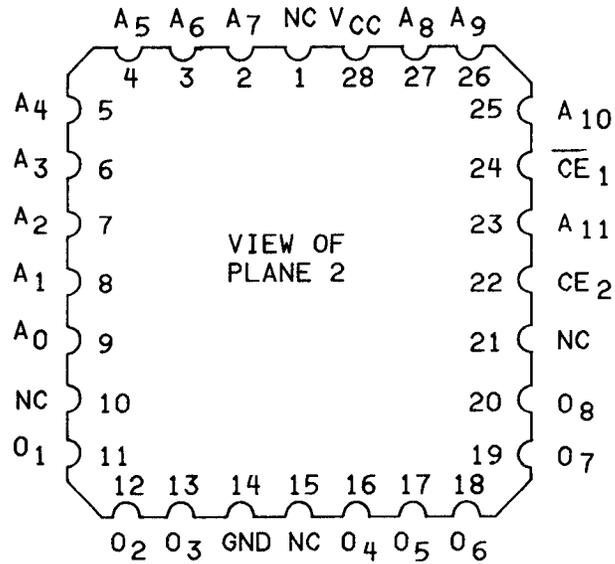


FIGURE 1. Terminal connections.

Circuit A

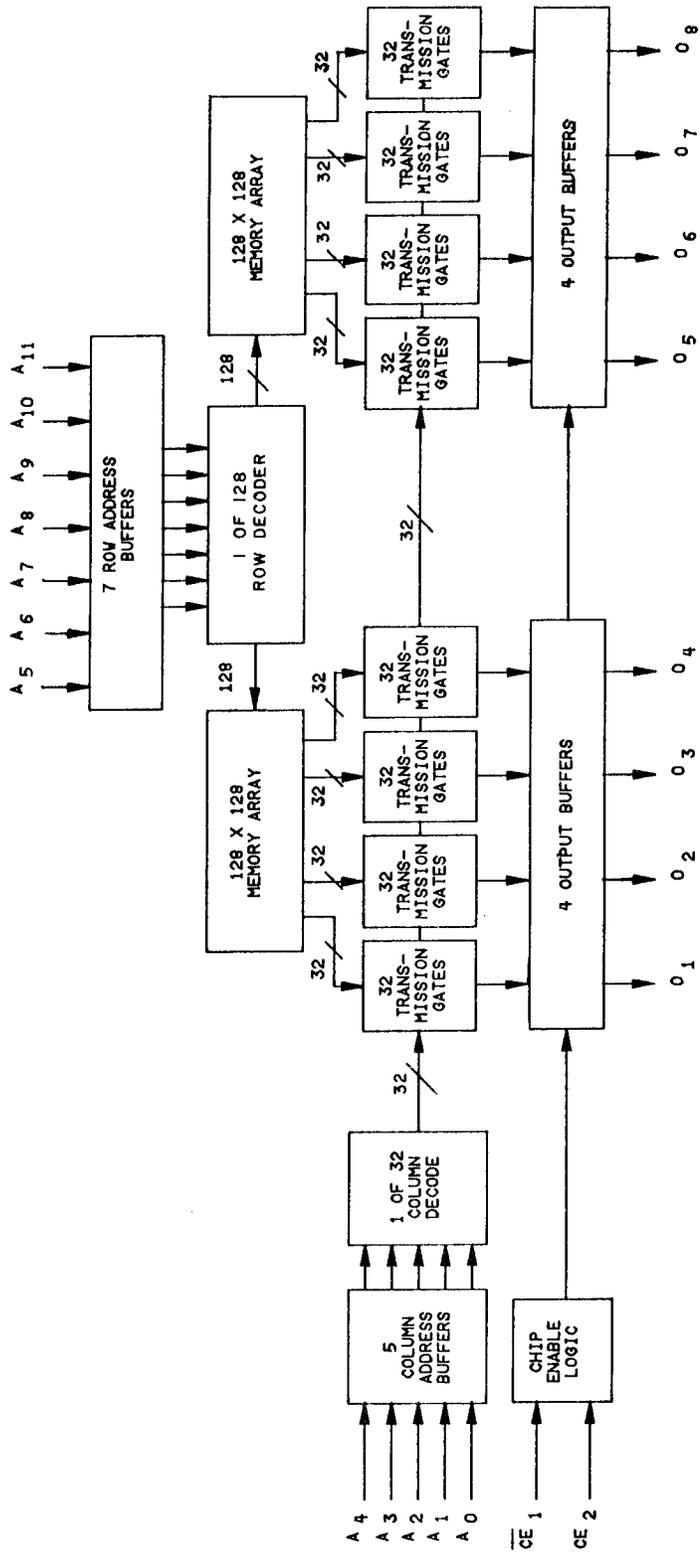


FIGURE 3. Functional block diagrams.

Circuit B

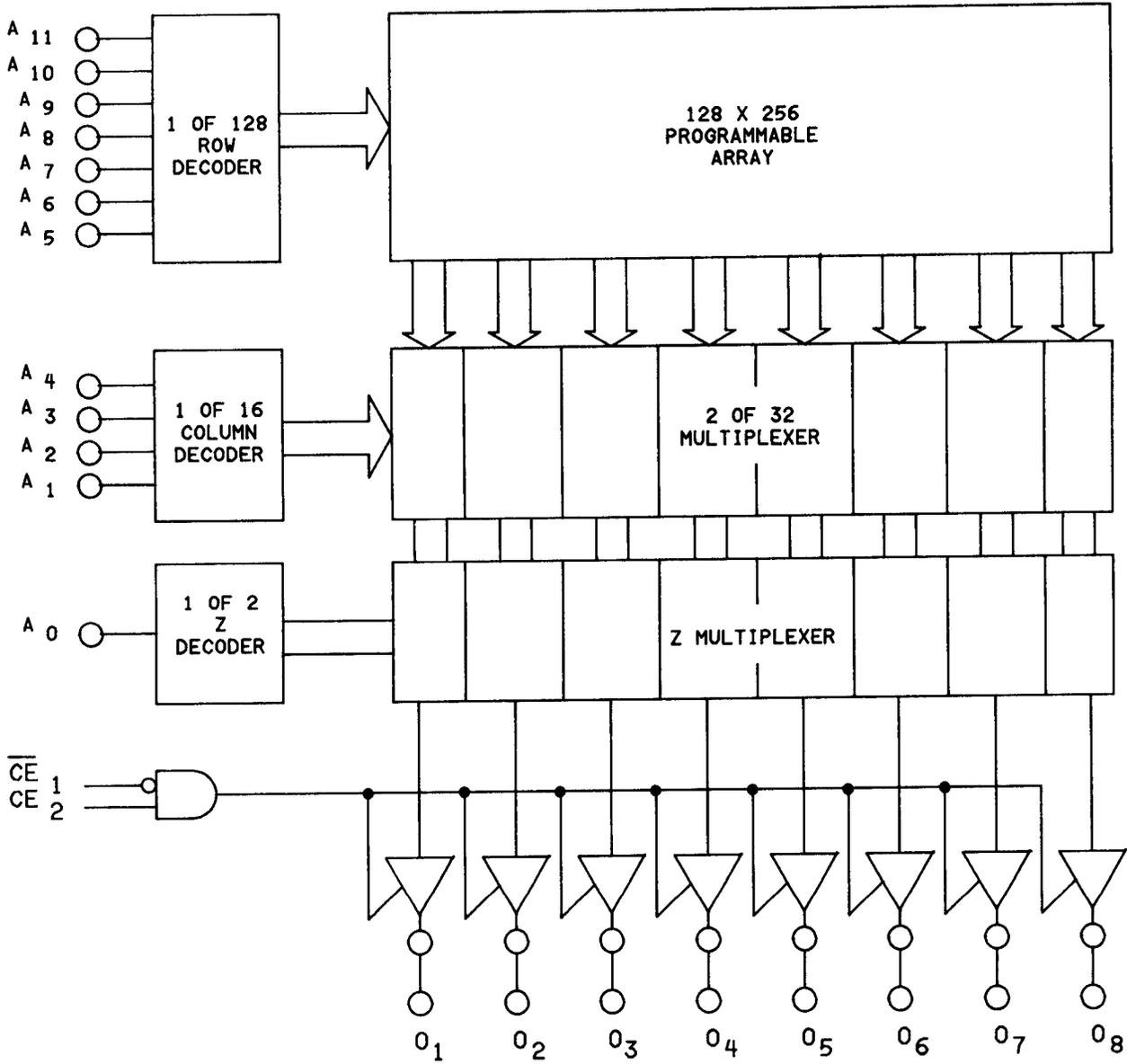


FIGURE 3. Functional block diagrams - Continued.

Circuit C

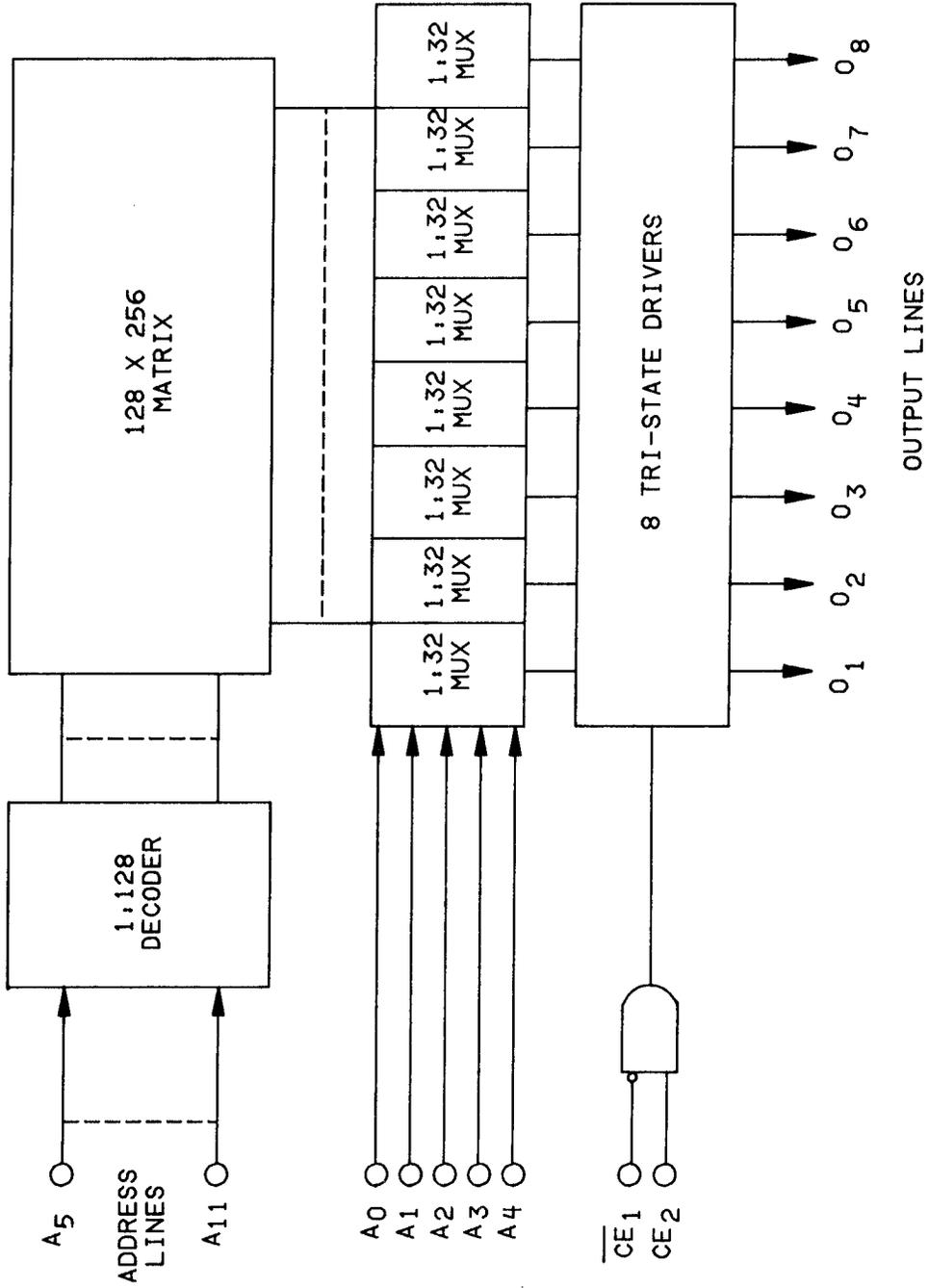


FIGURE 3. Functional block diagrams - Continued.

Circuit F

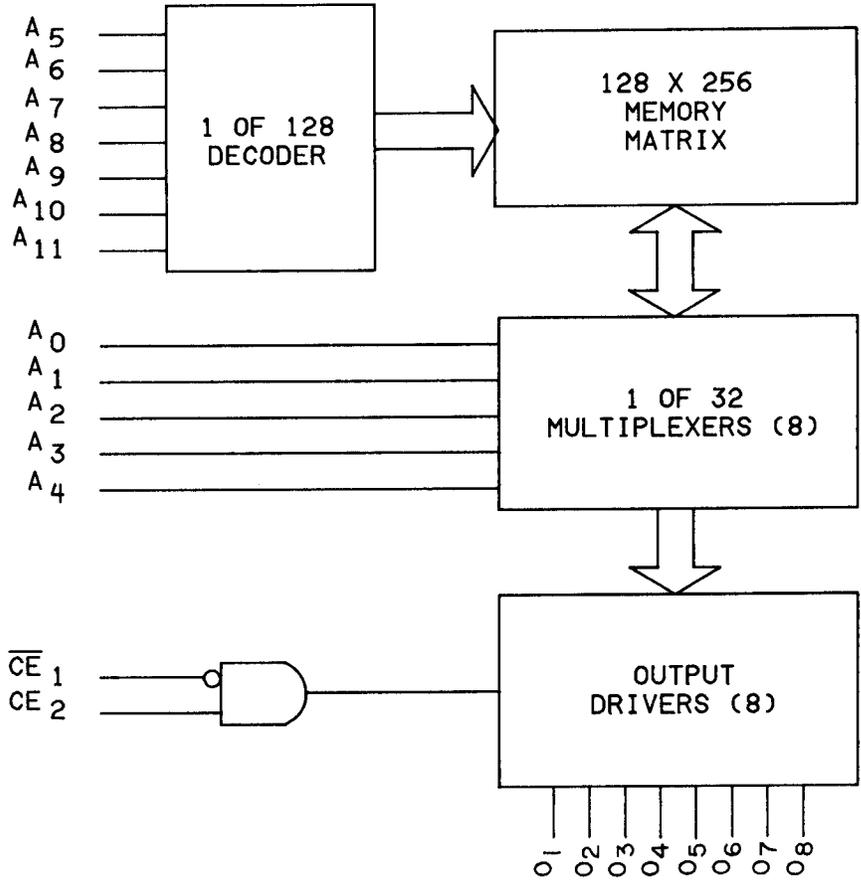
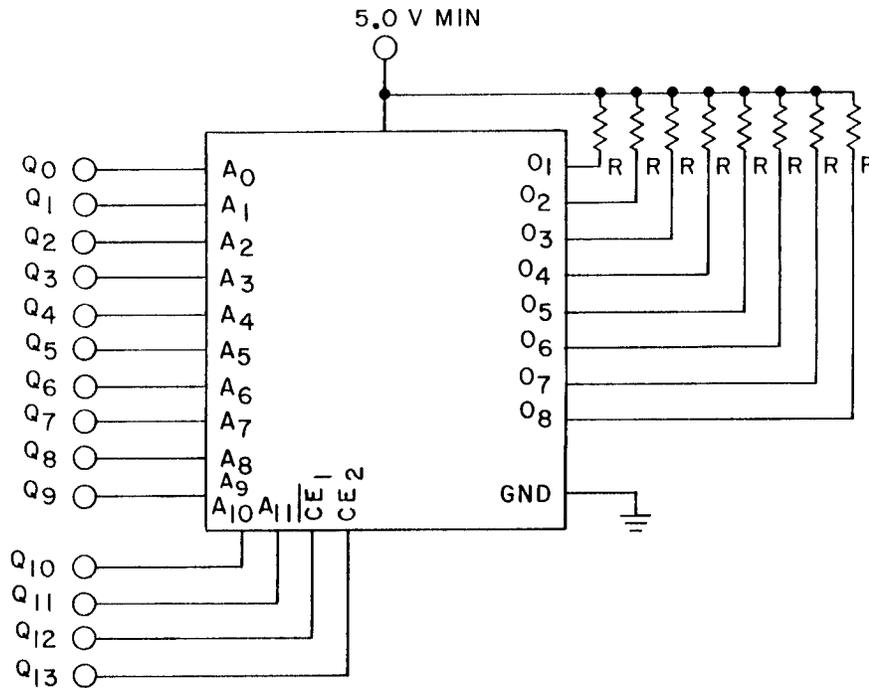


FIGURE 3. Functional block diagrams - Continued.



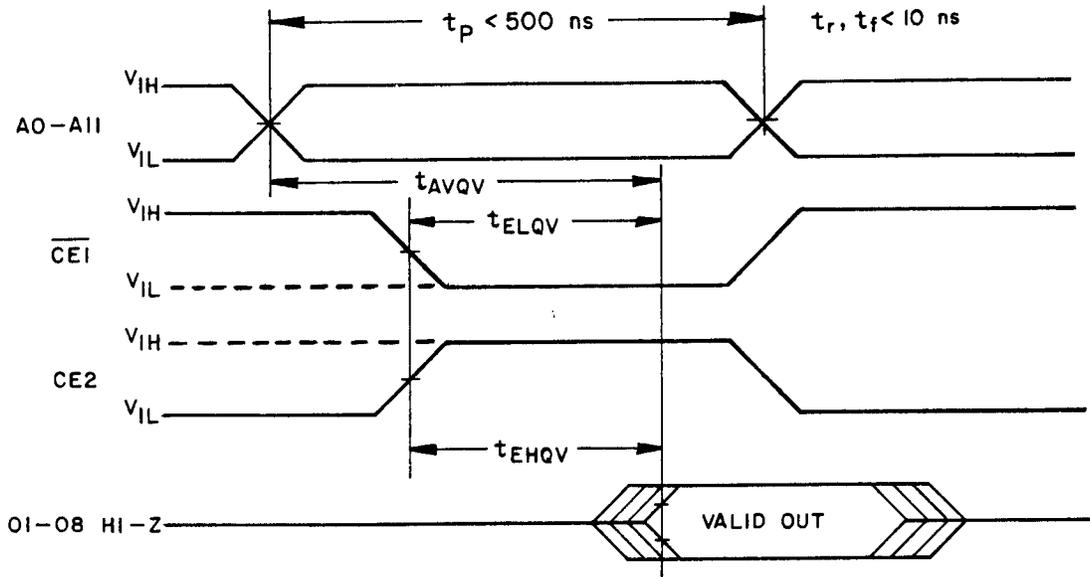
NOTES:

1. $R = 560\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics.
 $V_{IL} = 0.0$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies are as follows:

| Input | Frequency ($\pm 50\%$) |
|-------|--------------------------|
| Q0 | $f_0 = 100$ KHz Min |
| Q1 | $f_1 = 1/2 f_0$ |
| Q2 | $f_2 = 1/2 f_1$ |
| Q3 | $f_3 = 1/2 f_2$ |
| Q4 | $f_4 = 1/2 f_3$ |
| Q5 | $f_5 = 1/2 f_4$ |
| Q6 | $f_6 = 1/2 f_5$ |
| Q7 | $f_7 = 1/2 f_6$ |
| Q8 | $f_8 = 1/2 f_7$ |
| Q9 | $f_9 = 1/2 f_8$ |
| Q10 | $f_{10} = 1/2 f_9$ |
| Q11 | $f_{11} = 1/2 f_{10}$ |
| Q12 | $f_{12} = 1/2 f_{11}$ |
| Q13 | $f_{13} = 1/2 f_{12}$ |

FIGURE 4. Burn-in and life test circuit.

READ TIMING



OUTPUT DISABLE TIME

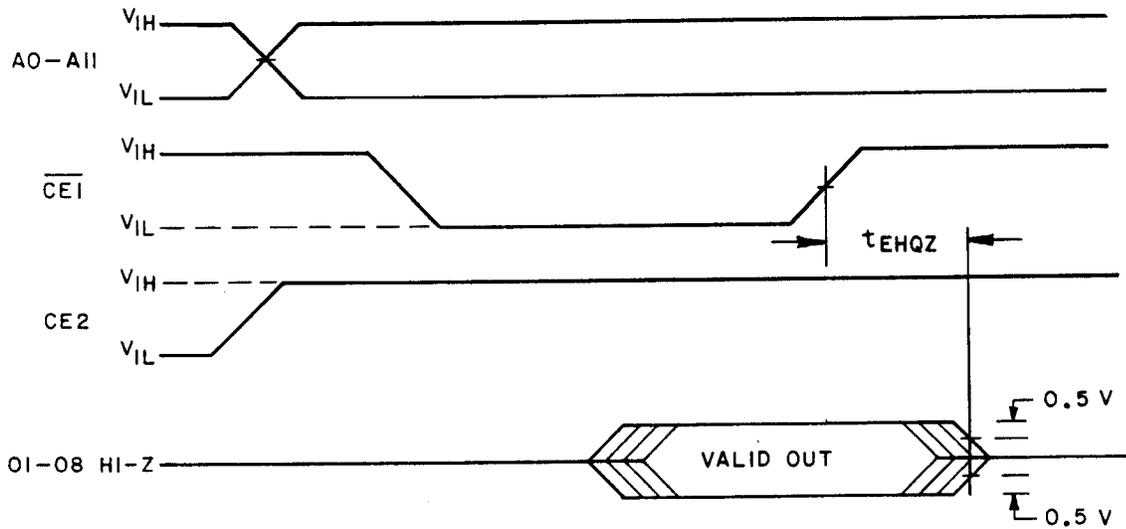
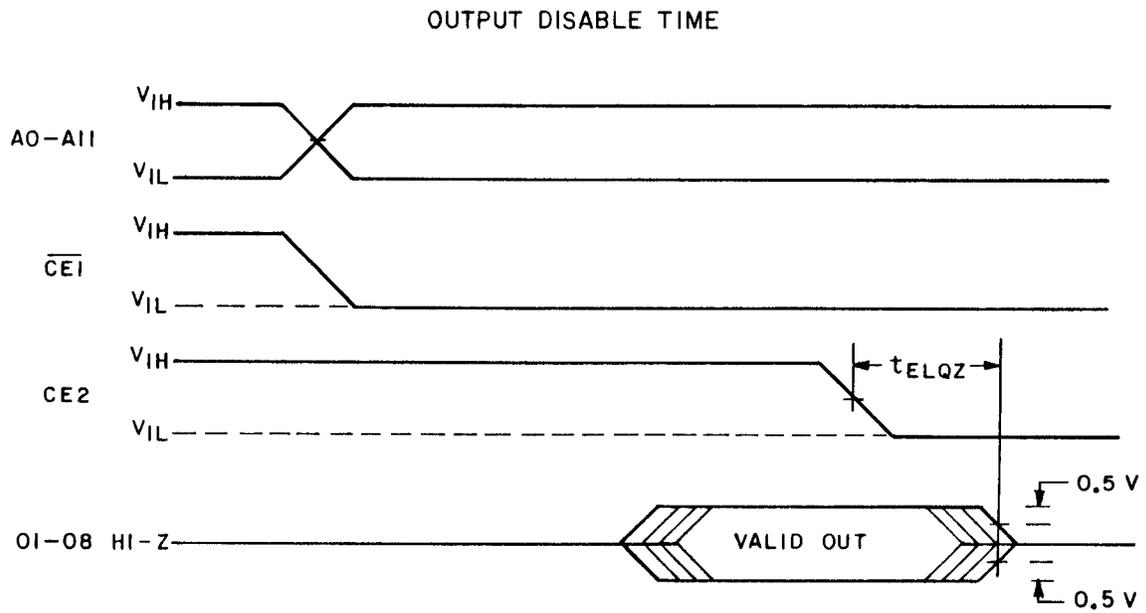


FIGURE 5. Switching time waveforms.

FIGURE 5. Switching time waveforms - Continued.

Footnotes for table III:

- 1/ Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage. Inputs not designated are high ≥ 2.0 V or low ≤ 0.8 V.
- 2/ For unprogrammed devices, apply 11.0 V on pin 1 (A₇) and pin 23 (A₈); apply 4.5 V to pin 8 (A₀) for circuit A.
- 3/ For programmed devices, select an appropriate address to acquire the desired output state. $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
- 4/ For unprogrammed devices, apply 12.0 V on pin 6 (A₂) and 0.0 V on pin 5 (A₃) for circuit F.
- 5/ For unprogrammed circuit C devices, apply 13.0 V on pin 3 (A₅); apply 0.0 V on pins 4 and 8 (A₄, A₀); apply 4.5 V on pins 2, 5, 6, and 7 (A₆, A₃, A₂, A₁).
- 5a/ $I_{OL} = 16$ mA for device type 01, circuit C.
- 6/ For unprogrammed devices, apply 12.0 V on pin 1 (A₇) and 3.0 V to all other X addresses - A₅, A₆, A₈ - A₁₁ for circuit B.
- 7/ Terminal conditions for the output leakage current tests shall be as follows:
 - a. $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
 - b. For I_{QHZ} :
Select an appropriate address to acquire a logic zero on the designated output. Apply V_{IH} to \overline{CE}_1 and V_{IL} to CE_2 . Measure the leakage current while applying the specified voltage.
 - c. For I_{QLZ} :
Select an appropriate address to acquire a logic one on the designated output. Apply V_{IH} to \overline{CE}_1 and V_{IL} to CE_2 . Measure the leakage current while applying the specified voltage.
- 8/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. Terminal conditions shall be as follows:
 - a. Inputs: H = 3.0 V, L = 0.0 V.
 - b. Outputs: Output voltage shall be either:
 1. H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator, or
 2. H > 1.5 V and L < 1.5 V when using a high-speed checker single comparator.
 - c. The functional tests shall be performed with $V_{CC} = 4.5$ V and $V_{CC} = 5.5$ V.
- 9/ For subgroups 9, 10, and 11, input/output conditions appear in table V. Timing diagram appears in figure 5 (Read timing). GALPAT (programmed PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{AVQV} . Each bit in the pattern is fixed by being programmed with an "H" or "L".

Description:

1. Word 0 is read.
2. Word 1 is read.
3. Word 0 is read.
4. Word 2 is read.
5. Word 0 is read.
6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 4095 is reached, then increments to the next word and reads back and forth as in steps 1 through 7 and shall include all words.
7. Pass execution time = $(n^2 + n) \times$ cycle time, $n = 4096$.
8. The GALPAT tests shall be performed with $V_{CC} = 4.5$ V and 5.5 V.

- 10/ Sequential test (programmed PROM). This program will test all bits in the array for t_{ELQV} or t_{EHQV} .

Description:

1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
2. Word 0 is addressed. Enable line is pulled HI to LO or LO to HI. t_{ELQV} or t_{EHQV} is read.
3. Word 1 is addressed. Same enable sequence as above.
4. The reading procedure continues until word 4095 is reached.
5. Pass execution time = 4096 x cycle time.
6. The sequential tests shall be performed with $V_{CC} = 4.5 \text{ V}$ and 5.5 V .

- 11/ The outputs are loaded in accordance with figure 8.

- 12/

| Parameter | Device type | |
|------------|-------------|-------|
| | 01 | 02 |
| t_{AVQV} | 45 ns | 85 ns |
| t_{ELQV} | 30 ns | 40 ns |
| t_{EHQV} | 30 ns | 40 ns |
| t_{EHQZ} | 30 ns | 40 ns |
| t_{ELQZ} | 30 ns | 40 ns |

- 13/ For subgroup 12, input/output conditions appear in table V. Timing waveforms appear in figure 5 (Output disable time). The outputs are loaded per figure 11. Additional terminal conditions are as follows:

- a. t_{EHQZ}
 1. Output in logic low state: Select an appropriate address to acquire a logic zero on the designated output. $\overline{CE}_2 = V_{IH}$.
 2. Output in logic high state: Select an appropriate address to acquire a logic one on the designated output. $\overline{CE}_2 = V_{IH}$.
- b. t_{ELQZ}
 1. Output in logic low state: Select an appropriate address to acquire a logic zero on the designated output. $\overline{CE}_1 = V_{IL}$.
 2. Output in logic high state: Select an appropriate address to acquire a logic one on the designated output. $\overline{CE}_1 = V_{IL}$.

4.7 Programming procedure A. The programming characteristics of table IVA and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6A and the programming characteristics of table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- c. Disable the chip by applying V_{IH} to \overline{CE}_1 input. The chip enable inputs are TTL compatible.
- d. Disable the programming circuitry by applying V_{OPD} to the outputs of the PROM.
- e. Raise V_{CC} to V_{PH} as specified on the waveforms in figure 6A.
- f. After a delay of t_D , apply only one V_{OPE} pulse with duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{PH} level by applying V_{OPE} pulses to each output to be programmed allowing a delay of t_p between pulses as shown on figure 6A.
- h. Repeat 4.7b through 4.7g for all other bits to be programmed.
- i. Lower V_{CC} to 4.5 volts following a delay of t_p from the last programming pulse applied to an output.
- j. Enable the chip by applying V_{IL} to \overline{CE}_1 input and verify the program.
- k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

4.8 Programming procedure B. The programming characteristics of table IVB and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6B and the programming characteristics of table IVB shall apply to these procedures.
- b. Apply V_{IH} to \overline{CE}_1 and the binary address of the PROM word to be programmed. Raise V_{CC} to V_{CCP} .
- c. After a t_D delay, apply only one V_{OP} pulse to the output to be programmed high. Apply V_{OP} to one output at a time.
- d. After a t_D delay, pulse \overline{CE}_1 to a V_{IL} level for a duration of t_p .
- e. After t_p and a t_D delay, remove V_{OP} from the programmed output.
- f. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OP} pulses to each output to be programmed and pulsing \overline{CE}_1 to the V_{IL} level, allowing the proper delays between V_{OP} and \overline{CE}_1 .
- g. Repeat 4.8b through 4.8e for all bits to be programmed.
- h. To verify programming, lower V_{CCP} to V_{CC} . Connect a 10 kilohm resistor between each output and V_{CC} . Apply V_{IL} to \overline{CE}_1 input. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.
- i. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVA. Programming procedure A characteristics.

| Parameter | Symbol | Limits <u>1/</u> | | | Unit |
|--|------------------------|------------------|-------------|--------------|---------|
| | | Min | Recommended | Max | |
| Address input voltage <u>2/</u> | V_{IH} V_{IL} | 2.4 0.0 | 5.0 0.4 | 5.0 0.8 | V |
| V_{CC} required during programming <u>3/</u> | V_{PH} V_{PL} | 11.75 4.5 | 12.0 4.5 | 12.25 5.5 | V |
| Programming input low current | I_{ILP} | -600 | -600 | -650 | μA |
| Programming voltage (V_{CC}) transition time | t_{TLH} t_{THL} | 1 1 | 1 1 | 10 10 | μs |
| Programming delay | t_D | 10 | 10 | 100 | μs |
| Programming pulse width | t_p | 90 | 100 | 180 | μs |
| Programming duty cycle | D.C. | | 50 | 90 | % |
| Output voltage Enable | V_{OPE} | 10.5 | 10.5 | 11.0 | V |
| Disable <u>4/</u> | V_{OPD} | 4.5 | 5.0 | 5.5 | |
| Output voltage enable current | I_{OPE} | 2 | 4 | 15 | mA |

1/ $T_C = +25^\circ C$.

2/ Address and chip enable shall not be left open for V_{IH} .

3/ V_{PH} supply shall be capable of sourcing one ampere.

4/ Disable condition can be met with output open circuit.

TABLE IVB. Programming procedure B characteristics.

| Parameter | Symbol | Conditions <u>1/</u> | Limits | | | Unit |
|---|-------------------|--|--------|-------------|------|------|
| | | | Min | Recommended | Max | |
| V _{CC} required during programming | V _{CCP} | | 11.5 | 11.75 | 12.0 | V |
| V _{OUT} current limit during programming | I _{OP} | | 15 | 20 | | mA |
| Output programming voltage | V _{OP} | | 11.5 | 11.75 | 12.0 | V |
| Pulse width of programming voltage | t _p | | 9 | 10 | 11 | μs |
| Programming delay | t _D | | 100 | 120 | | ns |
| V _{CCP} or V _{OUT} transition time | t _{TLH} | Rise time of V _{CC} or V _{OUT} | 1 | 5 | 10 | V/μs |
| V _{CCP} current | I _{CCP} | | 800 | 1,000 | | mA |
| Low V _{CC} for verification | V _{CCCL} | | 4.2 | 4.3 | 4.4 | V |
| High V _{CC} for verification | V _{CCCH} | | 5.8 | 6.0 | 6.2 | V |
| Address input voltage | V _{IH} | | 2.4 | 3.0 | 5.5 | V |
| | V _{IL} | | 0.0 | 0.0 | 0.5 | V |
| Maximum duty cycle during automatic programming of program pin and output pin | D.C. | t _p /t _c | | 25 | 25 | % |

1/ T_C = +25°C.

4.9 Programming procedure C. The programming characteristics of table IVC and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The output pins shall be terminated with a 10 kilohm resistor to GND and bypass V_{CC} to GND with a 0.01 μ F capacitor. The waveforms on figure 6C and the programming characteristics of table IVC shall apply to these procedures.
- b. Disable the device by applying V_{IH} to $\overline{CE_1}$ input and V_{IH} to CE_2 . The chip enable pins are TTL compatible.
- c. Apply V_{IL} to all other pins.
- d. Address the PROM with the binary address of the selected word to be programmed and reset $T_p = 5 \mu s$. Address inputs are TTL compatible.
- e. After a delay of T_{D1} , raise the V_{CC} pin to V_{CCP} .
- f. After a delay of T_{D2} and raise the corresponding output pin to V_{OPF} .
- g. After a delay of T_{D3} , lower $\overline{CE_1}$ to V_{IL} for a duration of T_p and simultaneously lower the output to V_{IL} and wait T_{D4} .
- h. Return the $\overline{CE_1}$ to V_{IH} .
- i. Wait T_{D5} and lower V_{CC} to V_{CCV} .
- j. Wait T_{D6} and lower $\overline{CE_1}$ to V_{IL} for the duration of T_v .
- k. A properly blown fuse will read V_{OL} and unblown fuse will read V_{OH} .
 1. If the fuse is blown, go to n.
 2. If the fuse is unblown, go to l.
- l. If T_p is less than 30 μs , increment T_p by 5 μs and go to e. If T_p is $\geq 5 \mu s$ go to m.
- m. If T_p is $\geq 30 \mu s$, the device is a reject.
- n. After a delay of T_{D7} , select the next output or address to be programmed.
- o. Repeat steps 4.9d through 4.9k until all required addresses are programmed.
- p. To verify the program keep V_{CC} pin at V_{CCV} . Apply V_{IL} to $\overline{CE_1}$. The programmed fuse will go to the low level and unblown fuse shall remain in the high level.
- q. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVC. Programming procedure C characteristics.

| Parameter | Symbol | Conditions <u>1/</u> | Limits | | | Unit |
|---|----------------------------------|---|--------|-------------|------|------|
| | | | Min | Recommended | Max | |
| Power supply voltage to <u>2/</u> program | V _{CCP} | I _{CCP} = 425 ±75 mA | 8.5 | 8.75 | 9.0 | V |
| Verify voltage | V _{CCV} | | 4.75 | 5.0 | 5.25 | V |
| High input voltage | V _{IH} | I _{IH} = 50 μA | 2.4 | 3.0 | 5.5 | V |
| Low input voltage | V _{IL} | I _{IL} = -500 μA | 0.0 | 0.0 | 0.5 | V |
| Forced output current | I _{OPF} | V _{OPF} = +17.5 ±0.5 V | 150 | 185 | 220 | mA |
| Forced output voltage <u>3/</u> (program) | V _{OPF2} | I _{OPF} = 300 ±25 mA | 20 | | 21.0 | V |
| Output high voltage | V _{OH} | | 2.4 | | 5.25 | V |
| Output low voltage | V _{OL} | | 0.0 | | 0.45 | V |
| V _{CC} delay time | T _{D1} | 50% ADD to 10% V _{CCP} | 10 | 10 | 25 | μs |
| V _{OUT} delay time | T _{D2} | 90% V _{CCP} to 10% V _{OPF} | 1 | 1 | 5 | μs |
| Pulse sequence delays | T _{D3} -T _{D8} | See figure 6C | 1 | 1 | 10 | μs |
| V _{CC} rise time | T _{R1} | 0% to 100% | 4 | 7 | 8 | μs |
| V _{OUT} rise time | T _{R2} | 10% to 90% | 3 | 10 | 17 | μs |
| V _{CC} fall time | T _{F1} | 100% to 0% | 2 | 4 | 10 | μs |
| V _{OUT} fall time | T _{F2} | 100% to 0% | 4 | 7 | 20 | μs |
| <u>CE</u> ₁ programming pulse <u>4/</u> width | T _p | 10% to 10% | 5 | 10 | 30 | μs |
| <u>CE</u> ₁ verify pulse <u>4/</u> width | T _v | 10% to 10% | 5 | 5 | 10 | μs |
| Clock pulse width (CK) | T _{WC} | 50% to 50% | .5 | .75 | 1 | μs |

1/ T_C = +25°C.

2/ If the overall program/verify cycle exceeds the recommended value, a 25% duty cycle must be used for V_{CCP}.

3/ V_{OPF} supply should regulate to ±0.25 V at I_{OPF}. Maximum slew rate for V_{OPF} should be 1.0 V/μs.

4/ CE₁ rise time slew rate should be 1.0 V/ns maximum. CE₁ fall time slew rate should be 10.0 V/ns maximum.

4.10 Programming procedure F. The programming characteristics of table IVD and the following procedures shall be used for programming the device:

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 6D and the programming characteristics of table IVD shall apply to these procedures.
- b. Raise V_{CC} to 5.5 V.
- c. Address the PROM with binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying V_{IH} to the $\overline{CE_1}$ input and V_{IL} to the CE_2 input. The chip enable inputs are TTL compatible.
- e. Apply the V_{pp} pulse to the programming pin $\overline{CE_1}$. In order to insure that the output transistor is OFF before increasing voltage on the output pin, the program pins voltage pulse shall precede the output pins programming pulse by t_{D1} and leave after the programming pins programming pulse by t_{D2} (see figure 6D).
- f. Apply one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

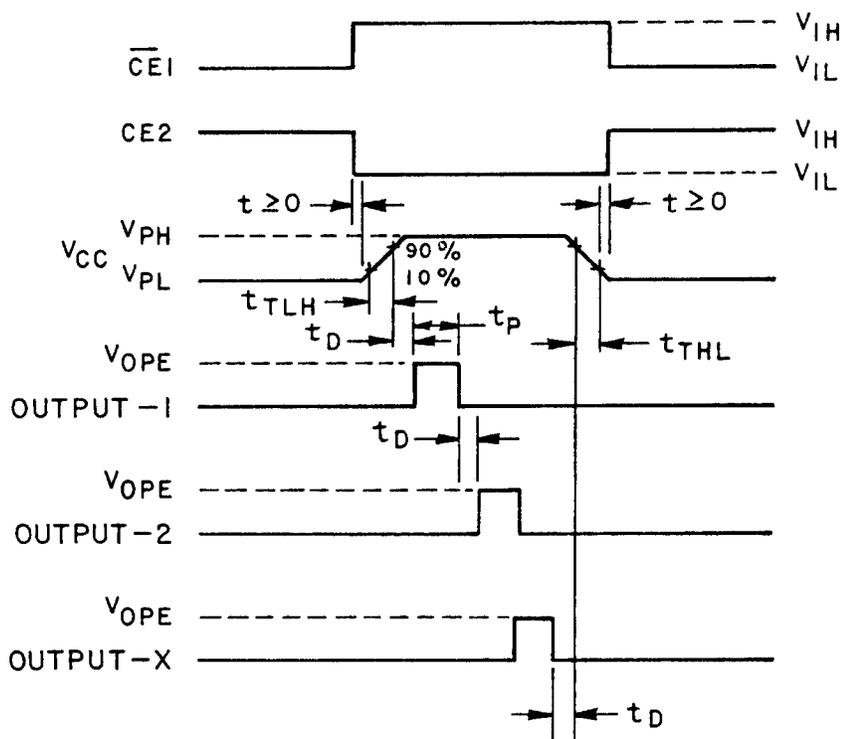
Note: The PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

- g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.
- h. Repeat 4.10b through 4.10g for all other bits to be programmed.
- i. Enable the chip by applying V_{IL} to the $\overline{CE_1}$ input and V_{IH} to the CE_2 input, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.2$ V and 0.2 mA at $V_{CC} = 6.0$ V at $T_A = +25^\circ\text{C}$.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IV D. Programming procedure F characteristics.

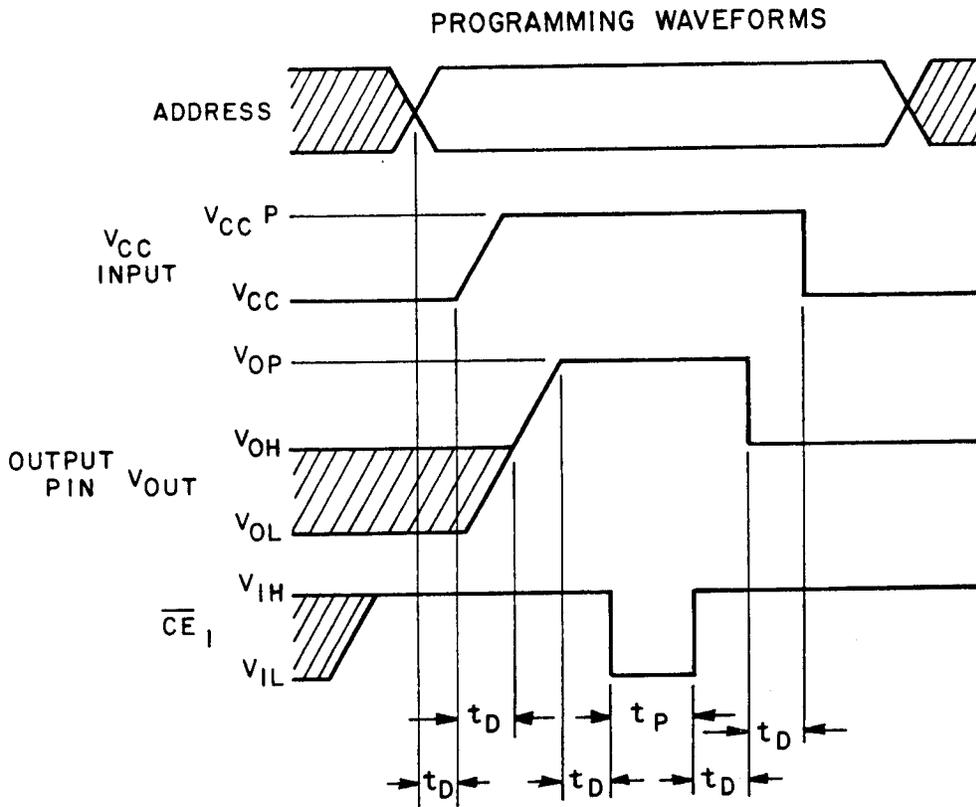
| Parameter | Symbol | Conditions 1/ | Limits | | | Unit |
|---|-------------------|--|--------|-------------|------|------|
| | | | Min | Recommended | Max | |
| V _{CC} required during programming | V _{CCP} | | 5.4 | 5.5 | 5.6 | V |
| Rise time of program pulse to data out or program pin | t _{TLH} | | 0.34 | 0.40 | 0.46 | V/μs |
| Programming voltage on program pin | V _{pp} | | 32.5 | 33 | 33.5 | V |
| Output programming voltage | V _{OUT} | | 25.5 | 26 | 26.5 | V |
| Programming pin pulse width (CE) | t _{pp} | Chip disabled | | 100 | 180 | μs |
| Pulse width of programming voltage | t _p | V _{CC} = 5.5 V | 1 | | 40 | μs |
| Required current limit of power supply feeding program pin and output during program | I _L | V _{pp} = 33 V, V _{OUT} = 26 V, V _{CC} = 5.5 V | 250 | | | mA |
| Required time delay between disabling memory output and application of output programming pulse | t _{D1} | Measured at 10% levels | 70 | 80 | 90 | μs |
| Required time delay between removal of programming pulse and enabling memory output | t _{D2} | | 100 | | | ns |
| Output current during verification | I _{OLV1} | Chip enabled V _{CC} = 4.2 V | 11 | 12 | 13 | mA |
| | I _{OLV2} | Chip enabled V _{CC} = 6.0 V | 0.19 | 0.2 | 0.21 | mA |
| Address input voltage | V _{IH} | | 2.4 | 5.0 | 5.5 | V |
| | V _{IL} | | 0.0 | 0.4 | 0.8 | V |
| Maximum duty cycle during automatic programming of program pin and output pin | D.C. | t _p /t _c | | | 50 | % |

1/ T_C = +25°C.



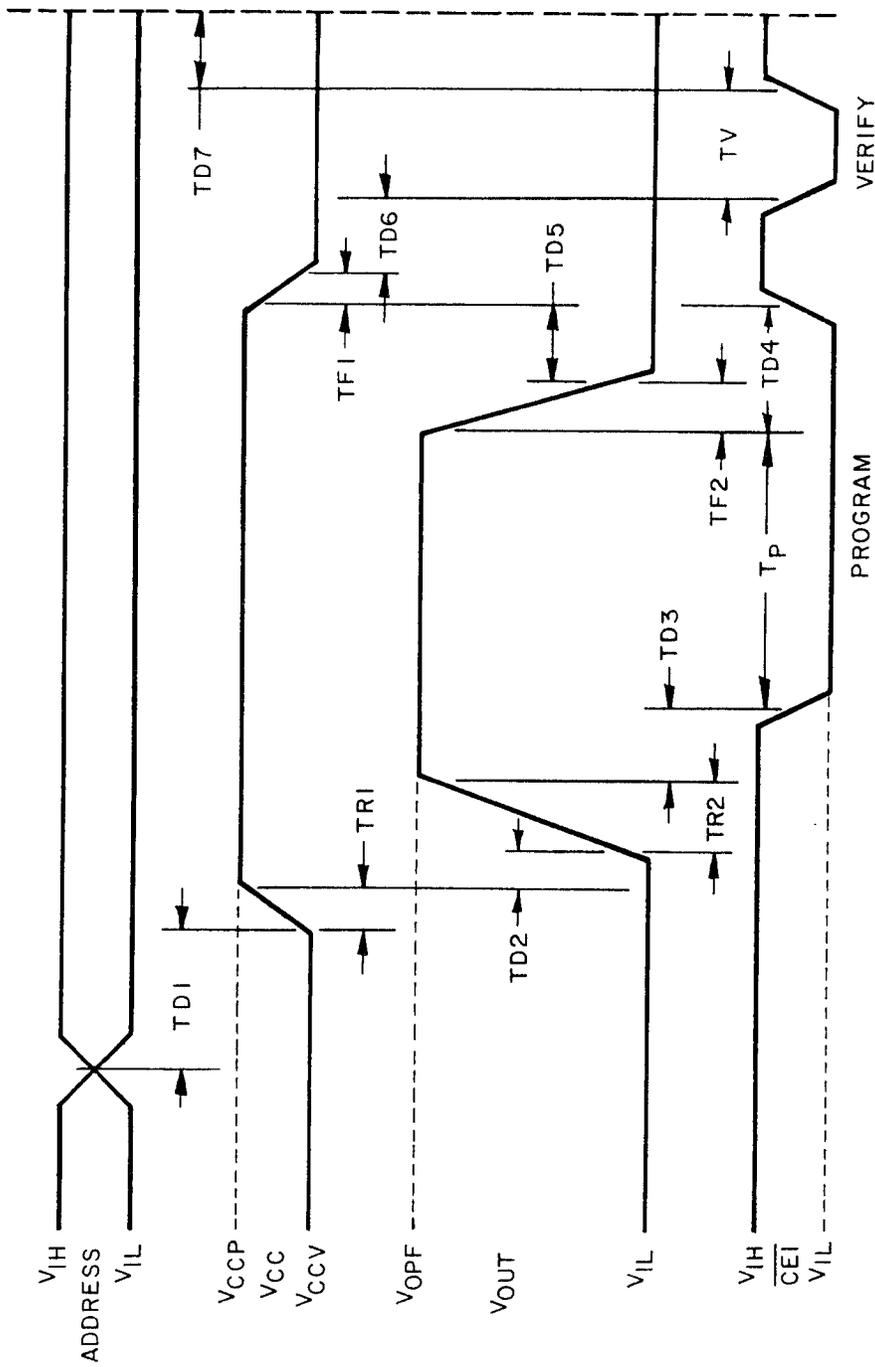
NOTE: All other waveform characteristics shall be as specified in table IV A.

FIGURE 6A. Programming voltage waveforms during programming procedure A.



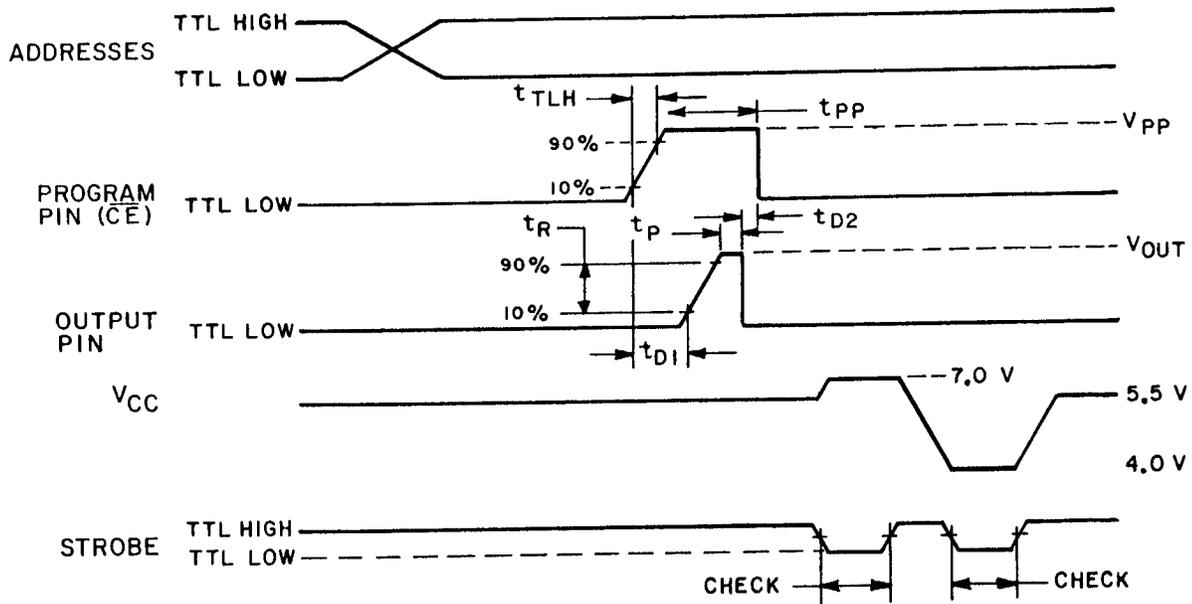
NOTE: All other waveform characteristics shall be as specified in table IV B.

FIGURE 6B. Programming voltage waveforms during programming procedure B.



- NOTES:
1. All other waveform characteristics shall be as specified in table IV C.
 2. Current clamp or voltage clamp will be needed.

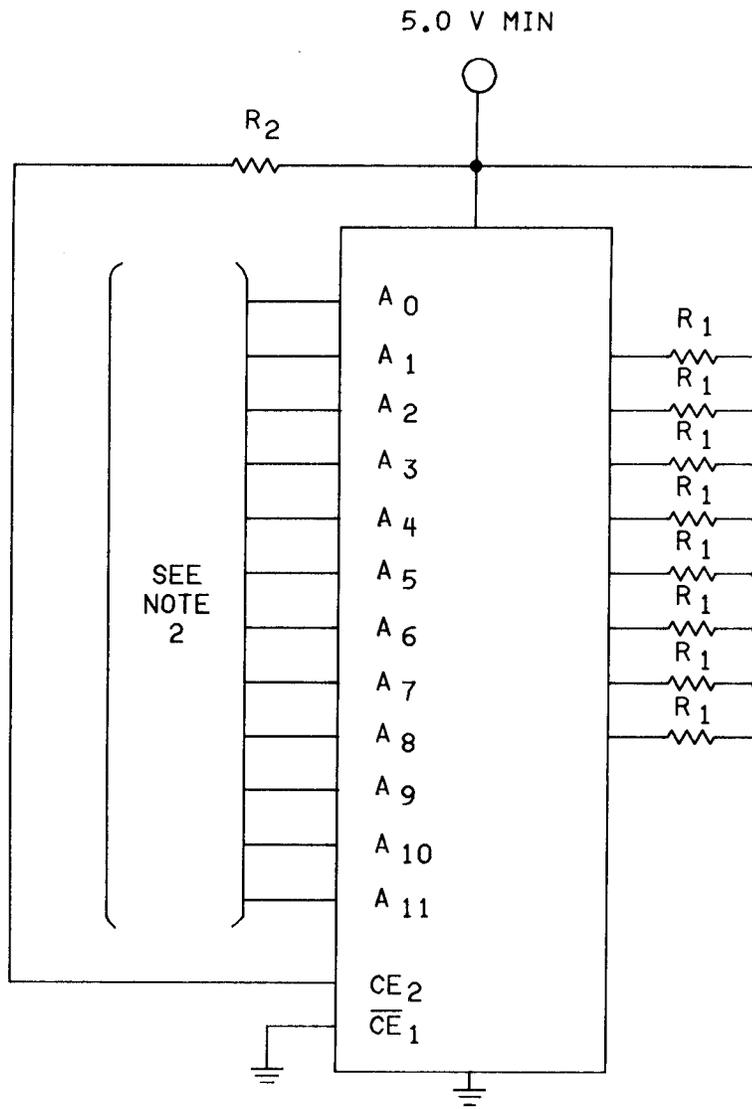
FIGURE 6C. Programming voltage waveforms during programming procedure C.



NOTES:

1. Output load is 0.2 mA and 12 mA during 6.0 V and 4.2 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVD.

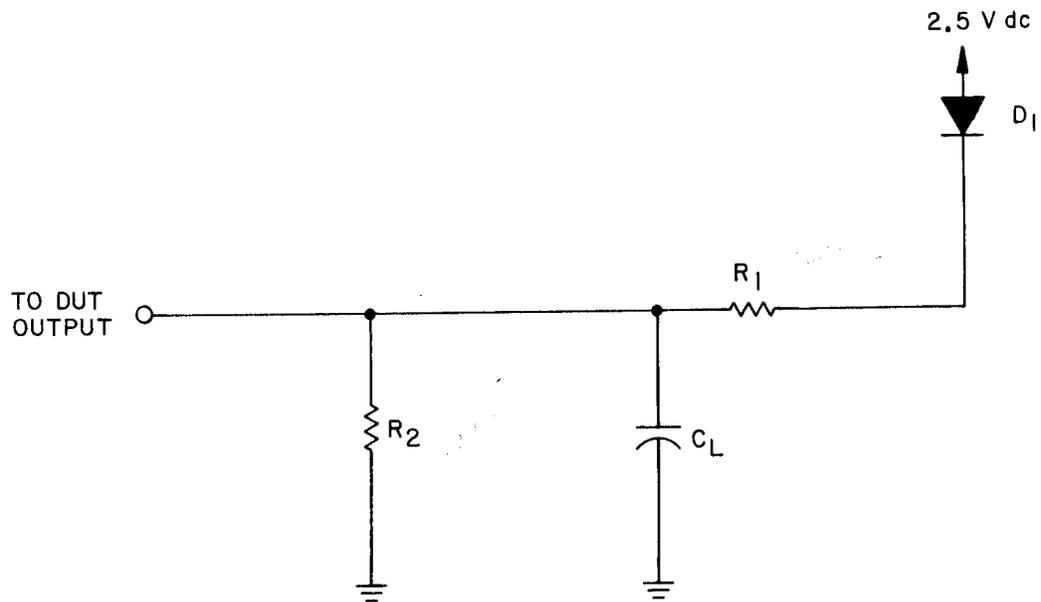
FIGURE 6D. Programming voltage waveforms during programming procedure F.



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5\%$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low or open.
3. Burn-in circuit may be used to perform this test. (See 4.2 d.) All address input shall be either high, low or open.
4. $R_2 = 1 \text{ k}\Omega \pm 5\%$.

FIGURE 7. Freeze-out test bias configuration.



NOTES:

1. $C_L = 50 \text{ pF}$, includes jig and probe capacitance.
2. $D_1 = 1N914$.
3. $R_1 = 160\Omega \pm 5\%$ for all 02 devices; $85\Omega \pm 5\%$ for all 01 devices, circuit C.
4. $R_2 = 1.2 \text{ k}\Omega \pm 5\%$.

FIGURE 8. Load circuit.

TABLE V. Input/output conditions for table III, subgroups 9, 10, 11, and 12. 1/ 2/

| Symbol | Terminal(s) | A | B | Units |
|---------------------------|-----------------|-----|-----|-------|
| V _{CC} | V _{CC} | 4.5 | 5.5 | V |
| V _{IH} | Logic inputs | 3.0 | 3.0 | V |
| V _{IL} | Logic inputs | 0.0 | 0.0 | V |
| V _{OH} <u>3/</u> | Logic outputs | 2.4 | 2.4 | V |
| V _{OL} <u>3/</u> | Logic outputs | 0.5 | 0.5 | V |

1/ Timing diagrams appear in figure 5.

2/ The output states shall be in accordance with the altered item drawing.

3/ Output compare levels for subgroups 9, 10, and 11.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original ~~equipment~~ design applications and logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

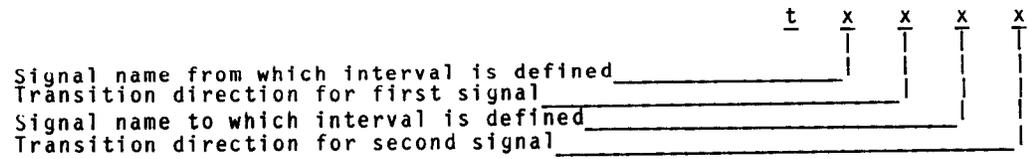
- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.

- g. Requirements for special lead lengths or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- i. Requirements for "JAN" marking.

6.4 Terms and definitions. The abbreviations, terms, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

| | | |
|--------------------------------------|-----------|---|
| V _{CC} | - - - - - | Supply voltage |
| AO-A11 | - - - - - | Address inputs, used to address 1 of 4096/8 bit locations in static storage array. |
| \overline{CE}_1 | - - - - - | Output-enable, used along with a second output-enable (CE_2) signal to control the state of the 8 data signals. |
| CE ₂ | - - - - - | Output enable |
| O1-O8 | - - - - - | Data output, 8 bit wide data bus through which data is accessed. |
| I _{CC} | - - - - - | Supply current |
| I _{OS} | - - - - - | Output short circuit current |
| I _{IH} , I _{IL} | - - - - - | Input leakage currents |
| I _{OHZ} , I _{O LZ} | - - - - - | High impedance output leakage currents |
| V _{IL} | - - - - - | Logical low input voltage |
| V _{IH} | - - - - - | Logical high input voltage |
| V _{OL} | - - - - - | Logical low output voltage |
| V _{OH} | - - - - - | Logical high output voltage |
| V _{IC} | - - - - - | Input clamp voltage |
| C _{IA} | - - - - - | Address input capacitance |
| C _{IE} | - - - - - | Output-enable input capacitance |
| C _o | - - - - - | Output capacitance |
| t _{AVQV} | - - - - - | Address access time |
| t _{ELQV} | - - - - - | \overline{CE}_1 access time |
| t _{EHQV} | - - - - - | CE_2 access time |
| t _{EHQZ} | - - - - - | \overline{CE}_1 disable time |
| t _{ELQZ} | - - - - - | CE_2 disable time |

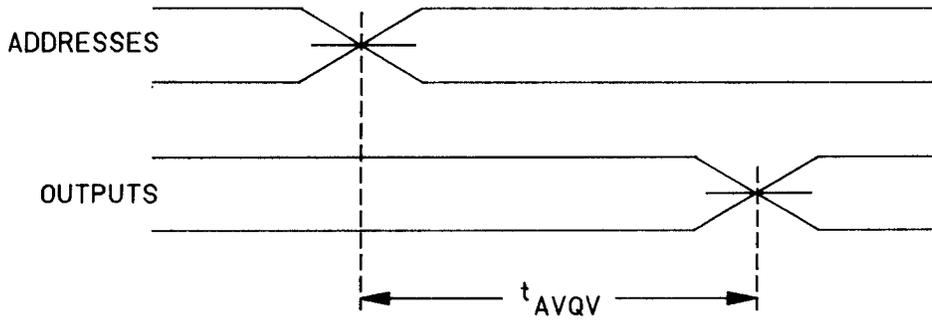
6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:



- a. Signal definitions:
- A = address
 - D = data in
 - Q = data out
 - E = output-enable

- b. Transition definitions:
- H = transition to high
 - L = transition to low
 - V = transition to valid
 - X = transition to invalid or don't care
 - Z = transition to off (high impedance)

Example:



The example shows address access time defined as t_{AVQV} time from address valid to output valid.

c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it.) On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d. Waveforms:

| WAVEFORM SYMBOL | INPUT | OUTPUT |
|-----------------|----------------------------------|-------------------------|
| | MUST BE VALID | WILL BE VALID |
| | CHANGE FROM H TO L | WILL CHANGE FROM H TO L |
| | CHANGE FROM L TO H | WILL CHANGE FROM L TO H |
| | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |
| | ————— | HIGH IMPEDANCE |

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistics support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

| <u>Military device type</u> | <u>Generic-industry type/manufacturer</u> | <u>Circuit designator</u> | <u>Fusible link</u> | <u>Symbol/CAGE number</u> |
|-----------------------------|---|---------------------------|---------------------|---------------------------|
| 02 | 76321 /Harris | A | NiCr | CDWD/34371 |
| 02 | 53S3281/Monolithic Memories | B | TiW | CECD/50364 |
| 02 | 29671 /Raytheon | F | NiCr | CRP/07933 |
| 01, 02 | 82HS321A/Signetics | C | ZVE * | CDKB/18324 |

* Zapped vertical emitter.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Preparing activity:
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

Agent:
DLA - ES

(Project 5962-0986)

User activities:
Army - SM
Navy - AS, CG, MC