

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 65,536 BIT SCHOTTKY, BIPOLAR,
PROGRAMMABLE READ-ONLY MEMORY (PROM),
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements of monolithic silicon, PROM microcircuits which employ thin film nichrome resistors (NiCr), titanium tungsten (TiW), polycrystalline silicon (polysilicon), platinum silicide, zapped vertical diode, or zapped vertical emitter as the fusible link or programming element. Two product assurance choices and a choice of case outlines and lead finishes are provide for each type and are reflected in the part number. A special test requirement is included in this specification to screen against devices that may contain excessive moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as follows:

Device type	Access times (ns)	Circuit
01	70	8192 words/8 bits per word PROM with active pullup and a third high impedance state output.
02	55	
03	50	
04	45	

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
J	D-3 (24-lead, 1/2" x 1 1/4"), dual-in-line package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package
L	D-9 (24-lead, 1/4" x 1 1/4"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}) 1/:	
Case J	40°C/W maximum
Case 3	60°C/W
Output voltage range	-0.5 V dc to +V _{CC}
Output sink current	100 mA
Maximum power dissipation (P _D) 2/	1.00 W
Maximum junction temperature (T _J)	+175°C

1/ Heat sinking is recommended to reduce junction temperature.

2/ Must withstand the added (P_D) due to the short circuit test (e.g., I_{OS}).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) - - -	2.0 V dc
Maximum low-level input voltage (V_{IL}) - - -	0.8 V dc
Normalized fan-out (each output) - - - - -	Output sink current $I_{OL} = 16$ mA at 0.5 V
	Output source current $I_{OH} = -2$ mA at 2.4 V
Case operating temperature range (T_C) - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.2.4 Case outlines. Case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements for each device class shall be as specified in table II and, where applicable, by the altered item drawing. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the acquisition contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1, tables II and III. It is recommended that users perform subgroups 1, 2, and 3, along with 7 and 8 at required access speeds after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition D or E using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$ minimum.
- b. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -2\text{ mA}$ $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.8\text{ V}$	A11	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 16\text{ mA}$ $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.8\text{ V}$	A11		0.5	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\text{ V}$, $I_{IN} = -10\text{ mA}$	A11		-1.0	V
High impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.2\text{ V}$	A11		50	μA
High impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$	A11		-50	μA
High level input current	I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 5.5\text{ V}$	A11		50	μA
Low level input current	I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0.5\text{ V}$	A11		-100	μA
Short-circuit output current	I_{OS}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.0\text{ V}$ <u>2/</u>	A11	-15	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0$; outputs = open	A11		185	mA
Propagation delay time, high-to-low level logic, address to output	t_{PHL1}	$V_{CC} = 4.5\text{ V}$ and 5.5 V ; $C_L = 50\text{ pF}$ See figure 5	01		70	ns
			02		55	
			03		50	
			04		45	
Propagation delay time, low-to-high level logic, address to output	t_{PLH1}	$V_{CC} = 4.5\text{ V}$ and 5.5 V ; $C_L = 50\text{ pF}$ See figure 5	01		70	ns
			02		55	
			03		50	
			04		45	
Propagation delay time, chip enabled to output (low and high level) (chip enable time)	t_{CEN}	$V_{CC} = 4.5\text{ V}$ and 5.5 V ; $C_L = 50\text{ pF}$ See figure 5	01,02		35	ns
			03,04		25	
			<u>3/</u>		<u>3/</u>	
Propagation delay time, chip disabled to output (high impedance)	t_{DIS}	$V_{CC} = 4.5\text{ V}$ and 5.5 V ; $C_L = 50\text{ pF}$ See figure 5	01,02		35	ns
			03,04		25	
			<u>3/</u>		<u>3/</u>	

1/ Complete terminal conditions shall be as specified in table III.

2/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

3/ t_{CEN} and $t_{DIS} = 35\text{ ns}$ maximum for device type 04, circuit B.

TABLE II. Electrical test requirements. 1/2/3/

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8,	1*, 2, 3, 7*, 8,
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3, 7, 8
Group D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ * indicates PDA applies to subgroups 1 and 7 (see 4.2c).

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

- d. The freeze-out test shall be conducted as a 100-percent screen on all class S devices having nichrome or platinum silicide as the fusing link. Within no more than 24 hours after completion of burn-in and prior to the final electrical test, all devices having nichrome or platinum silicide as the fusing link shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned at 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical test parameters shall be completed 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:

- (1) Connect devices in the electrical configuration of figure 6 or in the burn-in configuration of figure 4 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.
- (2) Reduce device temperature to $T_C = -10^\circ\text{C} \pm 2^\circ\text{C}$ with the bias cycled and maintain at that temperature for a minimum of 5 hours.
- (3) With the cycled bias maintained, allow T_C to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours after the completion of the 5-hour cold soak. T_C shall not exceed 35°C during this period.

(4) Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.

- e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7, 8, 9, 10, and 11 of group A shall be attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies the faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroup 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 5 tests.
- c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4, or equivalent, shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours except as permitted by method 1005 of MIL-STD-883.
- c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross-referenced in paragraph 6.5 herein with the manufacturer's symbol or CAGE number.

4.7 Programming procedure for circuit A.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7A and the programming characteristics of table IVa shall apply to these procedures.
- b. Address the word to be programmed by applying the appropriate voltages to address pins A0 through A12. Select the PROM by applying a low (V_{IL} level) to chip select input.
- c. Apply 5.0 V to V_{CC} for a read of the output to be programmed. The output to be programmed will be referred to as the selected output.
- d. Read the selected output and verify that it is in the unprogrammed logic '1' state.
- e. Set I_{CSP} (chip select programming current pulse) to I_{CSP} minimum (recommended value I_{CSP} minimum = 40 mA.)
- f. Raise V_{CC} to 6.5 V for programming.
- g. Deselect the PROM by applying 5 V to chip select.
- h. Raise all outputs to 12 V.
- i. Lower the voltage of the selected output below 5.5 V.
- j. Apply I_{CSP} to chip select.

- k. Check the bit to see if it has programmed by selecting the PROM, which is done by applying a low to chip select. Read the selected output. The output will read low if the bit has programmed. If the output reads low, continue with step 4.7.o. If the output still reads high, the bit has not been programmed; continue with step 4.7.l.
- l. Increment I_{CSP} by 10 mA. If I_{CSP} is less than or equal to I_{CSP} maximum (recommended value I_{CSP} maximum = 160 mA), repeat steps 4.7.g through 4.7.k.
- m. If I_{CSP} is greater than I_{CSP} maximum and the bit has not programmed, then go to 4.7.b and repeat the programming sequence (up to a maximum of 16 attempts total).
- n. If the bit is still unprogrammed, the device is considered a failure and no future attempts at programming should be made. The procedure then ends with this step.
- o. Lower V_{CC} to 0 V. Repeat the procedure from step 4.7.b until all desired bits in the memory have been programmed.
- p. After all desired bits in the memory have been programmed, raise V_{CC} to 4.5 V for the first pass final verification that all bits have been programmed correctly. If any bits read incorrectly, the device is a verify fail unit, and the procedure ends. If all bits read correctly, continue with step 4.7.q.
- q. Raise V_{CC} to 5.5 V for the second pass final verify. If any bits read incorrectly, the device is a verify fail unit. If all bits read correctly, the device is a passing unit.
- r. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

4.8 Programming procedures for circuit B. The programming characteristics on table IVb and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 7B and the programming characteristics of table IVb shall apply to these procedures.
- b. Output pins should be terminated with a 10-kilohm resistor to V_{CC} .
- c. Bypass V_{CC} to ground with a 0.01 μ F capacitor.
- d. Apply initial voltage of V_{IH} to the programming control pin (\overline{CE}) and appropriate voltage to chip enable pins (as applicable) in accordance with table IVb.
- e. Apply V_{IL} to all other pins.
- f. Select the word to be programmed by applying V_{IL} or V_{IH} on the appropriate address pins and reset t_p to 5 μ s.
- g. Wait t_{d1} and raise the V_{CC} pin to V_{CCP} .
- h. Wait t_{d2} and raise the corresponding output pin to V_{OPF} .
- i. Wait t_{d3} and lower the programming control pin (\overline{CE}) to V_{IL} for a duration of t_p .
- j. Simultaneously lower the output to V_{IL} and begin wait t_{d4} .
- k. Return the programming control pin \overline{CE} to V_{IH} .
- l. Wait t_{d5} and lower V_{CC} to V_{CCV} .

- m. Wait t_{d6} and lower input programming control pin \overline{CE} to V_{IL} for the duration of t_v .
- n. A properly blown fuse will read V_{0L} , and an unblown fuse will read V_{0H} .
- o. If the fuse is blown, go to 4.8.s.
- p. If fuse is unblown, go to 4.8.q.
- q. If t_p is less than $30 \mu s$, increment t_p by $5 \mu s$ and go to step 4.8.g. If t_p is equal or greater than $5 \mu s$, go to step 4.8.r.
- r. If t_p is equal to or greater than $30 \mu s$, then the device is a reject. STOP!
- s. Wait t_{d7} and select the next output or address to be programmed.
- t. Repeat steps 4.8b through 4.8n until all required addresses are programmed.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

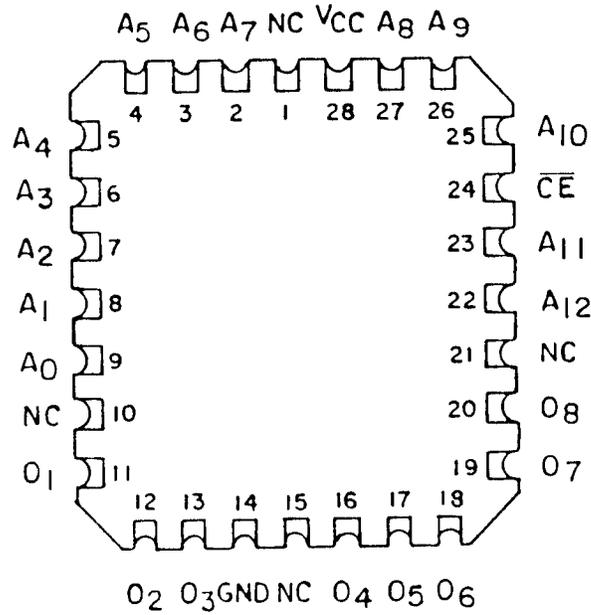
6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for use for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. Acquisition documents should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- i. Requirements for "JAN" marking.

Device types 01, 02, 03, and 04
Case 3



Device types 01, 02, 03, and 04
Case J and L

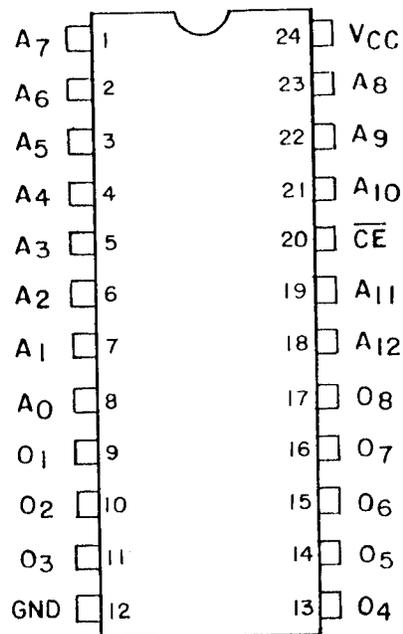


FIGURE 1. Terminal connections.

Device types 01, 02, 03, and 04

\overline{CE}	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₈	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁
L	X	X	X	X	X	X	X	X	X	X	X	X	X	*	*	*	*	*	*	*	*
H	X	X	X	X	X	X	X	X	X	X	X	X	X	OC							

(*) The outputs for all unprogrammed devices are high for both circuit A and circuit B.

NOTES:

1. X = Input may be high level, low level, or open circuit.
2. OC = Open circuit (high resistance output).
3. Program readout can only be accomplished with enable input at low level.

FIGURE 2. Truth table (unprogrammed).

Device types 01, 02, 03, and 04
Circuit A

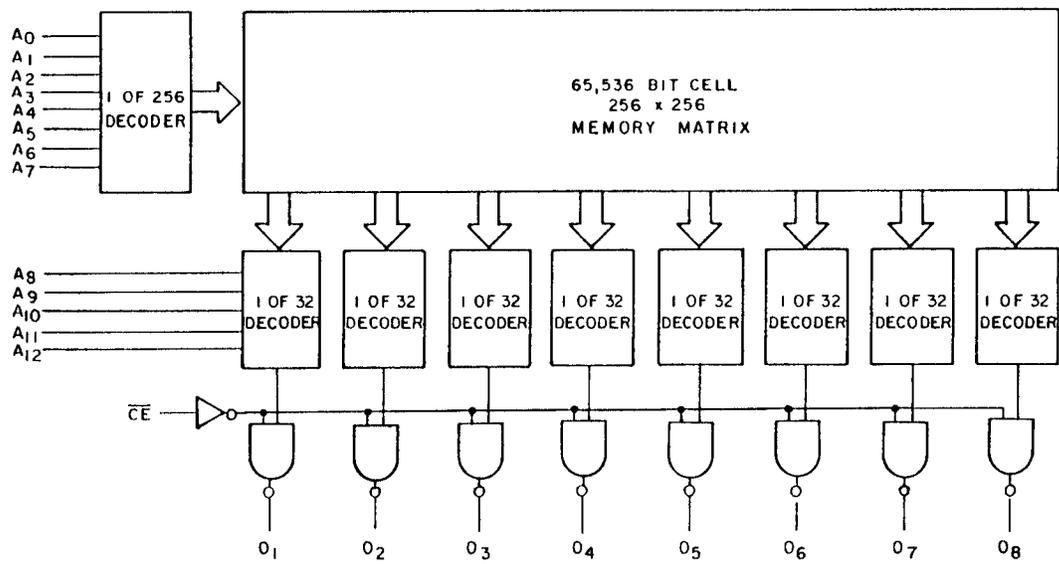


FIGURE 3. Functional block diagram.

Device types 01, 02, and 04
Circuit B

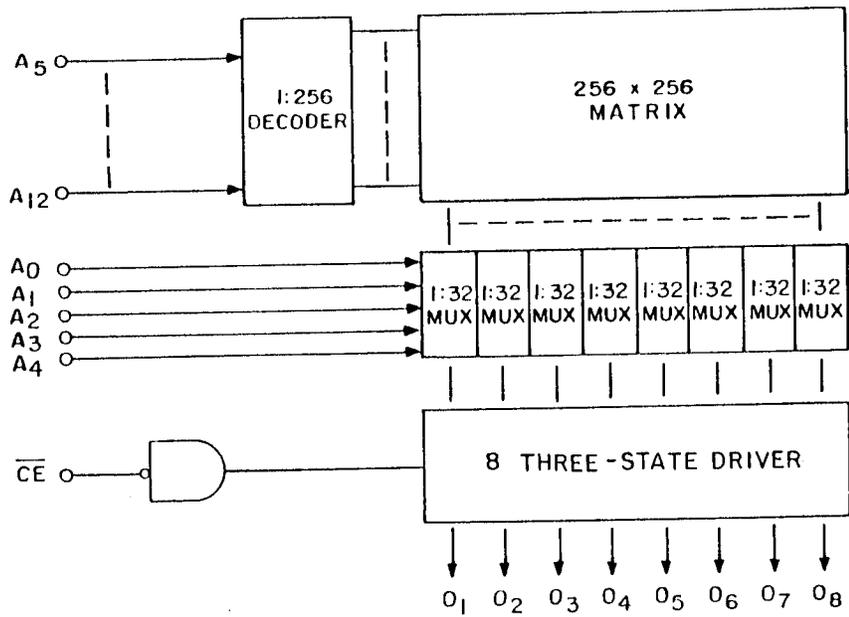
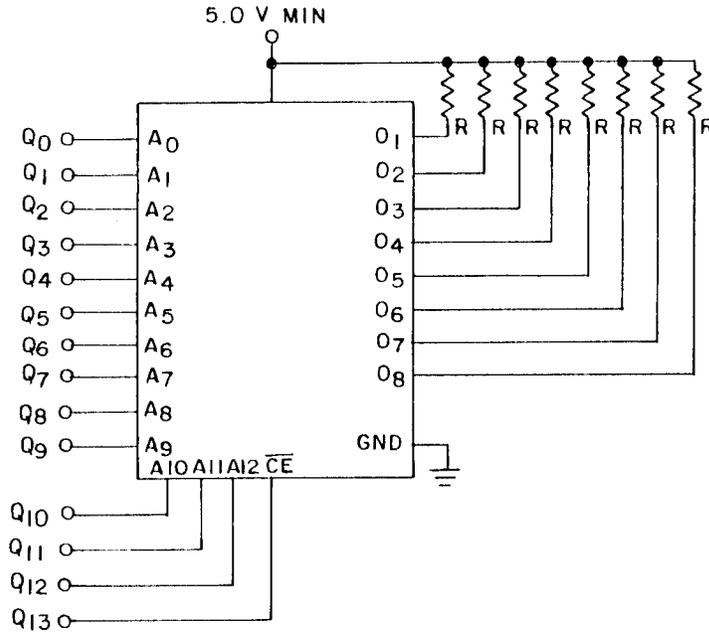


FIGURE 3. Functional block diagram - Continued.

Device types 01, 02, 03, and 04



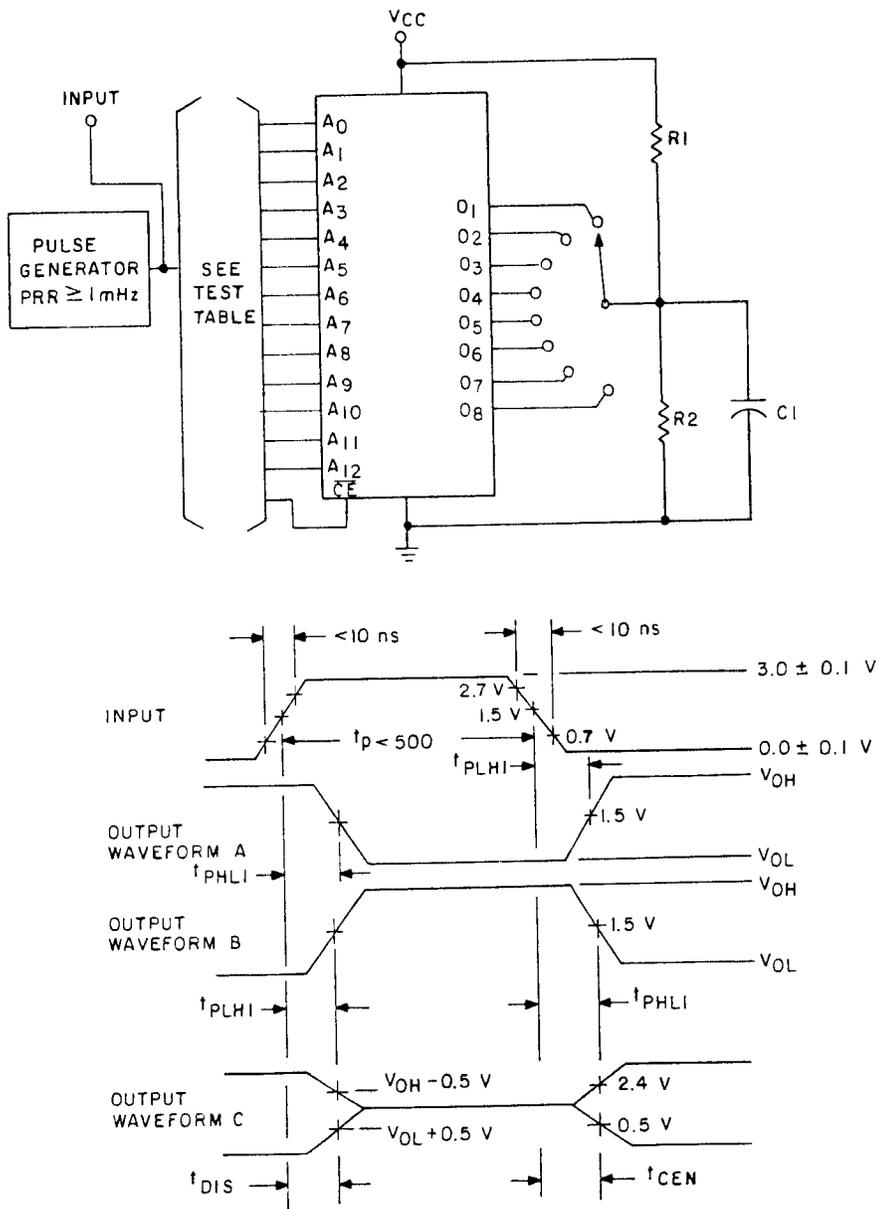
NOTES:

1. $R = 560\Omega \pm 5$ percent.
All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50 percent \pm 15 percent duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency (± 50 percent)
Q0	$f_0 = 100$ kHz Min
Q1	$f_1 = 1/2 f_0$
Q2	$f_2 = 1/2 f_1$
Q3	$f_3 = 1/2 f_2$
Q4	$f_4 = 1/2 f_3$
Q5	$f_5 = 1/2 f_4$
Q6	$f_6 = 1/2 f_5$
Q7	$f_7 = 1/2 f_6$
Q8	$f_8 = 1/2 f_7$
Q9	$f_9 = 1/2 f_8$
Q10	$f_{10} = 1/2 f_9$
Q11	$f_{11} = 1/2 f_{10}$
Q12	$f_{12} = 1/2 f_{11}$
Q13	$f_{13} = 1/2 f_{12}$

FIGURE 4. Burn-in and life test circuit.

Device types 01, 02, 03, and 04

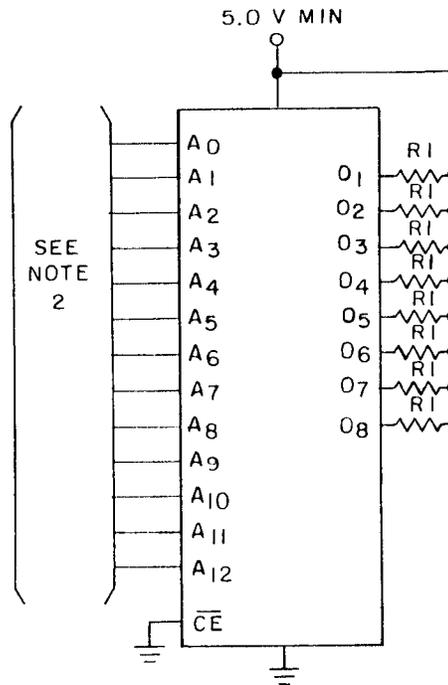


NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L = 50$ pF minimum, including jig and probe capacitances;
 $R_1 = 330\Omega \pm 25$ percent and $R_2 = 680\Omega \pm 20$ percent for t_{PHL1} and t_{PLH1} .
3. $C_L = 50$ pF, $R_1 = 3.6$ k Ω and $R_2 = 1.5$ k Ω , both ± 20 percent for t_{CEN} and t_{DIS} .
4. Outputs may be under load simultaneously.
5. For t_{CEN} and t_{DIS} , V_{OL} and V_{OH} must be measured for each part at the time of test.

FIGURE 5. Switching time test circuit.

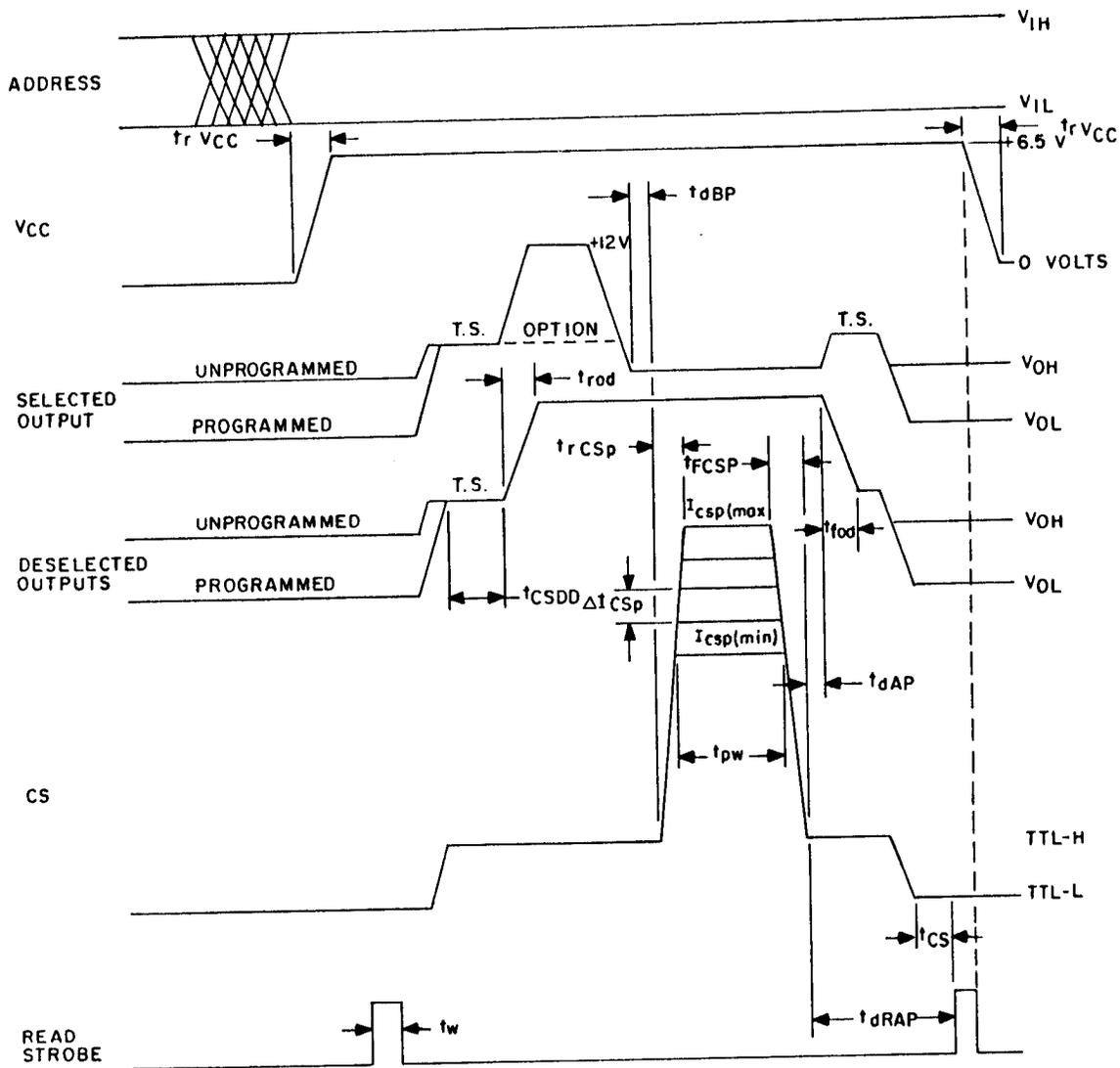
Device types 01, 02, 03, and 04



NOTES:

1. $R_1 = 4.7 \text{ k}\Omega \pm 5 \text{ percent}$. All bit outputs shall have separate identical loads.
2. All address inputs shall be either high, low, or open.
3. Burn-in circuit may be used to perform this test. (See 4.2.d) All address input shall be either high, low, or open.

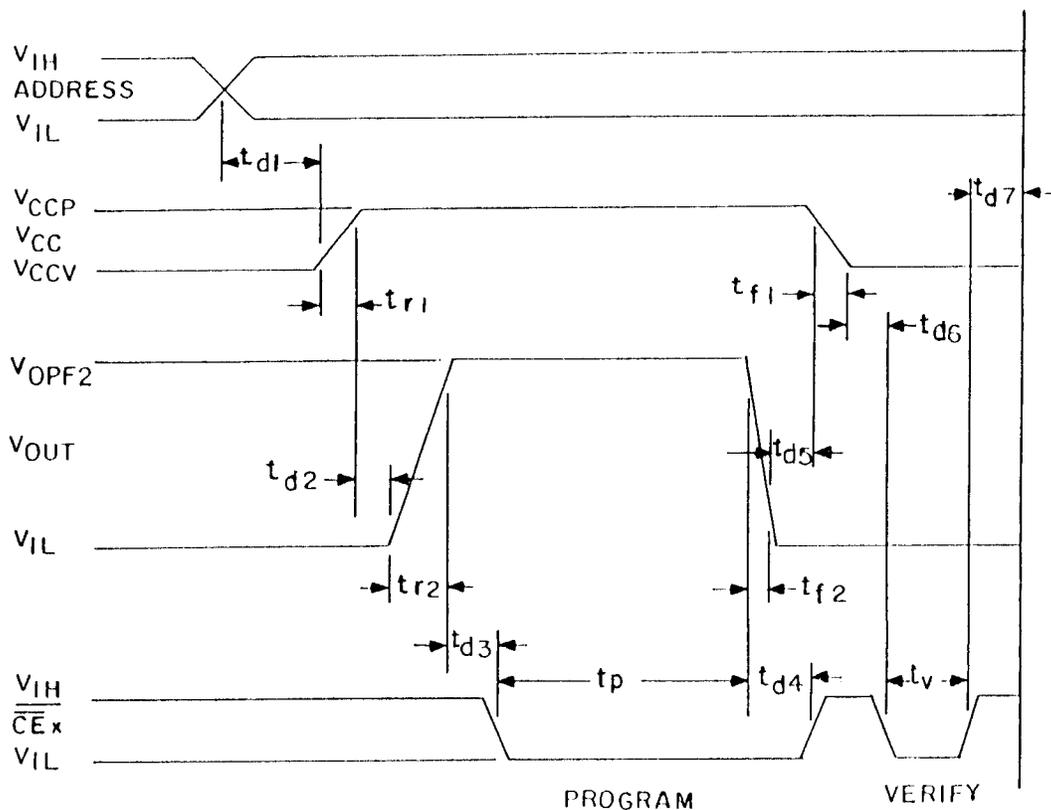
FIGURE 6. Freeze-out test bias configuration.



NOTES:

1. Typical output characteristics using a 1 kilohm pullup resistor to 5 volts. Twelve volts, TTL-H and TTL-L force voltages. T.S. is three-state.
2. All other waveform characteristics shall be as specified in table IVa.

FIGURE 7A. Programming voltage waveforms during programming for circuit A.



NOTE: All other waveform characteristics shall be as specified in table IVb.

FIGURE 7B. Programming voltage waveforms during programming for circuit B.

TABLE III. Group A Inspection for device types 01, 02, 03, and 04. Inputs are > 2.4 V or < 0.8 V. Outputs not designated are open or resistively coupled to ground or V_{CC}.

Subgroup	Symbol	MIL-STD-883 method	Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14								
1 T _C = +25°C	V _{IC}		Test no.	A7	A6	A5	A4	A3	A2	A1	A0	01	02	03	04	05									
				1	-10 mA																				
				2																					
				3																					
				4																					
				5																					
				6																					
				7																					
				8																					
				9																					
				10																					
				11																					
				12																					
				13																					
14																									
	V _{OL}	3007	15	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/	1/2/3/							
			16																						
			17																						
			18																						
			19																						
			20																						
			21																						
			22																						
				V _{OH}	3006	23	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/			
						24																			
						25																			
						26																			
						27																			
						28																			
29																									
30																									
	I _{IHL}	3009				31	10.5 V																		
						32																			
						33																			
						34																			
						35																			
						36																			
			37																						
			38																						
			39																						
			40																						
			41																						
			42																						
			43																						
			44																						
	I _{IHL}	3010	45	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V	15.5 V							
			46																						
			47																						
			48																						
			49																						
			50																						
			51																						
			52																						
			53																						
			54																						
			55																						
			56																						
			57																						
			58																						

See footnotes at end of table.

Table III. Group A inspection for device types O1, O2, O3, and O4 - Continued.
 Terminal conditions: Outputs not designated are open or resistively coupled to ground or V_{CC} . Inputs are > 2.4 V or < 0.8 V.

Subgroup	Symbol	A1 - STO-883 method	Test														Measured terminal	Limits		Units
			J	10	10	17	13	19	20	23	23	24	25	26	27	28		24	28	
1 $T_C = +25^\circ C$	V_{IC}	Test no.	1	06	07	08	A12	A11	05	A10	A9	A8	V_{CC}	A7	-1.0	V				
			2																	
			3																	
			4																	
			5																	
			6																	
			7																	
			8																	
			9																	
			10																	
			11																	
			12																	
			13																	
			14																	
V_{OL}	3007	"	15				11/3/	11/3/	0.5 V	3/11/3/	11/3/	11/3/	11/3/	31	0.5	V				
			16																	
			17																	
			18																	
			19																	
			20	16 mA																
			22																	
V_{OH}	3006	"	23										31	2.4	V					
			24																	
			25																	
			26																	
			27																	
			28	-2 mA																
			30																	
I_{IL}	3009	"	31										A7	-1.0	μA					
			32																	
			33																	
			34																	
			35																	
			36																	
			37																	
			38																	
			39																	
			40																	
			41																	
I_{IH}	3010	"	42										A7	5.0	μA					
			43																	
			44																	
			45																	
			46																	
			47																	
			48																	
			49																	
			50																	
			51																	
			52																	
53																				
54																				
55																				
56																				
57																				
58																				

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, 03, and 04 - Continued. Terminal conditions: Outputs not designated are open or resistively coupled to ground or VCC. Inputs are > 2.1 V or < 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
1 T _C = +25°C	I _{OHZ}		Case 3	A7	A6	A5	A4	A3	A2	A1	A0	J1	J2	J3	GND	J4	J5				
			59	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	5.2 V							
			60	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			61	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			62	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			64	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			65	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			66	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			2	I _{OLZ}		67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
68	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"		
69	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
70	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
71	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
72	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
73	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
74	"	"				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
3	I _{OS}		3011	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
7	Functional tests	3014	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/			
			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	
9 T _C = +25°C	t _{PHL1}	Ping-pong Figure 5 3003	84	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/			
			85	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/			
			86	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/		
			87	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	
			88	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	
10	t _{PL1}	Sequential Figure 5 3003	89	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/			
			90	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/		
11	t _{PL1}	Sequential Figure 5 3003	91	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/			
			92	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/		

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, 03, and 04 - Continued.
 Terminal conditions: Outputs not designated are open or resistively coupled to ground or V_{CC}. Inputs are > 2.4 V or < 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case no.	15	16	17	18	19	20	21	22	23	24	Limits		Units				
														Measured terminal	Min		Max			
1 T _C = +25°C	I _{OHZ}		Test no.	06	07	08	412	A11	OE	A10	A9	A6	V _{CC}							
				59			1/	1/	1/	1/	1/	1/	1/	1/	5.5 V			50	mA	
				60																
				61																
				62																
				63																
				64	5.2 V															
				65	5.2 V															
				66																
2	V _{OLZ}			07																
				67																
				68																
				69																
				70																
				71																
				72	0.5 V															
				73	0.5 V															
				74																
3	I _{OS}			75																
				76																
				77																
				78																
				79																
				80	GND															
				81	GND															
				82																
7	Functional tests	3014		34	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs			
9 T _C = +25°C	t _{PHL1}	Ping-pong Figure 5 3003		85	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	ns			
10	t _{PLH1}	Ping-pong Figure 5 3003		86	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	ns			
11	t _{CEV}	Sequential Figure 5 3003		87	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	ns			
12	t _{DIS}	Sequential Figure 5 3003		88	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	0/	ns			

- 1/ For programmed devices, select and appropriate address to acquire the desired output state.
 $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$.
- 2/ V_{OL} : For unprogrammed circuit B devices (01, 02, and 04), apply 12.0 V on pin 8 (A_0), apply 0.6 V on pins 1, 2, 3, and 4 (A_7 , A_6 , A_5 , A_4), and 2.2 V on pins 5, 6, and 7 (A_3 , A_2 , A_1).
- 3/ V_{OL} : For unprogrammed circuit A devices (01, 02, 03, and 04), apply 12.0 V on pin 3 (A_5), apply 3 V on pin 7 (A_1) and 0 V on all remaining inputs (A_0 , A_2 , A_3 , A_4 , A_6 , A_7 , A_8 , A_9 , A_{10} , A_{11} , A_{12} and CE).
- 4/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. Terminal conditions shall be as follows:
 - a. Inputs: H = 3.0 V, L = GND.
 - b. Outputs: Output voltage shall be either.:
 - (1) H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator.
 - (2) H > 2.4 V and L < 0.5 V maximum when using a high-speed checker single comparator.
 - c. The functional tests shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.
 - d. The outputs are loaded in accordance with figure 5.
- 5/ N^2 test (programmed PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PHL1} , t_{PLH1} . Each bit in the pattern is fixed by being programmed with a 1 or 0. A description is as follows:
 - a. Each word, starting with word 0 is used as the base bit.
 - b. The base bit is read and then every other bit within the array, always returning to the base bit between each of the other locations in the array.
 - c. The base bit is then incremented and step 2 repeated. This continues until the final word in the array becomes the base bit and step 2 is completed.
 - d. Pass execution time is $(8192)^2 \times \text{cycle time}$.
 - e. N^2 test shall be performed with $V_{CC} = 4.5 \text{ V}$ and 5.5 V .
- 6/ The outputs are loaded in accordance with figure 5.
- 7/ Sequential test (programmed PROM). This program will test all bits in the array for t_{CEN} and t_{DIS} . A description is as follows:
 - a. Each word in the pattern is tested from the enable lines to the output lines for recovery.
 - b. Word 0 is addressed. Same enable sequence as above.
 - c. Word 1 is addressed. Same enable sequence as above.
 - d. The reading procedure continues until word 8192 is reached.
 - e. Pass execution time $8192 \times \text{cycle time}$.
 - f. The sequential test shall be performed with $V_{CC} = 4.5 \text{ V}$ and 5.5 V .
- 8/ t_{PHL1} , $t_{PLH1} = 70 \text{ ns}$ for device type 01. t_{PHL1} , $t_{PLH1} = 50 \text{ ns}$ for device type 03.
 t_{PHL1} , $t_{PLH1} = 55 \text{ ns}$ for device type 02. t_{PHL1} , $t_{PLH1} = 45 \text{ ns}$ for device type 04.
- 9/ t_{CEN} , $t_{DIS} = 35 \text{ ns}$ for devices types 01 and 02, circuit A and circuit B.
 t_{CEN} , $t_{DIS} = 25 \text{ ns}$ for devices types 03 and 04 for only circuit A.
 t_{CEN} , $t_{DIS} = 35 \text{ ns}$ for devices type 04 for only circuit B.

TABLE IVa. Programming characteristics for circuit A.

Current-pulse programming specifications ^{1/}						
Symbol	Parameter	Min	Recommended value	Max	Units	Comments
Power supply						
V _{CC}	Power supply voltage	6.4	6.5	6.6	V	Typical I _{CC} at 6.5 V = 250 mA
t _{rVCC}	Power supply rise time ^{2/}	0.2	2.0		μs	
t _{fVCC}	Power supply fall time	0.2	2.0		μs	
t _{ON}	V _{CC} ON time	<u>3/</u>				See programming timing diagram
t _{OFF}	V _{CC} OFF time	<u>4/</u>				
	Duty cycle for V _{CC}			50	%	t _{ON} /(t _{OFF} + t _{ON})
Read strobe ^{5/}						
t _W	Fuse read time		1.0		μs	Machine cycle
t _{dRAP}	Delay to read after programming		3.0		μs	Verify
t _{CS}	Chip enable	0.1	1.0		μs	
Output deselect						
V _{OS}	Output deselect voltage	11.8	12	12.5	V	
I _{OS}	Output deselect current limit	20	50	100	mA	
V _{VS}	Output voltage select		5.0	5.5	V	TTL H or L
t _{rod}	Output deselect rise time	1.0	1.0	2.0	μs	
t _{fod}	Output deselect fall time	0.1	0.1	1.0	μs	
t _{CSDD}	Deselect chip to deselect output	0.1	1.0		μs	

See footnotes at end of table.

TABLE IVa. Programming characteristics for circuit A - Continued.

Current-pulse programming specifications ^{1/}						
Symbol	Parameter	Min	Recommended value	Max	Units	Comments
Programming current-pulse train on chip select						
I _{CSp} (min)	Initial current pulse		40	60	mA	
I _{CSp} (max)	CS programming current limit	155	160	180	mA	Apply current pulse to chip select pin 20
V _{CSp} (max)	CS programming voltage limit	24	25	26	V	
t _{rcsp}	Programming pulse rise time	160	100	100	mA/μs	
t _{dBP}	Delay to initial programming pulse	2.0	3.0		μs	
t _{dAP}	Delay after programming pulse	1.0	1.0		μs	
t _{pW}	Programming pulse widths	6.0	7.0	9.0	μs	
t _{fCSp}	Programming pulse fall time ^{2/}	0.1	0.1	.02	μs	
ΔI _{CSp}	Current pulse step increase	5.0	10.0	10.0	mA	
	Duty cycle for programming pulses	10	50	50	%	Each successive pulse is increased by I _{CSp}

1/ Recommended programming temperature T_C = +25°C ±10°C.

2/ Rise and fall times are from 10 to 90 percent.

3/ Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

4/ t_{OFF} is equal to or greater than t_{ON}.

5/ Proceed to next address after read strobe indicates programmed cell.

TABLE IVb. Programming characteristics for circuit B.

Parameter	Symbol	Conditions <u>1/</u>	Limits			Unit
			Min	Recommended	Max	
Programming voltage to V_{CC}	V_{CCP}	$I_{CCP} = 450 \pm 75 \text{ mA}$ <u>2/</u>	8.5	8.75	9.0	V
Verifying voltage	V_{CCV}		4.75	5.0	5.25	V
Input voltage high level "1"	V_{IH}	$I_{IH} = 50 \text{ } \mu\text{A}$	2.4	3.0	5.5	V
Input voltage low level "0"	V_{IL}	$I_{IL} = 500 \text{ } \mu\text{A}$	0.0	0.0	0.5	V
Forced output current	I_{OPF}		150	185	220	mA
Forced output voltage	V_{OPF}	<u>3/</u>	20		21	V
V_{CC} delay time	t_{d1}	50% ADD to 10% V_{CCP}	10	10	25	μs
V_{OUT} delay time	t_{d2}	90% V_{CCP} to 10% V_{OUT}	1	1	5	μs
Pulse sequence delays	t_{d3} thru t_{d8}		1	1	10	μs
V_{CC} rise time	t_{r1}	0% to 100%	4	7	8	μs
V_{OUT} rise time	t_{r2}	10% to 90%	3	10	17	μs
V_{CC} fall time	t_{f1}	100% to 0%	2	4	10	μs
V_{OUT} fall time	t_{f2}	100% to 0%	4	7	20	μs
CE programming	t_p	Pulse width 10% to 10% Rise time slew rate 1.0 V/ns maximum Fall time slew rate 10 V/ns maximum	5	10	30	μs
CE verify pulse	t_v	Pulse width 10% to 10%	5	5	10	μs

1/ $T_A = +25^\circ\text{C}$.

2/ Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.

3/ V_{OPF} supply should regulate to $\pm 0.25 \text{ V}$ at I_{OPF} . Maximum slew rate for V_{OPF} should be 1.0 V/ μs .

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

- GND - - - - - Ground zero voltage potential.
- V_{IN} - - - - - Voltage level at an input terminal.
- V_{IC} - - - - - Input clamp voltage.
- I_{IN} - - - - - Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type/manufacturer</u>	<u>Circuit designator</u>	<u>Fusible link</u>	<u>Symbol CAGE number</u>
01	(93Z665,93Z667 ^{1/})-70/Fairchild	A	ZVE ^{2/}	CFJ/07263
01	82HS641A-70/Signetics	B	ZVD ^{3/}	CDKB/18324
02	(93Z665,93Z667 ^{1/})-55/Fairchild	A	ZVE	---
02	82HS641A-55/Signetics	B	ZVD	---
03	(93Z665,93Z667 ^{1/})-50/Fairchild	A	ZVE	---
04	(93Z665,93Z667 ^{1/})-45/Fairchild	A	ZVE	---
04	82HS641A-45/Signetics	B	ZVD	---

^{1/} 93Z667 is the only part packaged in the D-9 case and no other case.
^{2/} Zapped vertical diode.
^{3/} Zapped vertical emitter.

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17

Review activities:
 Army - AR, MI
 Navy - OS, SH, TD
 Air Force - 11, 19, 85, 99
 DLA - ES

Agent:
 DLA - ES
 (Project 5962-0987)

User activities:
 Army - SM
 Navy - AS, CG, MC