Qualification requirements have been removed.

INCH-POUND

MIL-M-38510/22C
27 FEBRUARY 1989
SUPERSEDING
MIL-M-38510/22B
31 October 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, HIGH-SPEED, TTL, FLIP-FLOPS MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, high speed, TTL, bistable logic micorcircuits. Qualification requirements are removed for device types 01, 02, 03, 05, and 06. These device types are inactive for new design after the date of this revision. For the remaining device type, 04, two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. Device types shall be as shown in the following:

Device type 1/	Circuit
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop
03	Dual D-type edge-triggered flip-flop
04	Dual J-K master-slave flip-flop
05	Single J-K edge-triggered flip-flop
06	Dual J-K edge-triggered flip-flop

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
A	F-1 (14-lead, 1/4" x 1/4"), flat package
B	F-3 (14-lead, 1/4" x 1/8"), flat package
C	D-1 (14-lead, 1/4" x 3/4"), dual-in-line package
D	F-2 (14-lead, 1/4" x 3/8"), flat package
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

1/ Qualification requirements are removed for device types 01, 02, 03, 05, and 06.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center AFSC, RADC/RBE-2, Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.3 Absolute maximum ratings.

Supply voltage range - - - - - - - - - - - - -	-0.5 to 7.0 V dc
Input voltage range- - - - - - - - - - - - - -	-1.5 V dc at 12 mA to 5.5 V dc
Storage temperature range- - - - - - - - - - -	-65°C to 150°C
Maximum power dissipation per flip-flop (P_D):	2/
Device types 01, 02, 03, and 04 1/- - - -	137 mW
Device types 05 and 06 1/- - - - - - - - -	210 mW
Lead temperature (soldering, 10 seconds) - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Flat package - - - - - - - - - - - - - - - -	0.09°C/mW
Dual-in-line package - - - - - - - - - - - -	0.08°C/mW
Junction temperature (T_J)- - - - - - - - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage- - - - - - - - - - - - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage- - - - - -	2.0 V dc
Maximum low level input voltage - - - - - -	0.8 V dc
Normalized fanout (each output): 3/	
Device types 01, 02, 04, 05, and 06 1/- -	10 maximum
Device type 03 1/- - - - - - - - - - - - - -	10 maximum (low logic) 20 maximum (high logic)
Case operating temperature range (T_C) - - -	-55°C to +125°C
Width of clock pulse, t_p (clock):	
Device types 01, 02, and 04 1/ - - - - - -	12 ns, minimum
Device type 03 1/- - - - - - - - - - - - - -	15 ns, minimum
Device types 05 and 06 1/- - - - - - - - -	10 ns, minimum
Width of preset or clear pulse:	
Device types 01, 02, 04, 05, and 06 1/ -	16 ns, minimum
Device type 03 1/- - - - - - - - - - - - - -	25 ns, minimum
Input setup time $t_{(setup)}$:	
Device types 01, 02, and 04 1/ - - - - - -	> t_p(clock)
Device type 03 1/- - - - - - - - - - - - - -	15 ns, minimum (low level data) 10 ns, minimum (high level data)
Device types 05 and 06 1/- - - - - - - - -	10 ns, minimum (high level data) 13 ns, minimum (low level data)
Input hold time $t_{(hold)}$ - - - - - - - - - - -	5 minimum

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard, form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

1/ Qualification requirements are removed for device types 01, 02, 03, 05, and 06.
2/ Must withstand the added P_D due to short circuit condition (e.g., I_{OS}) at one output for 5 seconds duration.
3/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Schematic circuits. Schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in the specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS), as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained by the agent activity and will be available upon request.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification and quality conformance by device class are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used for device types 01, 02, 03, 05, and 06.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 3 (see MIL-M-38510, appendix E).

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line; not necessarily the line producing the device type described herein. This shall apply only for device types 01, 02, 03, 05, and 06.

3.10 Certification. Certification in accordance with MIL-M-38510 is not required for device types 01, 02, 03, 05, and 06 but shall be retained for device type 04.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55^{\circ}C < T_C < +125^{\circ}C$ unless otherwise specified	Device types	Terminals (device type) 01	02	03	04	05	06	Limits Min	Max	Unit
High level output voltage	V_{OH}	V_{IN} = 0.8 V V_{CC} = 4.5 V I_{OH} = -500 µA	01,02							2.4		V
		I_{OH} = -1 mA	03									
		I_{OH} = -0.5 mA	04,05, 06									
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 20 mA									0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -12 mA T_C = +25°C									-1.5	V
Low level input current	I_{IL1}	V_{CC} = 5.5 V V_{IN} = 0.4 V		J, K Clock	J, K Clock	D	J, K Clock	Preset J, K	J, K Clear	-1.0	-2.0	mA
Low level input current	I_{IL2}	V_{CC} = 5.5 V V_{IN} = 0.4 V	01,02, 03,04	Preset Clear	Clear	Preset Clock Clear	Preset Clear			-2.0	-4.0	mA
			05,06					Clock	Clock	-2.0	-4.8	
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.4 V		J, K	J, K	D	J,K	J, K,	J, K		50	µA
High level input current	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02, 03,04	J, K	J, K	D	J, K	J, K			100	µA
			05,06						J, K		1	mA
High level input current	I_{IH3}	V_{CC} = 5.5 V V_{IN} = 2.4 V	01,02, 03,04,05	Clear Preset	Clear	Clock Preset	Preset Clock Clear	Preset			100	µA
			06						Clock	-1	1	mA
High level input current	I_{IH4}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02, 03,04,05	Clear Preset	Clear	Clock Preset	Preset Clock Clear	Preset			200	µA
			06						Clock		1	mA
High level input current	I_{IH5}	V_{CC} = 5.5 V V_{IN} = 2.4 V	01,02	Clock	Clock						100	µA
			03			Clear					150	µA
			05					Clock			-1	mA
			06						Clear		100	µA
High level input current	I_{IH6}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02	Clock	Clock						200	µA
			03			Clear					300	µA
			05,06					Clock	Clear		1	mA
Short circuit output current 2/	I_{OS}	V_{CC} = 5.5 V V_{IN} = 0								-40	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V	01								25	mA
			02,03,04								50	
			05								38	
			06								76	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $-55^{\circ}C < T_C < +125^{\circ}C$ unless otherwise specified	Device types	Terminals (device type) 01	02	03	04	05	06	Limits Min	Max	Unit
Maximum clock frequency 3/	f_{MAX}	C_L = 50 pF										MHz
		R_L = 280Ω										"
		Figure 5	01							20		"
		Figure 7	02							20		"
		Figure 9	03							28		"
		Figure 12	04							20		"
		Figure 14	05							30		"
		Figure 16	06							30		"
Propagation delay to a logical 1 (clear or preset to output)	t_{PLH1}	C_L = 50 pF										
		R_L = 280Ω										
		Figure 4	01							2	20	ns
		Figure 6	02							"	20	"
		Figure 8	03							"	27	"
		Figure 11	04							"	20	"
		Figure 13	05							"	28	"
		Figure 15	06							"	18	"
Propagation delay to a logical 0 (clear or preset to output)	t_{PHL1}	C_L = 50 pF										
		R_L = 280Ω										
		Figure 4	01							"	31	"
		Figure 6	02							"	31	"
		Figure 8	03							"	38	"
		Figure 11	04							"	32	"
		Figure 13	05							"	28	"
		Figure 15	06							"	46	"
Propagation delay to a logical 1 (clock to output)	t_{PLH2}	C_L = 50 pF										
		R_L = 280Ω										
		Figure 5	01							"	28	"
		Figure 7	02							"	35	"
		Figure 9 and 10	03							"	22	"
		Figure 12	04							"	28	"
		Figure 14	05							"	23	"
		Figure 16	06							"	23	"
Propagation delay to a logical 0 (clock to output)	t_{PHL2}	C_L = 50 pF										
		R_L = 280Ω										
		Figure 5	01							"	37	"
		Figure 7	02							"	42	"
		Figure 9 and 10	03							"	28	"
		Figure 12	04							"	36	"
		Figure 14	05							"	28	"
		Figure 16	06							"	28	"

1/ Qualification requirements are removed for device types 01, 02, 03, 05, and 06.

2/ Not more than one output should be shorted at a time.

3/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, and C inspections (see 4.4.1, 4.4.2, and 4.4.3). After qualification of one or more electrically and structurally similar types with a single lead finish, other lead finishes of the same case outline may be qualified by submitting a single type in the qualified case outline to the group B, subgroup 3 test and the group C, subgroup 1, 3, and 4 tests. Qualification inspection is not required for device types 01, 02, 03, 05, and 06.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on device type 04, prior to qualification and quality conformance inspection, and on device types 01, 02, 03, 05, and 06, prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883).

(1) Test condition D, E, or F using the circuit shown on figure 3, or equivalent.

(2) T_A = +125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions, or equivalent:

(1) Test condition D or E using the circuit shown on figure 3, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004)	1*,2,3,7,9, 10,11	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11	1,2,3,7,9
Group C end point electrical parameters (method 5005)	N/A	1,2,3
Additional electrical subgroups for group C periodic inspection	N/A	10,11
Group D end point electrical parameters (method 5005)	1,2,3	1,2,3

*PDA applies to subgroup 1 (see 4.3c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity for device types 01, 02, 03, 05, and 06. In addition, notification to the qualifying activity for device type 04, if applicable.

e. For device type 04 requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options, device type 04. Requirements for packaging and packing, device types 01, 02, 03, 05, and 06.

g. Requirements for carriers, special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

h. Requirements for "JAN" marking. (This shall apply to device type 04 only.)

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - - - - Ground zero voltage potential.
I_{IN} - - - - - - - - - - - - - - - - Current flowing into an input terminal.
V_{IN} - - - - - - - - - - - - - - - - Voltage level at an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Generic test data. This shall apply only to device types 01, 02, 03, 05, and 06. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on data codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.6 In-lieu-of documents. MIL-M-0038510/25C(19) was issued as an "in-lieu-of" document for MIL-M-38510/25B. This revision MIL-M-38510/25D supersedes MIL-M-0038510/25C(19), MIL-M-38510/25C, MIL-M-38510/25B.

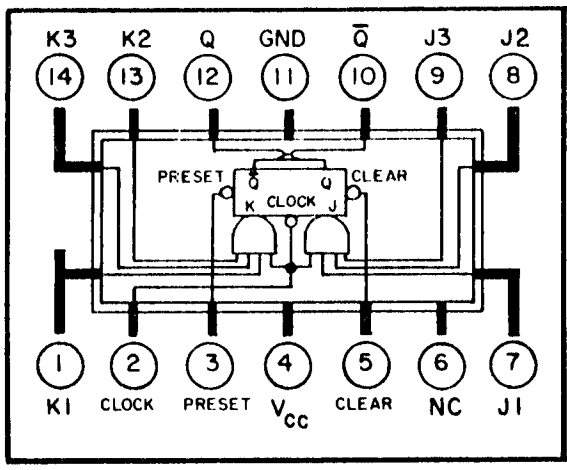
6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01*	54H72 (circuit A)
01*	S54H72 (circuit B)
02*	54H73 (circuit A)
02*	MC54H73 (circuit B)
02*	S54H73 (circuit C)
03*	54H74 (circuit A)
03*	MC54H74 (circuit B)
03*	S54H74 (circuit C)
04	54H76 (circuit A)
04	S54H76 (circuit B)
05*	54H101 (circuit A)
05*	MC54H101 (circuit B)
05*	S54H101 (circuit C)
06*	54H103 (circuit A)
06*	54H103 (circuit B)
06*	S54H103 (circuit C)

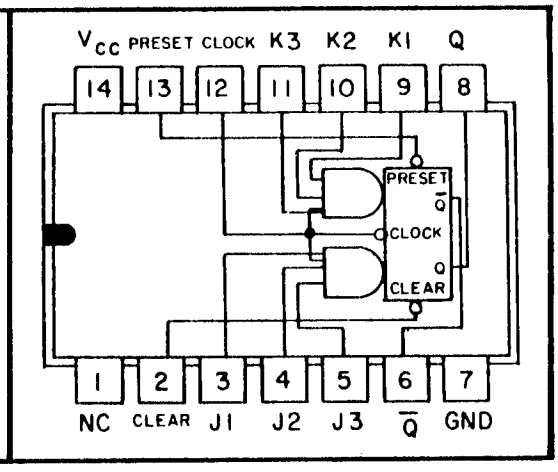
* Qualification requirements are removed for device types 01, 02, 03, 05, and 06.

Device type 01 (See note)

Cases A, B, and D

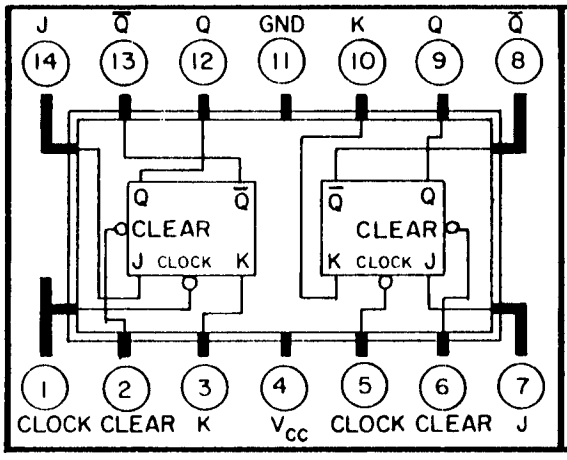


Case C

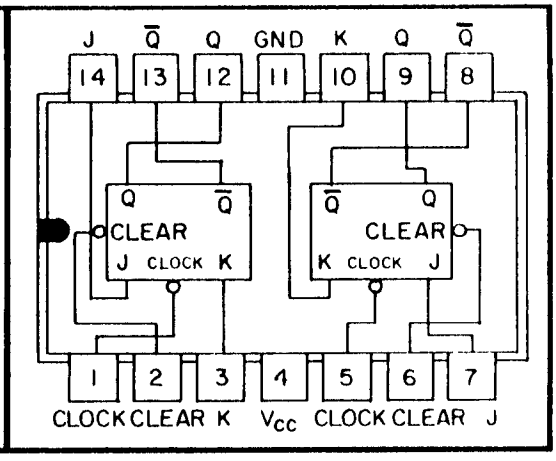


Device type 02 (See note)

Cases A, B, and D



Case C

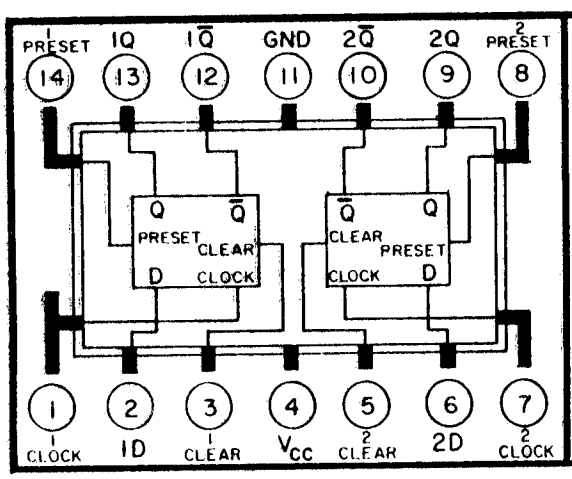


NOTE: Qualification requirements are removed for this device type.

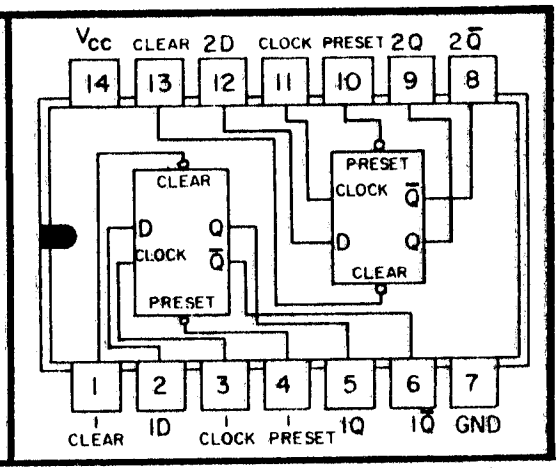
FIGURE 1. Terminal connections.

Device type 03 (See note)

Cases A, B, and D

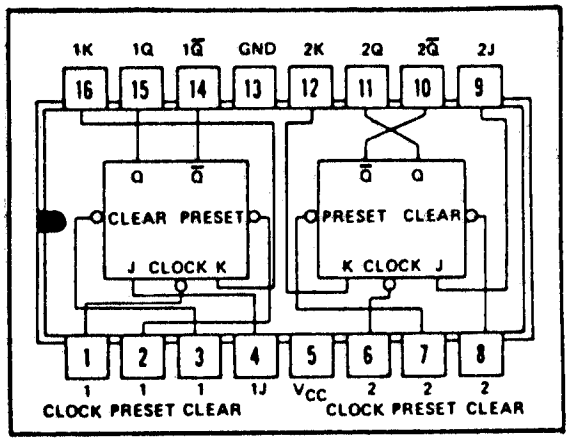


Case C



Device type 04

Cases E and F

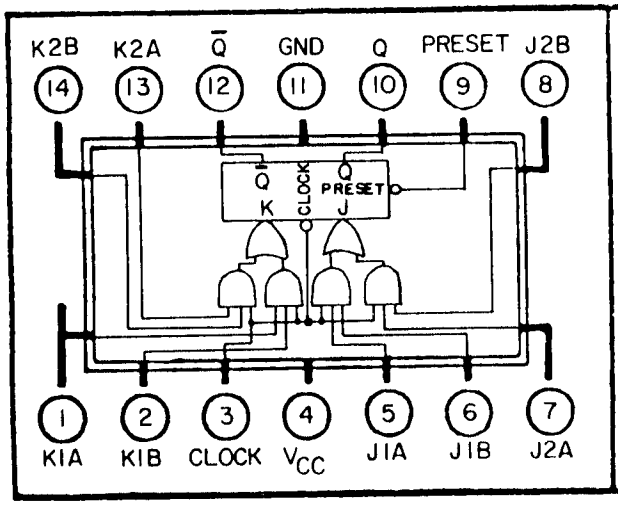


NOTE: Qualification requirements are removed for this device type.

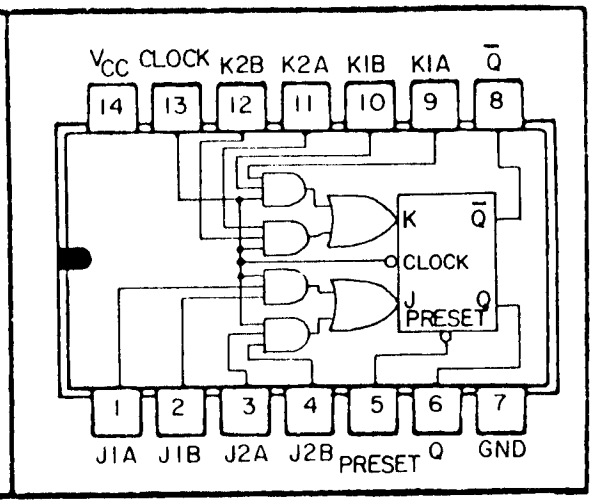
FIGURE 1. Terminal connections - Continued.

Device type 05 (See note)

Cases A, B, and D

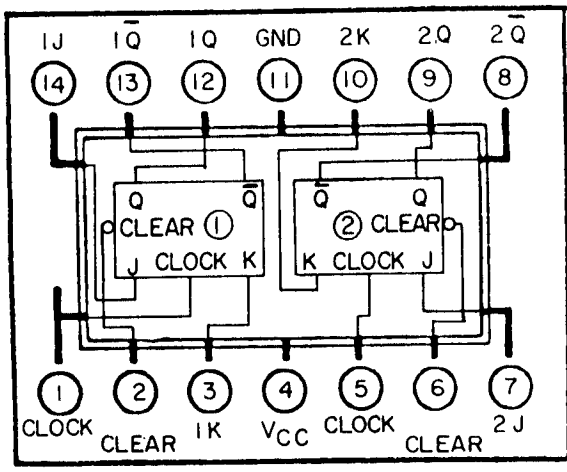


Case C

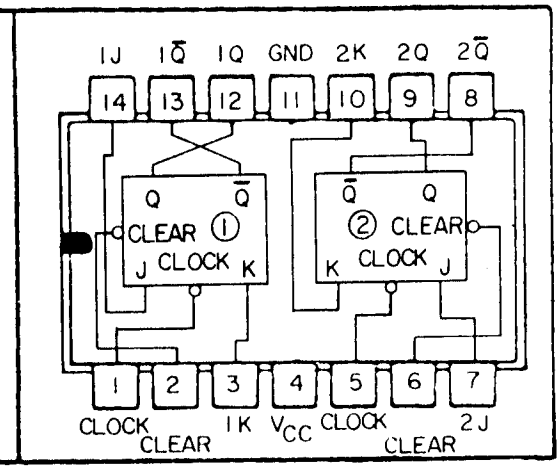


Device type 06 (See note)

Cases A, B, and D



Case C



NOTE: Qualification requirements are removed for this device type.

FIGURE 1. Terminal connections - Continued.

Device type 01

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level.
Low input to clear sets Q to low-level.
Preset and clear are independent of clock.

NOTES:
1. J = J1 . J2 . J3
2. K = K1 . K2 . K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. Qualification requirements are removed for this device type.

Device type 02

Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to clear sets Q to low-level.
Clear is independent of clock.

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.
3. Qualification requirements are removed for this device type.

FIGURE 2. Truth table.

Device type 03

Truth table Each flip-flop		
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
L	L	H
H	H	L

Positive logic: Low input to preset sets Q to high-level.
Low input to clear sets Q to low-level.
Clear and preset are independent of clock.

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.
3. Qualification requirements are removed for this device type.

Device type 04

Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level.
Low input to clear sets Q to low-level.
Clear and preset are independent of clock.

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

FIGURE 2. Truth table - Continued.

Device type 05

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level.
Preset is independent of clock.

NOTES:
1. J - (J1A . J1B) + (J2A . J2B).
2. K - (K1A . K1B) + (K2A . K2B).
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. Qualification requirements are removed for this device type.

Device type 06

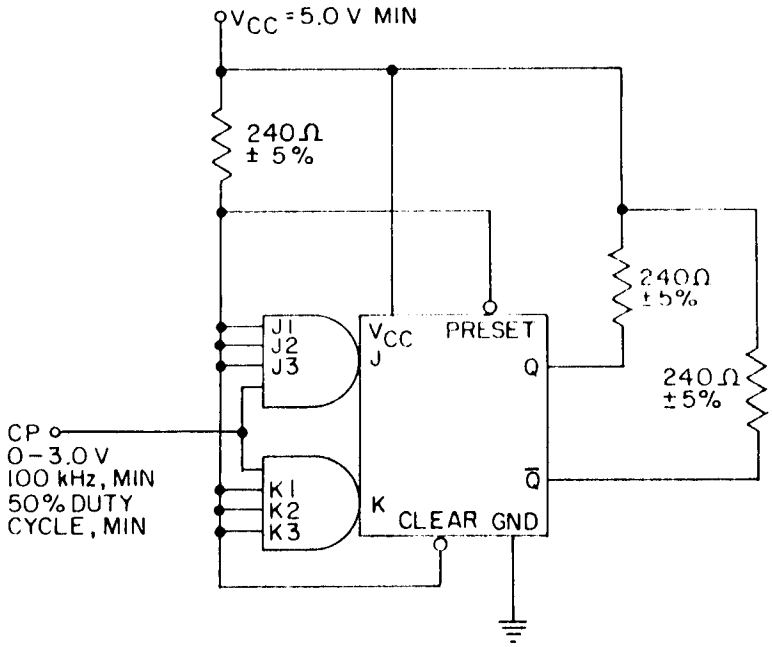
Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level.
Clear is independent of clock.

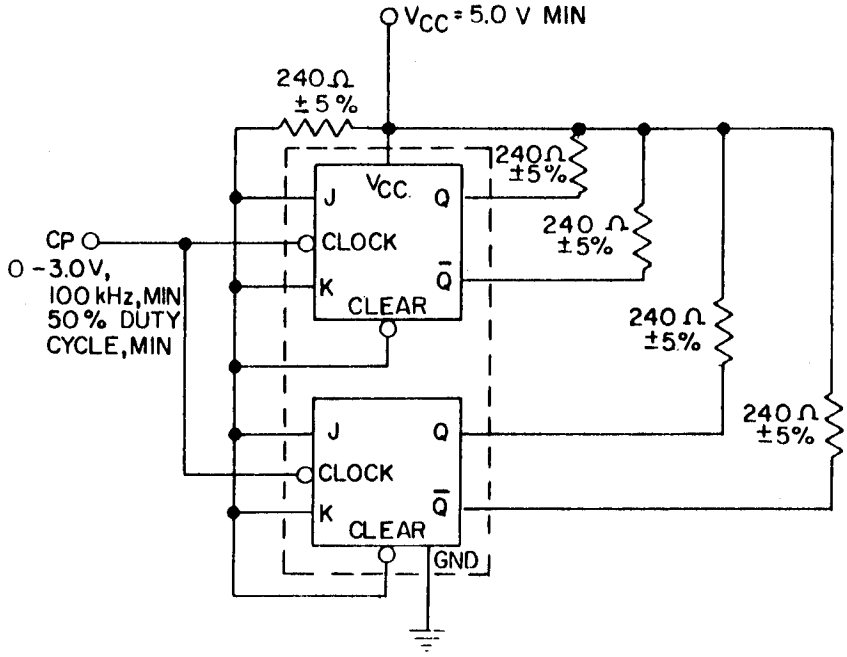
NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.
3. Qualification requirements are removed for this device type.

FIGURE 2. Truth table - Continued.

Device type 01 (see note)



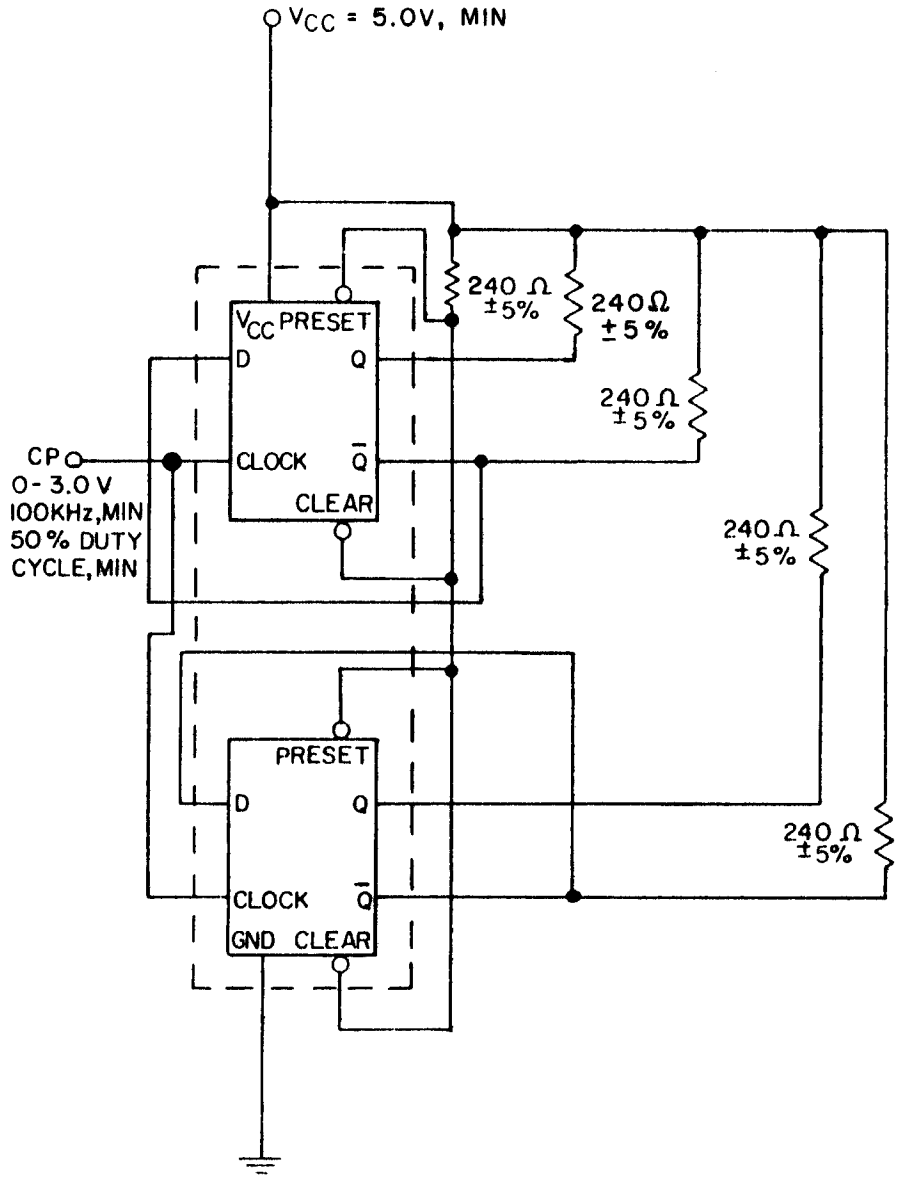
Device type 02 (see note)



NOTE: Qualification requirements are removed for this device type.

FIGURE 3. Burn-in and life-test circuits.

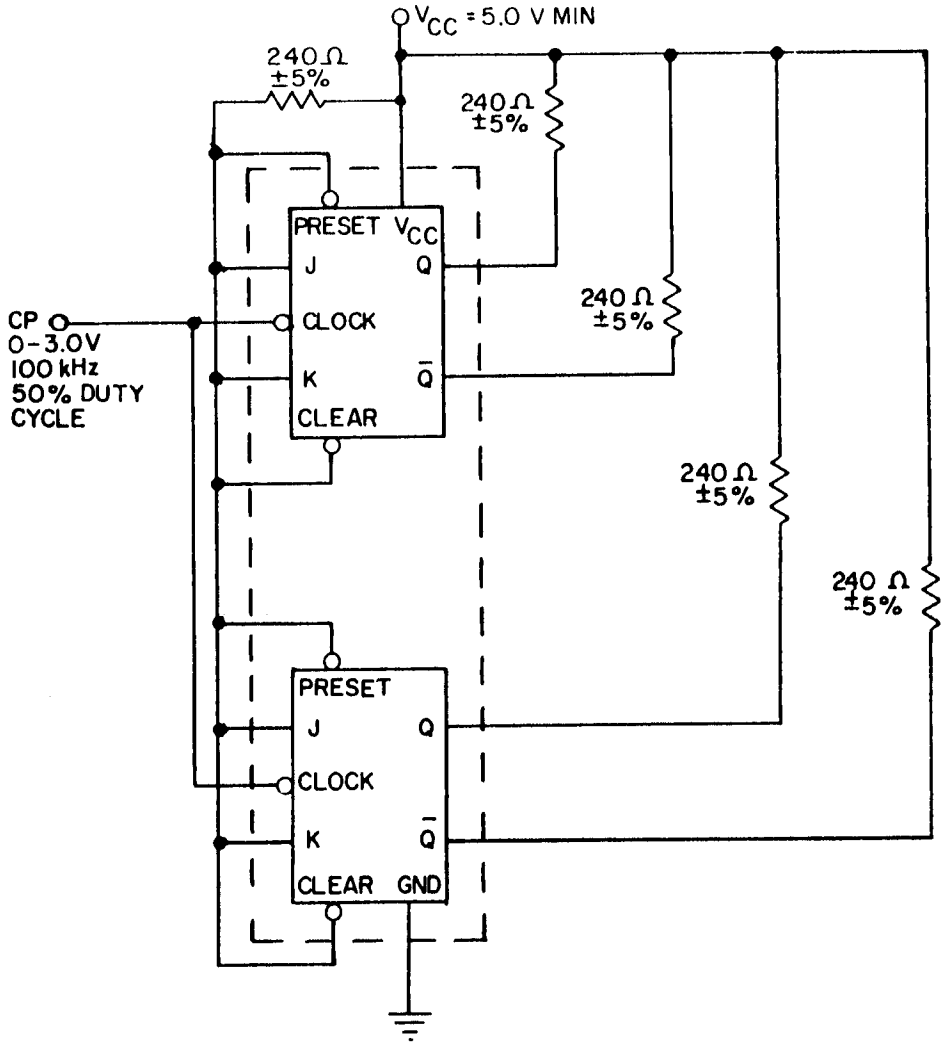
Device type 03 (see note)



NOTE: Qualification requirements are removed for this device type.

FIGURE 3. Burn-in and life-test circuits - Continued.

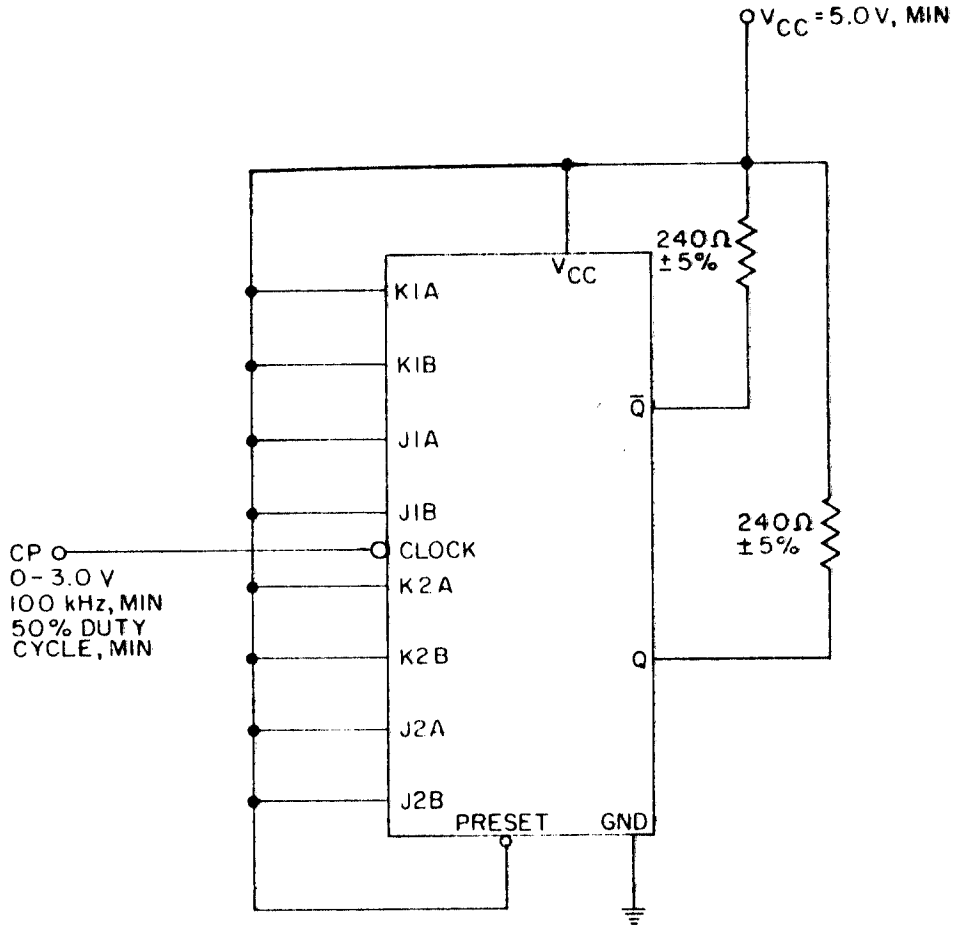
Device type 04 (see note)



NOTE: Qualification requirements are removed for this device type.

FIGURE 3. Burn-in and life-test circuits - Continued.

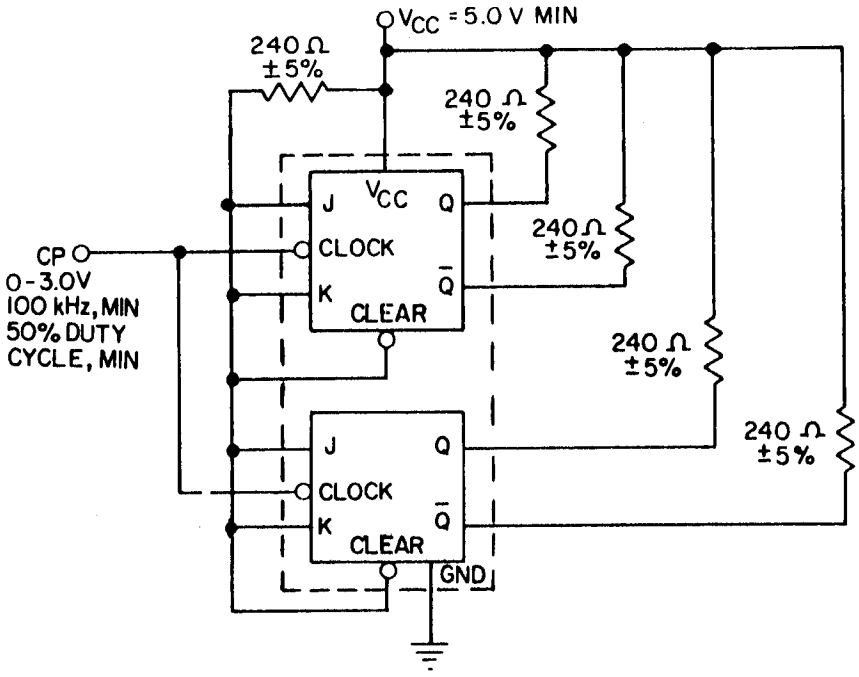
Device type 05 (see note)



NOTE: Qualification requirements are removed for this device type.

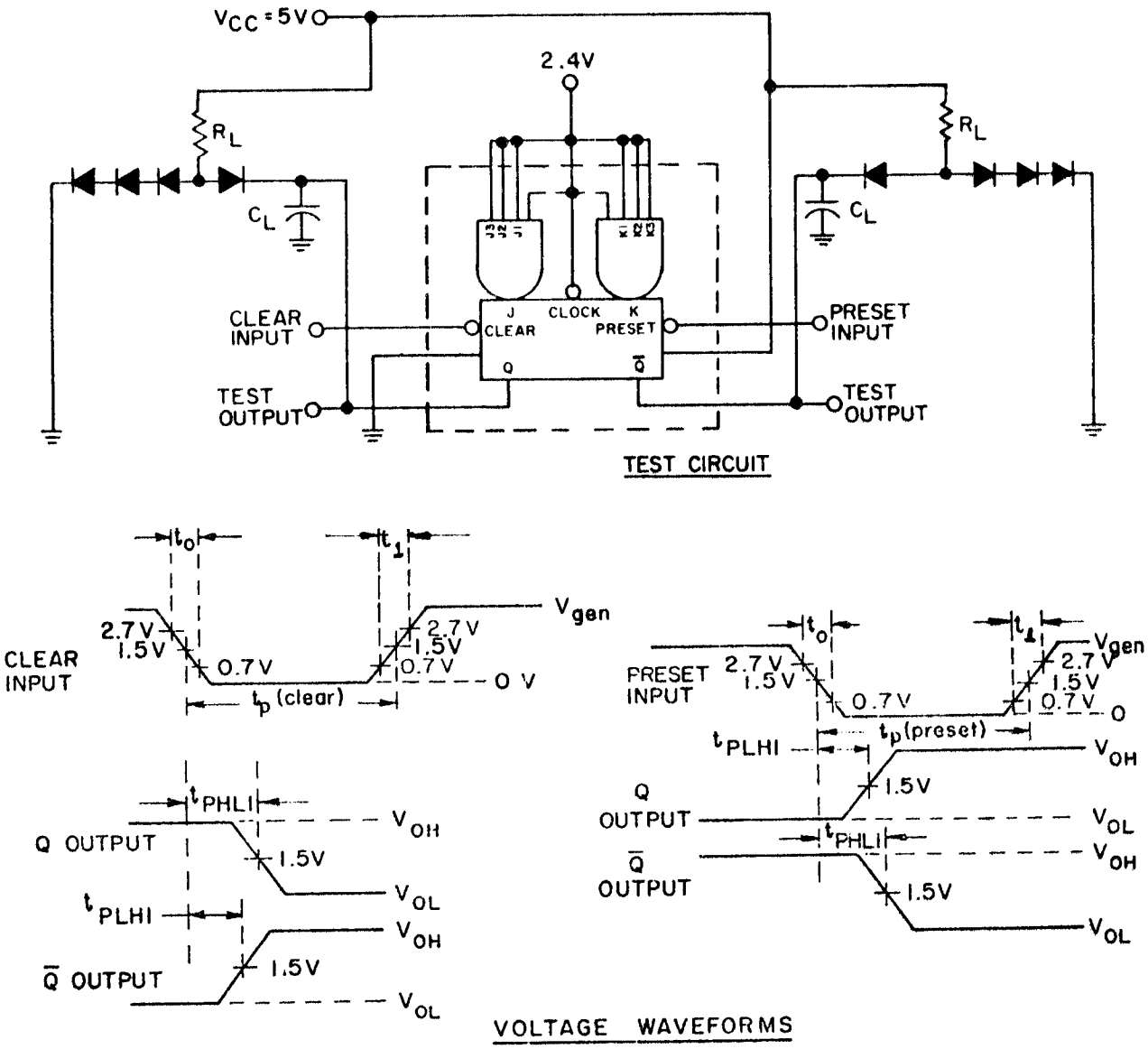
FIGURE 3. Burn-in and life-test circuits - Continued.

Device type 06 (see note)



NOTE: Qualification requirements are removed for this device type.

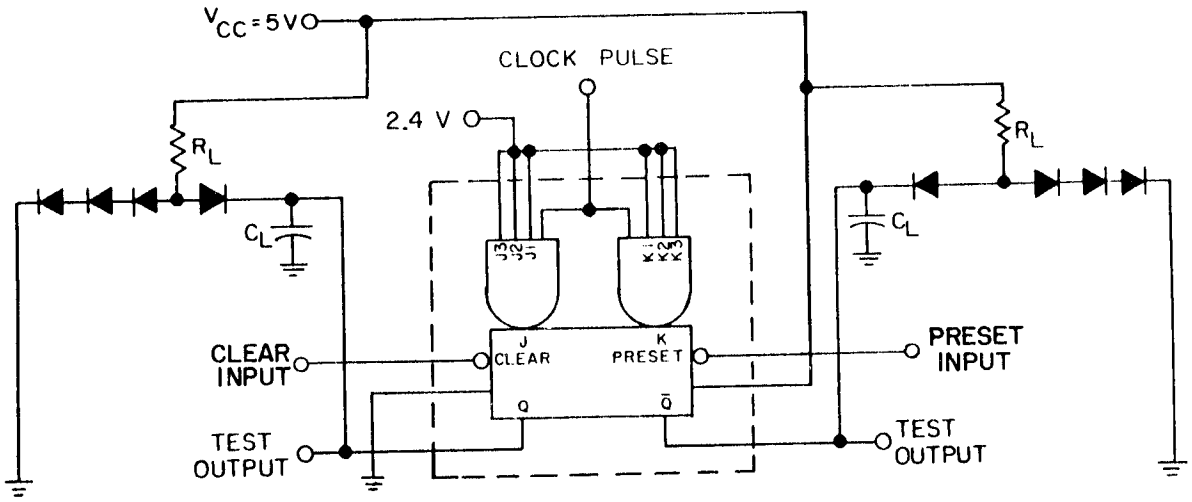
FIGURE 3. Burn-in and life-test circuits - Continued.



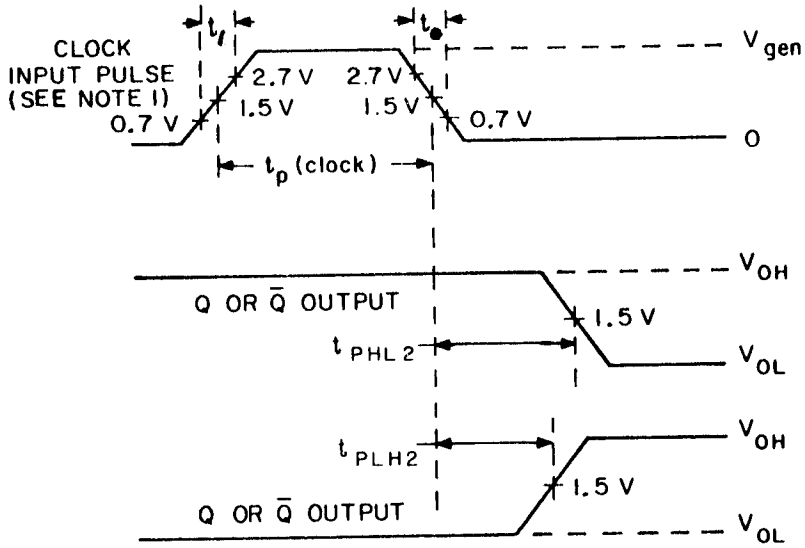
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3 V, $t_0 = t_1$ = 7 ns, t_p(clear) = t_p(preset) = 20 ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
3. C_L = 50 pF ±5% (C_L includes probe and jig capacitance).
4. R_L = 280Ω ±5%.
5. All diodes are 1N3064 or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).
7. Qualification requirements are removed for this device type.

FIGURE 4. Clear and preset switching test circuit and waveforms for device type 01.



TEST CIRCUIT

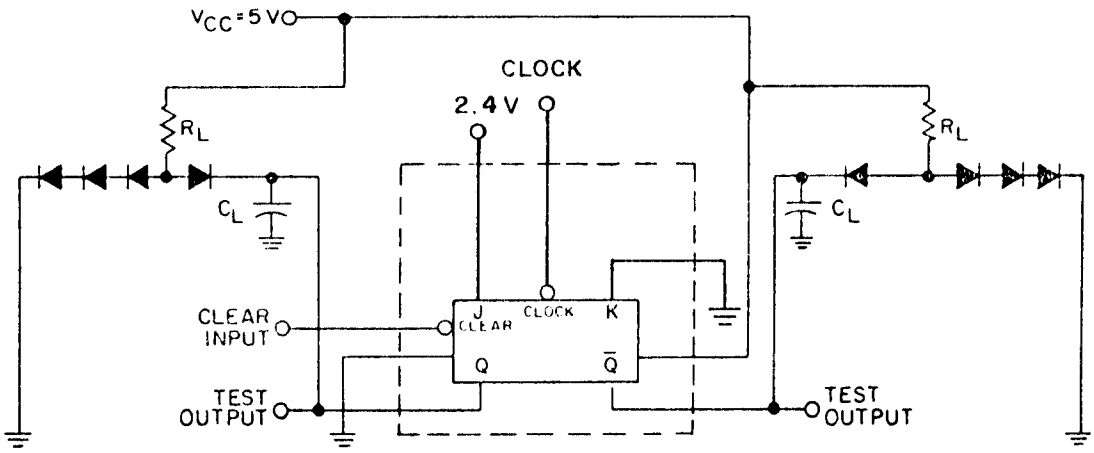


VOLTAGE WAVEFORMS

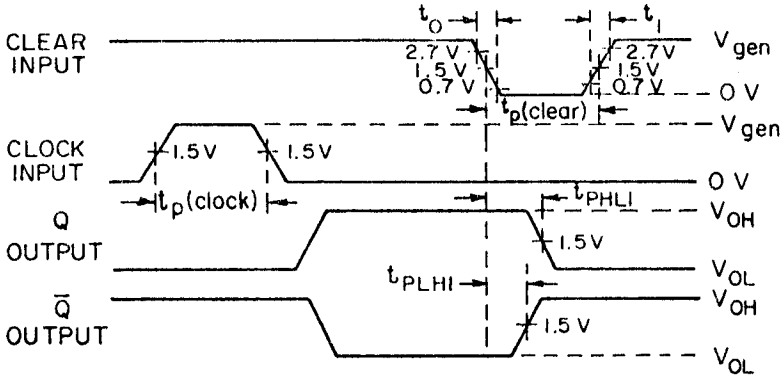
NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p(clock) = 20 ns, PRR = 1 MHz. All J and K innputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are V_{gen} = 3 V, $t_1 = t_0$ = 3 ns, t_p(clock) = 20 ns, f = 25 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. J = J1 . J2 . J3; and K = K1 . K2 . K3.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ±5% (C_L includes probe and jig capacitance).
5. R_L = 280Ω ±5%.
6. Qualification requirements are removed for this device type.

FIGURE 5. Synchronous switching test circuit for device type 01.



TEST CIRCUIT

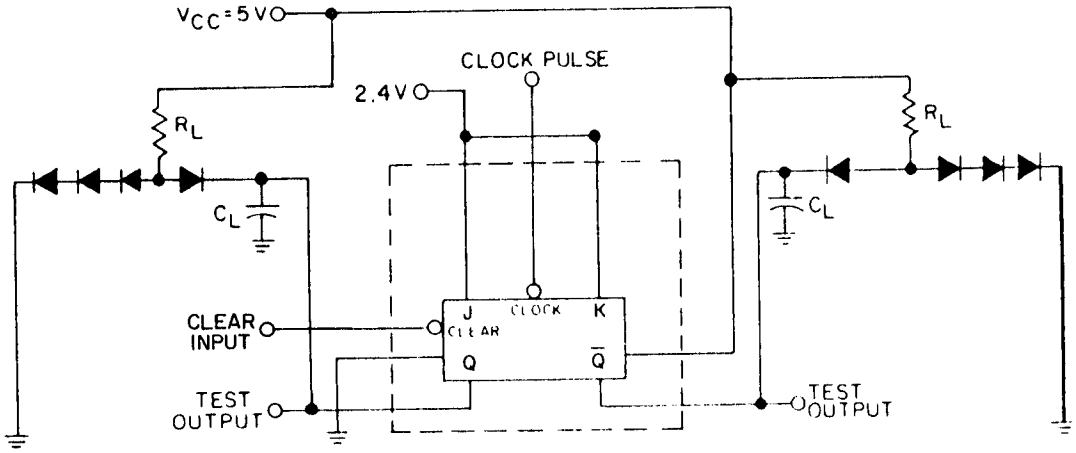


VOLTAGE WAVEFORMS

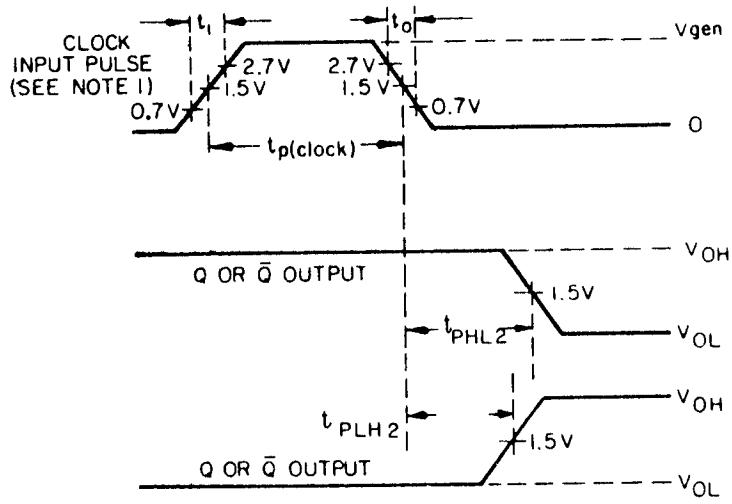
NOTES:

1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: V_{gen} = 3 V, t_0 = t_1 = 7 ns, t_p(clear) = 25 ns, PRR = 1 MHz.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. Clock input pulse characteristics: V_{gen} = 3 V, t_p(clock) $\geq$ 20 ns, PRR = 1 MHz.
7. Qualification requirements are removed for this device type.

FIGURE 6. Clear switching test circuit and waveforms for device type 02.



TEST CIRCUIT

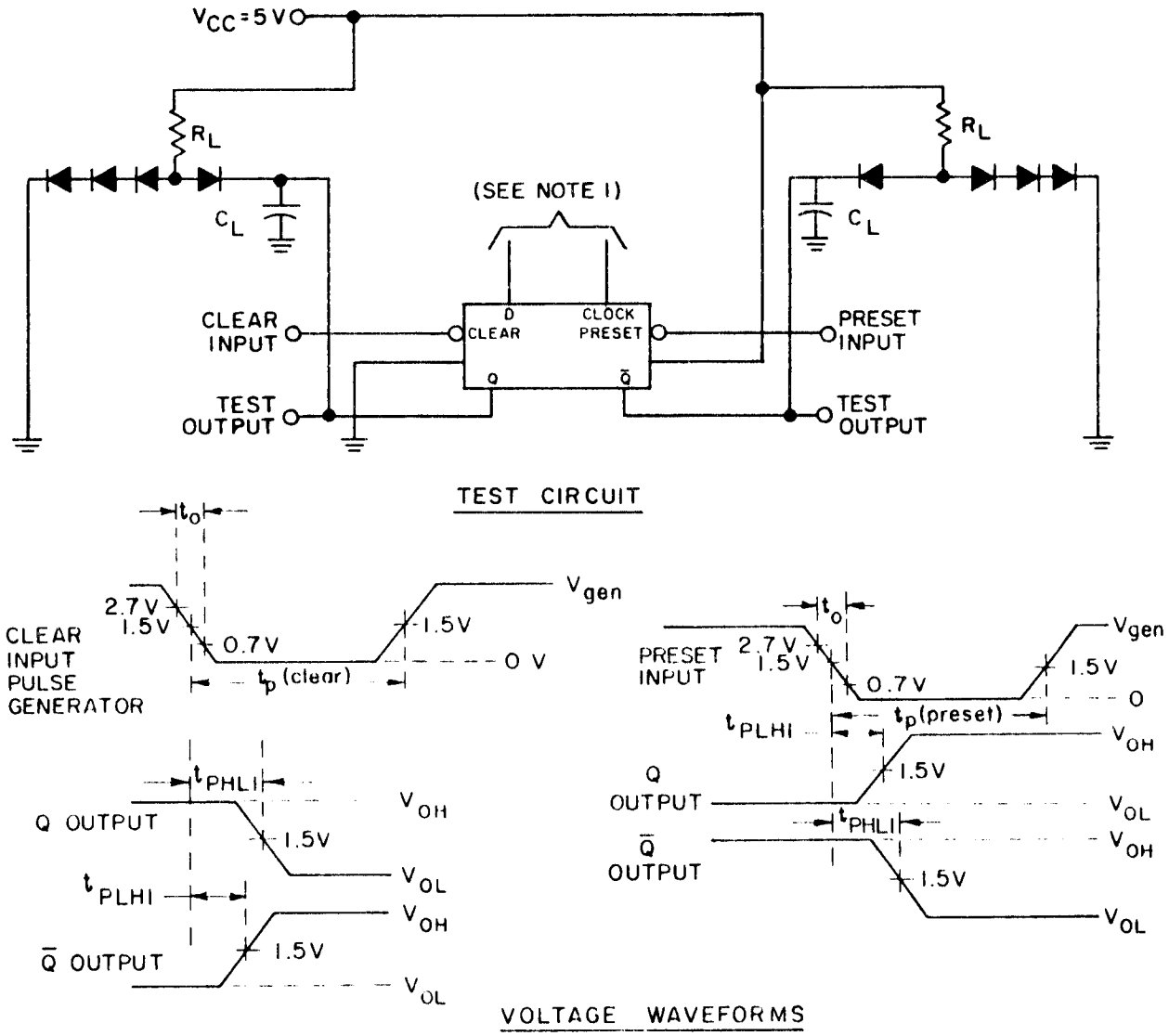


VOLTAGE WAVEFORMS

NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p(clock) = 25 ns, PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are V_{gen} = 3 V, $t_1 = t_0$ = 3 ns, t_p(clock) = 25 ns, f = 23 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280Ω ±5%.
5. Qualification requirements are removed for this device type.

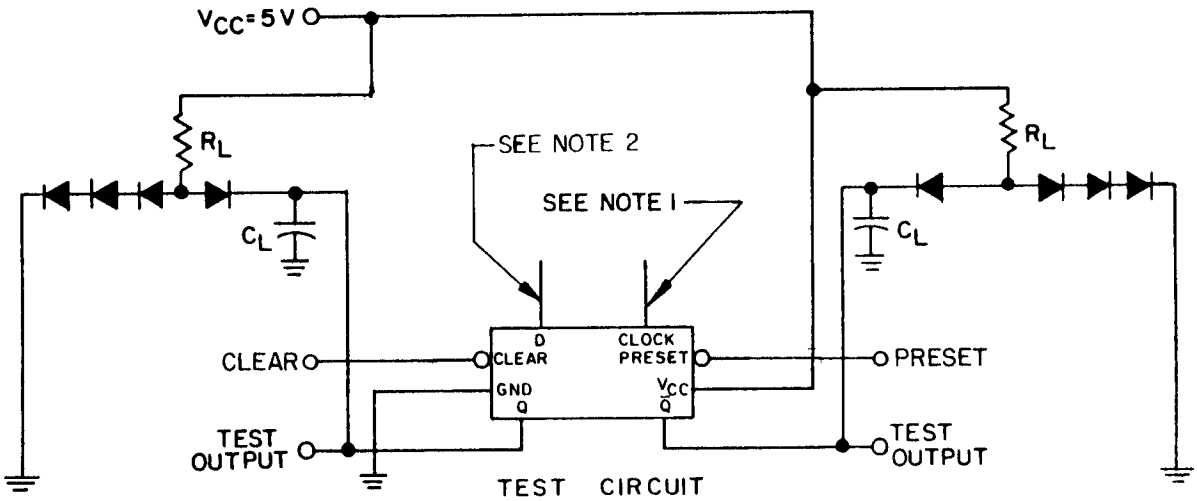
FIGURE 7. Synchronous switching test circuit for device type 02.



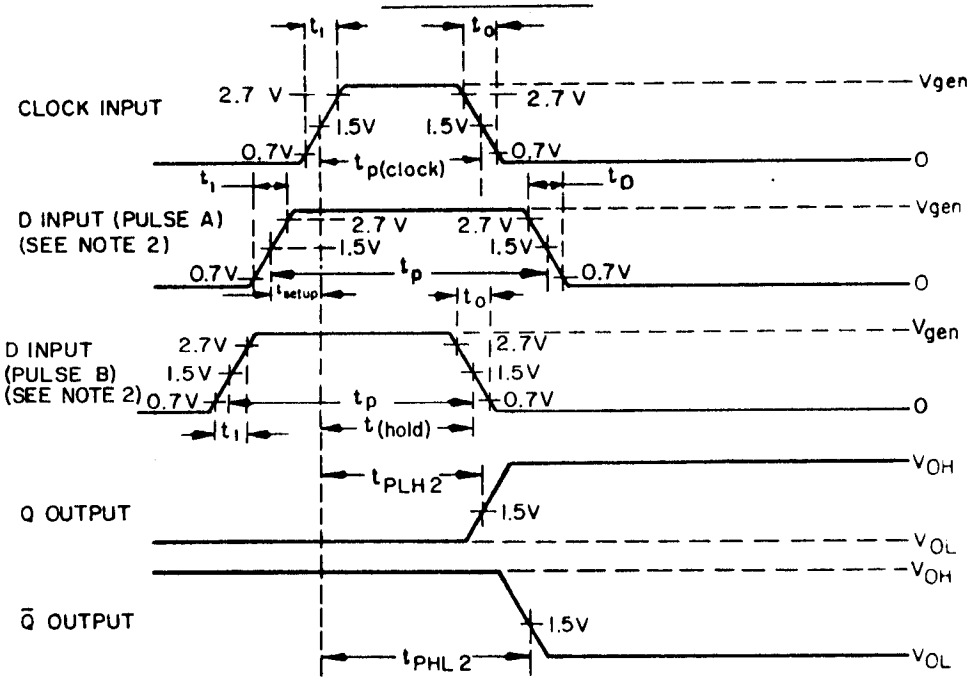
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or D inputs.
3. All diodes are 1N3064 or equivalent.
3. Clear or preset input pulse characteristics: V_{gen} = 3 V, $t_0 \leq 7$ ns, t_p(clear) = t_p(preset) = 25 ns, PRR = 1 MHz.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).
7. Qualification requirements are removed for this device type.

FIGURE 8. Clear and preset switching test circuit and waveforms for device type 03.



TEST CIRCUIT

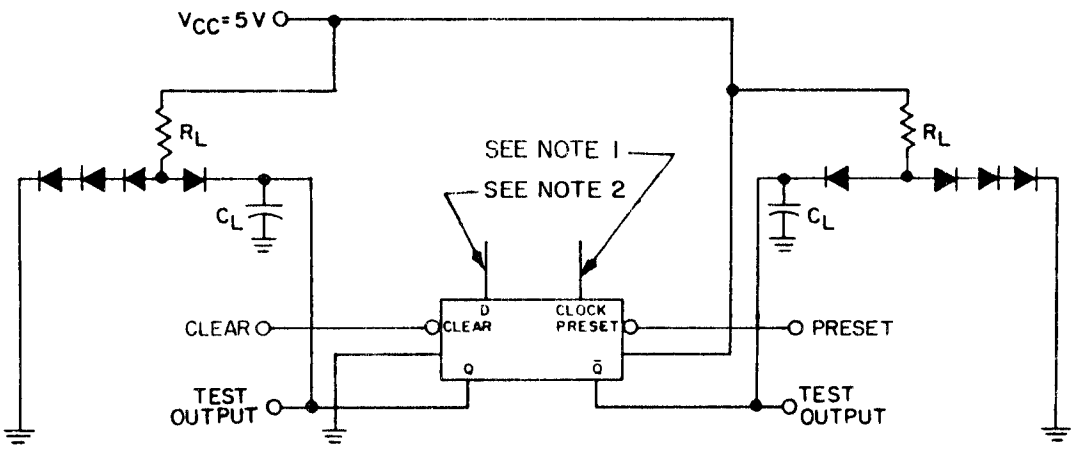


VOLTAGE WAVEFORMS

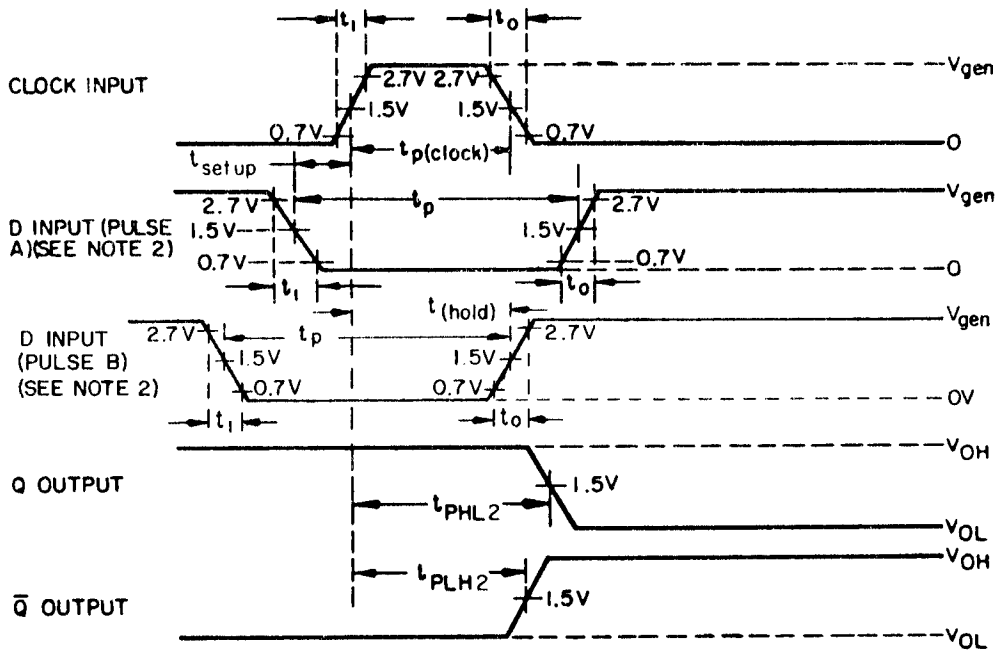
NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, t_p(clock) = 20 ns, and PRR = 1 MHz. When testing f_{MAX}, f = 36 MHz for subgroup 9 and f = 28 MHz for subgroups 10 and 11.
2. D input (pulse A) has the following characteristics: V_{gen} = 3 V, $t_0 \leq 7$ ns, t_{setup} = 10 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, t(hold) = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. Qualification requirements are removed for this device type.

FIGURE 9. Synchronous switching test circuit (high-level) for device type 03.



TEST CIRCUIT

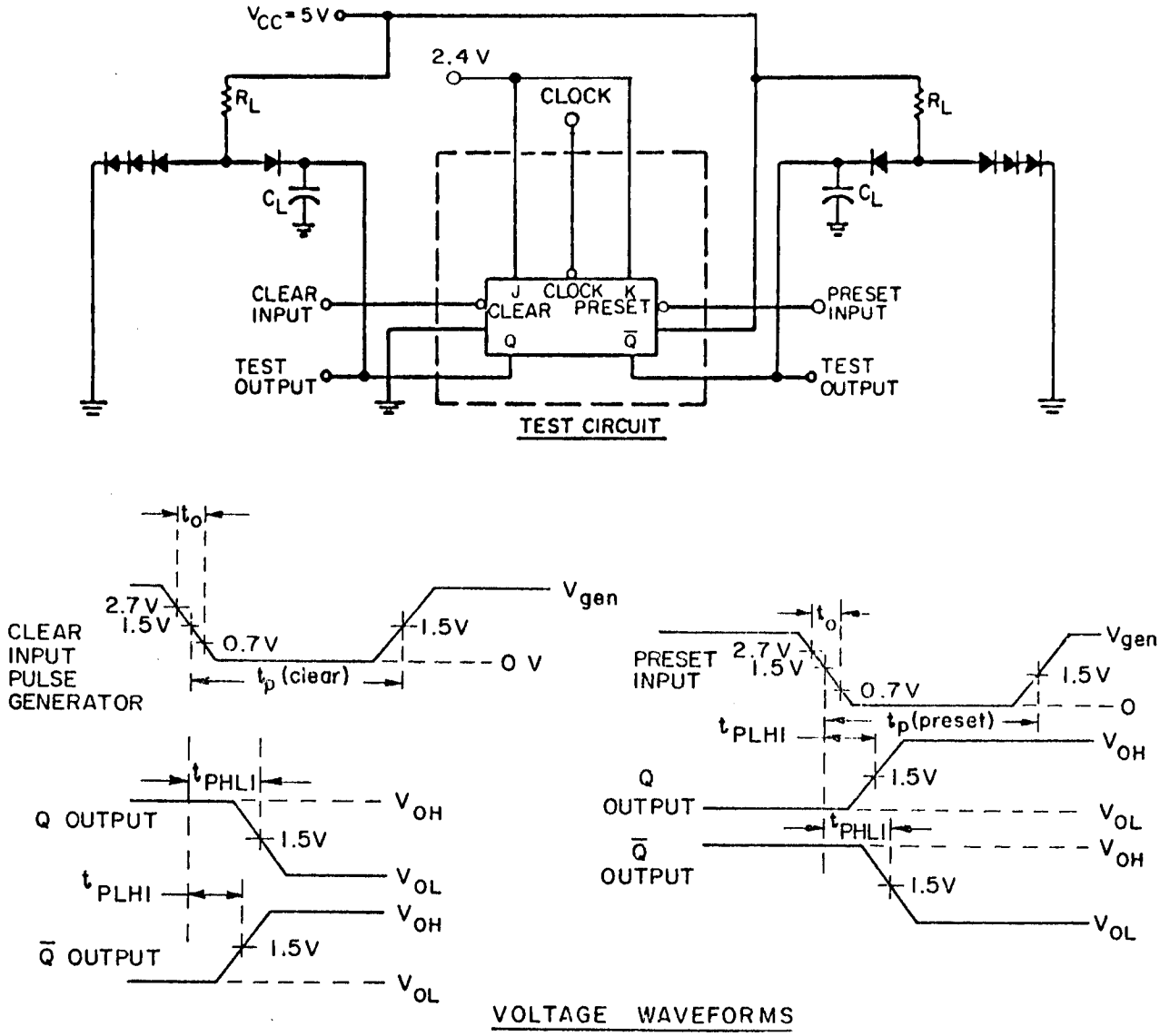


VOLTAGE WAVEFORMS

NOTES:

1. Clock input pulse characteristics: V_{gen} = 3 V, $t_0 = t_1$ = 7 ns, t_p(clock) = 20 ns, and PRR = 1 MHz.
2. D input (pulse A) has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, t_{setup} = 15 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, $t_{(hold)}$ = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. Qualification requirements are removed for this device type.

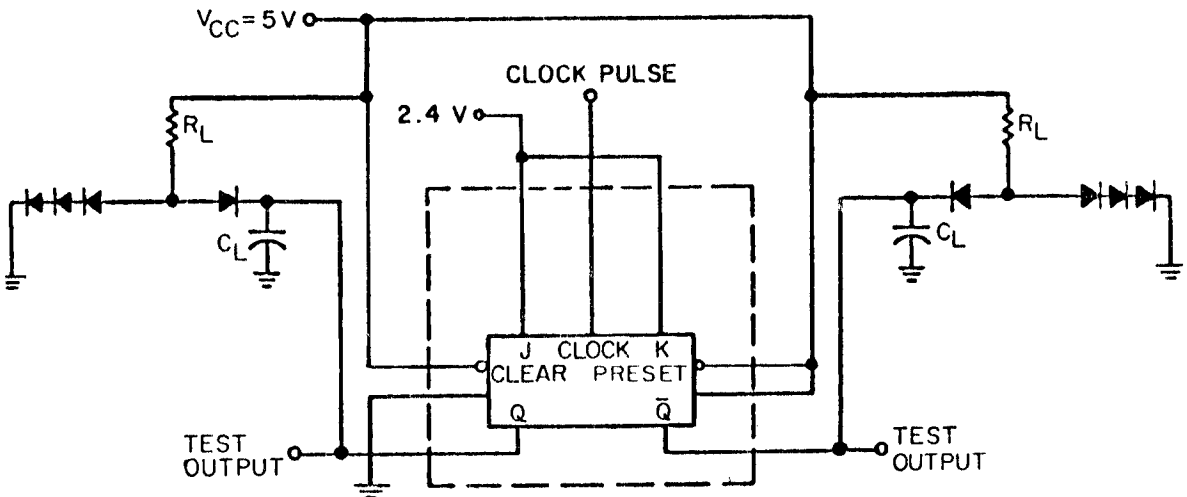
FIGURE 10. Synchronous switching test (low-level data) for device type 03.



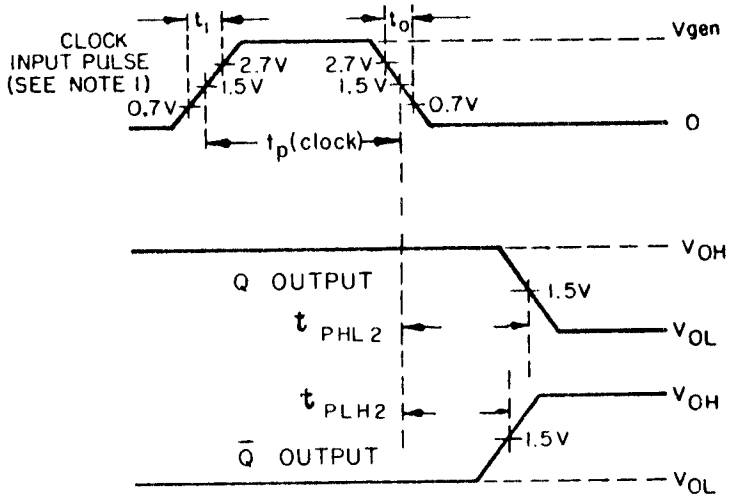
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3 V, t_0 = t_1 = 7 ns, t_p(clear) = t_p(preset) = 25 ns, PRR = 1 MHz, and Z_{OUT} ≈ 50Ω.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280Ω ±5%.
5. All diodes are 1N3064 or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 11. Clear and preset switching test circuit and waveforms for device type 04.



TEST CIRCUIT

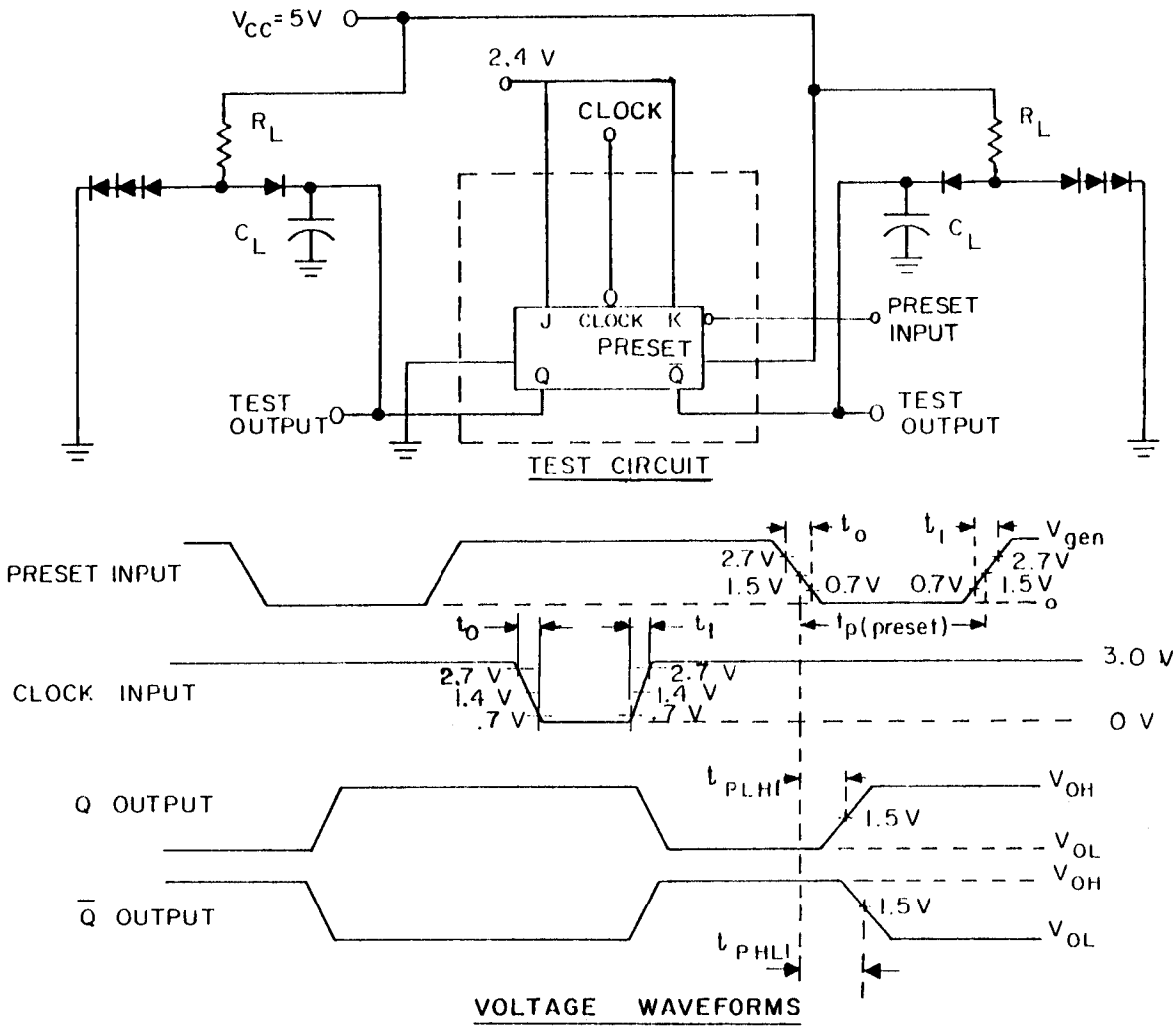


VOLTAGE WAVEFORMS

NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p(clock) = 25 ns, PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input pulse characteristics are V_{gen} = 3 V, $t_1 = t_0$ = 3 ns, t_p(clock) = 25 ns, f = 25 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280Ω ±5%.

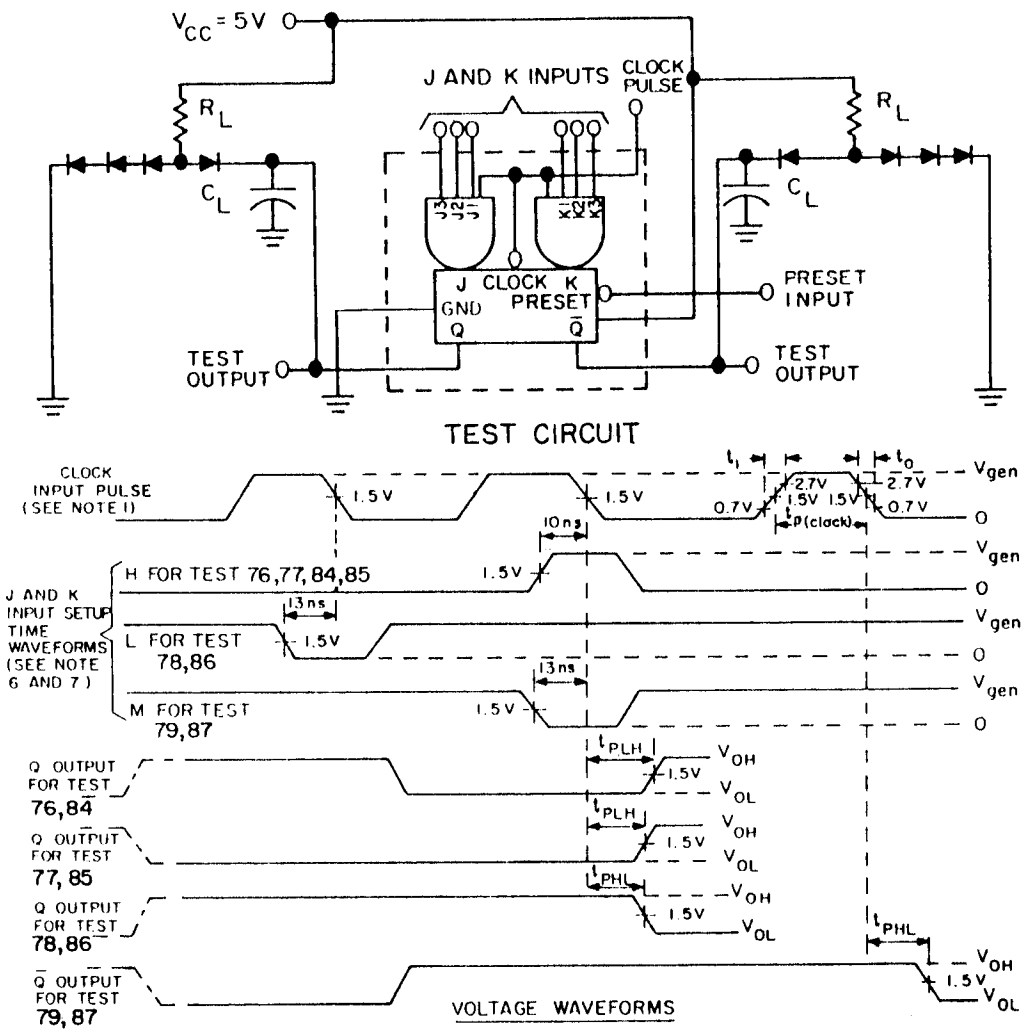
FIGURE 12. Synchronous switching test circuit for device type 04.



NOTES:

1. Preset inputs dominate regardless of the state of clock or J-K inputs.
2. Preset input pulse characteristics: V_{gen} = 3 V, t_0 = t_1 = 7 ns, t_p(preset) = 16 ns, PRR = 1 MHz, and Z_{OUT} ≈ 50Ω.
3. Clock input pulse characteristics: V_{gen} = 2.0 V, t_0 = t_1 = 3 ns, PRR = 1 MHz, , Z_{OUT} ≈ 50Ω, and t_p(clock) = 20 ns minimum.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. All diodes are 1N3064 or equivalent.
7. Qualification requirements are removed for this device type.

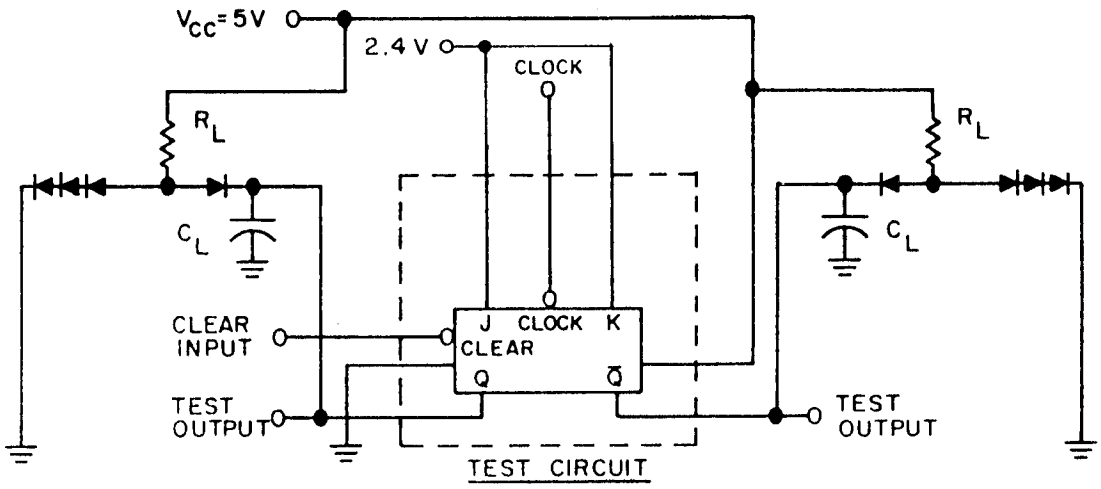
FIGURE 13. Preset switching test circuit and waveforms for device type 05.

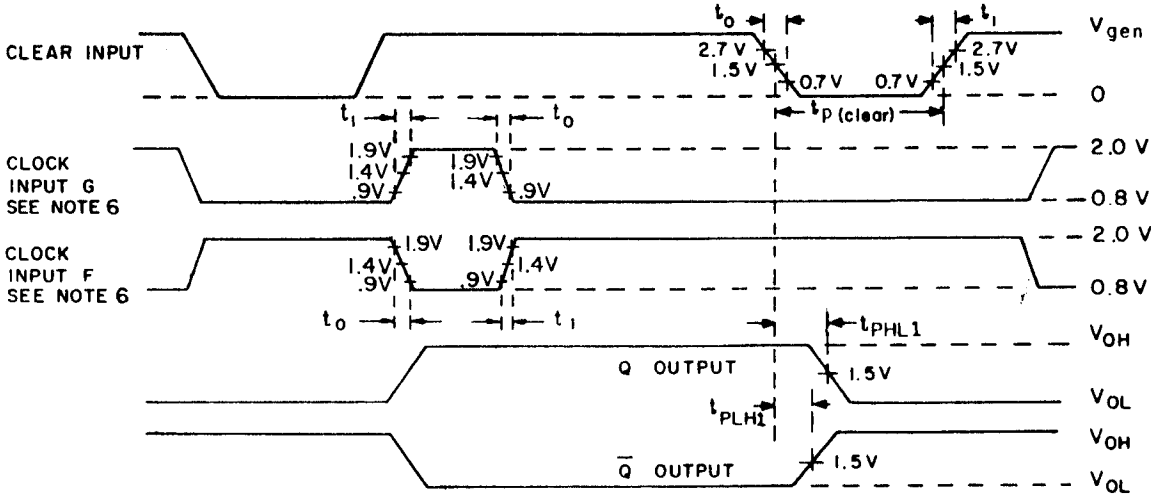


NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p(clock) = 20 ns, PRR = 1 MHz. When testing f_{MAX} the clock input pulse characteristics are V_{gen} = 3 V, $t_1 = t_0$ = 3 ns, t_p(clock) = 10 ns, f = 36 MHz for subgroup 9 and f = 30 MHz for subgroups 10 and 11. All J and K inputs are at 2.4 V.
2. J = (J1A . J1B) + (J2A . J2B) and K = (K1A . K1B) + (K2A . K2B)K3.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. J and K input characteristics for t_{PHL} and t_{PLH} are V_{gen} = 3 V, rise and fall times 10 ns maximum, and PW = 20 ns. See table III for which t_{setup} to use.
7. For test 84, 85, 86, and 87 (high low temperature) the t_{setup} value shown above should be increased from 10 and 13 ns to 15 and 20 ns respectively.
8. Qualification requirements are removed for this device type.

FIGURE 14. Synchronous switching test circuit for device type 05.



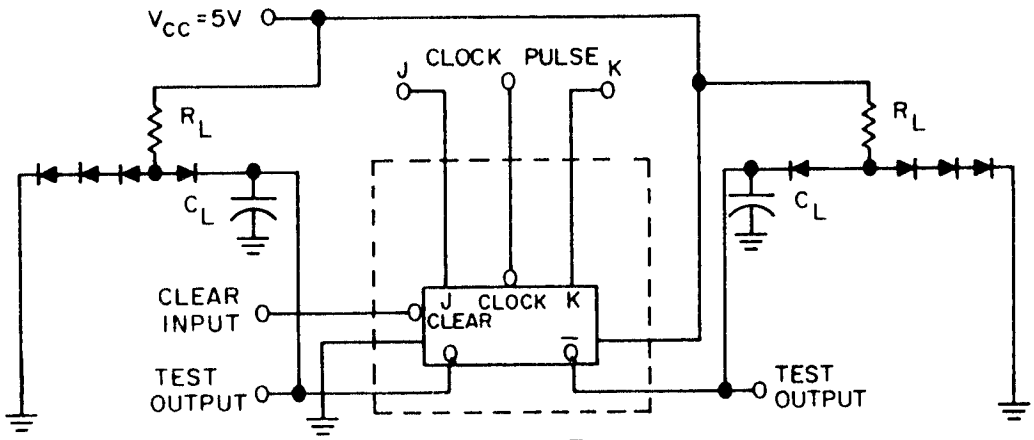


VOLTAGE WAVEFORMS

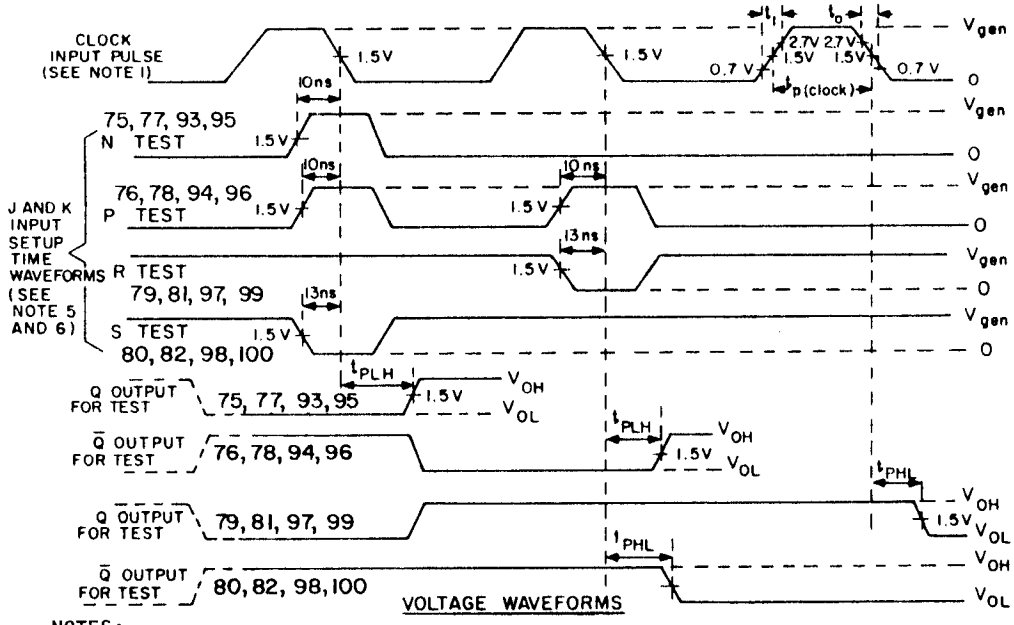
NOTES:

1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: V_{gen} = 3 V, t_0 = t_1 = 7 ns, t_p(clear) = 16 ns, PRR = 1 MHz, and Z_{OUT} ≃ 50Ω.
3. Clock input pulse characteristics: V_{gen} = 2.0 V, t_0 = t_1 = 3 ns, PRR = 1 MHz, and t_p(clock) = 20 ns minimum.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.
6. Apply clock pulse F or G as required by table III.
7. Qualification requirements are removed for this device type.

FIGURE 15. Clear switching test circuit and waveforms for device type 06.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p(clock) = 20 ns, PRR = 1 MHz. When testing f_{MAX} the clock input pulse characteristics are V_{gen} = 3 V, $t_1 = t_0$ = 3 ns, t_p(clock) = 10 ns, f = 36 MHz for subgroup 9 and f = 30 MHz for subgroups 10 and 11. All J and K inputs are at 2.4 V.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280Ω ±5%.
5. J and K input characteristics for t_{PHL} and t_{PLH} are: V_{gen} = 3 V, rise and fall times 10 ns maximum, and PW = 20 ns. See table III for which t_{setup} waveform to use.
6. For test 93 through 100 (high and low temperature), the t_{setup} values shown above should be increased from 10 and 13 ns to 15 and 20 ns respectively.
7. Qualification requirements are removed for this device type.

FIGURE 16. Synchronous switching test circuit for device type 06.

TABLE III. Group A inspection for device type 01. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits Min	Limits Max	Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11				
			Test no.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3				
T_C [1] = +25°C	V_{OH}	3006	1	0.8 V	A		4.5 V			2.0 V	2.0 V	2.0 V		GND	-0.5 mA	0.8 V	0.8 V	Q	2.4		V
			2	2.0 V	A		"			0.8 V	0.8 V	0.8 V	-0.5 mA	"		2.0 V	2.0 V	$\overline{Q}$	"		"
			3			0.8 V	"	2.0 V						"	-0.5 mA			Q	"		"
			4			2.0 V	"	0.8 V					-0.5 mA	"				$\overline{Q}$	"		"
	V_{OL}	3007	5	2.0 V	A		"			0.8 V	0.8 V	0.8 V		"	20 mA	2.0 V	2.0 V	Q		0.4	"
			6	0.8 V	A		"			2.0 V	2.0 V	2.0 v	20 mA	"		0.8 V	0.8 V	$\overline{Q}$		"	"
			7			0.8 V	"	2.0 V					20 mA	"				Q		"	"
			8			2.0 V	"	0.8 V						"	20 mA			$\overline{Q}$		"	"
	V_{IC}		9	-12 mA			"							"				K1		-1.5	"
			10				"							"		-12 mA		K2		"	"
			11				"							"			-12 mA	K3		"	"
			12				"			-12 mA				"				J1		"	"
			13				"				-12 mA			"				J2		"	"
			14				"					-12 mA		"				J3		"	"
			15				"	-12 mA						"				Clear		"	"
			16			-12 mA	"							"				Preset		"	"
			17		-12 mA		"							"				Clock		"	"
	I_{IL1}	3009	18	GND	4.5 V		5.5 V	8		0.4 V	4.5 V	4.5 V		"		GND	GND	J1	-1.0	-2.0	mA
			19	"	"		"	"		4.5 V	0.4 V	4.5 v		"		"	"	J2	"	"	"
			20	"	"		"	"		4.5 V	4.5 V	0.4 V		"		"	"	J3	"	"	"
			21	0.4 V	"	8	"			GND	GND	GND		"		4.5 V	4.5 V	K1	"	"	"
			22	4.5 V	"	"	"			"	"	"		"		0.4 V	4.5 V	K2	"	"	"
			23	"	"	"	"			"	"	"		"		4.5 V	0.4 V	K3	"	"	"
			24	"	0.4 V	"	"			4.5 V	4.5 V	4.5 V		"		"	4.5 V	Clock	"	"	"
			25	"	0.4 V		"	9		"	"	"		"		"	"	Clock	"	"	"
	I_{IL2}		26	"	4.5 V	0.4 V	"			"	"	"		"		"	"	Preset	-2.0	-4.0	"
			27	"	4.5 V		"	0.4 V		"	"	"		"		"	"	Clear	-2.0	-4.0	"
	I_{IH1}	3010	28		GND		"	GND		2.4 V	GND	GND		"				J1		50	µA
			29		"		"	"		GND	2.4 V	GND		"				J2		"	"
			30		"		"	"		GND	GND	2.4 V		"				J3		"	"
			31	2.4 V	"	GND	"							"		GND	GND	K1		"	"
			32	GND	"	"	"							"		2.4 V	GND	K2		"	"
			33	GND	"	"	"							"		GND	2.4 V	K3		"	"
	I_{IH2}		34		"		"	GND		5.5 V	GND	GND		"				J1		100	"
			35		"		"	"		GND	5.5 V	GND		"				J2		"	"
			36		"		"	"		GND	GND	5.5 V		"				J3		"	"
			37	5.5 V	"	GND	"							"		GND	GND	K1		"	"
			38	GND	"	"	"							"		5.5 V	GND	K2		"	"
			39	GND	"	"	"							"		GND	5.5 V	K3		"	"
	I_{IH3}		40		"		"	2.4 V		GND	GND	GND		"				Clear		"	"
			41	GND	"	2.4 V	"							"		GND	GND	Preset		"	"
	I_{IH4}		42	GND	"	5.5 V	"							"		GND	GND	Preset		200	"
			43		"		"	5.5 V		GND	GND	GND		"				Clear		200	"
	I_{IH5}		44	GND	2.4 V		"	GND		"	"	"		"		GND	GND	Clock		100	"
			45	"	2.4 V	GND	"			"	"	"		"		"	"	"		100	"
	I_{IH6}		46	"	5.5 V		"	GND		"	"	"		"		"	"	"		200	"
			47	"	5.5 V	GND	"			"	"	"		"		"	"	"		200	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D / Case C / Test no.	1 / 9 / K1	2 / 12 / Clock	3 / 13 / Preset	4 / 14 / V_{CC}	5 / 2 / Clear	6 / 1 / NC	7 / 3 / J1	8 / 4 / J2	9 / 5 / J3	10 / 6 / $\overline{Q}$	11 / 7 / GND	12 / 8 / Q	13 / 10 / K2	14 / 11 / K3	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	I_{OS}	3011	48	4.5 V	GND	GND	5.5 V			4.5 V	4.5 V	4.5 V		GND	GND	4.5 V	4.5 V	Q	-40	-100	mA
			49	4.5 V	"		"	GND		4.5 V	4.5 V	4.5 V	GND	"		4.5 V	4.5 V	$\overline{Q}$	-40	-100	"
	I_{CC}	3005	50	GND	"	GND	"			GND	GND	GND		"		GND	GND	V_{CC}		25	"
			51	GND	"		"	GND		GND	GND	GND		"		GND	GND	V_{CC}		25	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C = +25°C 3/ 4/			52	B	A	B	4.5 V	B	B	B	B	B	H	GND	H	B	B	All outputs	H or L as shown 5/		
			53	"	"	B	"	A	"	"	"	"	L	"	H	"	"	"	"		
			54	"	"	A	"	B	"	"	"	"	H	"	L	"	"	"	"		
			55	"	B	"	"	A	"	"	"	"	"	"	"	"	"	"	"		
			56	A	B	"	"	"	"	A	A	"	"	"	"	A	A	"	"		
			57	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			58	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			59	"	B	"	"	"	"	"	B	A	"	"	"	"	"	"	"		
			60	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			61	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			62	"	B	"	"	"	"	B	A	"	"	"	"	"	"	"	"		
			63	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			64	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			65	"	B	"	"	"	"	A	"	"	"	"	"	"	"	"	"		
			66	"	A	"	"	"	"	"	"	"	L	"	H	"	"	"	"		
			67	"	B	"	"	"	"	"	"	"	"	"	"	"	B	"	"		
			68	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			69	"	A	"	"	"	"	"	"	"	"	"	"	B	A	"	"		
			70	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			71	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			72	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			73	"	B	"	"	"	"	"	"	"	"	"	"	A	"	"	"		
			74	B	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			75	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			76	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			77	A	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			78	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			79	"	B	"	"	"	"	"	"	"	H	"	L	"	"	"	"		
8 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C = +25°C	f_{MAX} 6/	(Fig. 5)	90	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	25		MHz
			81	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	$\overline{Q}$	25		MHz
	t_{PLH1}	3003 (Fig. 4)	82	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to $\overline{Q}$	2	15	ns
			83	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to $\overline{Q}$	"	15	"
	t_{PHL1}		84	"	"	J	"	IN		"	"	"		"	OUT	"	"	Clear to Q	"	26	"
			85	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	26	"
	t_{PLH2}	3003 (Fig. 5)	86	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	23	"
			87	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	23	"
	t_{PHL2}		88	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to $\overline{Q}$	"	29	"
			89	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to Q	"	29	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max	
			Test no.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3				
10 T_C = +125°C	f_{MAX}	(Fig. 5)	90 6/	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	20		MHz
			91 6/	"	"	"	"	"		"	"	"	OUT	"		"	"	$\overline{Q}$	20		MHz
	t_{PLH1}	3003 (Fig. 4)	92	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to $\overline{Q}$	2	20	ns
			93	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to Q	"	20	"
	t_{PHL1}		94	"	"	J	"	IN		"	"	"		"	OUT	"	"	Clear to Q	"	31	"
			95	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	31	"
	t_{PLH2}	(Fig. 5)	96	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	28	"
			97	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	28	"
	t_{PHL2}		98	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	37	"
			99	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	37	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.

B = Momentary GND, then 4.5 V.

J = Input pulse $t_p \geq 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open).

2/ Qualification requirements are removed for this device type.

3/ Tests shall be performed in sequence.

4/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.

5/ Output voltages shall be either: H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or H $\geq$ 1.5 V and L $\leq$ 1.5 V when using a high speed checker single comparator.

6/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits Min	Limits Max	Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	Q1	$\overline{Q1}$	J1				
1 T_C = +25°C	V_{OH}	3006	1	A		0.8 V	4.5 V							GND	-0.5 mA		2.0 V	Q1	2.4		V
			2	A		2.0 V	"							"		-0.5 mA	0.8 V	$\overline{Q1}$	"		"
			3		0.8 V		"							"		-0.5 mA		$\overline{Q1}$	"		"
			4				"	A		2.0 V		-0.5 mA	0.8 V	"				Q2	"		"
			5				"	A		0.8 V	-0.5 mA		2.0 V	"				$\overline{Q2}$	"		"
			6				"		0.8 V		-0.5 mA			"				$\overline{Q2}$	"		"
	V_{OL}	3007	7	A		2.0 V	"							"	20 mA		0.8 V	Q1		0.4	"
			8	A		0.8 V	"							"		20 mA	2.0 V	$\overline{Q1}$		"	"
			9		0.8 V		"							"	20 mA			Q1		"	"
			10				"	A		0.8 V		20 mA	2.0 V	"				Q2		"	"
			11				"	A		2.0 V	20 mA		0.8 V	"				$\overline{Q2}$		"	"
			12				"		0.8 V			20 mA		"				Q2		"	"
	V_{IC}		13				"							"			-12 mA	J1		-1.5	"
			14				"			-12 mA				"				J2		"	"
			15			-12 mA	"							"				K1		"	"
			16				"						-12 mA	"				K2		"	"
			17		-12 mA		"							"				Clear 1		"	"
			18	-12 mA			"							"				Clock 1		"	"
			19				"		-12 mA					"				Clear 2		"	"
			20				"	-12 mA						"				Clock 2		"	"
	I_{IL1}	3009	21	3/	4.5 V		5.5 V							"			0.4 V	J1	-1.0	-2.0	mA
			22	3/	4.5 V	0.4 V	"							"				K1	"	"	"
			23				"	3/	4.5 V	0.4 V				"				J2	"	"	"
			24				"	3/	4.5 V				0.4 V	"				K2	"	"	"
			25	0.4 V	B	4.5 V	"							"			4.5 V	Clock 1	"	"	"
			26				"	0.4 V	B	4.5 V			4.5 V	"				Clock 2	"	"	"
	I_{IL2}		27	4.5 V	0.4 V		"							"			4.5 V	Clear 1	-2.0	-4.0	"
			28				"	4.5 V	0.4 V	4.5 V				"				Clear 2	-2.0	-4.0	"
	I_{IH1}	3010	29	GND	GND		"							"			2.4 V	J1		50	μA
			30	GND	B	2.4 V	"							"				K1		"	"
			31				"	GND	GND	2.4 V				"				J2		"	"
			32				"	GND	B				2.4 V	"				K2		"	"
	I_{IH2}		33	GND	GND		"							"			5.5 V	J1		100	"
			34	GND	B	5.5 V	"							"				K1		"	"
			35				"	GND	GND	5.5 V				"				J2		"	"
			36				"	GND	B				5.5 V	"				K2		"	"
	I_{IH3}		37	GND	E		"							"			GND	Clear 1		100	"
			38				"	GND	E	GND				"				Clear 2		100	"
	I_{IH4}		39	GND	F		"							"			GND	Clear 1		200	"
			40				"	GND	F	GND				"				Clear 2		200	"
	I_{IH5}		41	2.4 V	GND	GND	"							"			GND	Clock 1		100	"
			42				"	2.4 V	GND	GND			GND	"				Clock 2		100	"
	I_{IH6}		43	5.5 V	GND	GND	"							"			GND	Clock 1		200	"
			44				"	5.5 V	GND	GND			GND	"				Clock 2		200	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits Min	Limits Max	Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	Q1	$\overline{Q}1$	J1				
1 T_C = +25°C	I_{OS}	3011	45	2.4 V	GND	2.4 V	5.5 V							GND		GND	2.4 V	$\overline{Q}1$	-40	-100	mA
			46*		4.5 V		"							"	GND	GND		Q1	"	"	"
			47*				"		4.5 V		GND	GND		"				Q2	"	"	"
			48				"	2.4 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q}2$	"	"	"
	I_{CC}	3005	49	D	4.5 V	GND	"	D	4.5 V	4.5 V			GND	"			4.5 V	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C = +25°C 4/ 5/			50	A	B	B	4.5 V	A	B	B	H	L	B	GND	L	H	B	All outputs	H or L as shown 6/		
			51	A	A	"	"	A	A	"	"	"	"	"	"	"	"	"	"		
			52	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"		
			53	"	"	A	"	B	"	A	"	"	A	"	"	"	A	"	"		
			54	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"		
			55	B	"	"	"	B	"	"	L	H	"	"	H	L	"	"	"		
			56	A	"	"	"	A	"	"	L	H	"	"	H	L	"	"	"		
			57	"	B	"	"	"	B	"	H	L	"	"	L	H	"	"	"		
			58	"	A	"	"	"	A	"	H	L	"	"	L	H	"	"	"		
			59	B	A	"	"	B	A	"	L	H	"	"	H	L	"	"	"		
			60	"	B	"	"	"	B	"	H	L	"	"	L	H	"	"	"		
			61	"	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"		
			62	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"		
			63	B	"	"	"	B	"	"	L	H	"	"	H	L	"	"	"		
			64	B	"	B	"	B	"	B	"	"	B	"	"	"	B	"	"		
			65	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"		
			66	B	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"		
			67	B	"	A	"	B	"	A	"	"	A	"	"	"	A	"	"		
			68	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"		
			69	B	"	"	"	B	"	"	H	L	"	"	"	"	"	"	"		
8 4/ 5/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C = +25°C	f_{MAX} 6/	(Fig. 7)	70	IN		2.4 V	5.0 V							GND	OUT		2.4 V	Q1	23		MHz
			71	IN		2.4 V	"							"		OUT	2.4 V	$\overline{Q}1$	"		"
			72				"	IN		2.4 V		OUT	2.4 V	"				Q2	"		"
			73				"	IN		2.4 V	OUT		2.4 V	"				$\overline{Q}2$	"		"
	t_{PLH1}	3003 (Fig. 6)	74	IN	IN	GND	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}1$	2	20	ns
			75				"	IN	IN	2.4 V	OUT		GND	"				Clear 2 to $\overline{Q}2$	"	20	"
	t_{PHL1}		76	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	"	27	"
			77				"	IN	IN	2.4 V		OUT	GND	"				Clear 2 to Q2	"	27	"
	t_{PLH2}	3003 (Fig. 7)	78	IN		2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	26	"
			79	IN		2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			80				"	IN		2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			81				"	IN		2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"
	t_{PHL2}		82	IN		2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	34	"
			83	IN		2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			84				"	IN		2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			85				"	IN		2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits Min	Limits Max	Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	$\overline{Q1}$	Q1	J1				
10 T_C = +125°C	f_{MAX}	(Fig. 7)	86	IN		2.4 V	5.0 V							GND	OUT		2.4 V	Q1	20		MHz
			87	IN		2.4 V	*							*		OUT	2.4 V	$\overline{Q1}$	*		*
			88				*	IN		2.4 V		OUT	2.4 V	*				Q2	*		*
			89				*	IN		2.4 V	OUT		2.4 V	*				$\overline{Q2}$	*		*
	t_{PLH1}	3003 (Fig. 6)	90	IN	IN	GND	*							*		OUT	2.4 V	Clear 1 to $\overline{Q1}$	2	20	ns
			91				*	IN	IN	2.4 V	OUT		GND	*				Clear 2 to $\overline{Q2}$	*	20	*
	t_{PHL1}		92	IN	IN	GND	*							*	OUT		2.4 V	Clear 1 to Q1	*	31	*
			93				*	IN	IN	2.4 V		OUT	GND	*				Clear 2 to Q2	*	31	*
	t_{PLH2}	3003 (Fig. 7)	94	IN		2.4 V	*							*	OUT		2.4 V	Clock 1 to Q1	*	35	*
			95	IN		2.4 V	*							*		OUT	2.4 V	Clock 1 to $\overline{Q1}$	*	*	*
			96				*	IN		2.4 V		OUT	2.4 V	*				Clock 2 to Q2	*	*	*
			97				*	IN		2.4 V	OUT		2.4 V	*				Clock 2 to $\overline{Q2}$	*	*	*
	t_{PHL2}		98	IN		2.4 V	*							*	OUT		2.4 V	Clock 1 to Q1	*	42	*
			99	IN		2.4 V	*							*		OUT	2.4 V	Clock 1 to $\overline{Q1}$	*	*	*
			100				*	IN		2.4 V		OUT	2.4 V	*				Clock 2 to Q2	*	*	*
			101				*	IN		2.4 V	OUT		2.4 V	*				Clock 2 to $\overline{Q2}$	*	*	*
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.

B = Momentary GND, then 4.5 V.

D = Momentary 4.5 V, then GND.

E = Momentary GND, then 2.4 V.

F = Momentary GND, then 5.5 V.

* = Test time limit ≥ 100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Qualification requirements are removed for this device type.

3/ Input shall be one normal clock pulse, then 4.5 V.

4/ Tests shall be performed in sequence.

5/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.

6/ Output voltages shall be either: H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

7/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 03. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D / Case C / Test no.	1 / 3 / Clock 1	2 / 2 / D1	3 / 1 / Clear 1	4 / 14 / V_{CC}	5 / 13 / Clear 2	6 / 12 / D2	7 / 11 / Clock 2	8 / 10 / Preset 2	9 / 9 / Q2	10 / 8 / $\overline{Q2}$	11 / 7 / GND	12 / 6 / Q1	13 / 5 / $\overline{Q1}$	14 / 4 / Preset 1	Measured terminal	Limits Min	Limits Max	Unit
T_C = +25°C [1]	V_{OH}	3006	1	A	2.0 V		4.5 V							GND		-1 mA	2.0 V	Q1	2.4		V
			2	A	0.8 V		"							"	-1 mA		0.8 V	$\overline{Q1}$	"		"
			3			0.8 V	"							"	-1 mA	-1 mA		Q1	"		"
			4			2.0 V	"							"				Q1	"		"
			5				"		2.0 V	A		-1 mA		"				Q2	"		"
			6				"		0.8 V	A			-1 mA	"				$\overline{Q2}$	"		"
			7				"	0.8 V			2.0 V		-1 mA	"				$\overline{Q2}$	"		"
			8				"	2.0 V			0.8 V	-1 mA		"				Q2	"		"
	V_{OL}	3007	9	A	2.0 V		"							"	20 mA			$\overline{Q1}$		0.4	"
			10	A	0.8 V		"							"		20 mA	2.0 V	Q1		"	"
			11			0.8 V	"							"		20 mA	0.8 V	Q1		"	"
			12			2.0 V	"							"	20 mA			$\overline{Q1}$		"	"
			13				"		2.0 V	A			20 mA	"				$\overline{Q2}$		"	"
			14				"		0.8 V	A		20 mA		"				Q2		"	"
			15				"	0.8 V			2.0 V	20 mA		"				Q2		"	"
			16				"	2.0 V			0.8 V		20 mA	"				$\overline{Q2}$		"	"
	V_{IC}		17		-12 mA		"							"				D1		-1.5	"
			18	-12 mA			"							"				Clock 1		"	"
			19			-12 mA	"							"				Clear 1		"	"
			20				"							"			-12 mA	Preset 1		"	"
			21				"		-12 mA					"				D2		"	"
			22				"			-12 mA				"				Clock 2		"	"
			23				"	-12 mA						"				Clear 2		"	"
			24				"				-12 mA			"				Preset 2		"	"
	I_{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							"			GND	D1	-1.0	-2.0	mA
			26				"	4.5 V	0.4 V	4.5 V	GND			"				D2	"	"	"
			27	GND	GND	4.5 V	"							"			0.4 V	Preset 1	"	"	"
			28				"	4.5 V	GND	GND	0.4 V			"				Preset 2	"	"	"
	I_{IL2}		29	0.4 V	GND	4.5 V	"							"			GND	Clock 1	-2.0	-4.0	V
			30 CKT A,C	4.5 V	4.5 V	0.4 V	"							"			GND	Clear 1	-3.0	-6.0	"
			30 CKT B	0.8 V	4.5 V	0.4 V	"							"			4.5 V	Clear 1	-1.0	-4.0	"
			31				"	4.5 V	GND	0.4 V	GND			"				Clock 2	-2.0	-4.0	"
			32 CKT A,C				"	0.4 V	4.5 V	4.5 V	GND			"				Clear 2	-3.0	-6.0	"
			32 CKT B				"	0.4 V	4.5 V	0.8 V	4.5 V			"				Clear 2	-1.0	-4.0	"
	I_{IH1}	3010	33	4.5 V	2.4 V	GND	"							"			4.5 V	D1		50	uA
			34				"	GND	2.4 V	4.5 V	4.5 V			"				D2		50	"
	I_{IH2}		35	4.5 V	5.5 V	GND	"							"			4.5 V	D1		100	"
			36				"	GND	5.5 V	4.5 V	4.5 V			"				D2		"	"
	I_{IH3}		37	2.4 V	4.5 V	GND	"							"			4.5 V	Clock 1		"	"
			38	B	4.5 V	4.5 V	"							"			2.4 V	Preset 1		"	"
			39				"	GND	4.5 V	2.4 V	4.5 V			"				Clock 2		"	"
			40				"	4.5 V	4.5 V	B	2.4 V			"				Preset 2		"	"
	I_{IH4}		41	5.5 V	4.5 V	GND	"							"			4.5 V	Clock 1		200	"
			42	B	4.5 V	4.5 V	"							"			5.5 V	Preset 1		"	"
			43				"	GND	4.5 V	5.5 V	4.5 V			"				Clock 2		"	"
			44				"	4.5 V	4.5 V	B	5.5 V			"				Preset 2		"	"
	I_{IH5}		45	B	GND	2.4 V	"							"			4.5 V	Clear 1		150	"
			46				"	2.4 V	GND	B	4.5 V			"				Clear 2		150	"
	I_{IH6}		47	B	GND	5.5 V	"							"			4.5 V	Clear 1		300	"
			48				"	5.5 V	GND	B	4.5 V			"				Clear 2		300	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D / Case C / Test no.	1 / 3 / Clock 1	2 / 2 / D1	3 / 1 / Clear 1	4 / 14 / V_{CC}	5 / 13 / Clear 2	6 / 12 / D2	7 / 11 / Clock 2	8 / 10 / Preset 2	9 / 9 / Q2	10 / 8 / $\overline{Q2}$	11 / 7 / GND	12 / 6 / $\overline{Q1}$	13 / 5 / Q1	14 / 4 / Preset 1	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	I_{OS}	3011	49			GND	5.5 V				GND	GND	GND	GND	GND	GND	GND	Q1	-40	-100	mA
			50				"							"				$\overline{Q1}$	"	"	"
			51				"							"				Q2	"	"	"
			52				"	GND						"				$\overline{Q2}$	"	"	"
	I_{CC}	3005	53	GND	GND	4.5 V	"	4.5 V	GND	GND	GND			"			GND	V_{CC}		50	"
			54	GND	GND	GND	"	GND	GND	GND	4.5 V			"			4.5 V	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C = +25°C 3/ 4/			55	B	B	B	4.5 V	B	B	B	B	H	H	GND	H	H	B	All outputs	H or L as shown 5/		
			56	"	"	B	"	B	"	"	A	L	"	"	"	L	A	"	"		
			57	"	"	A	"	A	"	"	A	L	"	"	"	L	A	"	"		
			58	"	"	"	"	"	"	"	B	H	L	"	L	H	B	"	"		
			59	A	"	"	"	"	"	A	"	"	L	"	L	"	"	"	"		
			60	"	"	B	"	B	"	"	"	"	H	"	H	"	"	"	"		
			61	"	A	"	"	B	A	"	"	"	"	"	"	L	A	"	"		
			62	"	"	"	"	A	"	"	A	L	"	"	"	L	A	"	"		
			63	"	"	A	"	"	"	"	A	L	"	"	"	H	B	"	"		
			64	"	"	"	"	"	"	"	B	H	L	"	L	"	A	"	"		
			65	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"	"		
			66	B	"	"	"	"	"	B	"	"	"	"	"	"	"	"	"		
			67	B	B	"	"	"	B	B	"	"	"	"	"	"	"	"	"		
			68	A	"	"	"	"	"	A	"	L	H	"	H	L	B	"	"		
			69	"	"	"	"	"	"	"	B	H	L	"	L	H	"	"	"		
			70	"	A	B	"	B	A	"	"	"	H	"	H	"	"	"	"		
			71	"	B	"	"	"	B	"	"	"	"	"	"	"	A	"	"		
			72	"	"	"	"	"	"	"	A	L	"	"	"	L	"	"	"		
			73	"	"	A	"	A	"	"	"	"	"	"	"	"	"	"	"		
			74	B	A	"	"	"	A	B	"	"	"	"	"	"	"	"	"		
			75	A	"	"	"	"	"	A	"	H	L	"	"	H	B	"	"		
			76	"	"	"	"	"	"	"	B	"	"	"	"	"	A	"	"		
			77	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"	"		
			78	"	"	B	"	B	"	"	"	L	H	"	H	L	"	"	"		
			79	"	"	A	"	A	"	"	"	L	H	"	H	L	"	"	"		
			80	"	B	"	"	"	B	"	B	H	L	"	L	H	B	"	"		
			81	"	B	"	"	"	B	"	A	H	L	"	L	H	A	"	"		
8 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C = +25°C	f_{MAX} 6/	(Fig. 10)	82	IN	E		5.0 V				5.0 V	OUT		GND	OUT	OUT	5.0 V	Q1	35		MHz
			83	IN	E		"				5.0 V			"			5.0 V	$\overline{Q1}$	"		"
			84				"		E	IN				"				Q2	"		"
			85						E	IN			OUT	"				$\overline{Q2}$	"		"
	t_{PLH1}	3003 (Fig. 8)	86			IN	"							"	OUT		J	Clear 1 to Q1	2	20	ns
			87			J	"							"		OUT	IN	Preset 1 to Q1	"	"	"
			88				"	IN			J		OUT	"				Clear 2 to $\overline{Q2}$	"	"	"
			89				"	J			IN	OUT		"				Preset 2 to Q2	"	"	"
	t_{PHL1}		90			IN	"							"		OUT	J	Clear 1 to Q1	"	32	"
			91			J	"							"	OUT		IN	Preset 1 to $\overline{Q1}$	"	"	"
			92				"	IN			J	OUT		"				Clear 2 to Q2	"	"	"
			93				"	J			IN		OUT	"				Preset 2 to $\overline{Q2}$	"	"	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D / Case C / Test no.	1 / 3 / Clock 1	2 / 2 / D1	3 / 1 / Clear 1	4 / 14 / VCC	5 / 13 / Clear 2	6 / 12 / D2	7 / 11 / Clock 2	8 / 10 / Preset 2	9 / 9 / Q2	10 / 8 / $\overline{Q2}$	11 / 7 / GND	12 / 6 / $\overline{Q1}$	13 / 5 / Q1	14 / 4 / Preset 1	Measured terminal	Limits Min	Limits Max	Unit
9 T_C = +25°C	t_{PLH2}	3003 (Fig. 9)	94	IN	IN (A)	B	5.0 V							GND		OUT	5.0 V	Clock 1 to Q1	2	17	ns
		(Fig. 10)	95	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 9)	96				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 10)	97				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q2}$	"	"	"
	t_{PHL2}	3003 (Fig. 10)	98	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	22	"
		(Fig. 9)	99	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 10)	100				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 9)	101				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q2}$	"	"	"
10 T_C = +125°C	f_{MAX}	(Fig. 9) 6/	102	IN	E		"							"		OUT	5.0 V	Q1	28	"	MHz
			103	IN	E		"							"	OUT		5.0 V	$\overline{Q1}$	"	"	"
			104				"		E	IN	5.0 V	OUT		"				Q2	"	"	"
			105				"		E	IN	5.0 V		OUT	"				$\overline{Q2}$	"	"	"
	t_{PLH1}	3003 (Fig. 8)	106			IN	"							"	OUT		J	Clear 1 to Q1	2	27	ns
			107			J	"							"		OUT	IN	Preset 1 to $\overline{Q1}$	"	"	"
			108				"	IN			J		OUT	"				Clear 2 to Q2	"	"	"
			109				"	J			IN	OUT		"				Preset 2 to $\overline{Q2}$	"	"	"
	t_{PHL1}		110			IN	"							"		OUT	J	Clear 1 to $\overline{Q1}$	"	38	"
			111			IN	"							"	OUT		IN	Preset 1 to Q1	"	"	"
			112				"	IN			J	OUT		"				Clear 2 to $\overline{Q2}$	"	"	"
			113				"	J			IN		OUT	"				Preset 2 to Q2	"	"	"
	t_{PLH2}	3003 (Fig. 9)	114	IN	IN (A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	"	22	"
		(Fig. 10)	115	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 9)	116				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 10)	117				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q2}$	"	"	"
	t_{PHL2}	3003 (Fig. 10)	118	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	28	"
		(Fig. 9)	119	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 10)	120				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 9)	121				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q2}$	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
D = Momentary 4.5 V, then GND.
E = Input D connected to $\overline{Q}$.
J = Input pulse, $t_p \geq 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open).
2/ Qualification requirements are removed for this device type.
3/ Tests shall be performed in sequence.
4/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
5/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H $\geq$ 1.5 V and L $\leq$ 1.5 V when using a high speed checker single comparator.
6/ The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 04. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits Min	Limits Max	Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	$\overline{Q}1$	Q1	K1				
T_C = +25°C [1]	V_{OH}	3006	1	A			2.0 V	4.5 V								GND		-0.5 mA	0.8 V	Q1	2.4		V
			2	A			0.8 V	"								"	-0.5 mA		2.0 V	$\overline{Q}1$	"		"
			3		2.0 V	0.8 V		"								"	-0.5 mA			$\overline{Q}1$	"		"
			4		0.8 V	2.0 V		"								"		-0.5 mA		Q1	"		"
			5					"	A			2.0 V		-0.5 mA	0.8 V	"				$\overline{Q}2$	"		"
			6					"	A			0.8 V	-0.5 mA		2.0 V	"				$\overline{Q}2$	"		"
			7					"		2.0 V	0.8 V		-0.5 mA			"				$\overline{Q}2$	"		"
			8					"		0.8 V	2.0 V			-0.5 mA		"				Q2	"		"
	V_{OL}	3007	9	A			0.8 V	"								"		20 mA	2.0 V	Q1		0.4	"
			10	A			2.0 V	"								"	20 mA		0.8 V	$\overline{Q}1$		"	"
			11		0.8 V	2.0 V		"								"	20 mA			$\overline{Q}1$		"	"
			12		2.0 V	0.8 V		"								"		20 mA		Q1		"	"
			13					"	A			0.8 V		20 mA	2.0 V	"				Q2		"	"
			14					"	A			2.0 V	20 mA		0.8 V	"				$\overline{Q}2$		"	"
			15					"		0.8 V	2.0 V		20 mA			"				$\overline{Q}2$		"	"
			16					"		2.0 V	0.8 V			20 mA		"				Q2		"	"
	V_{IC}		17				-12 mA	"								"				J1		-1.5	"
			18					"				-12 mA				"			-12 mA	K1		"	"
			19					"							-12 mA	"				J2		"	"
			20					"								"				K2		"	"
			21	-12 mA				"								"				Clock 1		"	"
			22		-12 mA			"								"				Preset 1		"	"
			23			-12 mA		"								"				Clear 1		"	"
			24					"	-12 mA							"				Clock 2		"	"
			25					"		-12 mA						"				Preset 2		"	"
			26					"			-12 mA					"				Clear 2		"	"
	I_{IL1}	3009	27	4.5 V		B	0.4 V	5.5 V								"			0.4 V	J1	-1.0	-2.0	mA
			28	4.5 V	B			"								"				K1	"	"	"
			29					"	4.5 V		B	0.4 V				"				J2	"	"	"
			30					"	4.5 V	B					0.4 V	"				K2	"	"	"
			31	0.4 V	B		4.5 V	"								"			4.5 V	Clock 1	"	"	"
			32	0.4 V		B	4.5 V	"								"			4.5 V	Clock 1	"	"	"
			33					"	0.4 V	B		4.5 V			4.5 V	"				Clock 2	"	"	"
			34					"	0.4 V		B	4.5 V			4.5 V	"				Clock 2	"	"	"
	I_{IL2}		35	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-2.0	-4.0	"
			36	4.5 V	0.4 V		4.5 V	"								"			4.5 V	Preset 1	"	"	"
			37					"	4.5 V		0.4 V	4.5 V			4.5 V	"				Clear 2	"	"	"
			38					"	4.5 V	0.4 V		4.5 V			4.5 V	"				Preset 2	"	"	"
	I_{IH1}	3010	39	GND		GND	2.4 V	"								"				J1		50	"
			40	GND	GND			"								"			2.4 V	K1		"	"
			41					"	GND		GND	2.4 V				"				J2		"	"
			42					"	GND	GND					2.4 V	"				K2		"	"
	I_{IH2}		43	GND		GND	5.5 V	"								"				J1		100	"
			44	GND	GND			"								"			5.5 V	K1		"	"
			45					"	GND		GND	5.5 V				"				J2		"	"
			46					"	GND	GND					5.5 V	"				K2		"	"
	I_{IH3}		47	2.4 V		GND	GND	"								"			GND	Clock 1		100	"
			48	GND		E	GND	"								"				Clear 1		"	"
			49	GND	E			"								"			GND	Preset 1		"	"
			50					"	2.4 V		GND	GND			GND	"				Clock 2		"	"
			51					"	GND		E	GND				"				Clear 2		"	"
			52					"	GND	E					GND	"				Preset 2		"	"
	I_{IH4}		53	5.5 V		GND	GND	"								"			GND	Clock 1		200	"
			54	GND		F	GND	"								"				Clear 1		"	"
			55	GND	F			"								"			GND	Preset 1		"	"
			56					"	5.5 V		GND	GND			GND	"				Clock 2		"	"
			57					"	GND		F	GND				"				Clear 2		"	"
			58					"	GND	F					GND	"				Preset 2		"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits Min	Limits Max	Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	$\overline{Q}1$	Q1	K1				
1 T_C = +25°C	I_{OS}	3011	59**	2.4 V	GND	4.5 V	2.4 V	5.5 V								GND		GND	2.4 V	Q1	-40	-100	mA
			60	2.4 V	4.5 V	GND	2.4 V	"								"	GND		2.4 V	$\overline{Q}1$	"	"	"
			61**					"	2.4 V	GND	4.5 V	2.4 V		GND	2.4 V	"				Q2	"	"	"
			62					"	2.4 V	4.5 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q}2$	"	"	"
	I_{CC}	3005	63	GND	4.5 V	GND	GND	"	GND	4.5 V	GND	GND			GND	"			GND	V_{CC}		50	"
			64	GND	GND	4.5 V	GND	"	GND	GND	4.5 V	GND			GND	"			GND	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 T_C = +25°C 2/ 3/			65	A	B	B	B	4.5 V	A	B	B	B	H	H	B	GND	H	H	B	All Outputs	H or L as shown 4/		
			66	"	B	A	"	"	"	B	A	"	L	H	"	"	L	H	"	"	"		
			67	"	A	B	"	"	"	A	B	"	H	L	"	"	H	L	"	"	"		
			68	B	"	A	"	"	B	"	A	"	"	"	"	"	"	"	"	"	"	"		
			69	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"		
			70	B	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"		
			71	B	"	"	A	"	B	"	"	A	"	"	A	"	"	"	A	"	"	"		
			72	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"		
			73	B	"	"	"	"	B	"	"	"	L	H	"	"	L	H	"	"	"		
			74	B	"	"	B	"	B	"	"	B	"	"	B	"	"	"	B	"	"	"		
			75	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"		
			76	B	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"		
			77	B	"	"	A	"	B	"	"	A	"	"	A	"	"	"	A	"	"	"		
			78	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"		
			79	B	"	"	"	"	B	"	"	"A	H	L	"	"	H	L	"	"	"	"		
8 2/ 3/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																						
9 T_C = +25°C	f_{MAX} 5/	(Fig. 12)	80	IN	5.0 V	5.0 V	2.4 V	5.0 V								GND	OUT	OUT	2.4 V	Q1	25		MHz
			81	IN	5.0 V	5.0 V	2.4 V	"								"			2.4 V	$\overline{Q}1$	"		"
			82					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			83					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q}2$	"		"
	t_{PLH1}	3003 (Fig. 11)	84	2.4 V		IN	2.4 V	"								"	OUT		2.4 V	Clear 1 to $\overline{Q}1$	2	16	ns
			85	2.4 V	IN		2.4 V	"								"		OUT	2.4 V	Preset 1 to Q1	"	"	"
			86					"	2.4 V		IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}2$	"	"	"
			87					"	2.4 V	IN		2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	"	"
	t_{PHL1}		88	2.4 V		IN	2.4 V	"								"		OUT	2.4 V	Clear 1 to Q1	"	27	"
			89	2.4 V	IN		2.4 V	"								"	OUT		2.4 V	Preset 1 to $\overline{Q}1$	"	"	"
			90					"	2.4 V		IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q2	"	"	"
			91					"	2.4 V	IN		2.4 V	OUT		2.4 V	"				Preset 2 to $\overline{Q}2$	"	"	"
	t_{PLH2}	3003 (Fig. 12)	92	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	24	"
			93	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			94					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			95					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"
	t_{PHL2}		96	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	30	"
			97	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			98					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			99					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"

See footnotes at end of device 04.

TABLE III. Group A inspection for device type 04 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits Min	Limits Max	Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	$\overline{Q}1$	Q1	K1				
10 T_C = +125°C	f_{MAX} 5/	(Fig. 12)	100	IN	5.0 V	5.0 V	2.4 V	5.0 V								GND			2.4 V	Q1	20		MHz
			101	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	$\overline{Q}1$	"		"
			102					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			103					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q}2$	"		"
	t_{PLH1}	3003 (Fig. 11)	104	2.4 V		IN	2.4 V	"								"	OUT		2.4 V	Clear 1 to $\overline{Q}1$	2	20	ms
			105	2.4 V	IN		2.4 V	"								"		OUT	2.4 V	Preset 1 to Q1	"	"	"
			106					"	2.4 V		IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}2$	"	"	"
			107					"	2.4 V	IN		2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	"	"
	t_{PHL1}		108	2.4 V		IN	2.4 V	"								"		OUT	2.4 V	Clear 1 to Q1	"	32	"
			109	2.4 V	IN		2.4 V	"								"	OUT		2.4 V	Preset 1 to $\overline{Q}1$	"	"	"
			110					"	2.4 V		IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q2	"	"	"
			111					"	2.4 V	IN		2.4 V	OUT		2.4 V	"				Preset 2 to $\overline{Q}2$	"	"	"
	t_{PLH2}	3003 (Fig. 12)	112	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	28	"
			113	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			114					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			115					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"
	t_{PHL2}		116	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	36	"
			117	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}1$	"	"	"
			118					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			119					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}2$	"	"	"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																						

A = Normal clock pulse.

B = Momentary GND, then 4.5 V.

E = Momentary GND, then 2.4 V.

F = Momentary GND, then 5.5 V.

** = Test time limit ≤ 100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Tests shall be performed in sequence.

3/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.

4/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

6/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D Case C Test no.	1 9 K1A	2 10 K1B	3 13 Clock	4 14 V_{CC}	5 1 J1A	6 2 J1B	7 3 J2A	8 4 J2B	9 5 Preset	10 6 Q	11 7 GND	12 8 $\overline{Q}$	13 11 K2A	14 11 K2B	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	V_{OH}	3006	1	0.8 V	0.8 V	A	4.5 V	2.0 V	2.0 V	2.0 V	2.0 V		-0.5 mA	GND		0.8 V	0.8 V	Q	2.4		V
			2	2.0 V	2.0 V	A	"	0.8 V	0.8 V	0.8 V	0.8 V			"	-0.5 mA	2.0 V	2.0 V	$\overline{Q}$	"		"
			3	2.0 V	2.0 V	2.0 V	"	2.0 V	2.0 V	2.0 V			-0.5 mA	"		2.0 V	2.0 V	Q	"		"
	V_{OL}	3007	4	0.8 V	0.8 V	A	"	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V		"	20 mA	0.8 V	0.8 V	Q		0.4	"
			5	2.0 V	2.0 V	A	"	0.8 V	0.8 V	0.8 V	0.8 V		20 mA	"		2.0 V	2.0 V	$\overline{Q}$		"	"
			6	2.0 V	2.0 V	2.0 V	"	2.0 V	2.0 V	2.0 V		0.8 V		"	20 mA	2.0 V	2.0 V	$\overline{Q}$		"	"
	V_{IC}		7				"	-12 mA						"				J1A		-1.5	"
			8				"		-12 mA					"				J1B		"	"
			9				"			-12 mA				"				J2A		"	"
			10				"				-12 mA			"				J2B		"	"
			11	-12 mA			"							"				K1A		"	"
			12		-12 mA		"							"				K1B		"	"
			13				"							"		-12 mA		K2A		"	"
			14				"							"			-12 mA	K2B		"	"
			15			-12 mA	"							"				Clock		"	"
			16				"					-12 mA		"				Preset		"	"
	I_{IL1}	3009	17	4.5 V	4.5 V	4.5 V	5.5 V	4.5 V	4.5 V	4.5 V	4.5 V	0.4 V		"		4.5 V	4.5 V	Preset	-0.7	-2.0	mA
			18*	"	"	3/	"	0.4 V	4.5 V	GND	"	4.5 V		"		"	"	J1A	"	"	"
			19*	"	"	"	"	4.5 V	0.4 V	GND	"	"		"		"	"	J1B	"	"	"
			20*	"	"	"	"	GND	4.5 V	0.4 V	"	"		"		"	"	J2A	"	"	"
			21*	"	"	"	"	GND	"	4.5 V	0.4 V	"		"		"	"	J2B	"	"	"
			22	0.4 V	"	4.5 V	"	4.5 V	"	"	4.5 V	GND		"		"	"	K1A	"	"	"
			23	4.5 V	0.4 V	"	"	"	"	"	"	"		"		"	"	K1B	"	"	"
			24	"	4.5 V	"	"	"	"	"	"	"		"		0.4 V	"	K2A	"	"	"
			25	"	"	"	"	"	"	"	"	"		"		4.5 V	0.4 V	K2B	"	"	"
	I_{IL2}		26	"	"	0.4 V	"	"	"	"	"	"		"		"	4.5 V	Clock	-2.0	-4.8	"
	I_{IH1}	3010	27	"	"	GND	"	2.4 V	GND	GND	GND	"		"		"	"	J1A		50	µA
			28	"	"	"	"	GND	2.4 V	GND	GND	"		"		"	"	J1B		"	"
			29	"	"	"	"	"	GND	2.4 V	GND	"		"		"	"	J2A		"	"
			30	"	"	"	"	"	GND	GND	2.4 V	"		"		"	"	J2B		"	"
			31	2.4 V	GND	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		GND	GND	K1A		"	"
			32	GND	2.4 V	"	"	"	"	"	"	"		"		GND	"	K1B		"	"
			33	"	GND	"	"	"	"	"	"	"		"		2.4 V	"	K2A		"	"
			34	"	GND	"	"	"	"	"	"	"		"		GND	2.4 V	K2B		"	"
	I_{IH2}		35	4.5 V	4.5 V	"	"	5.5 V	GND	GND	GND	GND		"		4.5 V	4.5 V	J1A		100	"
			36	"	"	"	"	GND	4.5 V	GND	GND	"		"		"	"	J1B		"	"
			37	"	"	"	"	"	GND	5.5 V	GND	"		"		"	"	J2A		"	"
			38	"	"	"	"	"	GND	GND	5.5 V	"		"		"	"	J2B		"	"
			39	5.5 V	GND	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		GND	GND	K1A		"	"
			40	GND	5.5 V	"	"	"	"	"	"	"		"		GND	"	K1B		"	"
			41	"	GND	"	"	"	"	"	"	"		"		5.5 V	"	K2A		"	"
			42	"	"	"	"	"	"	"	"	"		"		GND	5.5 V	K2B		"	"
	I_{IH3}		43*	"	"	D	"	"	"	"	"	2.4 V		"		"	GND	Preset		"	"
	I_{IH4}		44*	"	"	D	"	"	"	"	"	5.5 V		"		"	"	Preset		200	"
	I_{IH5}		45	"	"	2.4 V	"	GND	GND	GND	GND	GND		"		"	"	Clock		-1	mA
	I_{IH6}		46	"	"	5.5 V	"	GND	GND	GND	GND	GND		"		"	"	Clock		1	mA

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D Case C Test no.	1 9 K1A	2 10 K1B	3 13 Clock	4 14 V_{CC}	5 1 J1A	6 2 J1B	7 3 J2A	8 4 J2B	9 5 Preset	10 6 Q	11 7 GND	12 8 $\overline{Q}$	13 11 K2A	14 11 K2B	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	I_{OS}	3011	47	2.4 V	2.4 V	2.4 V	5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	GND	GND		2.4 V	2.4 V	Q	-40	-100	mA
			48	2.4 V	2.4 V	2.4 V	"	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	"	GND	2.4 V	2.4 V	$\overline{Q}$	-40	-100	"
	I_{CC}	3005	49	GND	GND	GND	"	GND	GND	GND	GND	GND		"		GND	GND	V_{CC}		38	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C = +25°C 4/ 5/			50	B	A	A	4.5 V	B	A	B	A	B	H	GND	L	B	A	All outputs	H or L as shown 6/		
			51	"	"	A	"	"	"	"	"	A	"	"	"	"	"	"	"		
			52	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"		
			53	"	"	A	"	"	"	"	"	"	"	"	"	A	"	"	"		
			54	"	"	B	"	"	"	"	"	"	L	"	H	"	"	"	"		
			55	"	"	A	"	"	"	"	"	"	L	"	H	"	"	"	"		
			56	"	"	A	"	"	"	"	"	B	H	"	L	"	"	"	"		
			57	"	"	B	"	"	"	"	"	B	"	"	"	"	"	"	"		
			58	A	B	A	"	"	"	"	"	A	"	"	"	"	B	"	"		
			59	"	B	B	"	"	"	"	"	"	"	"	"	"	"	"	"		
			60	"	A	A	"	A	"	"	"	"	"	"	"	"	"	"	"		
			61	"	A	B	"	A	"	"	"	"	L	"	H	"	"	"	"		
			62	"	B	A	"	B	"	"	"	"	"	"	"	"	"	"	"		
			63	"	"	B	"	B	"	"	"	"	"	"	"	"	"	"	"		
			64	"	"	A	"	A	B	A	B	"	"	"	"	"	"	"	"		
			65	"	"	B	"	"	B	"	"	"	"	"	"	"	"	"	"		
			66	"	A	A	"	"	A	"	"	"	"	"	"	"	"	"	"		
			67	"	A	B	"	"	A	"	"	"	H	"	L	"	"	"	"		
			68	"	B	A	"	"	B	"	A	"	H	"	L	"	A	"	"		
			69	"	"	B	"	"	"	"	"	"	L	"	H	"	"	"	"		
			70	"	"	A	"	"	"	"	"	"	L	"	H	"	"	"	"		
			71	"	"	B	"	"	"	"	"	"	H	"	L	"	"	"	"		
8 4/5/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C = +25°C	f_{MAX} 5/	(Fig. 14)	72	2.4 V	2.4 V	IN	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	5.0 V	OUT	GND		2.4 V	2.4 V	Q	36		MHz
			73	"	"	"	"	"	"	"	"	5.0 V		"	OUT	"	"	$\overline{Q}$	36		MHz
	t_{PLH1}	3003 (Fig. 14)	74	"	"	"	"	"	"	"	"	IN	OUT	"		"	"	Preset to Q	2	23	ns
			75	"	"	"	"	"	"	"	"	IN		"	OUT	"	"	Preset to $\overline{Q}$	"	23	"
	t_{PLH2}	3003 (Fig. 14)	76	"	"	"	"	H	"	GND	GND		OUT	"		GND	GND	Clock Q	"	18	"
			77	H	"	"	"	2.4 V	"	"	"			"	OUT	"	"	Clock $\overline{Q}$	"	18	"
	t_{PHL2}		78	L	"	"	"	2.4 V	"	"	"		OUT	"		"	"	Clock Q	"	23	"
			79	2.4 V	"	"	"	H	"	"	"			"	OUT	"	"	Clock $\overline{Q}$	"	23	"

TABLE III. Group A inspection for device type 05 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	10	13	14	1	2	3	4	5	6	7	8	11	11		Min	Max	
			Test no.	K1A	K1B	Clock	V_{CC}	J1A	J1B	J2A	J2B	Preset	Q	GND	$\overline{Q}$	K2A	K2B				
10 T_C = +125°C	f_{MAX} 6/	(Fig. 14)	80	2.4 V	2.4 V	IN	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	5.0 V	OUT	GND		2.4 V	2.4 V	Q	30		MHz
			81	"	"	"	"	"	"	"	"	5.0 V		"	OUT	"	"	$\overline{Q}$	30		MHz
	t_{PLH1}	3003 (Fig. 14)	82	"	"	"	"	"	"	"	"	IN	OUT	"		"	"	Preset to Q	2	28	ns
			83	"	"	"	"	"	"	"	"	IN		"	OUT	"	"	Preset to $\overline{Q}$	"	28	"
	t_{PLH2}	3003 (Fig. 14)	84	"	"	"	"	H	"	GND	GND		OUT	"		GND	GND	Clock Q	"	23	"
			85	H	"	"	"	2.4 V	"	"	"			"	OUT	"	"	Clock $\overline{Q}$	"	23	"
	t_{PHL2}		86	L	"	"	"	2.4 V	"	"	"		OUT	"		"	"	Clock Q	"	28	"
			87	2.4 V	"	"	"	H	"	"	"			"	OUT	"	"	Clock $\overline{Q}$	"	28	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.

D = Momentary 4.5 V, then GND.

H = t_{setup} waveform, see figure 14.

L = t_{setup} waveform, see figure 14.

M = t_{setup} waveform, see figure 14.

* = Duration of test should not exceed 1 second.

** = Limit duration of this test to 100 ms.

1/ Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open).

2/ Qualification requirements are removed for this device type.

3/ The clock input shall be 4.5 V with a momentary low pulse and then 4.5 V(4.5 V).

4/ Tests shall be performed in sequence.

5/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.

6/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H $\geq$ 1.5 V and L $\leq$ 1.5 V when using a high speed checker single comparator.

7/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 06. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D / Case C / Test no.	1 / 1 / Clock 1	2 / 2 / Clear 1	3 / 3 / K1	4 / 4 / V_{CC}	5 / 5 / Clock 2	6 / 6 / Clear 2	7 / 7 / J2	8 / 8 / $\overline{Q}2$	9 / 9 / Q2	10 / 10 / K2	11 / 11 / GND	12 / 12 / Q1	13 / 13 / $\overline{Q}1$	14 / 14 / J1	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	V_{OH}	3006	1	D		0.8 V	4.5 V							GND	-0.5 mA		2.0 V	Q1	2.4		V
			2	D		2.0 V	"							"		-0.5 mA	0.8 V	$\overline{Q}1$	"		"
			3		0.8 V		"							"		-0.5 mA		$\overline{Q}1$	"		"
			4				"	D		2.0 V		-0.5 mA	0.8 V	"				Q2	"		"
			5				"	D		0.8 V	-0.5 mA		2.0 V	"				$\overline{Q}2$	"		"
			6				"		0.8 V		-0.5 mA			"				$\overline{Q}2$	"		"
	V_{OL}	3007	7	D		2.0 V	"							"	20 mA		0.8 V	Q1		0.4	"
			8	D		0.8 V	"							"		20 mA	2.0 V	$\overline{Q}1$		"	"
			9		0.8 V		"							"	20 mA			Q1		"	"
			10				"	D		0.8 V		20 mA	2.0 V	"				Q2		"	"
			11				"	D		2.0 V	20 mA		0.8 V	"				$\overline{Q}2$		"	"
			12				"		0.8 V			20 mA		"				Q2		"	"
	V_{IC}		13				"							"			-12 mA	J1		-1.5	"
			14				"			-12 mA				"				J2		"	"
			15			-12 mA	"							"				K1		"	"
			16				"						-12 mA	"				K2		"	"
			17		-12 mA		"							"				Clear 1		"	"
			18	-12 mA			"							"				Clock 1		"	"
			19				"		-12 mA					"				Clear 2		"	"
			20				"	-12 mA						"				Clock 2		"	"
	I_{IL1}	3009	21	4.5 V	GND	4.5 V	5.5 V							"			0.4 V	J1	-0.7	-2.0	mA
			22**	3/	4.5 V	0.4 V	"							"			4.5 V	K1	"	"	"
			23				"	4.5 V	GND	0.4 V			4.5 V	"		GND		J2	"	"	"
			24**				"	3/	4.5 V	4.5 V	GND		0.4 V	"				K2	"	"	"
			25	4.5 V	0.4 V	4.5 V	"							"			4.5 V	Clear 1	"	"	"
			26				"	4.5 V	0.4 V	4.5 V			4.5 V	"				Clear 2	"	"	"
	I_{IL2}		27	0.4 V	GND	4.5 V	"							"			4.5 V	Clock 1	-2.0	-4.8	"
			28				"	0.4 V	GND	4.5 V			4.5 V	"				Clock 2	-2.0	-4.8	"
	I_{IH1}	3010	29	D	4.5 V	GND	"							"			2.4 V	J1		50	μA
			30				"	D	4.5 V	2.4 V			GND	"				J2		"	"
			31	GND	GND	2.4 V	"							"			4.5 V	K1		"	"
			32				"	GND	GND	4.5 V			2.4 V	"				K2		"	"
	I_{IH2}		33	D	4.5 V	GND	"							"			5.5 V	J1		1	mA
			34				"	D	4.5 V	5.5 V			GND	"				J2		"	"
			35	GND	GND	5.5 V	"							"			4.5 V	K1		"	"
			36				"	GND	GND	4.5 V			5.5 V	"				K2		"	"
	I_{IH3}		37	2.4 V	GND	GND	"							"			GND	Clock 1	-1	"	"
			38				"	2.4 V	GND	GND			GND	"				Clock 2	-1	"	"
	I_{IH4}		39	5.5 V	GND	GND	"							"			GND	Clock 1		"	"
			40				"	5.5 V	GND	GND			GND	"				Clock 2		"	"
	I_{IH5}		41*	3/	2.4 V	4.5 V	"							"			GND	Clear 1		100	μA
			42*				"	3/	2.4 V	GND			4.5 V	"				Clear 2		100	μA
	I_{IH6}		43*	3/	5.5 V	4.5 V	"							"			GND	Clear 1		1	mA
			44*				"	3/	5.5 V	GND			4.5 V	"				Clear 2		1	mA

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D Case C Test no.	1 Clock 1	2 Clear 1	3 K1	4 V_{CC}	5 Clock 2	6 Clear 2	7 J2	8 $\overline{Q2}$	9 Q2	10 K2	11 GND	12 Q1	13 $\overline{Q1}$	14 J1	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	I_{OS}	3011	45**	2.4 V	2.4 V	2.4 V	5.5 V							GND	GND	GND	2.4 V	$\overline{Q1}$	-40	-100	mA
			46	2.4 V	GND	2.4 V	"							"		GND	2.4 V	Q1	"	"	"
			47**				"	2.4 V	2.4 V	2.4 V	GND	GND	2.4 V	"				Q2	"	"	"
			48				"	2.4 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q2}$	"	"	"
	I_{CC}	3005	49	GND	GND	GND	"	GND	GND	GND			GND	"			GND	V_{CC}		76	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C = +25°C 4/ 5/			50	A	B	B	4.5 V	A	B	B	H	L	B	GND	L	H	B	All outputs	H or L as shown 6/		
			51	A	A	"	"	A	A	"	"	"	"	"	"	"	"	"	"		
			52	B	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"		
			53	A	"	"	"	A	"	A	"	"	"	"	"	"	A	"	"		
			54	B	"	"	"	B	"	"	L	H	"	"	H	L	"	"	"		
			55	A	"	"	"	A	"	"	L	H	"	"	H	L	"	"	"		
			56	A	B	"	"	A	B	"	H	L	"	"	L	H	"	"	"		
			57	B	B	"	"	B	B	"	"	"	"	"	"	"	"	"	"		
			58	A	A	A	"	A	A	"	"	"	A	"	"	"	"	"	"		
			59	B	"	A	"	B	"	"	L	H	A	"	H	L	"	"	"		
			60	A	"	B	"	A	"	B	"	"	B	"	"	"	B	"	"		
			61	B	"	B	"	B	"	B	"	"	B	"	"	"	B	"	"		
			62	A	"	A	"	A	"	A	"	"	A	"	"	"	A	"	"		
			63	B	"	A	"	B	"	A	H	L	A	"	L	H	A	"	"		
8 4/ 5/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C = +25°C	f_{MAX} 6/	(Fig. 16)	64	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Q1	36		MHz
			65	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	$\overline{Q1}$	"		"
			66				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			67				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q2}$	"		"
	t_{PLH1}	3003 (Fig. 15)	68	G	IN	2.4 V	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}$	2	15	ns
			69				"	S	IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}$	"	15	"
	t_{PHL1}		70	F	IN	2.4 V	"							"	OUT		2.4 V	Clear 1 to Q	"	38	"
			71				"	F	IN	2.4 V		OUT	2.4 V	"				Clock 2 to Q	"	38	"
			72	G	IN	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q	"	23	"
			73				"	S	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q	"	23	"
	t_{PLH2}	3003 (Fig. 16)	74	IN		2.4 V	"							"	OUT		N	Clock 1 to Q	"	18	"
			75	IN		P	"					OUT	2.4 V	"				Clock 1 to $\overline{Q}$	"	"	"
			76				"	IN		IN		OUT	2.4 V	"				Clock 2 to Q	"	"	"
			77				"	IN		2.4 V	OUT		P	"				Clock 2 to $\overline{Q}$	"	"	"
	t_{PHL2}		78	IN		R	"							"	OUT		2.4 V	Clock 1 to Q	"	23	"
			79	IN		2.4 V	"					OUT	S	"				Clock 1 to $\overline{Q}$	"	"	"
			80				"	IN		2.4 V		OUT	R	"				Clock 2 to Q	"	"	"
			81				"	IN		S	OUT		2.4 V	"				Clock 2 to $\overline{Q}$	"	"	"

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued. 1/ 2/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits Min	Limits Max	Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	Q1	$\overline{Q}1$	J1				
10 T_C = +125°C	f_{MAX} 6/	(Fig. 16)	82	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Q1	30		MHz
			83	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	$\overline{Q}1$	"		"
			84				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			85				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q}2$	"		"
	t_{PLH1}	3003 (Fig. 15)	86	G	IN	2.4 V	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}$	2	18	ns
			87				"	G	IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}$	"	18	"
	t_{PHL1}		88	F	IN	2.4 V	"							"	OUT		2.4 V	Clear 1 to Q	"	46	"
			89				"	F	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q	"	46	"
			90	G	IN	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q	"	28	"
			91				"	G	IN	2.4 V		OUT	2.4 V	"				Clock 2 to Q	"	28	"
	t_{PLH2}	3003 (Fig. 16)	92	IN		2.4 V	"							"	OUT		N	Clock 1 to Q	"	23	"
			93	IN		P	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}$	"	"	"
			94				"	IN		N		OUT	2.4 V	"				Clock 2 to Q	"	"	"
			95				"	IN		2.4 V	OUT		P	"				Clock 2 to $\overline{Q}$	"	"	"
	t_{PHL2}		96	IN		R	"							"	OUT		2.4 V	Clock 1 to Q	"	28	"
			97	IN		2.4 V	"							"		OUT	S	Clock 1 to $\overline{Q}$	"	"	"
			98				"	IN		2.4 V		OUT	R	"				Clock 2 to Q	"	"	"
			99				"	IN		S	OUT		2.4 V	"				Clock 2 to $\overline{Q}$	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.

D = Momentary 4.5 V, then GND.

F = Momentary 0 V, then Vgen, see figure 15.

G = Momentary Vgen, then 0 V, see figure 15.

N = t_{setup} waveform, see figure 16.

P = t_{setup} waveform, see figure 16.

R = t_{setup} waveform, see figure 16.

S = t_{setup} waveform, see figure 16.

* = Duration of test should not exceed 1 second.

** = Limit duration of this test to 100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Qualification requirements are removed for this device type.

3/ Input shall be 4.5 V with a momentary ground, then 4.5 V (⊓ 4.5 V / 0 V).

4/ Tests shall be performed in sequence.

5/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.

6/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator: or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

7/ f_{MAX}, minimum limit specified is the frequency of the input pulse [illegible] put frequency shall be one-half of the input frequency.

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification for device types 01, 02, 03, 05, and 06, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
NASA - NA
DLA - ES

User activities:
Army - SM
Navy - AC, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1072-3)