MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS, 4096 BIT, STATIC RANDOM ACCESS MEMORY (SRAM), BULK SILICON AND SILICON ON SAPPHIRE

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for bulk silicon and silicon on sapphire (SOS), static, 4096 bit, random access memory microcircuits. Two product assurance classes, four radiation hardness assurance levels, and a choice of case outlines and lead finishes are provided and are reflected in the part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit	Access time
01 (bulk silicon)	4096x1 bit RAM	120 ns
02 (bulk silicon)	1024x4 bit RAM	120 ns
03 (synchronous; bulk silicon)	4096x1 bit RAM	320 ns
04 (synchronous; bulk silicon)	1024x4 bit RAM	320 ns
05 (asynchronous; SOS)	4096x1 bit RAM	250 ns
06 (asynchronous; SOS)	1024x4 bit RAM	250 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
V	D-6 (18-lead, 1/4" x 15/16"), dual-in-line package
K	F-6A (24-lead, 3/8" x 5/8"), flat package

1.2.4 Radiation hardness level. Radiation hardness levels shall be as defined in MIL-M-38510.

1.3 Absolute maximum ratings.	Device types 01, 02, 03, 04	Device types 05, 06
Supply voltage range (V_{DD} - V_{SS})	-0.3 V to +7.0 V	-0.5 V to +7.0 V
Input voltage range	V_{SS} -0.3 V to V_{DD} +0.3 V	V_{SS} -0.5 V to V_{DD} +0.5 V
Input current, any one input		10 mA
Storage temperature range	-65°C to +150°C	-65°C to +150°C
Maximum power dissipation	200 mW	500 mW
MPD per output transistor		100 mW
Lead temperature (soldering) 10 seconds maximum	300°C	300°C
Thermal resistance junction to case	0.04°C/mW	
Junction temperature	175°C	175°C
Radiation level	As indicated by RHA level designator	

1.4 Recommended operating conditions.	Device types 01, 02, 03, 04	Device types 05, 06
Supply voltage (V_{DD} - V_{SS})	4.5 V to 5.5 V	4.75 V to 5.25 V
Input low (V_{IL}) voltage range	V_{SS} -0.3 V to V_{SS} +0.8 V	V_{SS} +0.8 V maximum
Input high (V_{IH}) voltage range	V_{DD} -2.0 V to V_{DD} +0.3 V	V_{DD}/2 minimum
Case operating temperature range	-55°C to +125°C	-55°C to +125°C
Timing parameters	(See figure 7)	(See figure 7)

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein. At present epoxy die bonding may be performed using conductive silver paste or other qualified epoxy. However, upon release of test method 5011 of MIL-STD-883, all expoxies must be qualified to test method 5011. Laser scribing shall be allowed only for SOS technology product and only to the back side of the wafer.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Truth tables and timing waveforms. The truth tables and timing waveforms shall be as specified on figure 6.

3.2.4 Case outline. The case outline shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.4.1 Post-irradiation performance characteristics. The electrical performance characteristics of radiation hardness assured devices following exposure to the designated radiation levels are as specified in table VI and apply at an ambient temperature of +25°C.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.5.1 Functional tests. The functional tests used to test these devices are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, then alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.6.1 Serialization. All class S devices shall be serialized in accordance with MIL-M-38510.

3.6.2 Correctness of indexing and marking. All devices shall be subjected to the final electrical test specified in table II after marking to verify that they are correctly indexed and identified by part number. Optionally, an approved electrical test may be devised especially for this requirement.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Step coverage. The step coverage acceptance criteria of paragraph 3.7.1 of method 2018 should read "Oxide steps. All four directional edges of every type of oxide step (contact window or other type of oxide step) shall be examined (refer to 3.4.2). A directional edge shall be unacceptable if any defect or combination of defects, excluding thinning, reduces the cross-sectional area of the metal at the directional edge to less than 75 percent of the metal cross-sectional area on either side of the directional edge. The metal shall not be thinned to less than 4,000 Å. For an oxide step (contact window or other type of oxide step) to be acceptable, all four directional edges must be covered with metallization (per 3.4.2) and be acceptable (per the preceding sentence), except in the cases described in 3.7.1a and 3.7.1b. Where all contact cuts are completely covered by metal, the metallization viewed from the normal viewing angle (refer to 3.4.1) will show evidence of contoured metal flow into the contact area. Verification of the actual step coverage shall be determined by cross sectioning an additional die from the same wafer or using a test die to show contact step coverage of 4,000 Å or more."

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspections. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.

b. Burn-in test (method 1015 of MIL-STD-883).

(1) Static test (test condition A) using the circuit shown on figure 3, or equivalent. Ambient temperature (T_A) shall be +125°C minimum. Test duration for the static test shall be 48 hours minimum for class S. The 48 hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements. Static II for class B is a minimum of 168 hours.

(2) Dynamic test (test condition D or E) using the circuit shown on figure 4 or equivalent. Test duration and temperature shall be in accordance with method 5004 of MIL-STD-883.

c. Interim and final electrical test parameters shall be as specified in table II (see 3.5).

d. For class S devices, post dynamic burn-in, or class B devices, post dynamic burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.

e. The manufacturers of SOS devices shall use a high temperature stress test prior to the static burn-in. Conditions shall be dynamic, +125°C, supply voltage at 7 ±.5 volts, and a duration of 160 hours minimum. A PDA of 5 percent shall be imposed. Devices need not be serialized prior to stress testing.

f. At the manufacturer's option, the following visual inspection method shall be used. For class S, visual inspection is to be performed to MIL-STD-883, method 2010, condition A except as follows:

(1) High magnification inspection is performed at 100X to 300X.

(2) Criteria 3.1.1.1 and 3.1.1.2 shall be replaced by criteria 3.2.1.1 and 3.2.1.2 respectively, however the 75 percent of the original metal width over a passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.

(3) Criteria 3.1.1.7 shall apply to 3 areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and consist only of the area in the immediate field of view.

(4) Criteria 3.1.3c shall be replaced by 3.2.3c. Cracks greater than 5 mils are rejected only if they point to or cross the scribe grid line.

(5) Burn in testing shall be performed at an operating voltage of 7 ±.5 volts, if this option is chosen.

g. At the manufacturer's option, the class B visual inspection is to be performed to MIL-STD-883, method 2010, condition B except as follows:

(1) Criteria 3.2.1.1 and 3.2.1.2 metallization scratches and voids, the 75 percent of the original metal width over a passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.

(2) Criteria 3.2.1.7 shall apply to 3 areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and consist only of the area in the immediate field of view.

(3) Criteria 3.2.3c. Cracks greater than 5 mils are rejected only if they point or cross the scribe grid line.

(4) Burn in testing shall be performed at an operating voltage of 7 ±.5 volts, if this option is chosen.

h. For SOS product, diffusion fault criteria, passivation fault criteria, and oxide gate bridge inspection criteria are difficult to apply. Therefore inspect these devices for complete islands, bridging between islands, and missing adjacent contacts from a row in a contact chain.

4.2.1 Percent defective allowable (PDA).

a. The class S device PDA shall be 5 percent for static burn-in and 5 percent for dynamic burn-in for all failures, with a 3 percent maximum on functional failures for either burn-in. Static burn-in failures for the split sequence shall be cumulative for determining PDA.

b. If interim electrical parameter measurements are made to remove defective devices from the lot prior to the burn-in sequence, the number of devices that fail these measurements may be excluded from the PDA calculations for class S and B devices. Following this, pre and post burn-in electrical parameter measurements results shall be used as specified to compute PDA's.

c. Those devices whose measured characteristics after burn-in exceed the specified delta (Δ) limits or specified electrical parameter limits are failures and shall be removed from the lot (see 3.5 and 4.5.3). The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA or one device whichever is greater.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 7 shall be omitted.

c. Subgroup 4 (C_I measurement) shall be measured only for initial qualification and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. This test shall be performed using a fixed sample size of 25 devices and an acceptance number of zero.

d. Subgroup 12 shall be added to the group A inspection requirements using an LTPD = 15 and consist of the procedures, test conditions, and limits specified in table III.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Class S steady state life test circuit of figure 4 or equivalent shall be used.

b. A special subgroup shall be added using an LTPD of 15 for classes S and B. This subgroup shall consist of a high voltage test of the input protection circuits, V_{ZAP} (see 4.5.4). With the release of Notice 5 of MIL-STD-883, the procedure and requirements of test method 3015 of Notice 5 will replace the V_{ZAP} test of this paragraph.

c. Class S electrical test requirements shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady state life test (method 1015 of MIL-STD-883) conditions, or equivalent:

(1) Test condition D or E, and as specified in 4.5.2 and figure 4, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions V_{SS} = 0 V, V_{DD} = 5.5 V -55°C < T_C < +125°C		Device type	Limits Min	Limits Max	Unit
Low level output voltage	V_{OL}	V_{DD} = 4.5 V I_{OL} = 2 mA		01, 02, 03, 04		0.4	V
Output low drive current	I_{OL}	V_{DD} = 4.75 V V_{OUT} = 0.4 V		05	2.5		mA
				06	1.7		
High level output voltage	V_{OH}	V_{DD} = 4.5 V I_{OH} = -1 mA		01, 02, 03, 04	2.4		V
Output high drive current	I_{OH}	V_{DD} = 4.75 V V_{OUT} = 4.35 V		05	2.0		mA
				06	1.1		
Positive clamping voltage	V_{IC} (POS)	I_{IN} = 100 µA	T_C = +25°C	01, 02	0.1	2.0	V
		I_{IN} = 50 µA	T_C = +25°C	03, 04	0.1	2.0	
		I_{IN} = 100 µA	T_C = +25°C	05	0.1	3.0	
				06	0.2	3.0	
Negative clamping voltage	V_{IC} (NEG)	I_{IN} = -100 µA	T_C = +25°C	01, 02	-0.1	-2.0	V
		I_{IN} = -50 µA	T_C = +25°C	03, 04	-0.1	-2.0	
		I_{IN} = -100 µA	T_C = +25°C	05	-0.1	-3.0	
				06	-0.2	-3.0	
Input leakage current	I_{IH}	V_{DD} = 5.5 V	V_{IN} = 5.5 V	01, 02, 03, 04		1	µA
		V_{DD} = 5.25 V	V_{IN} = 5.25 V	05, 06		10	
Input leakage current	I_{IL}	V_{DD} = 5.5 V	V_{IN} = 0 V	01, 02, 03, 04		-1	µA
		V_{DD} = 5.25 V	V_{IN} = 0 V	05, 06		-10	
High impedance output leakage	I_{OHZ}	V_{DD} = 5.5 V	V_{OUT} = 5.5 V	01, 02		1.0	µA
				03, 04		10	
		V_{DD} = 5.25 V	V_{OUT} = 5.25 V	05		30	
				06		50	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{DD} = 5.5 V -55°C < T_C < +125°C	Device type	Limits Min	Limits Max	Unit
High impedance output leakage	I_{OLZ}	V_{DD} = 5.5 V V_{OUT} = GND	01, 02		-1.0	µA
			03, 04		-10	
		V_{DD} = 5.25 V V_{OUT} = GND	05		-30	
			06		-50	
Quiescent supply current	I_{DD} or I_{SS}	V_{DD} = 5.5 V	01, 02		50	µA
			03		200	
			04		250	
		V_{DD} = 5.25 V	05, 06		-1,000	
Data retention supply voltage	PWR DWN	Functional test	01, 02	2.0		V
			03, 04	3.0		
			05, 06	2.5		
Operating current	I_{DDOP}	V_{DD} = 5.5 V T_C = +25°C f = 1 MHz	01, 02, 03, 04		7	mA
		V_{DD} = 5.25 V T_C = +25°C f = 1 MHz	05		4	
			06		6	
Data retention quiescent supply current	I_{CCDR}	V_{DD} = 2 V I_{OUT} = 0 V_{IN} = rail voltages	01, 02		25	µA
		V_{DD} = 3 V I_{OUT} = 0 V_{IN} = rail voltages	03		100	
			04		100	
		V_{DD} = 2.5 V I_{OUT} = 0 V_{IN} = rail voltages	05		400	
			06		500	
Input capacitance	C_I	V_{DD} = 5.5 V V_{IN} = rail voltage f = 1 MHz	01, 02		8	pF
			03, 04 1/		8	
			05, 06 1/		5	
Address access time	t_{AVQV}	See table III	01, 02		120	ns
			03, 04		320	
			05, 06		250	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{DD} = 5.5 V -55°C < T_C < +125°C	Device type	Limits Min	Limits Max	Unit
Chip enable access time	t_{ELQV}	See table III	01, 02		120	ns
			03, 04		300	
			05		280	
			06		200	
Chip enable output time 1/	t_{ELQX}		01, 02	10		ns
			03, 04		100	
			06	20		
Chip enable output disable time 1/	t_{EHQZ}		01, 02		50	ns
			03, 04		100	
			05		100	
			06		140	
Chip enable pulse negative width	t_{ELEH}		01, 02	120		ns
			03, 04	300		
			05	220		
			06	200		
Chip enable pulse positive width	t_{EHEL}		01, 02	50		ns
			03, 04	120		
Address setup time	t_{AVEL}		01, 02	0		ns
			03, 04	20		
Address hold time	t_{ELAX}		01, 02	40		ns
			03	50		
			04	100		
Address hold time from write	t_{WHAX}		05	45		ns
			06	40		
Write enable pulse width	t_{WLWH}		01	20		ns
			02	120		
			03	80		
			04	300		
			05	145		
			06	150		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{DD} = 5.5 V -55°C < T_C < +125°C	Device type	Limits Min	Limits Max	Unit
Write enable pulse setup time	t_{WLEH}	See table III	01	70		ns
			02	120		
			03	200		
			04	300		
Early write pulse setup time	t_{WLEL}		01, 02, 03, 04	0		ns
Write enable read mode setup time	t_{WHEL}		01, 03	0		ns
Early write pulse hold time	t_{ELWH}		01	40		ns
			02	120		
			03	80		
			04	300		
			05	205		
			06	200		
Data setup time	t_{DVWL}		01, 03	0		ns
Early write data setup time	t_{DVEL}		01, 03	0		ns
Data hold time	t_{WLDX}		01	25		ns
			03	80		
Early write data hold time	t_{ELDX}		01	25		ns
			03	80		
Data valid to write time	t_{QVWL}		01, 03	0		ns
Read or write cycle time	t_{ELEL}		01, 02	170		ns
			03, 04	420		
	t_{AVAV}		05, 06	250		
Write enable output disable time	t_{WLQZ}		02		50	ns
			04 1/		100	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{DD} = 5.5 V -55°C < T_C < +125°C	Device type	Limits Min	Limits Max	Unit
Data hold time	t_{WHDX}	See table III	02	0		ns
			04	30		
			05	10		
			06	5		
Write data delay time	t_{WLDV}		02	70		ns
			04	100		
Late output high-Z time	t_{EHWH}		02, 04	0		ns
Address setup to end of write time	t_{AVWH}		05	205		ns
			06	200		
Address to write setup time	t_{AVWL}		05	0		ns
			06	0		
Output hold from address change time	t_{AVQZ} 1/		05		100	ns
			06		150	
Data setup time	t_{DVWH}		02	50		ns
			04	200		
			05	120		
			06	75		

1/ This parameter is guaranteed but not tested.

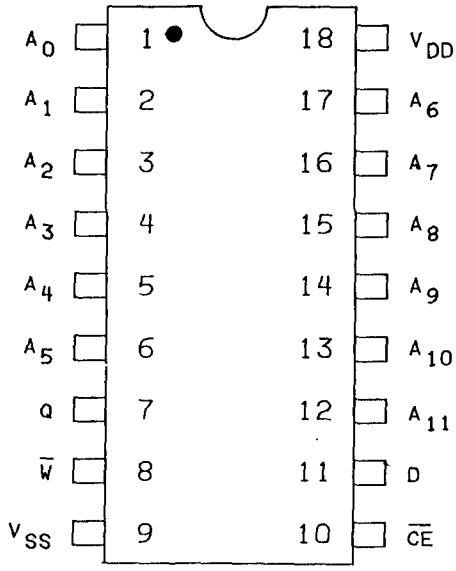
TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Class S device 1/ 2/				Class B device 1/ 2/			
		Ref par.	Table III 3/ subgroups	Table IV 4/ delta limits	Test circuit figure	Ref par.	Table III 3/ subgroups	Table IV 4/ delta limits	Test circuit figure
1	Interim electrical parameters method 5004	4.2e	1				1		
2	Static burn-in I method 1015	4.2b,e 4.2f(5) 4.5.2			3		Not required		
3	Same as line 1		1*	Δ					
4	Static burn-in II method 1015	4.2f(5) 4.5.2			3	4.2b,g(4) 4.5.2	5/ Required		3
5	Same as line 1	4.2d	1*	Δ		4.2d	1*	Δ	
6	Dynamic burn-in method 1015	4.2b,f(6) 4.5.2	5/		4		Not required		
7	Same as line 1	4.2d	1*	Δ					
8	Final electrical parameters method 5004		1*,2,3, 8,9,10,11				1*,2,3, 8, 9		
9	Group A test requirements method 5005	4.4.1	1,2,3,4, 8,9,10, 11,12			4.4.1	1,2,3,4, 9,10,11		
10	Group B test requirements method 5005	4.4.2	1,2,3,8, 9,10,11	Δ		4.4.2 4.5.3	1		
11	Group C end-point electrical parameters method 5005					4.4.3	1,2	Δ	
12	Group D end-point electrical parameters method 5005	4.4.4	1,2,3			4.4.4	1,2		
13	Group E test requirements method 1019	4.5.6	Table VI		Table VII	4.5.6	Table VI		Table VII

1/ Blank spaces indicate tests are not applicable.
2/ For subgroups 9, 10, and 11, only the worst value measured per device need be recorded when variables data is required (e.g. during qualification).
3/ (*) indicates PDA applies to subgroup 1 (see 4.2.1).
4/ (Δ) indicates delta limits shall be required, and delta values shall be computed with reference to either the initial recorded electrical parameters (see 4.5.3), or to the previous interim electrical parameters, as indicated to the qualifying activity.
5/ The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in (removal of temperature or bias) perform the final electrical parameter measurements, subgroup A1.

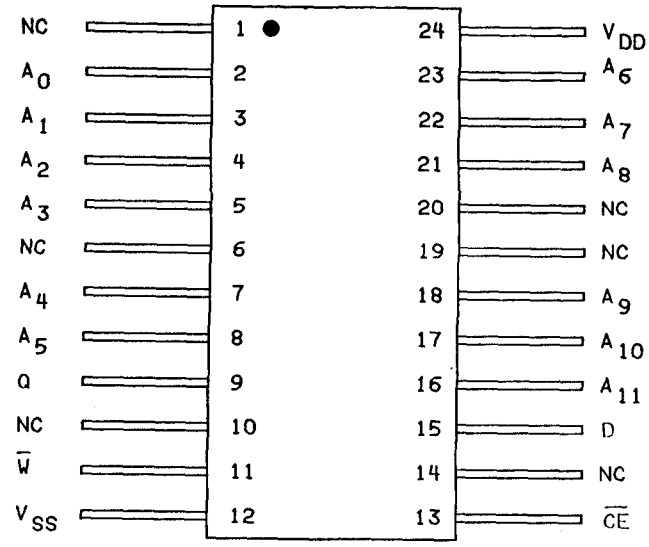
Device types 01, 03, and 05

Case V



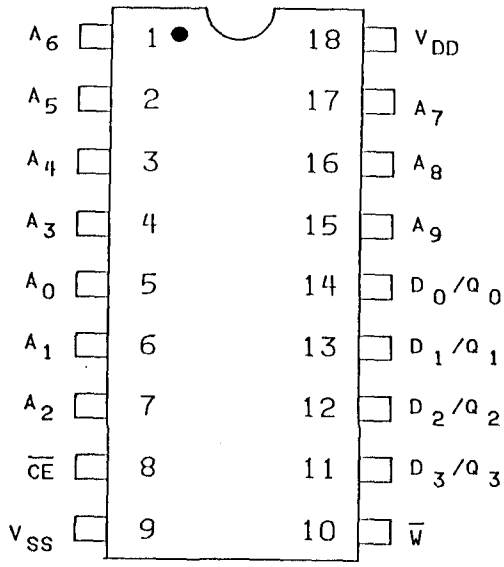
Device types 03 and 05

Case K



Device types 02, 04, and 06

Case V



Device types 04 and 06

Case K

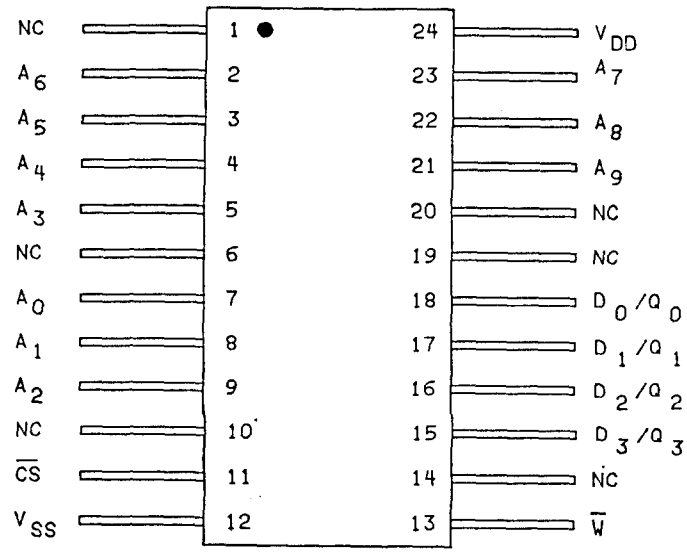
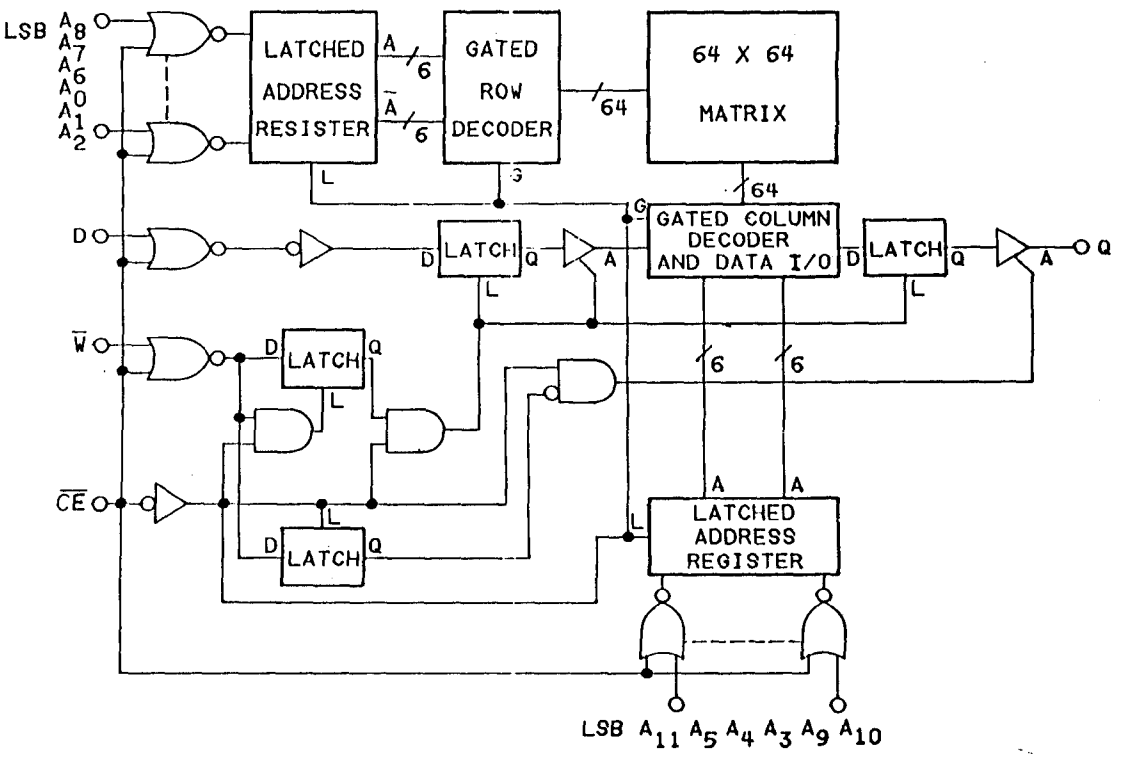


FIGURE 1. Terminal connections.

Device types 01 and 03



Device types 02 and 04

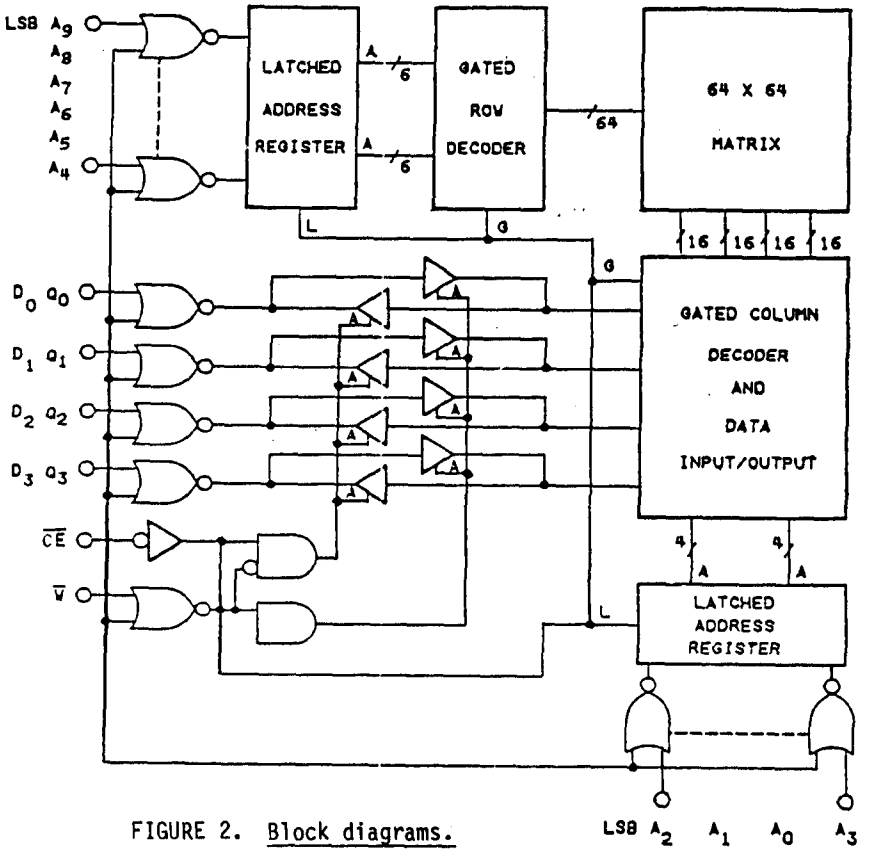
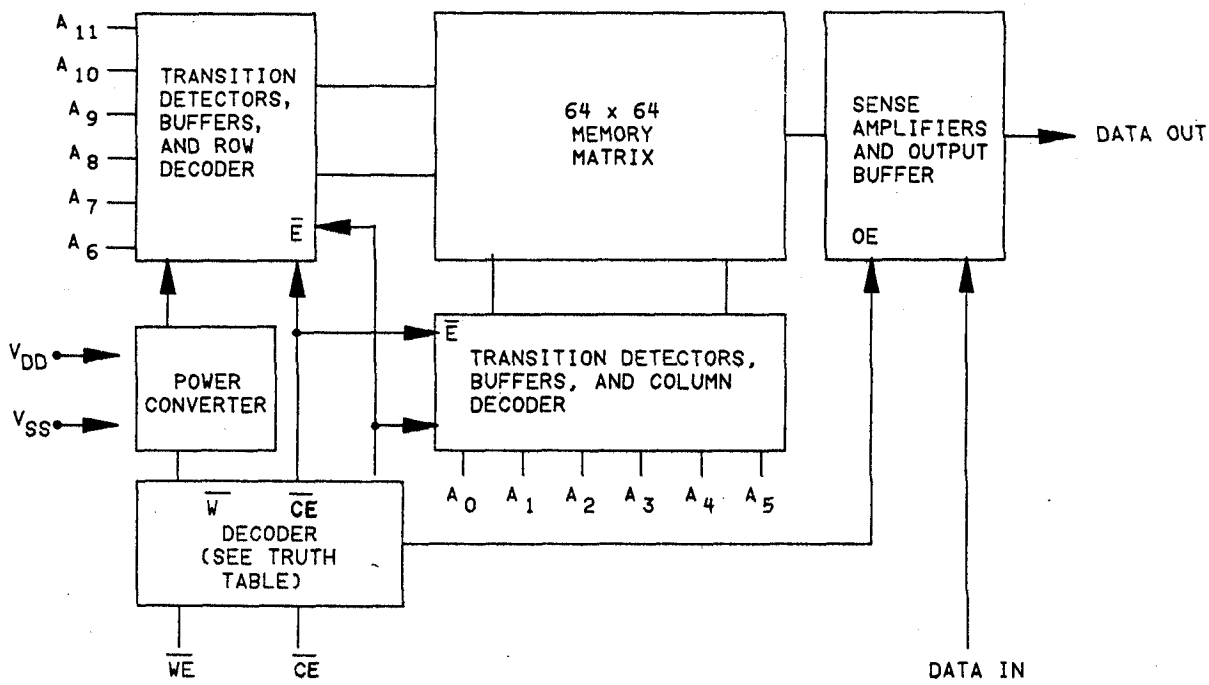


FIGURE 2. Block diagrams.

Device type 05



Device type 06

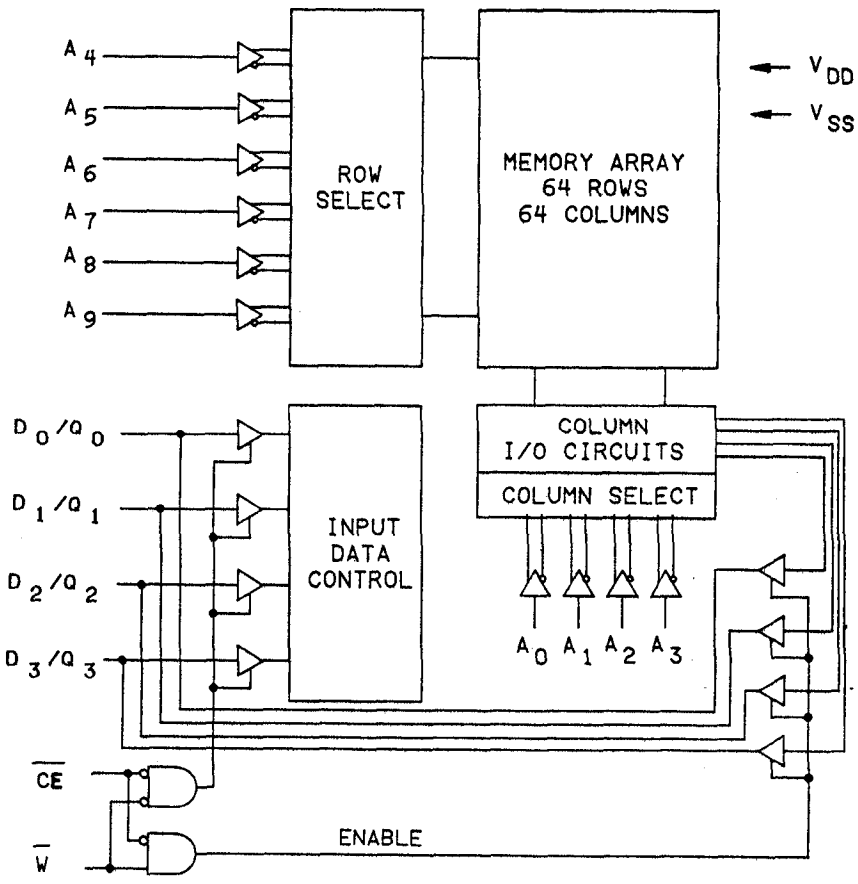
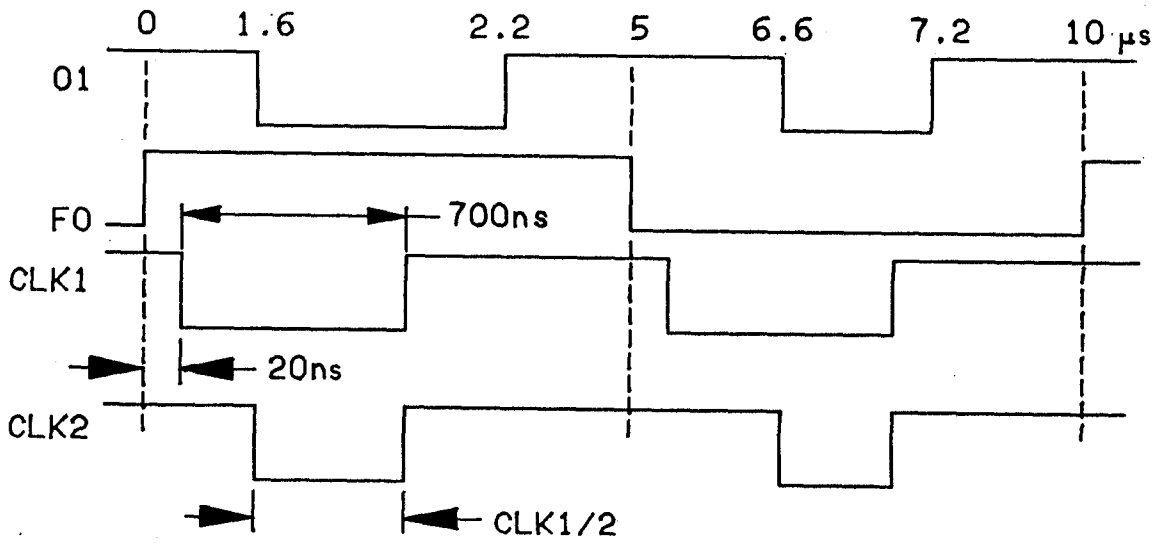


FIGURE 2. Block diagrams - Continued.

Device type	V_{DD} min	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	$\overline{CE}$	$\overline{W}$	$D0/Q_0$	$D1/Q_1$	$D2/Q_2$	$D3/Q_3$	Q
01	5.0 V	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F0	F1	F2				F2
02	5.0 V	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12			F0	F1	F2	F2	F2	F2	
03	6.0 V	F0	F1	F2	F3	F4	F5	F6	F7	F8	F10	F11	F12	CLK1	CLK2	F2				F9
04	6.0 V	F4	F5	F9	F3	F2	F1	F0	F6	F7	F8			CLK2	CLK1	F10	F11	F12	F13	
05	7.0 V	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F13	01	F12				$\frac{Vdd}{2}$
06	7.0 V	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9			F14	01	F10	F11	F12	F13	

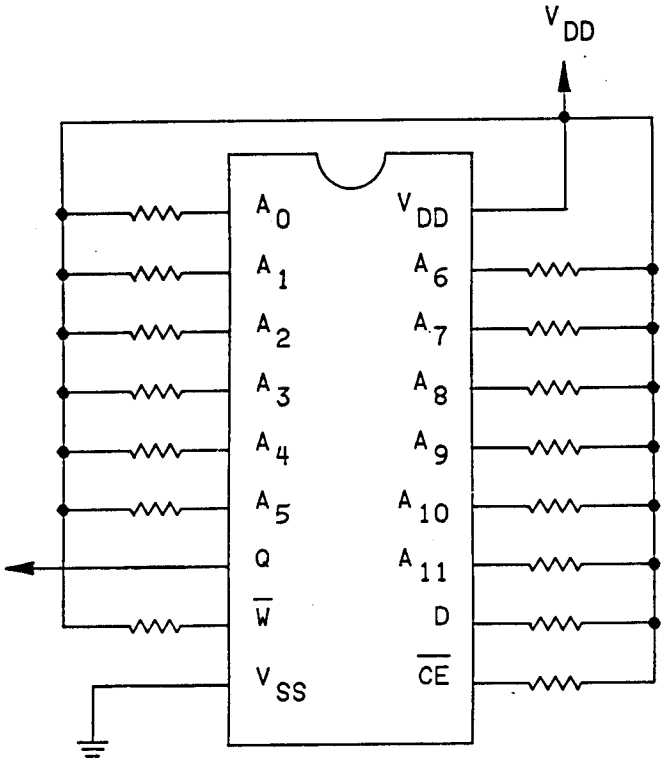
NOTES:
1. F0 = 100 kHz minimum, F1 = 1/2 F0, F2 = 1/4 F0 ect.



2. Resistors: (all values ±5%)
   Type 01, 02; all input and output pins 47 kΩ.
   Type 03, 04; same burn-in board both types, with pins 7, 11, 12, 13, and 14 connected through 27 kΩ resistors to frequencies shown in table. 300Ω resistors on other pins.
   Type 05, 06; pins connected through 2 kΩ to 15 kΩ, depending on pin function, as indicated in table.

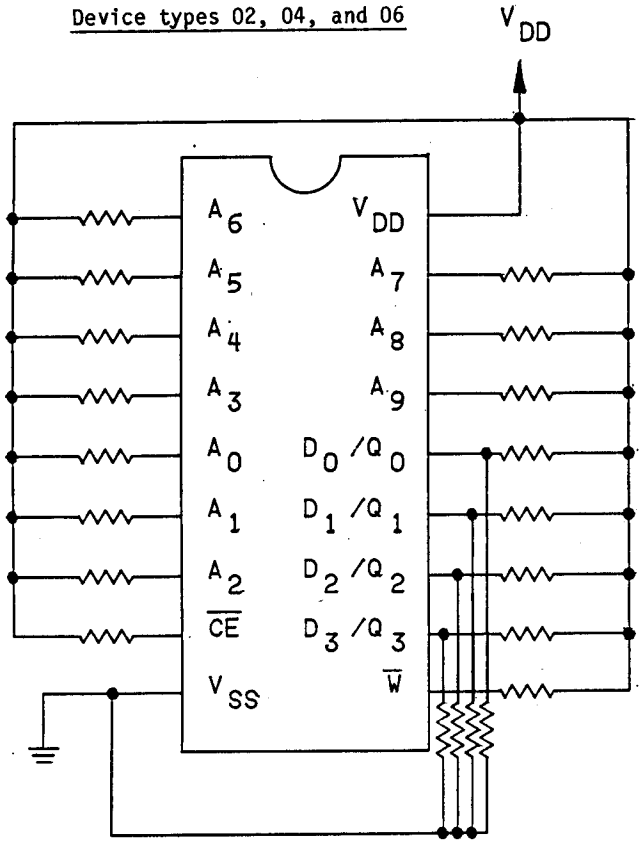
FIGURE 4. Dynamic burn-in and steady state life test circuit.

Device types 01, 03, and 05



Device type	Q min
01	$\frac{V_{DD}}{2}$
03	$\frac{V_{DD}}{2.5}$
05	$\frac{V_{DD}}{2}$

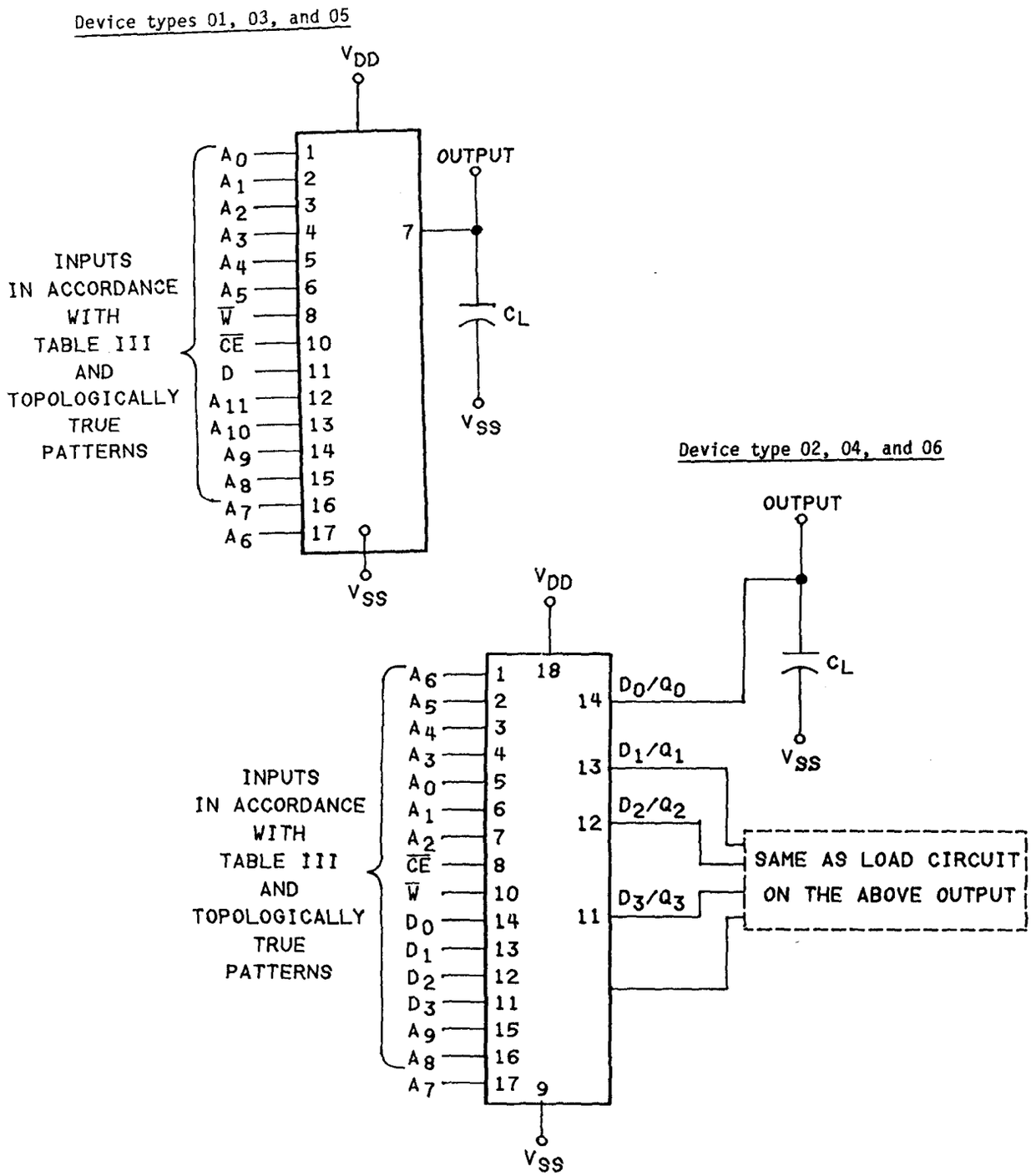
Device types 02, 04, and 06



Device type	V_{DD} min
01	5.0 V
02	5.0 V
03	6.0 V
04	6.0 V
05	7.0 V
06	7.0 V

NOTES:
1. All inputs are connected through a 1 kΩ to 15 kΩ resistor.
2. 05, 06; For static II burn-in change input connections to V_{SS}.
3. 05, 06; Checkerboard pattern filling array for Static I.
4. 05, 06; Inverse checkerboard pattern filling array for Static II.
5. For device type 06 the pull down resistors on the outputs are not required.
6. Output pin device types 01, 03, 05; connected either through a resistor to a power supply or directly to a voltage divider across the supply rationed as shown.

FIGURE 3. Static burn-in circuit.

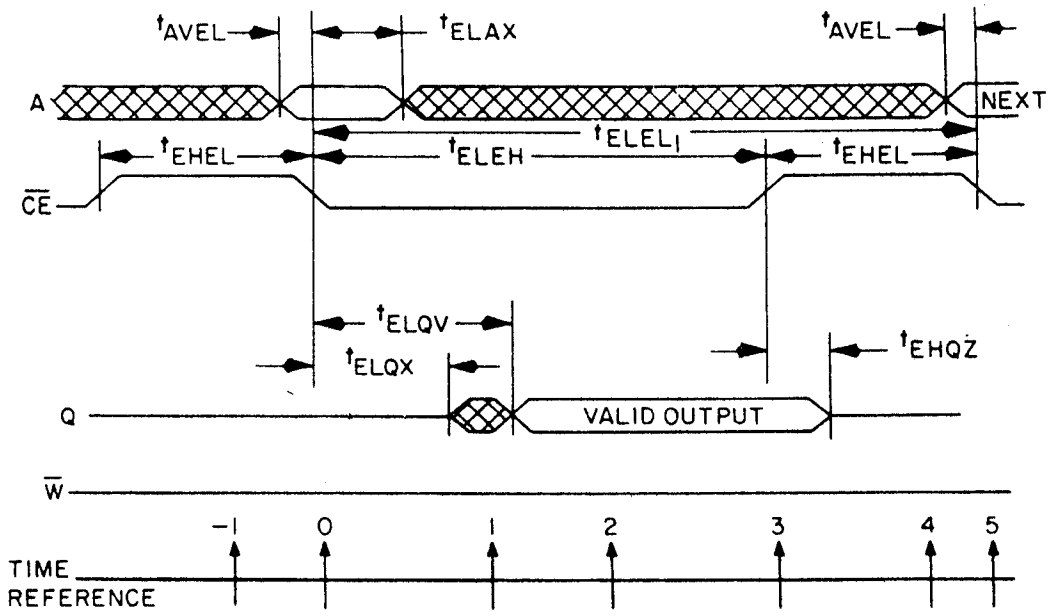


NOTES:
1. C_L = 50 pF ±10%.
2. Dynamic current load forces if used by tester. I_{OL} = 2.0 mA and I_{OH} = -1.0 mA.
3. All t_{TLH} and $t_{THL} \leq 10$ ns.
4. All generator output impedance = 50Ω.
5. All voltages measured with respect to GND terminal.
6. Load should be modified for high Z measurements.
7. See figure 6 for waveforms and figure 7 for timing conditions.

FIGURE 5. Switching time test circuit.

Device types 01 and 03

READ CYCLE WAVEFORM



TRUTH TABLE

Time reference	Inputs			Output	Function
	$\overline{CE}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory disable
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Output enabled
2	L	H	X	V	Output valid
3	↑	H	X	V	Read accomplished
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

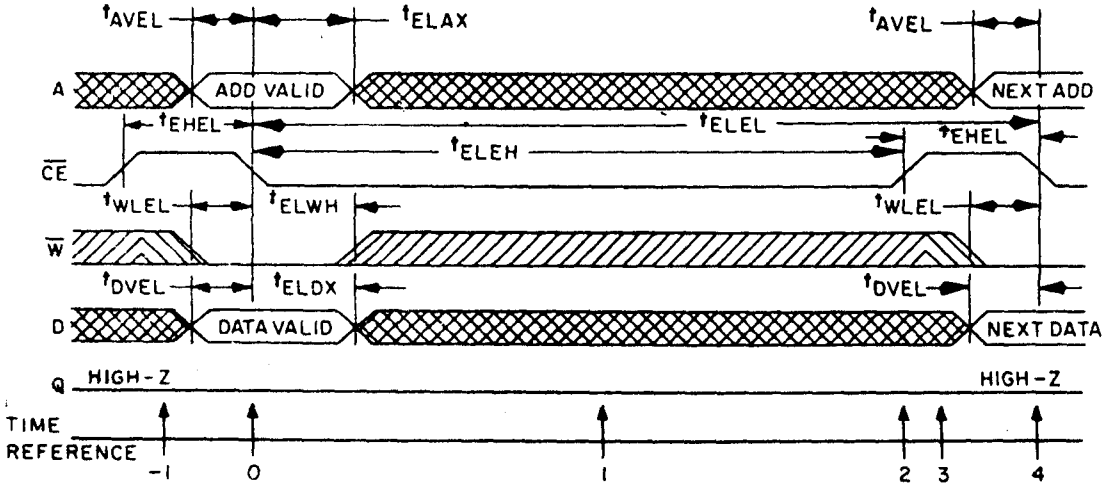
The address information is latched in on the chip registers on the falling edge of $\overline{CE}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{CE}$ may return high (T = 3). This will disable the output buffer and ready the SRAM for the next memory cycle (T = 4).

NOTE: See figure 7 for test conditions.

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables.

Device types 01 and 03

WRITE CYCLE



TRUTH TABLE

Time reference	Inputs $\overline{CE}$	$\overline{W}$	A	D	Output Q	Function
-1	H	X	X	X	Z	Memory disabled
0	↓	L	V	V	Z	Cycle begins, addresses are latched
1	L	X	X	X	Z	Write in progress internally
2	↑	X	X	X	Z	Write completed
3	H	X	X	X	Z	Prepare for next cycle (same as -1)
4	↓	L	V	V	Z	Cycle ends, next cycle begins (same as 0)

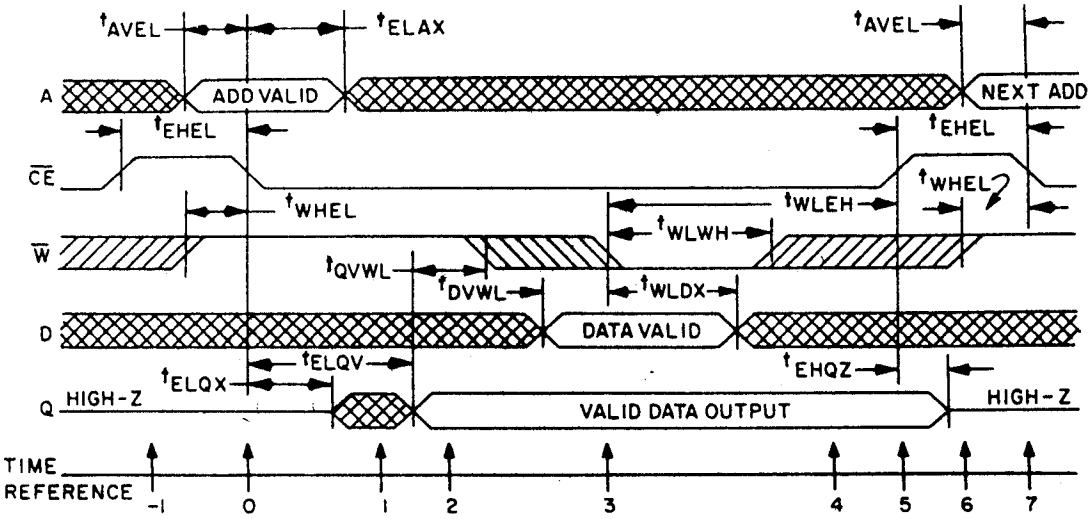
The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{CE}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{CE}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low in the early write cycle, the output buffer is latched into the high impedance state and will remain in the state until $\overline{CE}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{CE}$ going low; therefore data set up and hold times should be referenced to $\overline{CE}$. When $\overline{CE}$ (T = 2) returns to the high state, the output buffer disables and signals are unlatched. The device is now ready for the next cycle.

NOTE: See figure 7 for test conditions.

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 01 and 03

READ/MODIFY/WRITE CYCLE



TRUTH TABLE

Time reference	Inputs $\overline{CE}$	$\overline{W}$	A	D	Output Q	Function
-1	H	X	X	X	Z	Memory disabled
0	↓	H	V	X	Z	Cycle begins, addresses are latched
1	L	H	X	X	X	Output enabled
2	L	H	X	X	V	Output valid, read and modify time
3	L	↓	X	V	V	Write begins, data is latched
4	L	X	X	X	V	Write in progress internally
5	↑	X	X	X	V	Write completed
6	H	X	X	X	Z	Prepare for next cycle (same as -1)
7	↓	H	V	X	Z	Cycle ends, next cycle begins (same as 0)

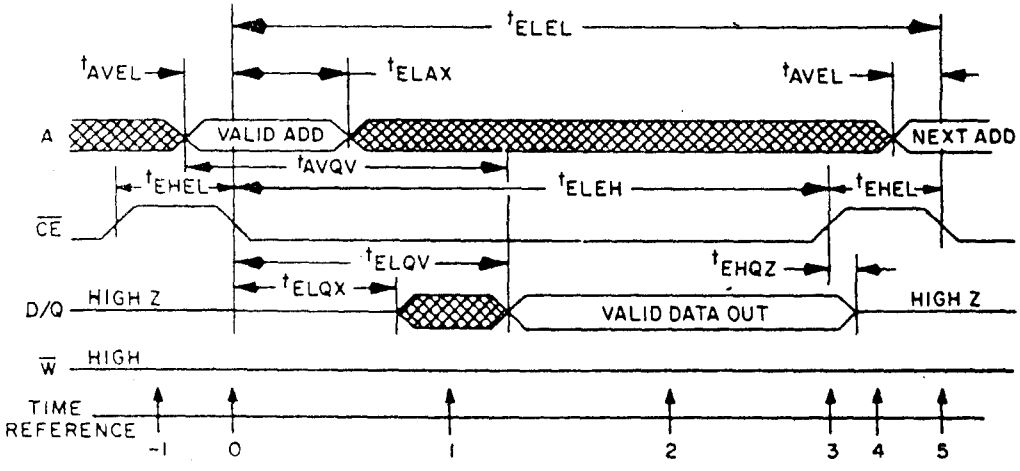
The read/modify/write cycle begins as all other cycles on the falling edge of $\overline{CE}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3), the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{CE}$ have been latched and have no further effect on the SRAM. The rising edge of $\overline{CE}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the SRAM is ready for the next cycle.

NOTE: See figure 7 for test conditions.

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 02 and 04

READ CYCLE



TRUTH TABLE

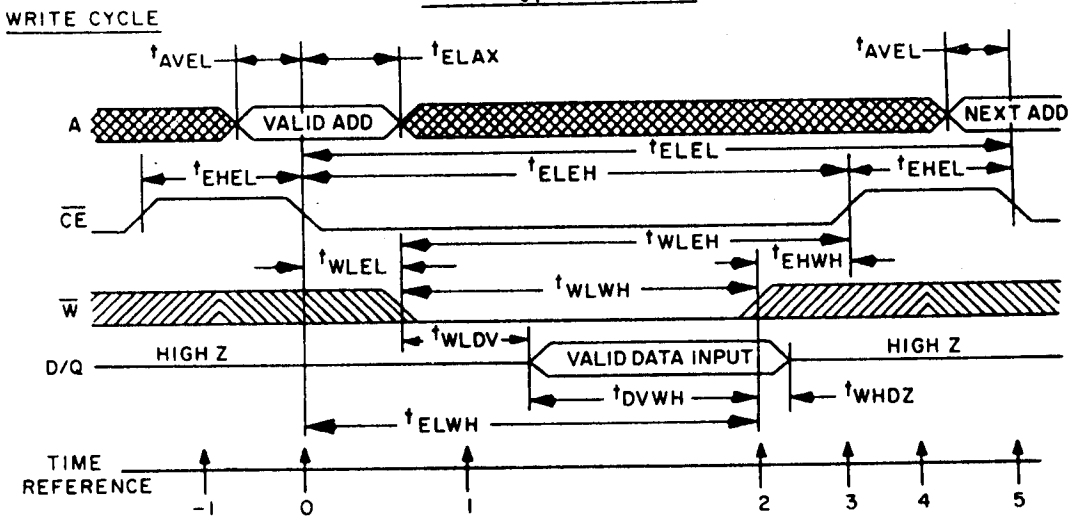
Time reference	Inputs CE	W	A	Data I/O DQ	Function
-1	H	X	X	Z	Memory disabled
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Output enabled
2	L	H	X	V	Output valid
3	↑	H	X	V	Read accomplished
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

The address information is latched in on the chip registers on the falling edge of CE (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2). W must remain high throughout the read cycle. After the data has been read, CE may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

NOTE: See figure 7 for test conditions

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 02 and 04



Time reference	Inputs $\overline{CE}$	$\overline{W}$	A	DQ	Function
-1	H	X	X	Z	Memory disabled
0	↓	X	V	Z	Cycle begins, addresses are latched
1	L	L	X	Z	Write period begins
2	L	↑	X	V	Data in is written
3	↑	H	X	Z	Write completed
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	X	V	Z	Cycle ends, next cycle begins (same as 0)

The write cycle is initiated on the falling edge of $\overline{CE}$ (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active, t_{WLEL} and t_{EHWH} must be met. Under these conditions, t_{WLDV} is unnecessary and input data may be applied at any convenient time as long as t_{DVWH} is still met. If t_{WLEL} is not met, then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (t_{ELQZ}) must be met before the input data is applied (t_{WLQZ} = t_{WLDV}). Similiarly, if t_{EHWH} is not met the outputs may enable briefly near the end of the cycle.

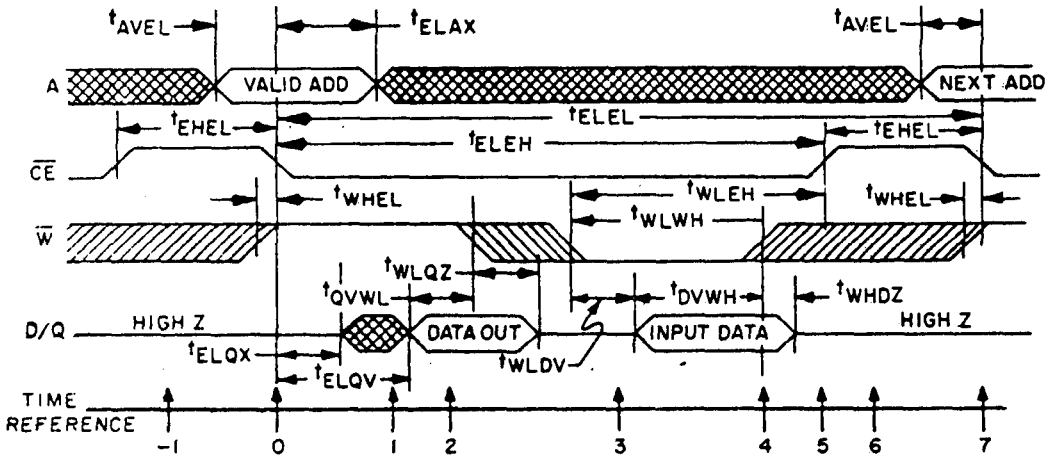
The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{CE}$ (T = 3). After the minimum required $\overline{CE}$ high time (t_{EHEL}), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{CE}$.

NOTE: See figure 7 for test conditions.

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 02 and 04

READ MODIFY WRITE CYCLE



TRUTH TABLE

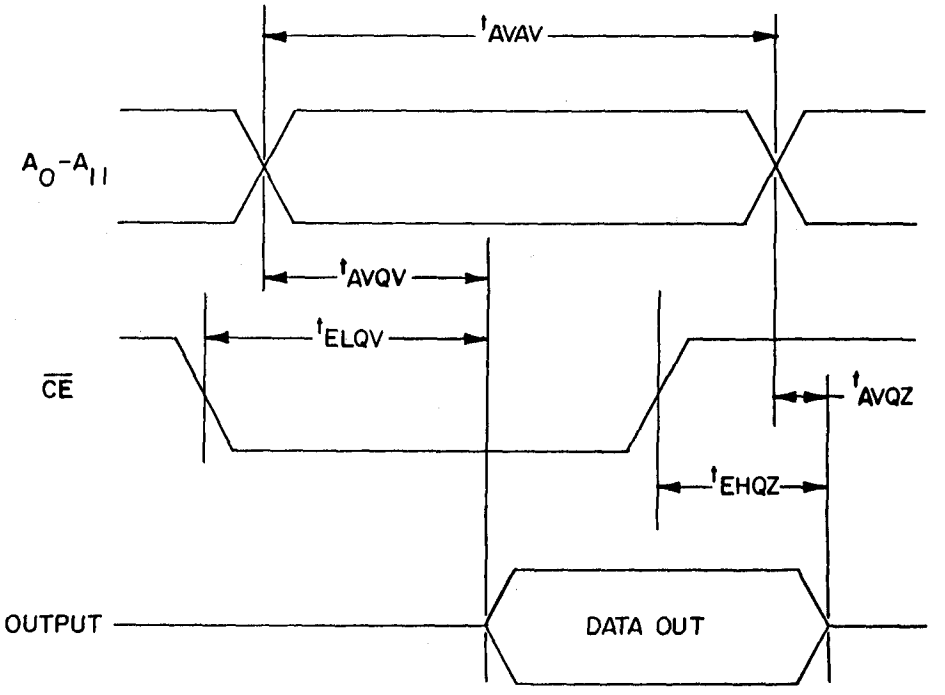
Time reference	Inputs CE	Inputs W	Inputs A	Data I/O DQ	Function
-1	H	X	X	Z	Memory disabled
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Read mode, output enabled
2	L	H	X	V	Read mode, output valid
3	L	L	X	Z	Write mode, output high Z
4	L	∫	X	V	Write mode, data is written
5	∫	H	X	Z	Write completed
6	H	X	X	Z	Prepare for next cycle (same as -1)
7	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{CE}$, a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum t_{WLWH}, $\overline{W}$ may return high. The information just written may now be read or $\overline{CE}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{CE}$ is low providing all timing requirements are met.

NOTE: See figure 7 for test conditions.

FIGURE 6. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device type 05



$\overline{CE}$	$\overline{W}$	Mode	Output
H	X	Not Selected	High Z
L	L	Write	High Z
L	H	Read	D out

FIGURE 6. Read-cycle timing waveforms.

Device type 05

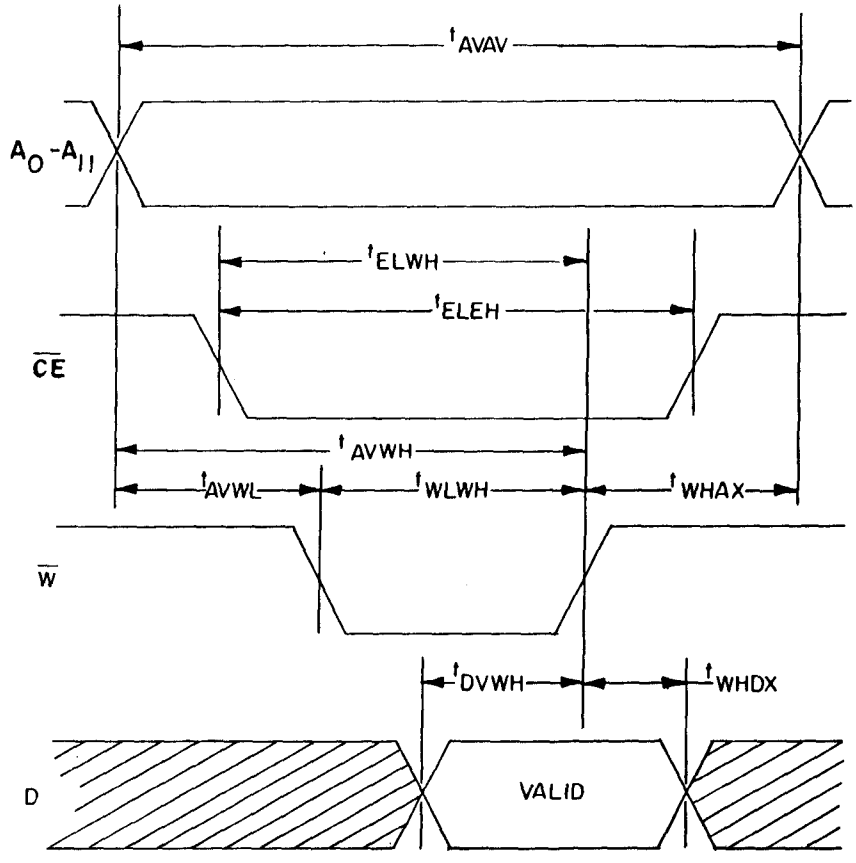


FIGURE 6. Write-cycle timing waveforms.

Device type 06

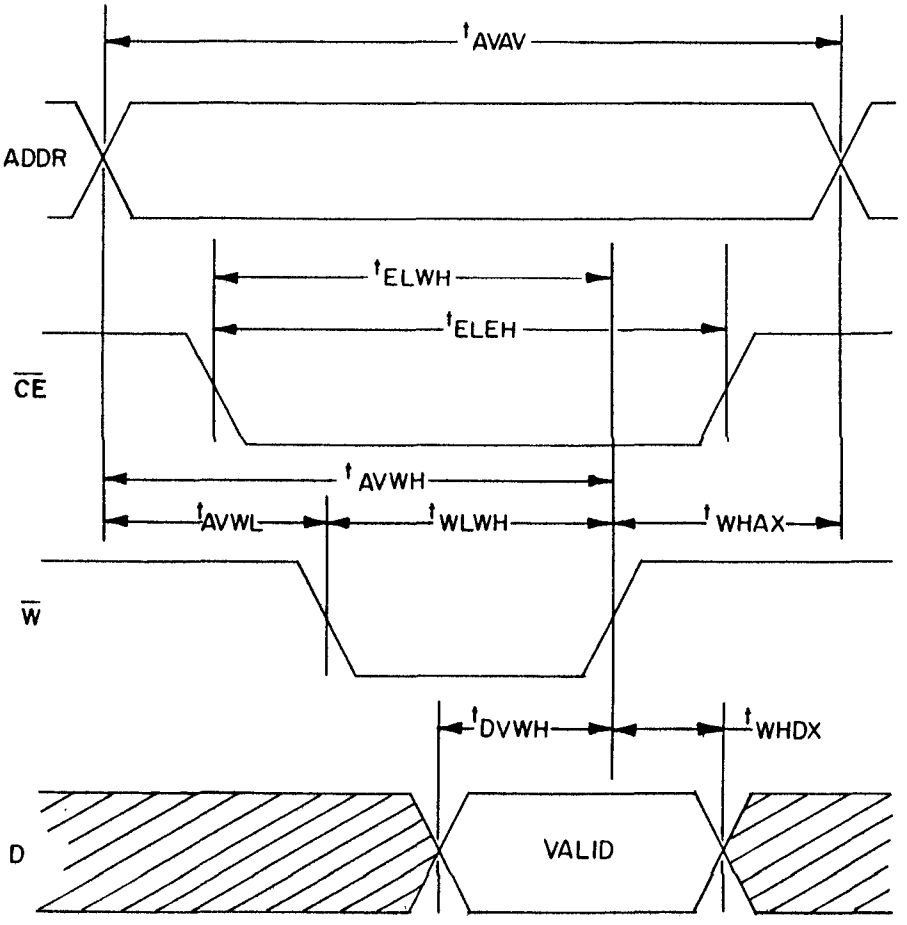
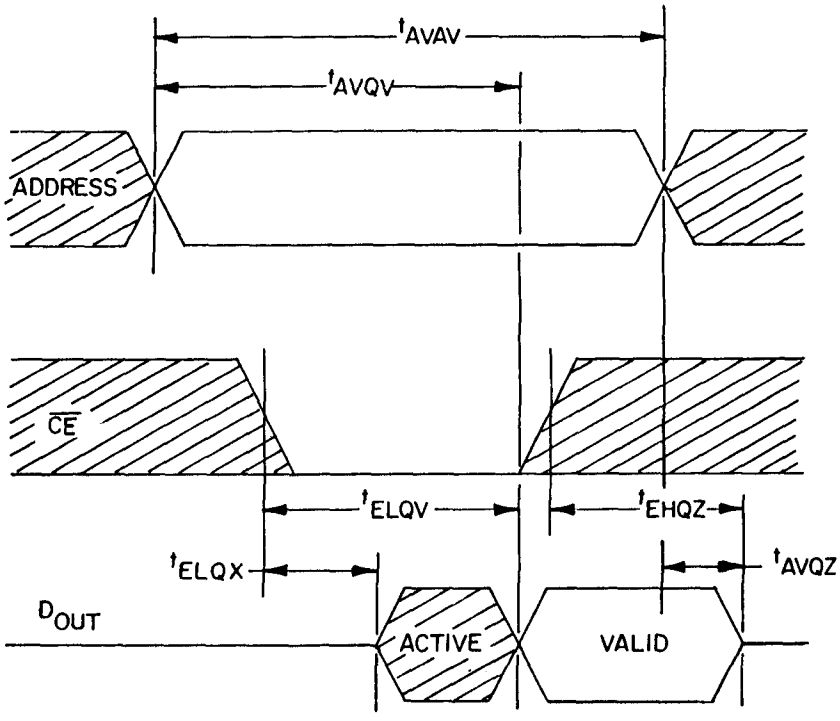


FIGURE 6. Write-cycle timing waveforms.

Device type 06



Function	$\overline{CE}$	$\overline{W}$	Data pins
Read	0	1	Output dependent on data
Write	0	0	Input
Not selected	1	X	High Z

FIGURE 6. Read-cycle timing waveforms.

Timing parameter	Description	Device types				
		01		02		Unit
		Min	Max	Min	Max	
t_{ELQV}	Chip enable access time		120		120	ns
t_{AVQV}	Address access time		120		120	ns
t_{ELQX}	Chip enable output enable time	10		10		ns
t_{WLQZ}	Write enable output disable time				50	ns
t_{EHQZ}	Chip enable output disable time		50		50	ns
t_{ELEH}	Chip enable pulse negative width	120		120		ns
t_{EHEL}	Chip enable pulse positive width	50		50		ns
t_{AVEL}	Address setup time	0		0		ns
t_{ELAX}	Address hold time	40		40		ns
t_{WLWH}	Write enable pulse negative width	20		120		ns
t_{WLEH}	Write enable pulse setup time to chip disable	70		120		ns
t_{WLEL}	Write enable pulse setup time to chip enable	0		0		ns
t_{ELWH}	Write enable pulse hold time from chip enable	40		120		ns
t_{ELDX}	Write data hold time	25				ns
t_{DVWH}	Data setup time			50		ns
t_{WHDX}	Data hold time			0		ns
t_{ELEL}	Read or write cycle time	170		170		ns
t_{DVEL}	Write data setup time	0				ns
t_{WHEH}	Write enable high to chip enable high	10				ns
t_{QVWL}	Data valid to write time			0		ns
t_{EHWH}	Output high-Z time			0		ns
t_{DVWL}	Data setup time	0				ns
t_{WLDX}	Data hold time	25				ns
t_{WLDV}	Write data delay time			70		ns
t_{WHEL}	Write enable read mode setup time	0				ns

FIGURE 7. Timing test conditions over operating temperature range.

Timing parameter	Description	Device types								
		03		04		05		06		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ELQV}	Chip enable access time		300		300		280		200	ns
t_{AVQV}	Address access time		320		320		250		250	ns
t_{ELQX}	Chip enable output enable time		100		100			20		ns
t_{WLQZ}	Write enable output disable time				100					ns
t_{ELEH}	Chip enable pulse negative width	300		300		220		200		ns
t_{EHEL}	Chip enable pulse positive width	120		120						ns
t_{AVEL}	Address setup time	20		20						ns
t_{ELAX}	Address hold time	50		100						ns
t_{WHAX}	Address hold time					45		40		ns
t_{WLWH}	Write enable pulse negative width	80		300		145		150		ns
t_{WLEH}	Write enable pulse setup time to chip disable	200		300						ns
t_{WLEL}	Write enable pulse setup time to chip enable	0		0						ns
t_{ELWH}	Write enable pulse hold time from chip enable	80		300						ns
t_{ELDX}	Write data hold time	80								ns
t_{DVWH}	Data setup time			200		120		75		ns
t_{WHDX}	Data hold time			30		10		5		ns
t_{ELEL}	Read or write cycle time	420		420						ns
t_{AVAV}	Read or write address cycle time					250		250		ns
t_{DVEL}	Write data setup time	0								ns
t_{WHEH}	Write enable high to chip enable high	0								ns
t_{ELWL}	Write output output high-Z time	0		0						ns
t_{QVWL}	Data valid to write time	0		0						ns
t_{EHWH}	Output high-Z time	0		0						ns
t_{DVWL}	Data setup time	0								ns
t_{WLDX}	Data hold time	80								ns
t_{ELDX}	Early write data	80				ns				ns
t_{WLDV}	Write data delay time			100		ns				ns
t_{WHEL}	Write enable read mode setup time	0				ns				ns
t_{AVWH}	Address setup to end write time					205		200		ns

FIGURE 7. Timing test conditions over operating temperature range - Continued.

TABLE III. Group A inspection for device type 01.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	100 μA	GND	GND	GND	GND	GND		GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	A_0	0.1	2.0					V
		2	GND	100 μA	GND	"	"	"		"		"	"	"	"	"	"	"	"	"	A_1	"	"					"
		3	"	GND	100 μA	"	"	"		"		"	"	"	"	"	"	"	"	"	A_2	"	"					"
		4	"	"	GND	100 μA	"	"		"		"	"	"	"	"	"	"	"	"	A_3	"	"					"
		5	"	"	"	GND	100 μA	"		"		"	"	"	"	"	"	"	"	"	A_4	"	"					"
		6	"	"	"	"	GND	100 μA		"		"	"	"	"	"	"	"	"	"	A_5	"	"					"
		7	"	"	"	"	"	GND		100 μA		"	"	"	"	"	"	"	"	"	$\overline{W}$	"	"					"
		8	"	"	"	"	"	"		GND		100 μA	"	"	"	"	"	"	"	"	$\overline{CE}$	"	"					"
		9	"	"	"	"	"	"		"		GND	100 μA	"	"	"	"	"	"	"	D	"	"					"
		10	"	"	"	"	"	"		"		"	GND	100 μA	"	"	"	"	"	"	A_{11}	"	"					"
		11	"	"	"	"	"	"		"		"	"	GND	100 μA	"	"	"	"	"	A_{10}	"	"					"
		12	"	"	"	"	"	"		"		"	"	"	GND	100 μA	"	"	"	"	A_9	"	"					"
		13	"	"	"	"	"	"		"		"	"	"	"	GND	100 μA	"	"	"	A_8	"	"					"
		14	"	"	"	"	"	"		"		"	"	"	"	"	GND	100 μA	"	"	A_7	"	"					"
		15	"	"	"	"	"	"		"		"	"	"	"	"	GND	GND	100 μA	"	A_6	"	"					"
$V_{IC(NEG)}$		16	-100 μA	"	"	"	"	"		"	GND	"	"	"	"	"	"	"	GND		A_0	-0.1	-2.0					"
		17	GND	-100 μA	"	"	"	"		"	"	"	"	"	"	"	"	"	"		A_1	"	"					"
		18	"	GND	-100 μA	"	"	"		"	"	"	"	"	"	"	"	"	"		A_2	"	"					"
		19	"	"	GND	-100 μA	"	"		"	"	"	"	"	"	"	"	"	"		A_3	"	"					"
		20	"	"	"	GND	-100 μA	"		"	"	"	"	"	"	"	"	"	"		A_4	"	"					"
		21	"	"	"	"	GND	-100 μA		"	"	"	"	"	"	"	"	"	"		A_5	"	"					"
		22	"	"	"	"	"	GND		-100 μA	"	"	"	"	"	"	"	"	"		$\overline{W}$	"	"					"
		23	"	"	"	"	"	"		GND	"	-100 μA	"	"	"	"	"	"	"		$\overline{CE}$	"	"					"
		24	"	"	"	"	"	"		"	"	GND	100 μA	"	"	"	"	"	"		D	"	"					"
		25	"	"	"	"	"	"		"	"	"	GND	-100 μA	"	"	"	"	"		A_{11}	"	"					"
		26	"	"	"	"	"	"		"	"	"	"	GND	-100 μA	"	"	"	"		A_{10}	"	"					"
		27	"	"	"	"	"	"		"	"	"	"	"	GND	-100 μA	"	"	"		A_9	"	"					"
		28	"	"	"	"	"	"		"	"	"	"	"	"	GND	-100 μA	"	"		A_8	"	"					"
		29	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	-100 μA	"		A_7	"	"					"
		30	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	GND	-100 μA		A_6	"	"					"
V_{OL}	3007	31	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	2/	2.5 V	"	0.8 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	Q		0.4		0.4		0.4	"
V_{OH}	3006	32	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	2.5 V	"	0.8 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	Q	2.4		2.4		2.4		"
I_{IH} 4/	3010	33	5.5 V	GND	GND	GND	GND	GND		GND	"	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	A_0				1.0			μA
		34	GND	5.5 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1				"			"
		35	"	GND	5.5 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2				"			"
		36	"	"	GND	5.5 V	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3				"			"
		37	"	"	"	GND	5.5 V	"		"	"	"	"	"	"	"	"	"	"	"	A_4				"			"
		38	"	"	"	"	GND	5.5 V		"	"	"	"	"	"	"	"	"	"	"	A_5				"			"
		39	"	"	"	"	"	GND		5.5 V	"	"	"	"	"	"	"	"	"	"	$\overline{W}$				"			"
		40	"	"	"	"	"	"		GND	"	5.5 V	"	"	"	"	"	"	"	"	$\overline{CE}$				"			"
		41	"	"	"	"	"	"		"	"	GND	.5 V	"	"	"	"	"	"	"	D				"			"
		42	"	"	"	"	"	"		"	"	"	GND	5.5 V	"	"	"	"	"	"	A_{11}				"			"
		43	"	"	"	"	"	"		"	"	"	"	GND	5.5 V	"	"	"	"	"	A_{10}				"			"
		44	"	"	"	"	"	"		"	"	"	"	"	GND	5.5 V	"	"	"	"	A_9				"			"
		45	"	"	"	"	"	"		"	"	"	"	"	"	GND	5.5 V	"	"	"	A_8				"			"
		46	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	5.5 V	"	"	A_7				"			"
		47	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	GND	5.5 V	"	A_6				"			"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 01 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IL} 4/	3009	48	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A_0				-1.0			µA
		49	5.5 V	GND	5.5 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1				"			"
		50	"	5.5 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2				"			"
		51	"	"	5.5 V	GND	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3				"			"
		52	"	"	"	5.5 V	GND	"		"	"	"	"	"	"	"	"	"	"	"	A_4				"			"
		53	"	"	"	"	5.5 V	GND		"	"	"	"	"	"	"	"	"	"	"	A_5				"			"
		54	"	"	"	"	"	5.5 V		GND	"	"	"	"	"	"	"	"	"	"	$\overline{W}$				"			"
		55	"	"	"	"	"	"		5.5 V	"	GND	"	"	"	"	"	"	"	"	$\overline{CE}$				"			"
		56	"	"	"	"	"	"		"	"	5.5 V	GND	"	"	"	"	"	"	"	D				"			"
		57	"	"	"	"	"	"		"	"	"	5.5 V	GND	"	"	"	"	"	"	A_{11}				"			"
		58	"	"	"	"	"	"		"	"	"	"	5.5 V	GND	"	"	"	"	"	A_{10}				"			"
		59	"	"	"	"	"	"		"	"	"	"	"	5.5 V	GND	"	"	"	"	A_9				"			"
		60	"	"	"	"	"	"		"	"	"	"	"	"	5.5 V	GND	"	"	"	A_8				"			"
		61	"	"	"	"	"	"		"	"	"	"	"	"	"	5.5 V	GND	"	"	A_7				"			"
		62	"	"	"	"	"	"		"	"	"	"	"	"	"	5.5 V	5.5 V	GND	"	A_6				"			"
I_{OHZ}		63	GND	GND	GND	GND	GND	GND	5.5 V	"	"	5.5 V	GND	GND	GND	GND	GND	GND	GND	5.5 V	Q		1.0		1.0		1.0	"
		64	GND	GND	GND	GND	GND	GND	5.5 V	0.8 V	"	GND	GND	GND	GND	GND	GND	GND	GND	"	Q		1.0		1.0		1.0	"
I_{OLZ}		65	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	Q		-1.0		-1.0		-1.0	"
		66	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	0.8 V	"	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	Q		-1.0		-1.0		-1.0	"
I_{DD1}	3005	67	GND	GND	GND	GND	GND	GND		GND	"	"	GND	GND	GND	GND	GND	GND	GND	"	V_{DD} 5/		50		50		50	"
I_{DD2}		68	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 6/		"		"		"	"
I_{DD3}		69	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 7/		"		"		"	"
I_{DD4}		70	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 13/		"		"		"	"
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	71	8/	8/	8/	8/	8/	8/		8/	GND	8/	8/	8/	8/	8/	8/	8/	8/	GND	Each input		8					pF
																						Subgroup 8 T_C = +125°C						
																						Min	Max					
PWR DWN		72	9/	9/	9/	9/	9/	9/		9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	V_{DD}		2.0					V
ADD COMP		73	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	Q	10/	10/					V

See footnotes at end of table III.

TABLE III. Group A inspection for device type 01 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6	74	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		120		120		120	ns
t_{ELQV}		75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		120		120		120	"
t_{ELQX} 14/		76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	10		10		10		"
t_{EHQZ} 14/		77	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50		50		50	"
																						Subgroup 12 T_C = +25°C						
																						Min	Max					
I_{DDOP}		78	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V			7					mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 02.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	100 µA																	GND	A_6	0.1	2.0					V
		2		100 µA																"	A_5	"	"					"
		3			100 µA															"	A_4	"	"					"
		4				100 µA														"	A_3	"	"					"
		5					100 µA													"	A_0	"	"					"
		6						100 µA												"	A_1	"	"					"
		7							100 µA											"	A_2	"	"					"
		8								100 µA										"	$\overline{CE}$	"	"					"
		9										100 µA								"	$\overline{W}$	"	"					"
		10											100 µA							"	D_3/Q_3	"	"					"
		11												100 µA						"	D_2/Q_2	"	"					"
		12													100 µA					"	D_1/Q_1	"	"					"
		13														100 µA				"	D_0/Q_0	"	"					"
		14															100 µA			"	A_9	"	"					"
		15																100 µA		"	A_8	"	"					"
		16																	100 µA	"	A_7	"	"					"
$V_{IC(NEG)}$		17	-100 µA								GND										A_6	-0.1	-2.0					"
		18		-100 µA							"										A_5	"	"					"
		19			-100 µA						"										A_4	"	"					"
		20				-100 µA					"										A_3	"	"					"
		21					-100 µA				"										A_0	"	"					"
		22						-100 µA			"										A_1	"	"					"
		23							-100 µA		"										A_2	"	"					"
		24								-100 µA	"										$\overline{CE}$	"	"					"
		25									"	-100 µA									$\overline{W}$	"	"					"
		26									"		-100 µA								D_3/Q_3	"	"					"
		27									"			-100 µA							D_2/Q_2	"	"					"
		28									"				-100 µA						D_1/Q_1	"	"					"
		29									"					-100 µA					D_0/Q_0	"	"					"
		30									"						-100 µA				A_9	"	"					"
		31									"							-100 µA			A_8	"	"					"
		32									"								-100 µA		A_7	"	"					"
V_{OL}	3007	33	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	0.8 V	"	2.5 V	2/	2/	2/	2/	4.5 V	4.5 V	4.5 V	4.5 V	Q		0.4		0.4		0.4	"
V_{OH}	3006	34	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	0.8 V	"	2.5 V	3/	3/	3/	3/	4.5 V	4.5 V	4.5 V	4.5 V	Q	2.4		2.4		2.4		"
I_{IH1} 4/	3010	35	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	All inputs together		1.0					µA
I_{IH2}		36	5.5 V	GND	GND	GND	GND	GND	GND	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	"	A_6		1.0		1.0			"
		37	GND	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		38	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		39	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		40	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		41	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		42	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		43	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		44	"	"	"	"	"	"	"	GND	"	5.5 V	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		45	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		46	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	D_2/Q_2		"		"			"
		47	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	D_1/Q_1		"		"			"
		48	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	D_0/Q_0		"		"			"
		49	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	A_9		"		"			"
		50	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	A_8		"		"			"
		51	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	GND	5.5 V	"	A_7		"		"			"
I_{IL1} 4/	3009	52	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	"	All inputs together		-1.0					"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 02 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IL2}	3009	53	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A_6		-1		-1			μA
		54	5.5 V	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		55	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		56	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		57	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		58	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		59	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		60	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		61	"	"	"	"	"	"	"	5.5 V	"	GND	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		62	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		63	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	D_2/Q_2		"		"			"
		64	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	D_1/Q_1		"		"			"
		65	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	D_0/Q_0		"		"			"
		66	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	A_9		"		"			"
		67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	A_8		"		"			"
		68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	5.5 V	GND	A_7		"		"			"
I_{OHZ}		69	GND	GND	GND	GND	GND	GND	GND	5.5 V	"	"	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	GND	"	Q_3/Q_3		1.0		1.0		1.0	"
		70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_2/Q_2		"		"		"	"
		71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_1/Q_1		"		"		"	"
		72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_0/Q_0		"		"		"	"
		73	"	"	"	"	"	"	"	GND	"	0.8 V	"	"	"	"	"	"	"	"	Q_3/Q_3		"		"		"	"
		74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_2/Q_2		"		"		"	"
		75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_1/Q_1		"		"		"	"
		76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_0/Q_0		"		"		"	"
I_{OLZ}		77	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	GND	GND	GND	GND	5.5 V	5.5 V	5.5 V	"	Q_3/Q_3		-1.0		-1.0		-1.0	"
		78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_2/Q_2		"		"		"	"
		79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_1/Q_1		"		"		"	"
		80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_0/Q_0		"		"		"	"
		81	"	"	"	"	"	"	"	GND	"	0.8 V	"	"	"	"	"	"	"	"	Q_3/Q_3		"		"		"	"
		82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_2/Q_2		"		"		"	"
		83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_1/Q_1		"		"		"	"
		84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q_0/Q_0		"		"		"	"
I_{DD1}	3005	85	GND	GND	GND	GND	GND	GND	GND	"	"	GND					GND	GND	GND	"	V_{DD} 5/		50		50		50	"
I_{DD2}		86	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 6/		"		"		"	"
I_{DD3}		87	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 7/		"		"		"	"
I_{DD4}		88	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 13/		"		"		"	"
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	89	8/	8/	8/	8/	8/	8/		8/	GND	8/					8/	8/	8/	GND	Each input		8					pF

See footnotes at end of table III.

TABLE III. Group A inspection for device type 02 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 8 T_C = +25°C						
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max					
PWR DWN		90	9/	9/	9/	9/	9/	9/		9/	GND	9/					9/	9/	9/	9/	Q		2.0					V
ADD COMP		91	10/	10/	10/	10/	10/	10/		10/	GND	10/					10/	10/	10/	10/	Q	10/	10/					V
																						Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
																						Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6	92	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		120		120		120	ns
t_{ELQV}		93	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		120		120		120	"
t_{ELQX} 14/		94	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	10		10		10		"
T_{EHQZ} 14/		95	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50		50		50	"
																						Subgroup 12 T_C = +25°C						
																						Min	Max					
I_{DDOP}		96	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V	V_{DD}		7					mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 03.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	50 μA																	GND	A_0	0.1	2.0					V
		2		50 μA																"	A_1	"	"					"
		3			50 μA															"	A_2	"	"					"
		4				50 μA														"	A_3	"	"					"
		5					50 μA													"	A_4	"	"					"
		6						50 μA												"	A_5	"	"					"
		7								50 μA										"	$\overline{W}$	"	"					"
		8										50 μA								"	$\overline{CE}$	"	"					"
		9											50 μA							"	D	"	"					"
		10												50 μA						"	A_{11}	"	"					"
		11													50 μA					"	A_{10}	"	"					"
		12														50 μA				"	A_9	"	"					"
		13															50 μA			"	A_8	"	"					"
		14																50 μA		"	A_7	"	"					"
		15																	50 μA	"	A_6	"	"					"
$V_{IC(NEG)}$		16	-50 μA								GND										A_0	-0.1	-2.0					"
		17		-50 μA							"										A_1	"	"					"
		18			-50 μA						"										A_2	"	"					"
		19				-50 μA					"										A_3	"	"					"
		20					-50 μA				"										A_4	"	"					"
		21						-50 μA			"										A_5	"	"					"
		22								-50 μA	"										$\overline{W}$	"	"					"
		23									"	-50 μA									$\overline{CE}$	"	"					"
		24									"		-50 μA								D	"	"					"
		25									"			-50 μA							A_{11}	"	"					"
		26									"				-50 μA						A_{10}	"	"					"
		27									"					-50 μA					A_9	"	"					"
		28									"						-50 μA				A_8	"	"					"
		29									"							-50 μA			A_7	"	"					"
		30									"								-50 μA		A_6	"	"					"
V_{OL}	3007	31	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	2/	4.5 V	"	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	Q		0.4		0.4		0.4	"
V_{OH}	3006	32	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	4.5 V	"	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	Q	2.4		2.4		2.4		"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 03 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
																						Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18								
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IH}	3010	33	5.5 V	GND	GND	GND	GND	GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	A_0				1.0			µA
		34	GND	5.5 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1				"			"
		35	"	GND	5.5 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2				"			"
		36	"	"	GND	5.5 V	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3				"			"
		37	"	"	"	GND	5.5 V	"		"	"	"	"	"	"	"	"	"	"	"	A_4				"			"
		38	"	"	"	"	GND	5.5 V		"	"	"	"	"	"	"	"	"	"	"	A_5				"			"
		39	"	"	"	"	"	GND		5.5 V	"	"	"	"	"	"	"	"	"	"	$\overline{W}$				"			"
		40	"	"	"	"	"	"		GND	"	5.5 V	"	"	"	"	"	"	"	"	$\overline{CE}$				"			"
		41	"	"	"	"	"	"		"	"	GND	5.5 V	"	"	"	"	"	"	"	D				"			"
		42	"	"	"	"	"	"		"	"	"	GND	5.5 V	"	"	"	"	"	"	A_{11}				"			"
		43	"	"	"	"	"	"		"	"	"	"	GND	5.5 V	"	"	"	"	"	A_{10}				"			"
		44	"	"	"	"	"	"		"	"	"	"	"	GND	5.5 V	"	"	"	"	A_9				"			"
		45	"	"	"	"	"	"		"	"	"	"	"	"	GND	5.5 V	"	"	"	A_8				"			"
		46	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	5.5 V	"	"	A_7				"			"
		47	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	GND	5.5 V	"	A_6				"			"
I_{IL}	3009	48	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	A_0				-1.0			"
		49	5.5 V	GND	5.5 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1				"			"
		50	"	5.5 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2				"			"
		51	"	"	5.5 V	GND	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3				"			"
		52	"	"	"	5.5 V	GND	"		"	"	"	"	"	"	"	"	"	"	"	A_4				"			"
		53	"	"	"	"	5.5 V	GND		"	"	"	"	"	"	"	"	"	"	"	A_5				"			"
		54	"	"	"	"	"	5.5 V		GND	"	"	"	"	"	"	"	"	"	"	$\overline{W}$				"			"
		55	"	"	"	"	"	"		5.5 V	"	GND	"	"	"	"	"	"	"	"	$\overline{CE}$				"			"
		56	"	"	"	"	"	"		"	"	5.5 V	GND	"	"	"	"	"	"	"	D				"			"
		57	"	"	"	"	"	"		"	"	"	5.5 V	GND	"	"	"	"	"	"	A_{11}				"			"
		58	"	"	"	"	"	"		"	"	"	"	5.5 V	GND	"	"	"	"	"	A_{10}				"			"
		59	"	"	"	"	"	"		"	"	"	"	"	5.5 V	GND	"	"	"	"	A_9				"			"
		60	"	"	"	"	"	"		"	"	"	"	"	"	5.5 V	GND	"	"	"	A_8				"			"
		61	"	"	"	"	"	"		"	"	"	"	"	"	"	5.5 V	GND	"	"	A_7				"			"
		62	"	"	"	"	"	"		"	"	"	"	"	"	"	5.5 V	5.5 V	GND	"	A_6				"			"
I_{DHZ}		63	GND	GND	GND	GND	GND	GND	5.5 V	"	"	"	GND	GND	GND	GND	GND	GND	GND	"	Q		10		10		10	"
		64	GND	GND	GND	GND	GND	GND	5.5 V	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	"	Q		10		10		10	"
I_{OLZ}		65	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	Q		-10		-10		-10	"
		66	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	"	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	Q		-10		-10		-10	"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 03 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{DD1}	3005	67	GND	GND	GND	GND	GND	GND		"	"	"	GND	GND	GND	GND	GND	GND	GND	5.5 V	V_{DD} 5/		200		200		200	μA
I_{DD2}		68	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 6/		"		"		"	μA
I_{DD3}		69	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 7/		"		"		"	μA
I_{DD4}		70	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{DD} 13/		"		"		"	μA
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	71	8/	8/	8/	8/	8/	8/		8/	GND	8/	8/	8/	8/	8/	8/	8/	8/	GND	Each input		8					pF
																						Subgroup 8 T_C = +125°C						
																						Min	Max					
PWR DWN		72	9/	9/	9/	9/	9/	9/		9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	V_{DD}		3.0					V
Functional tests		73	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	Q	10/	10/					V
																						Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
																						Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6	74	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		320		320		320	ns
t_{ELQV}		75	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		300		300		300	ns
																						Subgroup 12 T_C = +25°C						
																						Min	Max					
I_{DDOP}		76	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V	V_{DD}		7					mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 04.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	50 µA																	GND	A_6	0.1	2.0					V
		2		50 µA																"	A_5	"	"					"
		3			50 µA															"	A_4	"	"					"
		4				50 µA														"	A_3	"	"					"
		5					50 µA													"	A_0	"	"					"
		6						50 µA												"	A_1	"	"					"
		7							50 µA											"	A_2	"	"					"
		8								50 µA										"	$\overline{CE}$	"	"					"
		9										50 µA								"	$\overline{W}$	"	"					"
		10											50 µA							"	D_3/Q_3	"	"					"
		11												50 µA						"	D_2/Q_2	"	"					"
		12													50 µA					"	D_1/Q_1	"	"					"
		13														50 µA				"	D_0/Q_0	"	"					"
		14															50 µA			"	A_9	"	"					"
		15																50 µA		"	A_8	"	"					"
		16																	50 µA	"	A_7	"	"					"
$V_{IC(NEG)}$		17	-50 µA								GND										A_6	-0.1	-2.0					"
		18		-50 µA							"										A_5	"	"					"
		19			-50 µA						"										A_4	"	"					"
		20				-50 µA					"										A_3	"	"					"
		21					-50 µA				"										A_0	"	"					"
		22						-50 µA			"										A_1	"	"					"
		23							-50 µA		"										A_2	"	"					"
		24								-50 µA	"										$\overline{CE}$	"	"					"
		25									"	-50 µA									$\overline{W}$	"	"					"
		26									"		-50 µA								D_3/Q_3	"	"					"
		27									"			-50 µA							D_2/Q_2	"	"					"
		28									"				-50 µA						D_1/Q_1	"	"					"
		29									"					-50 µA					D_0/Q_0	"	"					"
		30									"						-50 µA				A_9	"	"					"
		31									"							-50 µA			A_8	"	"					"
		32									"								-50 µA		A_7	"	"					"
V_{OL}	3007	33	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	"	4.5 V	2/	2/	2/	2/	4.5 V	4.5 V	4.5 V	4.5 V	Q_3-Q_0		0.4		0.4		0.4	"
V_{OH}	3006	34	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	"	4.5 V	3/	3/	3/	3/	4.5 V	4.5 V	4.5 V	4.5 V	Q_3-Q_0	2.4		2.4		2.4		"
I_{IH1} 4/	3010	35	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	All inputs together		1.0					µA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 04 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
																						Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18								
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IH2}	3010	36	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	A_6		1.0		1.0			μA
		37	GND	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		38	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		39	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		40	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		41	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		42	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		43	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		44	"	"	"	"	"	"	"	GND	"	5.5 V	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		45	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		46	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	D_2/Q_2		"		"			"
		47	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	D_1/Q_1		"		"			"
		48	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	D_0/Q_0		"		"			"
		49	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	A_9		"		"			"
		50	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	A_8		"		"			"
		51	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	GND	5.5 V	"	A_7		"		"			"
I_{IL1} 4/	3009	52	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	All inputs together		"		"			"
I_{IL2}		53	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	"	A_6		-1.0		-1.0			"
		54	5.5 V	GND	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		55	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		56	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		57	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		58	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		59	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		60	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		61	"	"	"	"	"	"	"	5.5 V	"	GND	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		62	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		63	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	D_2/Q_2		"		"			"
		64	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	D_1/Q_1		"		"			"
		65	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	D_0/Q_0		"		"			"
		66	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	A_9		"		"			"
		67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	A_8		"		"			"
		68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	5.5 V	GND	"	A_7		"		"			"
I_{OHZ}		69	GND	GND	GND	GND	GND	GND	GND	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	"	"	D_3/Q_3		10		10		10	"
		70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
		73	"	"	"	"	"	"	"	GND	"	GND	"	"	"	"	"	"	"	"	D_3/Q_3		"		"		"	"
		74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
I_{OLZ}		77	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	GND	GND	GND	GND	5.5 V	5.5 V	5.5 V	"	D_3/Q_3		-10		-10		-10	"
		78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
		81	"	"	"	"	"	"	"	GND	"	GND	"	"	"	"	"	"	"	"	D_3/Q_3		"		"		"	"
		82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 04 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{DD1}	3005	85	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	GND	GND	5.5 V	V_{DD} 5/		250		250		250	µA
I_{DD2}		86	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 6/		"		"		"	"
I_{DD3}		87	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 7/		"		"		"	"
I_{DD4}		88	"	"	"	"	"	"	"	"	"	"					"	"	"	"	V_{DD} 13/		"		"		"	"
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	89	8/	8/	8/	8/	8/	8/	8/	8/	GND	8/					8/	8/	8/	GND	Each input		8					pF
																						Subgroup 8 T_C = +25°C						
																						Min	Max					
PWR DWN		90	9/	9/	9/	9/	9/	9/	9/	9/	GND	9/					9/	9/	9/	9/	Q		3.0					V
Functional tests		91	10/	10/	10/	10/	10/	10/	10/	10/	GND	10/					10/	10/	10/	10/	Q	10/	10/					V
																						Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
																						Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6	92	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		320		320		320	ns
t_{ELQV}		93	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Q		300		300		300	ns
																						Subgroup 12 T_C = +25°C						
																						Min	Max					
I_{DDOP}		94	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V	V_{DD}		7					mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 05.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	100 μA																	GND	A_0	0.1	3.0					V
		2		100 μA																"	A_1	"	"					"
		3			100 μA															"	A_2	"	"					"
		4				100 μA														"	A_3	"	"					"
		5					100 μA													"	A_4	"	"					"
		6						100 μA												"	A_5	"	"					"
		7								100 μA										"	$\overline{W}$	"	"					"
		8										100 μA								"	$\overline{CE}$	"	"					"
		9											100 μA							"	D	"	"					"
		10												100 μA						"	A_{11}	"	"					"
		11													100 μA					"	A_{10}	"	"					"
		12														100 μA				"	A_9	"	"					"
		13															100 μA			"	A_8	"	"					"
		14																100 μA		"	A_7	"	"					"
		15																	100 μA	"	A_6	"	"					"
$V_{IC(NEG)}$		16	-100 μA								GND										A_0	-0.1	-3.0					"
		17		-100 μA							"										A_1	"	"					"
		18			-100 μA						"										A_2	"	"					"
		19				-100 μA					"										A_3	"	"					"
		20					-100 μA				"										A_4	"	"					"
		21						-100 μA			"										A_5	"	"					"
		22								-100 μA	"										$\overline{W}$	"	"					"
		23									"	-100 μA									$\overline{CE}$	"	"					"
		24									"		-100 μA								D	"	"					"
		25									"			-100 μA							A_{11}	"	"					"
		26									"				-100 μA						A_{10}	"	"					"
		27									"					-100 μA					A_9	"	"					"
		28									"						-100 μA				A_8	"	"					"
		29									"							-100 μA			A_7	"	"					"
		30									"								-100 μA		A_6	"	"					"
I_{OL}	3007	31	GND	GND	GND	GND	GND	GND	0.4 V	4.75 V	"	GND	GND	GND	GND	GND	GND	GND	GND	4.75 V	Q	4.0		2.5		4.0		mA
I_{OH}	3006	32	GND	GND	GND	GND	GND	GND	4.35 V	4.75 V	"	GND	GND	GND	GND	GND	GND	GND	GND	4.75 V	Q	-3.0		-2.0		-3.0		mA
I_{IH}	3010	33	5.25 V	GND	GND	GND	GND	GND		GND	"	GND	"	"	"	"	"	"	"	5.25 V	A_0		2.0		10			μA
		34	GND	5.25 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		35	"	GND	5.25 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		36	"	"	GND	5.25 V	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		37	"	"	"	GND	5.25 V	"		"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		38	"	"	"	"	GND	5.25 V		"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		39	"	"	"	"	"	GND		5.25 V	"	"	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		40	"	"	"	"	"	"		GND	"	5.25 V	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		41	"	"	"	"	"	"		"	"	GND	5.25 V	"	"	"	"	"	"	"	D		"		"			"
		42	"	"	"	"	"	"		"	"	"	GND	5.25 V	"	"	"	"	"	"	A_{11}		"		"			"
		43	"	"	"	"	"	"		"	"	"	"	GND	5.25 V	"	"	"	"	"	A_{10}		"		"			"
		44	"	"	"	"	"	"		"	"	"	"	"	GND	5.25 V	"	"	"	"	A_9		"		"			"
		45	"	"	"	"	"	"		"	"	"	"	"	"	GND	5.25 V	"	"	"	A_8		"		"			"
		46	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	5.25 V	"	"	A_7		"		"			"
		47	"	"	"	"	"	"		"	"	"	"	"	"	"	GND	GND	5.25 V	"	A_6		"		"			"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 05 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IL}	3009	48	GND	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V		5.25 V	GND	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	A_0		-2.0		-10			μA
		49	5.25 V	GND	5.25 V	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		50	"	5.25 V	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		51	"	"	5.25 V	GND	"	"		"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		52	"	"	"	5.25 V	GND	"		"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		53	"	"	"	"	5.25 V	GND		"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		54	"	"	"	"	"	5.25 V		GND	"	"	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		55	"	"	"	"	"	"		5.25 V	"	GND	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		56	"	"	"	"	"	"		"	"	5.25 V	GND	"	"	"	"	"	"	"	D		"		"			"
		57	"	"	"	"	"	"		"	"	"	5.25 V	GND	"	"	"	"	"	"	A_{11}		"		"			"
		58	"	"	"	"	"	"		"	"	"	"	5.25 V	GND	"	"	"	"	"	A_{10}		"		"			"
		59	"	"	"	"	"	"		"	"	"	"	"	5.25 V	GND	"	"	"	"	A_9		"		"			"
		60	"	"	"	"	"	"		"	"	"	"	"	"	5.25 V	GND	"	"	"	A_8		"		"			"
		61	"	"	"	"	"	"		"	"	"	"	"	"	"	5.25 V	GND	"	"	A_7		"		"			"
		62	"	"	"	"	"	"		"	"	"	"	"	"	"	5.25 V	5.25 V	GND	"	A_6		"		"			"
I_{OHZ}		63	"	"	"	"	"	"	5.25 V	"	"	"	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	"	Q		5.0		30		5.0	"
		64	"	"	"	"	"	"	5.25 V	GND	"	GND	"	"	"	"	"	"	"	"	Q		5.0		30		5.0	"
I_{OLZ}		65	"	"	"	"	"	"	GND	5.25 V	"	5.25 V	"	"	"	"	"	"	"	"	Q		-5.0		-30		-5.0	"
		66	"	"	"	"	"	"	GND	GND	"	GND	"	"	"	"	"	"	"	"	Q		-5.0		-30		-5.0	"
I_{SS1}	3005	67	"	"	"	"	"	"		5.25 V	"	5.25 V	"	"	"	"	"	"	"	"	V_{SS} 5/		-100		-1000		-100	"
I_{SS2}		68	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 6/		"		"		"	"
I_{SS3}		69	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 7/		"		"		"	"
I_{SS4}		70	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 13/		"		"		"	"
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	71	8/	8/	8/	8/	8/	8/		8/	GND	8/	8/	8/	8/	8/	8/	8/	8/	GND	Each input		5					pF

See footnotes at end of table III.

TABLE III. Group A inspection for device type 05 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 8 T_C = +125°C						
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_0	A_1	A_2	A_3	A_4	A_5	Q	$\overline{W}$	V_{SS}	$\overline{CE}$	D	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{DD}		Min	Max					
I_{CCDR}	9/	72	9/	9/	9/	9/	9/	9/	9/	9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	V_{DD}		400					μA
PWR DWN		73	9/	9/	9/	9/	9/	9/		9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	V_{DD}		2.5					V
Functional tests	15/	74	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	Q	10/	10/					V
																						Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
																						Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6 15/	75	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.75 V	Q		200		250		200	ns
t_{ELQV}		76	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.75 V	Q		220		280		220	ns
																						Subgroup 12 T_C = 25°C						
																						Min	Max					
I_{DDOP}		77	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.25 V	V_{DD}		4.0					mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 06.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	100 μA																	GND	A_6	0.2	3.0					V
		2		100 μA																"	A_5	"	"					"
		3			100 μA															"	A_4	"	"					"
		4				100 μA														"	A_3	"	"					"
		5					100 μA													"	A_0	"	"					"
		6						100 μA												"	A_1	"	"					"
		7							100 μA											"	A_2	"	"					"
		8								100 μA										"	$\overline{CE}$	"	"					"
		9										100 μA								"	$\overline{W}$	"	"					"
		10											100 μA							"	D_3/Q_3	"	"					"
		11												100 μA						"	D_2/Q_2	"	"					"
		12													100 μA					"	D_1/Q_1	"	"					"
		13														100 μA				"	D_0/Q_0	"	"					"
		14															100 μA			"	A_9	"	"					"
		15																100 μA		"	A_8	"	"					"
		16																	100 μA	"	A_7	"	"					"
$V_{IC(NEG)}$		17	-100 μA								GND										A_6	-0.2	-3.0					"
		18		-100 μA							"										A_5	"	"					"
		19			-100 μA						"										A_4	"	"					"
		20				-100 μA					"										A_3	"	"					"
		21					-100 μA				"										A_0	"	"					"
		22						-100 μA			"										A_1	"	"					"
		23							-100 μA		"										A_2	"	"					"
		24								-100 μA	"										$\overline{CE}$	"	"					"
		25									"	-100 μA									$\overline{W}$	"	"					"
		26									"		-100 μA								D_3/Q_3	"	"					"
		27									"			-100 μA							D_2/Q_2	"	"					"
		28									"				-100 μA						D_1/Q_1	"	"					"
		29									"					-100 μA					D_0/Q_0	"	"					"
		30									"						-100 μA				A_9	"	"					"
		31									"							-100 μA			A_8	"	"					"
		32									"								-100 μA		A_7	"	"					"
I_{OL}	3007	33	GND	GND	GND	GND	GND	GND	GND	GND	"	4.75 V	0.4 V	0.4 V	0.4 V	0.4 V	GND	GND	GND	4.75 V	Q_3-Q_0	2.6		1.7		2.6		mA
I_{OH}	3006	34	GND	GND	GND	GND	GND	GND	GND	GND	"	4.75 V	4.35 V	4.35 V	4.35 V	4.35 V	GND	GND	GND	4.75 V	Q_3-Q_0	-1.8		-1.1		-1.8		mA

See footnotes at end of table III.

TABLE III. Group A inspection for device type 06 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
																						Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18								
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IH1} 4/	3010	35	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	GND	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	All inputs together		32		160			µA
I_{IH2}		36	5.25 V	GND	GND	GND	GND	GND	GND	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	"	A_6		2.0		10			"
		37	GND	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		38	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		39	"	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		40	"	"	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		41	"	"	"	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		42	"	"	"	"	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		43	"	"	"	"	"	"	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		44	"	"	"	"	"	"	"	GND	"	5.25 V	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		45	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		46	"	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	"	"	"	"	D_2/Q_2		"		"			"
		47	"	"	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	"	"	"	D_1/Q_1		"		"			"
		48	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	"	"	D_0/Q_0		"		"			"
		49	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	"	A_9		"		"			"
		50	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.25 V	"	"	A_8		"		"			"
		51	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	GND	5.25 V	"	A_7		"		"			"
I_{IL1} 4/	3009	52	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	"	All inputs together		-32		-160			"
I_{IL2}		53	GND	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	"	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	"	A_6		-2.0		-10			"
		54	5.25 V	GND	5.25 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_5		"		"			"
		55	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_4		"		"			"
		56	"	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_3		"		"			"
		57	"	"	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	A_0		"		"			"
		58	"	"	"	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	A_1		"		"			"
		59	"	"	"	"	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	"	A_2		"		"			"
		60	"	"	"	"	"	"	5.25 V	GND	"	"	"	"	"	"	"	"	"	"	$\overline{CE}$		"		"			"
		61	"	"	"	"	"	"	"	5.25 V	"	GND	"	"	"	"	"	"	"	"	$\overline{W}$		"		"			"
		62	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	"	"	"	"	"	D_3/Q_3		"		"			"
		63	"	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	"	"	"	"	D_2/Q_2		"		"			"
		64	"	"	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	"	"	"	D_1/Q_1		"		"			"
		65	"	"	"	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	"	"	D_0/Q_0		"		"			"
		66	"	"	"	"	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	"	A_9		"		"			"
		67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.25 V	GND	"	"	A_8		"		"			"
		68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.25 V	5.25 V	GND	"	A_7		"		"			"

See footnotes at end of table III.

TABLE III. Group A inspection for device type 06 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 1 T_C = +25°C		Subgroup 2 T_C = +125°C		Subgroup 3 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{OHZ}	7/	69	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	GND	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	5.25 V	D_3/Q_3		5.0		50		5.0	µA
		70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
		73	"	"	"	"	"	"	"	GND	"	GND	"	"	"	"	"	"	"	"	D_3/Q_3		"		"		"	"
		74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
I_{OLZ}	6/	77	"	"	"	"	"	"	"	5.25 V	"	5.25 V	GND	GND	GND	GND	"	"	"	"	D_3/Q_3		-5.0		-50		-5.0	"
		78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
		81	"	"	"	"	"	"	"	GND	"	GND	"	"	"	"	"	"	"	"	D_3/Q_3		"		"		"	"
		82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2/Q_2		"		"		"	"
		83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1/Q_1		"		"		"	"
		84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_0/Q_0		"		"		"	"
I_{SS1}	3005	85	GND	GND	GND	GND	GND	GND	GND	5.25 V	"	5.25 V	GND	GND	GND	GND	GND	GND	GND	5.25 V	V_{SS} 5/		-100		-1000		-100	"
I_{SS2}		86	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 6/		"		"		"	"
I_{SS3}		87	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 7/		"		"		"	"
I_{SS4}		88	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	V_{SS} 13/		"		"		"	"
																						Subgroup 4 T_C = +25°C						
																						Min	Max					
C_I	3012	89	8/	8/	8/	8/	8/	8/	8/	8/	GND	8/					8/	8/	8/	GND	Each input		5					pF
																						Subgroup 8 T_C = +125°C						
																						Min	Max					
I_{CCDR}		90	9/	9/	9/	9/	9/	9/	9/	9/		9/					9/	9/	9/	9/	V_{DD}		500					µA
PWR DWN		91	9/	9/	9/	9/	9/	9/	9/	9/	GND	9/					9/	9/	9/	9/	Q		2.5					V
Functional tests	15/	92	10/	10/	10/	10/	10/	10/	10/	10/	GND	10/					10/	10/	10/	10/	Q	10/	10/					V

See footnotes at end of table III.

TABLE III. Group A inspection for device type 06 - Continued.

Symbol	MIL-STD-883 method	Case V	Terminal conditions 1/																		Measured terminal	Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		Subgroup 9 T_C = +25°C		Subgroup 10 T_C = +125°C		Subgroup 11 T_C = -55°C		
		K	2	3	4	5	7	8	9	11	12	13	15	16	17	18	21	22	23	24								
		Test no.	A_6	A_5	A_4	A_3	A_0	A_1	A_2	$\overline{CE}$	V_{SS}	$\overline{W}$	D_3/Q_3	D_2/Q_2	D_1/Q_1	D_0/Q_0	A_9	A_8	A_7	V_{DD}		Min	Max	Min	Max	Min	Max	
t_{AVQV}	Fig. 6	93	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.75 V	Q		200		250		200	ns
t_{ELQV}		94	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.75 V	Q		160		200		160	ns
																						Subgroup 12 T_C = +25°C						
																						Min	Max					
I_{DDOP}		95	12/	12/	12/	12/	12/	12/	12/	12/	GND	12/	12/	12/	12/	12/	12/	12/	12/	5.25 V	V_{DD}		6					mA

1/ Pins not designated may be high level logic or low level logic. Exceptions are as follows: $V_{IC(pos)}$ test, the V_{SS} terminal shall be open, or if tester limitations prevent open, the GND condition is permitted; $V_{IC(neg)}$ tests, the V_{DD} terminal shall be open; I_{DD} test, the output terminal shall be open.

2/ Contents of addressed cell shall be data 0, I_{OL} = 2 mA for V_{OL} measurements, or V_{OL} = 0.4 V for I_{OL} measurments.

3/ Contents of addressed cell shall be data 1, I_{OH} = -1 mA for V_{OH} measurements, or V_{OH} = 4.35 V for I_{OH} measurements.

4/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at +25°C for each individual input or measure all inputs together.

5/ Fill memory with checkerboard data pattern.

6/ Fill memory with 1's.

7/ Fill memory with 0's.

8/ See 4.4.1c.

9/ Power down test (PWRDWN) terminal conditions shall be as follows:

a. Use load specified on figure 5.

b. The power down test shall be performed as follows:

(1) Power up RAM to full functional voltage.

(2) Write topologically true checkboard pattern into RAM memory array.

(3) Reduce V_{DD} to required voltage. All device inputs shall be reduced along with V_{DD}, exercising special care to avoid latch-up.

(4) Maintain RAM at reduced voltage.

(5) Measure the leakage current during this period.

(6) Raise V_{DD} to full functional voltage.

(7) Verify RAM contents to be unchanged from patten written in (2) above.

(8) Repeat steps (1) through (6) using the inverse checkerboard pattern.

10/ Functional test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 6.

b. Use several patterns (see appendix).

c. Use load specified on figure 5.

d. V_{DD} per appropriate type, see table III; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$.

11/ Timing test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 6.

b. Use pattern of choice.

c. Use load specified on figure 7.

d. V_{DD} per appropriate type, see table III; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$.

12/ Operating current test (I_{DDOP}) terminal conditions shall be as follows:

a. Period = 1 μs using a write cycle loop during measurement.

b. Use topologically true checkerboard pattern (see appendix).

c. V_{IL} = 0 V; V_{IH} = 5.5 V for device types 01 to 04, V_{IH} = 5.25 V for device types 05 and 06.

13/ Inverse checkerboard data pattern.

14/ Guaranteed but not tested.

15/ a. $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$ for 4.75 V MARCH, MASEST, GALPAT, t_{AVQV}, and t_{ELQV} tests.

b. V_{IL} = 0.8 V, $V_{IH} = V_{DD}/2$ maximum for noise immunity and 4.3 V MARCH tests. 1 MHz cycle.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for devices intended to be marked as radiation hardened. When group E testing is performed, it shall be in accordance with table V of method 5005 of MIL-STD-883 and 4.5.5 herein.

4.4.6 Inspection of packaging. The inspection of packaging shall be as specified in MIL-M-38510.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

NOTE: In order to prevent "latch-up" during device turn-on and also prevent a high initial operating current (I_{DDOP}), set all device terminals equal to V_{SS}. Raise V_{DD} and $\overline{CE}$ simultaneously to normal system operating V_{DD}. Do not allow V_{IH} at $\overline{CE}$ to exceed V_{DD} +0.3 volts while rising. Not necessary for SOS products.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown, and electrical test procedure. When devices are measured at +25°C following application of the steady state life or burn-in test condition, all devices shall be cooled to +35°C prior to removal of bias voltages. Any electrical tests required shall first be performed at -55°C or +25°C prior to any +125°C tests that are required.

4.5.3 Delta measurements. Delta measurements, as specified in table II, shall be made and recorded before and after the required burn-in screens and steady state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IV.

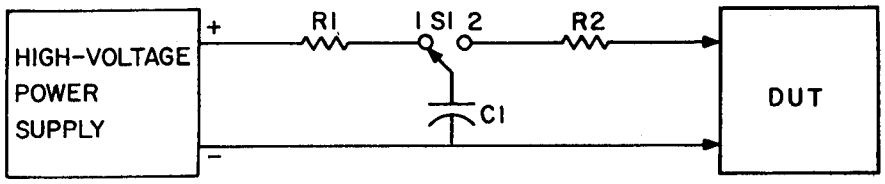
TABLE IV. Delta limits at +25°C.

Parameters 1/	Limits			
	01, 02	03	04	05, 06
I_{DD}	+5 μA	±15 μA	±25 μA	±30 μA
V_{OL}	±60 mV	±60 mV	±60 mV	
V_{OH}	±200 mV	±400 mV	±400 mV	
I_{OL}, I_{OH}				±10%
I_{OHZ}, I_{OLZ}				±500 nA
I_{IL}, I_{IH}	+50 nA	±100 nA	±100 nA	

1/ Conditions and mechanization of measurements shall be as specified in table III, subgroup 1.
2/ Delta limits apply to an increase from the initial value (e.g., pre-life test I_{IH} = -120 nA, post-life test I_{IH} = -170 nA).

4.5.4 High voltage (V_{ZAP}) test of input protection circuits. All input terminals (up to a maximum of 4) of the devices under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V. This destructive test shall be conducted as follows using the test circuit on figure 8:

a. Measure I_{IL} and I_{IH} at the inputs selected, as stated above, at +25°C. The test limit for each input tested shall be ±1 μA of all pins at V_{DD} = 5.5 V. Measure I_{SS} on (DUT) at +25°C. The test limit for this measurement shall be increased a maximum of 20 percent of the specified I_{SS} table III limit at V_{DD} = 5.5 V dc.



V_{ZAP} = 400 V minimum charge on C1.
10 MΩ ≤ R1 ≤ 50 MΩ.
R2 = 1.5 kΩ ±5%
C1 = 100 pF ±20%
S1 = Hg-wetted "bounceless" relay.

FIGURE 8. High voltage (V_{ZAP}) test circuit.

b. V_{ZAP} is applied to the DUT in the following modes (see table V) by charging C1 to V_{ZAP} with S1 in position 1 and then switching to position 2.

TABLE V. Modes for high-voltage test.

Mode	+ Terminal	-Terminal
1	V_{DD}	Input
2	Input	V_{SS}

c. Within 24 hours repeat the I_{SS}, I_{IH} and I_{IL} measurements on the same terminal as performed above. If a DUT exhibits leakage currents in excess of the specified limits after the V_{ZAP} test, it shall be classified as a failure.

4.5.5 Radiation hardness assurance (RHA) testing. The RHA testing shall be performed in accordance with procedures and sampling specified in table V of method 5005 of MIL-STD-883 and herein:

a. Before irradiation, selected samples shall be assembled in qualified packages and pass the governing electrical parameters (group A, subgroup 1 at +25°C).

b. Radiation exposure shall be performed according to method 1019 of MIL-STD-883 with the devices biased per table VII and meet the end-point electrical parameters as defined in table VI at +25°C after exposure.

c. Bias may be interrupted for up to 1 minute to remove devices to remote bias fixture. The start and completion of the end-point electrical parameter measurements shall not exceed 1 hour following irradiation.

4.5.6 Quiescent supply current test. When performing quiescent supply current measurements, the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the contract or purchase order, a copy of the following data, as applicable, shall be supplied:

a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and steady state life test.

b. A copy of each radiograph.

c. The quality conformance inspection data (see 4.4).

d. Parameter distribution data on parameters evaluated during burn-in.

e. Final electrical parameters data.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

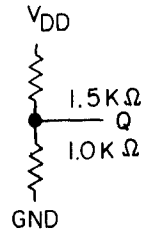
TABLE VI. Group E end-point electrical parameter limits for RHA devices.

Test	Symbol	Conditions V_{SS} = 0 V, T_C = +25°C		Device type	Limits Min	Limits Max	Unit
Low level output voltage	V_{OL}	V_{DD} = 4.5 V	I_{OL} = 2 mA	03, 04		0.4	V
Output low drive current	I_{OL}	V_{DD} = 4.75 V	V_{OUT} = 0.4 V	05	2.5		mA
				06	1.7		
High level output voltage	V_{OH}	V_{DD} = 4.5 V	I_{OH} - -1 mA	03, 04	2.4		V
Output high drive current	I_{OH}	V_{DD} = 4.75 V	V_{OUT} = 4.35 V	05	2.0		mA
				06	1.1		
Input leakage current	I_{IH} I_{IL}	V_{DD} = 5.5 V	V_{IN} = rail	03, 04		±1	µA
		V_{DD} = 5.25 V	V_{IN} = rail	05, 06		±10	
High impedance output leakage	I_{OHZ} I_{OLZ}	V_{DD} = 5.5 V	V_{OUT} = rail	03, 04		±10	µA
		V_{DD} = 5.25 V	V_{OUT} = rail	05		±30	
				06		±50	
Quiescent supply current	I_{DD}	V_{DD} = 5.5 V		03		200	µA
				04		250	
	I_{SS}	V_{DD} = 5.25 V		05, 06		1,000	
Operating current	I_{DDOP}	V_{DD} = 5.5 V	f = 1 MHz	03, 04		7	mA
		V_{DD} = 5.25 V	f = 1 MHz	05		4	
				06		6	
Address access time	t_{AVQV}	See table III		03, 04		320	ns
				05, 06		250	
Read or write cycle time	t_{ELEL}	See table III		03, 04		420	ns
	t_{AVAV}	See table III		05, 06		250	
Data retention quiescent supply current	I_{CCDR}	V_{DD} = 3 V		03, 04		100	µA
		V_{DD} = 2.5 V		05		400	
				06		500	

TABLE VII. Bias during exposure to radiation.

Device type	Pin connections		
	V_{DD} (through a 1 kΩ to 60 kΩ resistor)	V_{SS} = GND	V_{DD} = 5 V dc
03	1, 2, 3, 4, 5, 6, 7*, 8, 10, 11, 12, 13, 14, 15, 16, 17	9	18
04	1, 2, 3, 4, 5, 6, 7, 8, 10, 11*, 12*, 13*, 14*, 15, 16, 17	9	18
05	1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17	9	18
06	1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17	9	18

* Output pins connected to voltage divider.



6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. Acquisition documents should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special lead lengths or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_I - - - - - - - - - - - - - - *Input capacitance.*

I_{DD} I_{SS} - - - - - - - - - - - Quiescent supply current.

I_{DDOP} - - - - - - - - - - - - Operating supply current.

I_I - - - - - - - - - - - - - - Input leakage current.

I_{OH} - - - - - - - - - - - - - Logical high output current.

I_{OL} - - - - - - - - - - - - - Logical low output current.

I_{OZ} - - - - - - - - - - - - - Output leakage current.

V_{DD} - - - - - - - - - - - - - Supply voltage.

V_{DDR} - - - - - - - - - - - - - Data retention supply voltage.

V_{IH} - - - - - - - - - - - - - Logical high input voltage.

V_{IL} - - - - - - - - - - - - - Logical low input voltage.

V_{OH} - - - - - - - - - - - - - Logical high output voltage.

V_{OL} - - - - - - - - - - - - - Logical low output voltage.

t_{AVEL} - - - - - - - - - - - - Address setup time.

t_{AVQV} - - - - - - - - - - - - Address access time.

t_{AVWH} - - - - - - - - - - - - Address to end of write setup time.

t_{AVWL} - - - - - - - - - - - - Address setup to start of write time.

t_{DVEL} - - - - - - - - - - - - *Write data setup time*

t_{DVWH} - - - - - - - - - - - - Data setup time.

t_{ELQV} - - - - - - - - - - - - Chip enable access time.

t_{WHEL} - - - - - - - - - - - - Write enable high to chip enable low

t_{WLEL} - - - - - - - - - - - - Write enable pulse setup time to chip enable.

t_{ELQX} - - - - - - - - - - - - Chip enable output enable time.

t_{WLQZ} - - - - - - - - - - - - Write enable output disable time.

t_{EHQZ} - - - - - - - - - - - - Chip enable output disable time.

t_{EHWH} - - - - - - - - - - - - Output high-Z time.

t_{ELDX} - - - - - - - - - - - - Write data hold time

t_{QVWL} - - - - - - - - - - - - Data valid to write time.

t_{ELEH} - - - - - - - - - - - - Chip enable pulse negative width.

t_{EHEL} - - - - - - - - - - - - - Chip enable pulse positive width.

t_{ELAX} - - - - - - - - - - - - - Address hold time.

t_{WLWH} - - - - - - - - - - - - - Write enable pulse negative width.

t_{WLEH} - - - - - - - - - - - - - Write enable pulse setup time to chip enable.

t_{ELWH} - - - - - - - - - - - - - Write enable pulse hold time from chip enable.

t_{WHDX} - - - - - - - - - - - - - Data hold time.

t_{ELEL} - - - - - - - - - - - - - Read or write cycle time.

6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

```
                                                    t
                                                      X   X   X   X
                                                      |   |   |   |
                                                      |   |   |   |
Signal name from which interval is defined____________|   |   |   |
                                                          |   |   |
Transition direction for first signal_____________________|   |   |
                                                              |   |
Signal name to which interval is defined__________________________|   |
                                                                      |
Transition direction for second signal________________________________|
```

a. Signal definitions:

A = Address

D = Data in

Q = Data out

W = Write enable

E = Chip enable

S = Chip select

G = Output enable

b. Transition definitions:

H = Transition to high

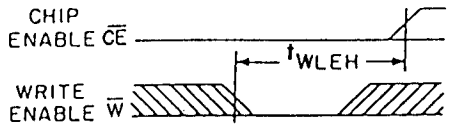
L = Transition to low

V = Transition to valid

X = Transition to invalid or don't care

Z = Transition to off (high impedance)

EXAMPLE:



The example shows write pulse setup time defined as t_{WLEH}-time from write enable low to chip enable high.

c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d. Waveforms:

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer lead lengths and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	6504
02	6514
03	6504RH
04	6514RH
05	CMM5104
06	CMM5114

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static build-up. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment and tools.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive foam, or carriers.

e. The uses of plastic, rubber, or silk in MOS areas should be avoided.

f. Relative humidity should be maintained above 50 percent, if practical.

g. Operator should be grounded when handling devices.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access (RAM) memory. Each algorithm serves a specific purpose for testing the different modes of operation of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A.

30.1.1 GALPAT.

a. Write a background pattern of 0's throughout memory.

b. Write a 1 (test bit) at the first location.

c. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location.

d. Move the test bit to second location and repeat the sequence in step c.

e. Repeat the sequence until each cell is used as test bit location.

f. Repeat steps b through e with a background pattern of 1's throughout memory.

30.2 Algorithm B.

30.2.1 CHECKERBOARD.

a. Write 0 and 1 alternately in the first or even row.

b. Write 1 and 0 alternately in the second or odd row.

c. Repeat steps a and b through all rows.

d. Read 0 and 1 alternately in the first or even row.

e. Read 1 and 0 alternately in the second or odd row.

f. Repeat steps d and e through all rows.

g. Repeat steps a through f with complement data.

30.3 Algorithm C.

30.3.1 ADDCOMP.

a. Write a true checkerboard throughout the memory.

b. Verify each location by the address sequence: address, address complement, address, address +1, etc.

c. Read out data pattern from memory.

30.4 Algorithm D.

30.4.1 MARCH.

a. i = address 0 to 1023.

b. Write 0's into all address locations.

c. Starting at cell 0, read a 0, write a 1, read a 1.

d. Address sequence: i, i+1, i+2 ---i+n ($1 \leq n \leq 1023$) (T = 0).

e. Starting at cell 1023, read a 1, write a 0, read a 0.

f. Address sequence: i, i-1, i-2, ---i-n ($1 \leq n \leq 1023$) (T = 1023).

g. Repeat with opposite data.

30.5 Algorithm E.

30.5.1 MASEST.

a. i = address 0 to 1023.

b. Write alternating pattern 101010 --- into all cells.

c. Read cell i+n, go to cell i+n, and read the complement of cell i+n.

d. Address sequence i, $\overline{i}$, i+1, $\overline{i+1}$, ---1+n, $\overline{i+n}$ ($0 \leq n \leq 1023$) (i = 0).

e. Repeat steps b and c with the complement checkerboard pattern.

30.6 Algorithm F.

30.6.1 DISTURB.

a. Write 1's into all memory locations.

b. Read all 1's.

c. Disable write as follows: Make $\overline{CS} = V_{DD}$.

d. Attempt to write 0's into all memory locations.

e. Read all 1's to verify original data.

f. Repeat with opposite data.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-0993)

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