

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, NMOS, 262,144 BIT DYNAMIC
RANDOM ACCESS MEMORY (DRAM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, NMOS, 262,144/1-bit, dynamic random access memory. Two product assurance classes, two electrical performance categories, two refresh mode options, and two case styles are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510 and as specified herein.

1.2.1 Device types. The device types shall be as shown in the following:

Device type	Device organization	Temperature range (case)	Access time	CAS before RAS refresh	Refresh
01	262,144/1-bit RAM	-55°C to +110°C <u>1/</u>	120 ns	No	2 ms
02	262,144/1-bit RAM	-55°C to +110°C <u>1/</u>	150 ns	No	2 ms
03	262,144/1-bit RAM	-55°C to +110°C <u>1/</u>	120 ns	Yes	2 ms
04	262,144/1-bit RAM	-55°C to +110°C <u>1/</u>	150 ns	Yes	2 ms

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 0.250" x 0.875"), dual-in-line package
X	(18-terminal, 0.285" x 0.495"), chip carrier (see figure 1)

1/ See initialization in 6.4.1

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3 Absolute maximum ratings. 2/

Voltage on any pin relative to V_{SS}	-1.5 V to +7.0 V
Storage temperature range (ambient)	-65°C to +150°C
Power dissipation (minimum cycle time)	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J) 3/	+150°C
Short circuit output current	50 mA
Thermal resistance (minimum cycle time):	
Case E	See MIL-M-38510, appendix C
Case X	$\theta_{JC} = 60^\circ\text{C/W}$ 4/

1.3.1 Alpha particle induced error rate. The error rate shall not exceed 9.16×10^{-11} errors per bit-day at sea level, under the following test conditions:

- a. $V_{CC} = 4.5$ V.
- b. $T_C = +25^\circ\text{C}$.
- c. Data pattern = checkerboard.
- d. Cycle time = 250 ns.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Power supply and signal reference (V_{SS}) 5/	0.0 V dc
High level input voltage: all inputs (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Low level input voltage: all inputs (V_{IL})	-1.5 V dc minimum to +0.8 V dc maximum
Refresh cycle time (t_{REFSH})	2.0 ms
Operating case temperature range (T_C)	-55°C to +110°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

- 2/ Operation at maximum rating for extended periods of time will impair the reliability of the device.
- 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 4/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
- 5/ V_{SS} is common for all supply voltages.

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be as specified in 1.2.3 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Truth table. The truth table shall be as specified on figure 4.

3.2.4.1 Functional tests. The functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, then alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.2.5 Die overcoat. All devices supplied under this specification shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. Polyimide and silicone coatings are allowed as an overcoat on the die for alpha particle protection provided each lot (i.e., polyimide and silicone coating lot) shall be subjected to and pass the internal moisture content test. The internal moisture content after completion of all screening shall not exceed 5,000 ppm at +100°C.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.5 herein.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 46 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

TABLE I. Electrical performance characteristics.

Characteristic	Symbol	Conditions $-55^{\circ}\text{C} < T_C < +110^{\circ}\text{C}$ ^{1/2/}	Device	Limits		Unit
				Min	Max	
Supply current from V_{CC} (active) ^{3/}	I_{CC1}	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling $t_{RL2RL2} = 220 \text{ ns}$ $t_{RL2RL2} = 260 \text{ ns}$	01, 03 02, 04		90 90	mA mA
Supply current from V_{CC} (standby)	I_{CC2}	$\overline{\text{RAS}}$ and $\overline{\text{CAS}} = V_{IH}$	A11		10	mA
Supply current from V_{CC} (refresh) ^{3/}	I_{CC3}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} = V_{IH}$ $t_{RL2RL2} = 220 \text{ ns}$ $t_{RL2RL2} = 260 \text{ ns}$	01, 03 02, 04		80 80	mA mA
Output high voltage	V_{OH}	$I_{OH} = -5 \text{ mA}$	A11	2.4	V_{CC}	V
Output low voltage	V_{OL}	$I_{OL} = 4 \text{ mA}$	A11		0.4	V
Input leakage	I_{IH} I_{IL}	$V_{IN} = 0.0 \text{ V to } 6.5 \text{ V}$	A11	-10	10	μA
Output leakage	I_{OZ}	$\overline{\text{RAS}}$ and $\overline{\text{CAS}} = V_{IH}$ $V_{OUT} = V_{SS} \text{ to } V_{CC}$	A11	-10	10	μA
Input capacitance address ($A_0 - A_8$)	C_{IN1}		A11		7	pF
Input capacitance Clk ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, V_{IN})	C_{IN2}		A11		10	pF
Output capacitance	C_{OUT}		A11		8	pF
Random read or write cycle time	t_{RL2RL2}	See figures 6 through 11	01, 03 02, 04	220 260	10,000 10,000	ns ns
Read-modify-write or read-write cycle time	t_{RL2RL2}	See figure 9	01, 03 02, 04	260 310	10,000 10,000	ns ns
Access time from $\overline{\text{RAS}}$ ^{3/}	t_{RL1QV}	See figures 6, 7, 9	01, 03 02, 04		120 150	ns ns
Access time from $\overline{\text{CAS}}$ ^{3/}	t_{CL1QV}	See figures 6, 7, 9	01, 03 02, 04		60 75	ns ns
$\overline{\text{RAS}}$ pulse width	t_{RL1RH1}	See figures 7 through 11	01, 03 02, 04	120 150	10,000 10,000	ns ns
$\overline{\text{CAS}}$ pulse width	t_{CL1CH1}	See figures 7, 8, 9	01, 03 02, 04	60 75	10,000 10,000	ns ns

See footnotes at end of table.

TABLE 1. Electrical performance characteristics - Continued.

Characteristic	Symbol	Conditions $55^{\circ}\text{C} \leq T_C \leq +110^{\circ}\text{C}$	1/2/ Device	Limits		Unit
				Min	Max	
$\overline{\text{RAS}}$ precharge time	t_{RH2RL2}	See figures 7 through 11	01, 03 02, 04	90 100		ns ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge	t_{CH2RL2}	See figures 7 through 9	A11	20		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t_{RL1CL1}	See figures 7 through 9	01, 03 02, 04	30 30	60 75	ns ns
$\overline{\text{RAS}}$ hold time	t_{CL1RH1}	See figures 7 through 9	01, 03 02, 04	60 75		ns ns
$\overline{\text{CAS}}$ hold time	t_{RL1CH1}	See figures 7 through 9	01, 03 02, 04	120 150		ns ns
Row address setup time	t_{AVRL2}	See figures 7 through 10	A11	0		ns
Row address hold time	t_{RL1AX}	See figures 7 through 10	A11	^{4/} 20		ns
Column address setup time	t_{AVCL2}	See figures 7 through 9	A11	0		ns
Column address hold time	t_{CL1AX}	See figures 7 through 9	A11	30		ns
Read command setup	t_{WH2AV}	See figure 9	A11	0		ns
Read command hold (referenced to $\overline{\text{CAS}}$)	t_{CH2WL2}	See figure 7	A11	0		ns
Read command hold (referenced to $\overline{\text{RAS}}$)	t_{RH2WL2}	See figure 7	01, 03 02, 04	20 25		ns ns
Output disable delay	t_{CH2QX}	See figures 6, 7, 9, and 11	A11		40	ns
Write command setup	t_{WL1CL2}	See figure 8	A11	0		ns
Write command hold (referenced to $\overline{\text{CAS}}$)	t_{CL1WH1}	See figure 8	01, 03 02, 04	40 45		ns ns
Write command hold (referenced to $\overline{\text{RAS}}$)	t_{RL1WH1}	See figure 8	01, 03 02, 04	100 120		ns ns
WRITE pulse width	t_{WL1WH1}	See figures 8 and 9	01, 03 02, 04	40 45		ns ns
WRITE to $\overline{\text{RAS}}$ lead	t_{WL1RH1}	See figures 8 and 9	01, 03 02, 04	40 45		ns ns
WRITE to $\overline{\text{CAS}}$ lead	t_{WL1CH1}	See figures 8 and 9	01, 03 02, 04	40 45		ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristic	Symbol	Conditions $55^{\circ}\text{C} \leq T_C \leq +110^{\circ}\text{C}$ ^{1/2/}	Device	Limits		Unit
				Min	Max	
Data-in setup time	t _{DVCL2}	See figure 8	A11	0		ns
Data-in hold time	t _{CL1DX}	See figure 8	01, 03 02, 04	40 45		ns ns
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	t _{CL1WL2}	See figure 9	01, 03 02, 04	50 60		ns ns
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	t _{RL1WL2}	See figure 9	01, 03 02, 04	110 135		ns ns
Refresh $\overline{\text{CAS}}$ setup time	t _{CL1RL2}	See figure 11	03 04	25 30		ns ns
Refresh CAS hold time	t _{RL1CH1}	See figure 11	03 04	25 30		ns ns
Data-in setup time (referenced to $\overline{\text{WRITE}}$)	t _{DVWL2}	See figure 9	A11	0		ns
Data-in hold time (referenced to $\overline{\text{WRITE}}$)	t _{WL1DX}	See figure 9	01, 03 02, 04	40 45		ns ns
Refresh precharge to $\overline{\text{CAS}}$ time	t _{RH2CL2}	See figure 11	03 04	20 20		ns ns
Refresh $\overline{\text{CAS}}$ precharge time	t _{CH2CL2}	See figure 11	03 04	25 30		ns ns
Refresh period	t _{RFSH}		A11		2	ms
Transition time (rise and fall for RAS and CAS)	t _T		A11	3	50	ns

- 1/ Complete terminal conditions shall be as specified on table III.
 2/ AC characteristics assume transition times (t_T) = 5 ns.
 3/ Output load = one Schottky TTL and 100 pF to V_{SS} or equivalent.
 4/ For hidden refresh cycles t_{RL1AX} minimum = 100 ns.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	2, 10	2, 10
Final electrical test parameters (method 5005)	1, 2*, 3, 9, 10*, 11	1, 2*, 3, 10*, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 9, 10, 11	1, 2, 3, 4, 10, 11
Group B test requirements (method 5005, subgroup 5)	1, 2, 3, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3, 10, 11
Group D end-point electrical parameters (method 5005)	1, 2, 3, 10, 11	1, 2, 3, 10, 11

^a The PDA applies to subgroup 2 and tests 38 and 41 of subgroup 10, except use pattern 15, "Up Down March" as the test algorithm and use time set T05, nominal timing in place of the requirements as indicated in Note 11 of table III (see 4.2d).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. When the alternate screening option of method 5004 of MIL-STD-883 is applied to class B, the following additional items are applicable:
 - (1) Burn-in duration for class B shall be 160 hours minimum. The burn-in table listed in MIL-STD-883, method 1015 may be substituted for this requirement.
 - (2) The following voltage stress test may be used to satisfy the alternate screening qualifications of method 5004 of MIL-STD-883. This voltage stress test shall be added to the screening procedure after seal and before the interim electrical screen on method 5004. This voltage stress condition is shown on figure 5, (same as burn-in, or equivalent) with the following voltage modifications:
 - (a) $V_{CC} = 7.0$ V minimum.
 - (b) $T_A = +125^{\circ}\text{C}$ minimum for 12 hours minimum, or alternately $T_A = +140^{\circ}\text{C}$ minimum for 8 hours minimum.
- b. Burn-in (method 1015 of MIL-STD-883);
 - (1) Test condition D or E, using the circuits shown on figure 5, options A or B, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$ minimum.

- c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- d. The percent defective allowable (PDA) shall be 2.5 percent for initial burn-in and 1.5 percent for reburn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device type may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein.
- b. Subgroups 5, 6, 7, and 8 for class S and subgroups 5, 6, 7, 8, and 9 for class B, of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect capacitance. Perform C_{IN1} , C_{IN2} , and C_{OUT} parameter measurements to table I limits.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II, method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein.
- b. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 5 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III, method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Soft error rate (method 1032 of MIL-STD-883) shall be performed only for initial qualification and after process or design changes which may affect soft error rate. System testing to be performed using conditions stated in 1.3.1. Accumulate 10^6 device hours minimum for the specified generic device type. Note: As an alternate a manufacturer may submit a plan that contains an accelerated technique that can be demonstrated to show that the soft error rate requirement will be met.

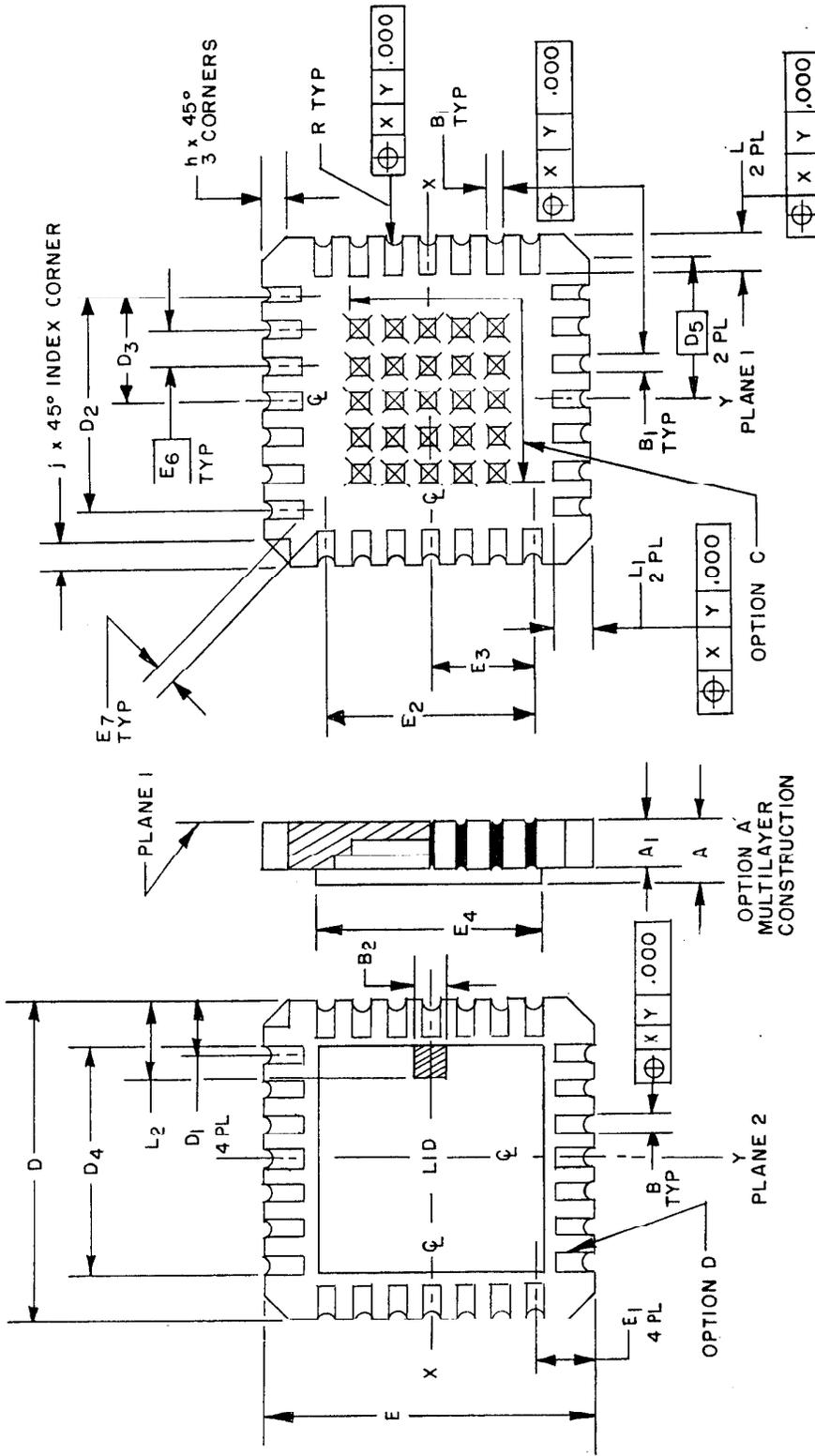


FIGURE 1. Case outline X (18 terminal, 0.285 x 0.495 chip carrier).

Symbol	Dimensions shown in				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.060	.100	1.52	2.54	11
A ₁	.050	.088	1.27	2.24	
A ₂	--	--	--	--	
B	--	--	--	--	
B ₁	.022	.028	.560	.710	7
B ₂	.022	.041	.560	1.04	9
D	.280	.305	7.11	7.75	
D ₁	.070 REF		1.91 REF		
D ₂	.150 REF		3.81 REF		
D ₃	.075 BSC		1.78 BSC		
D ₄	-	.305	-	7.75	8
D ₅	.120 BSC		3.05 BSC		
E	.480	.505	12.19	12.83	
E ₁	.145 REF		3.68 REF		
E ₂	.200 REF		5.08 REF		
E ₃	.100 REF		2.54 REF		
E ₄	-	.365	-	9.27	8
E ₅	-		-		
E ₆	.050 BSC		1.27 BSC		
E ₇	.015	-	.380	-	4
h	.035	.045	.890	1.14	17
j	.010	.025	.380	1.640	17
L	.040	.060	1.02	1.40	
L ₁	.110	.142	2.79	3.10	
L ₂	.040	.155	1.02	3.94	9
N	18		18		5
R	.007	.011	1.80	1.280	3
IND	4		4		5
NE	5		5		5

FIGURE 1. Case outline X (18 terminal, 0.285 x 0.495 chip carrier) - Continued.

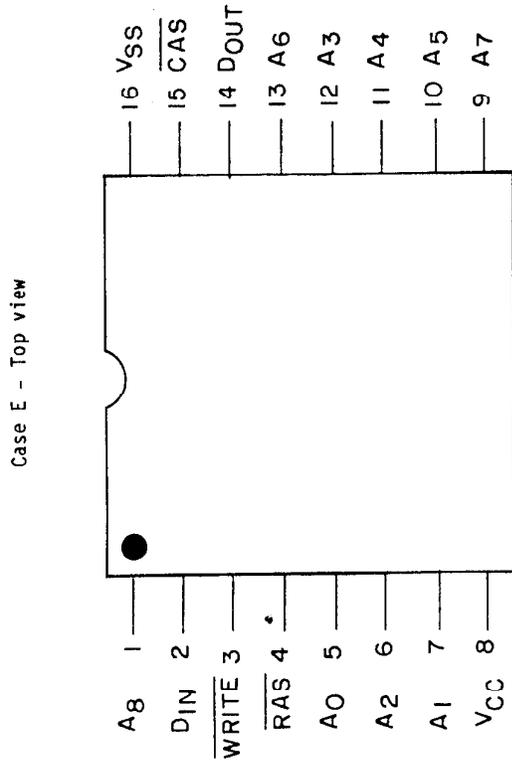
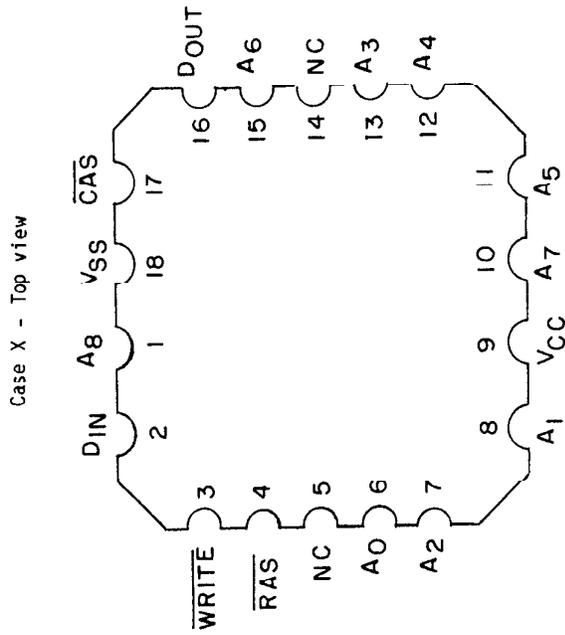
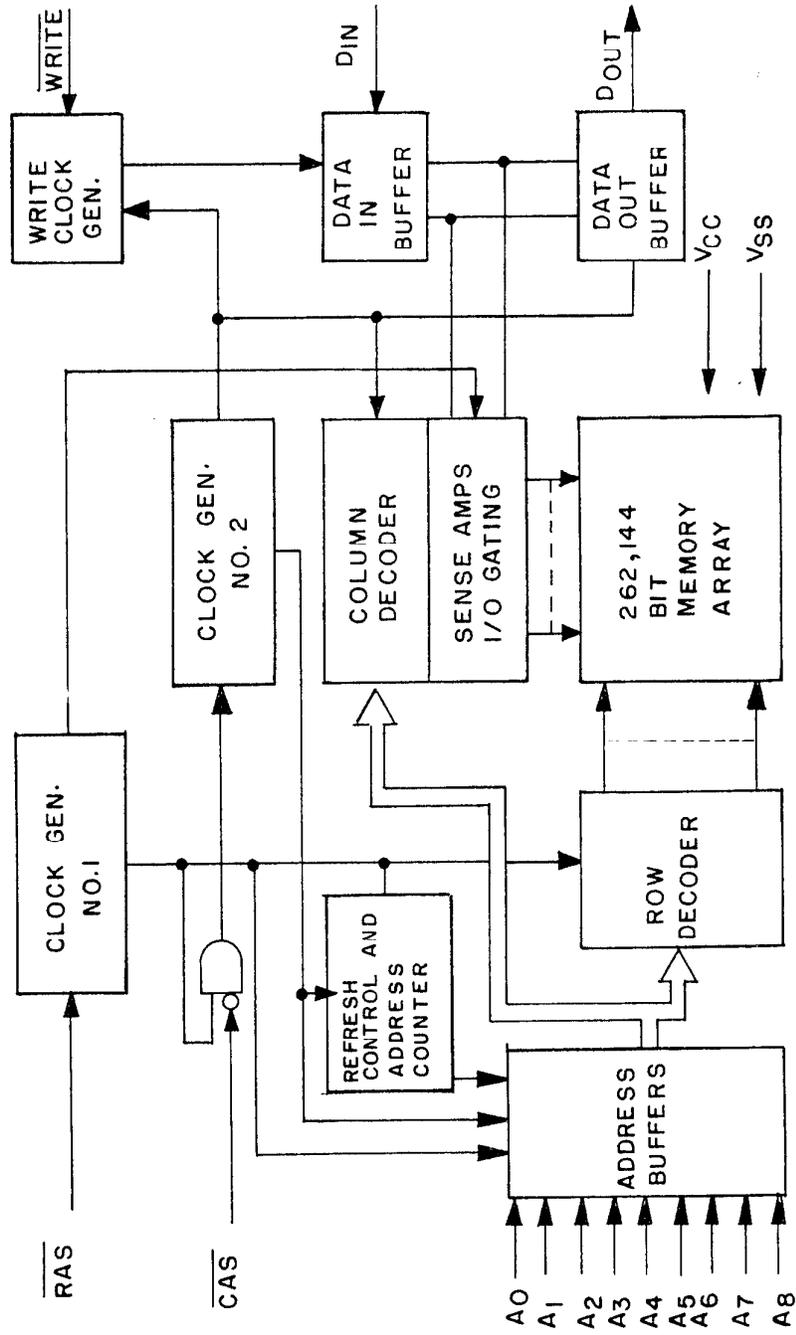


FIGURE 2. Terminal connections.



Clock no. 2 connected to "Refresh control and address counter" for device types 03 and 04 for circuit A..

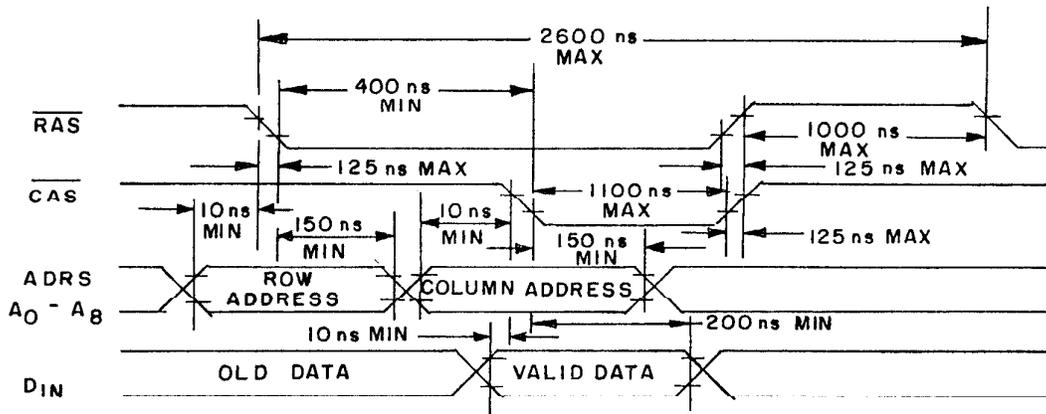
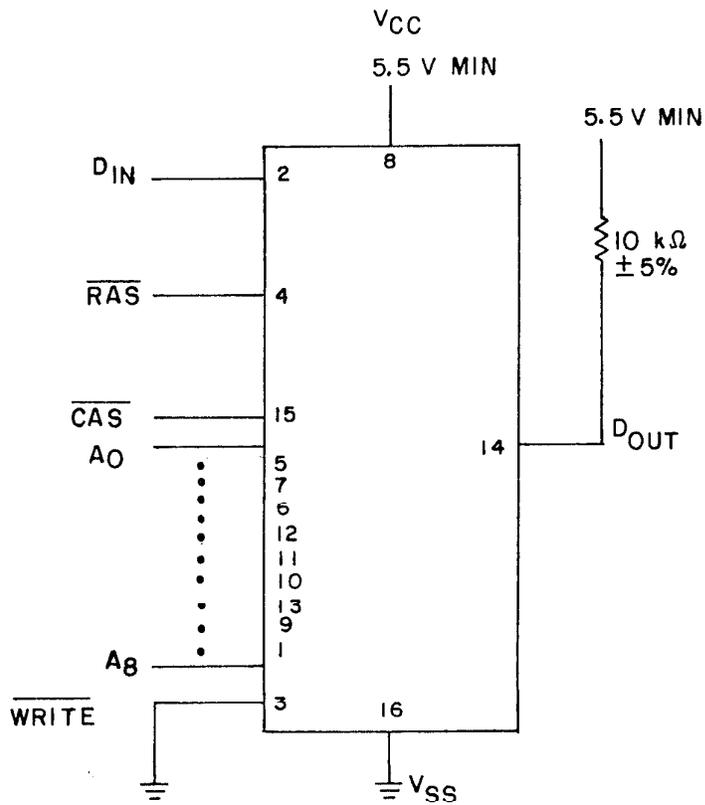
FIGURE 3. Functional block diagram.

Truth table						
Operation <u>1/</u>	Inputs <u>2/</u>				Write	Output
	RAS	CAS	DIN	A0-A8		
Deselected	H	H	X	X	X	High-Z
Write 'L' to cell A(xy) <u>3/</u>	L	L	L	A(xy)	L	High-Z ^{4/}
Write 'H' to cell A(xy)	L	L	H	A(xy)	L	High-Z ^{4/}
Read cell A(xy)	L	L	X	A(xy)	H	Data (xy)
RAS-Only-Refresh	L	H	X	A(x) ^{5/}	X	High-Z
Hidden-Refresh <u>6/</u>	L	L	X	A(x)	H	Data A(x-n, y-n)
CAS before RAS refresh <u>7/</u>	L	L	X	X	H	High-Z <u>8/</u>

- 1/ A 500 μ s pause is required after power-up, followed by 8 RAS cycles before any truth table function.
- 2/ 'X' = Valid high or valid low.
- 3/ A (xy) denotes proper address logic to address cell A(xy)
- 4/ For 'Early Write' timing, data-out remains at high impedance. For 'Late Write' timing, data out is valid from access time until CAS goes to a high level.
- 5/ A (x) depends only on A0-A7; A8 is either valid high or valid low.
- 6/ When CAS = VIL, the data output will contain data from the last valid read cycle (i. e. N cycles before).
- 7/ Refresh row address is automatically incremented at the end of each CAS before RAS cycle. Applies to device types 03 and 04 only.
- 8/ Output will not be "high-Z" if CAS before RAS is entered after a hidden refresh without CAS recovery.

FIGURE 4. Truth table.

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NOTES: Measurement points are V_{IL} and V_{IH}
 A_0-A_8 = Binary count LSB-MSB
 t_{RISE} = 125 ns maximum
 t_{FALL} = 125 ns maximum

FIGURE 5. Burn-in and steady state life test circuit.

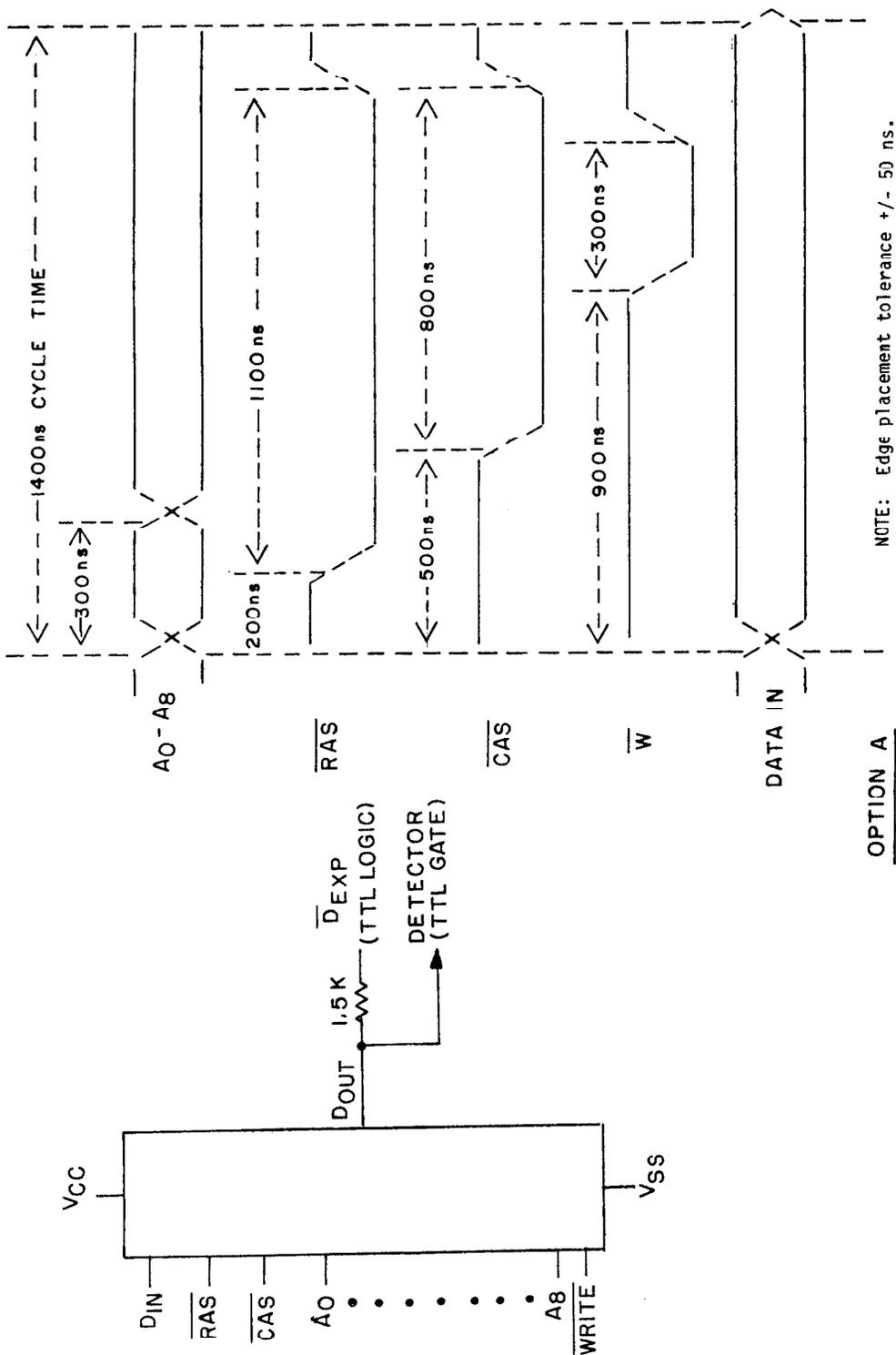


FIGURE 5. Alternative burn-in and steady-state life test circuits. - continued.

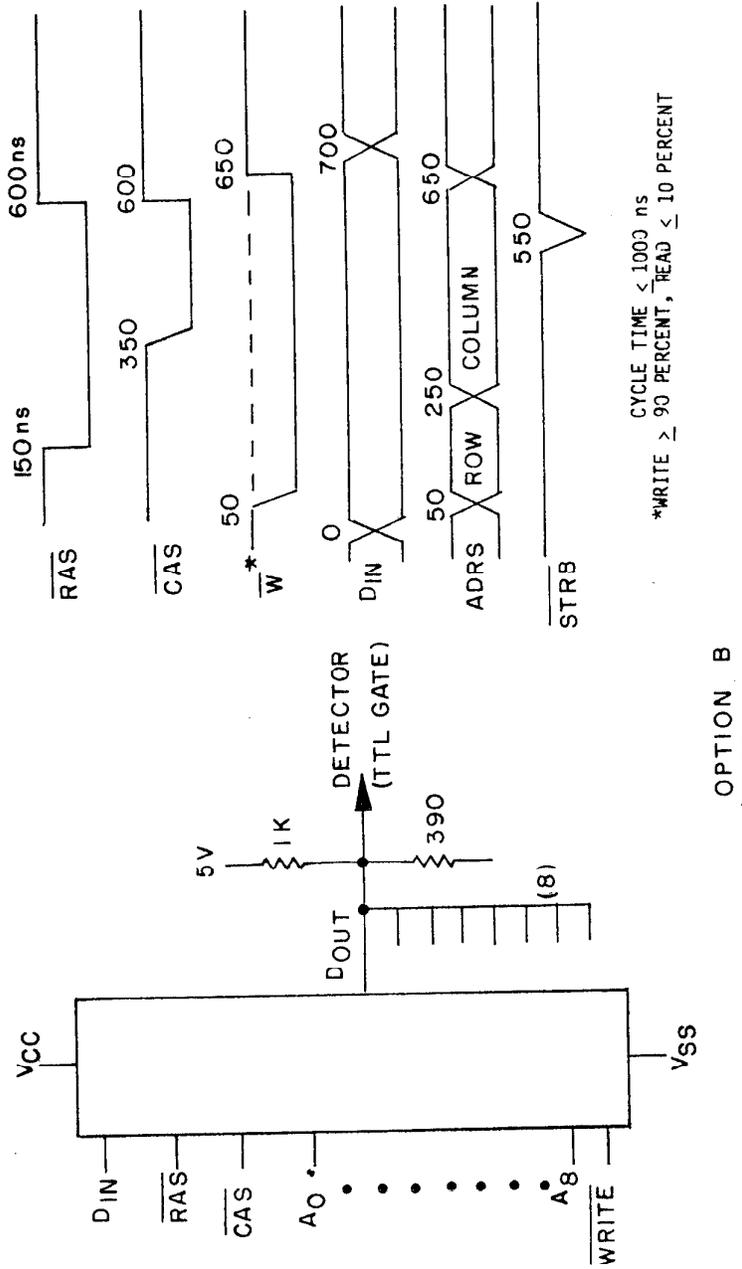
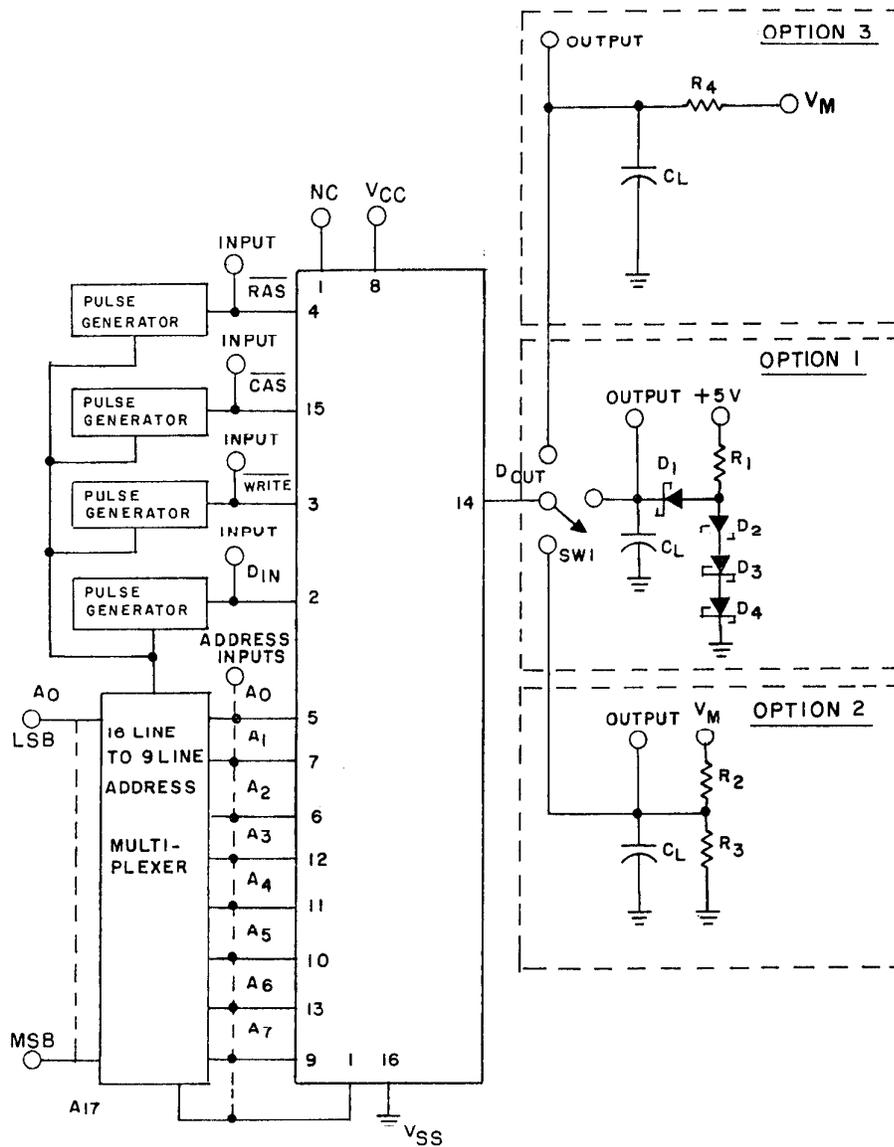


FIGURE 5. Alternative burn-in and steady-state life test circuits - Continued.



NOTES:

1. $C_L = 100$ pF min-(includes scope probe, wiring, and stray wiring without package in test fixture).
2. D1-D4 are 1N3064 or equivalent.
3. All generators t_{PLH} and $t_{PHL} \leq 10$ ns.
4. All resistors are 1/2 watt.
5. Option 1 or option 2 load circuit may be used for all A C tests except the high impedance test, where option 2 shall be used.
6. SW₁ is a software switch.
7. Option conditions are: $V_M = 5.0$ V, $R_2 = 910\Omega \pm 5$ percent, $R_3 = 320\Omega \pm 5$ percent.
8. Option 1 conditions are: $R_1 = 2.8$ k $\Omega \pm 1$ percent.
9. Option 3 conditions are: $V_M = 1.3$ V, $R_4 = 220\Omega \pm 5$ percent.

FIGURE 6. Switching time test circuit.

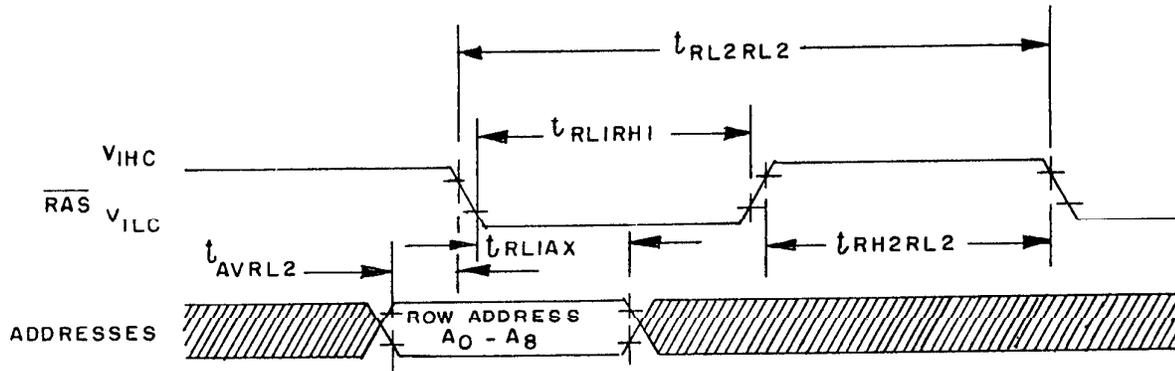


FIGURE 10. RAS-only refresh cycle waveforms.

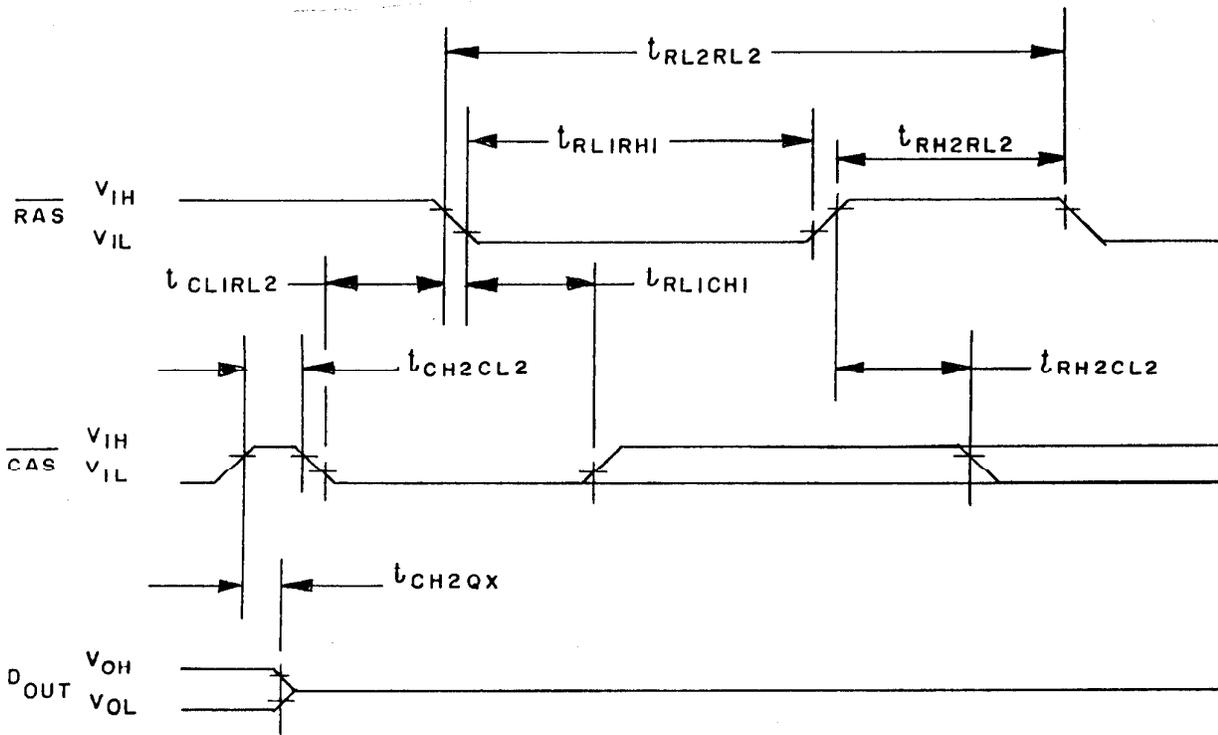


FIGURE 11. CAS before RAS refresh cycle waveforms.

TABLE IVa. Timing sets for device types 01 and 03.

Parameter symbol	T01	T02	T03	T04	T05	T06	T07	T08
t _{RL2RL2}	220	220		260	300	260	280	220
t _{RL1QV} (max)	120	120			150		150	120
t _{CL1QV} (max)		60	60	100	80			
t _{CH2QX}							0	
t _{CH2QX} (max)						30		
t _{RH2RL2}	90			120	120	100	100	90
t _{RL1RH1}		120		160				
t _{RL1RH1} (max)							12,000	
t _{CL1RH1}		60						
t _{RL1CH1}		120						
t _{CL1CH1}		60		100	150			
t _{CL1CH1} (max)							12,000	
t _{RL1CL1}	25			60	70	30	30	35
t _{CH2RL2}	0					0		
t _{AVRL2}	0	0	0		0	0		
t _{RL1AX}		15	15		40			
t _{AVCL2}	0	0	0	0	10	0	0	0
t _{CL1AX}			20					
t _{RL1CAX}		90						
t _{WH2CL2}				0				
t _{CH2WL2}				0				
t _{RH2WL2}				10				
t _{CL1WH1}		20			100			95
t _{RL1WH1}	95	80				95		
t _{WL1WH1}			20				45	
t _{WL1RH1}			30				70	
t _{WL1CH1}			30					
t _{DVCL2}	0	0		0	10	0		0
t _{CL1DX}		20		25	100			95
t _{RL1DX}	95	80				95		
t _{WL1CL2}	0	0			10	0		
Read/modify/write								
t _{RL2RL2}			260					
t _{CL1WL2}			30					
t _{RL1WL2}			100					
t _{WL1DX}			20				45	
t _{DVWL2}			0				0	
CAS before RAS refresh								
t _{CL1RL2}								10
t _{RL1CH1}								25
t _{RH2CL2}								0
t _{CH2CL2}								25
	RAS Access	CAS Access	R-M-W	Read Timing	Nominal Time	Q Turnoff	Long Cycle	CAS Before RAS

TABLE IVb. Timing sets for device types 02 and 04.

Parameter symbol	T01	T02	T03	T04	T05	T06	T07	T08
t _{RL2RL2}	260	260		260	300	260	280	260
t _{RL1QV} (max)	150		150		150		150	150
t _{CL1QV} (max)		75	75	100	80			
t _{CH2QX}							0	
t _{CH2QX} (max)						30		
t _{RH2RL2}	100			120	120	100	100	100
t _{RL1RH1}		150		160				
t _{RL1RH1} (max)							12,000	
t _{CL1RH1}		75						
t _{RL1CH1}		150						
t _{CL1CH1}		75		100	150			
t _{CL1CH1} (max)							12,000	
t _{RL1CL1}	25			60	70	30	30	40
t _{CH2RL2}	0					0		
t _{AVRL2}	0	0	0		0	0		
t _{RL1AX}		15	15		40			
t _{AVCL2}	0	0	0	0	10	0	0	0
t _{CL1AX}			25					
t _{RL1CAX}		105						
t _{WH2CL2}				0				
t _{CH2WL2}				0				
t _{KH2WL2}				10				
t _{CL1WH1}		25			100			95
t _{RL1WH1}	95					95		
t _{WL1WH1}			25				45	
t _{WL1RH1}			45				70	
t _{WL1CH1}			40					
t _{DVCL2}	0	0		0	10	0		0
t _{CL1DX}		25		25	100			95
t _{RL1DX}	95					95		
t _{WL1CL2}	0	0			10	0		
Read/modify/write								
t _{RL2RL2}			310					
t _{CL1WL2}			35					
t _{RL1WL2}			125					
t _{WL1DX}			20				45	
t _{DVWL2}			0				0	
CAS before RAS refresh								
t _{CL1RL2}								10
t _{RL1CH1}								30
t _{RH2CL2}								0
t _{CH2CL2}								30
	RAS Access	CAS Access	R-M-W	Read Timing	Nominal Time	Q Turnoff	Long Cycle	CAS Before RAS

c. Steady state life test (method 1005 of MIL-STD-883) conditions:

- (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
- (2) $T_A = +125^\circ\text{C}$ minimum.
- (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

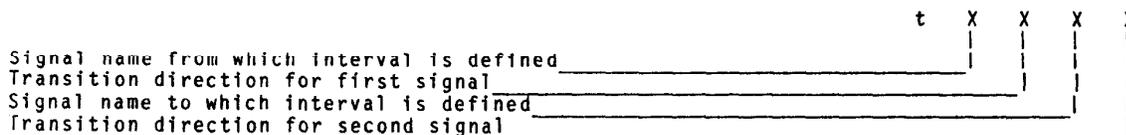
6.2 Ordering data. Acquisition documents should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

VCC	- - - - -	Supply voltage.
VSS	- - - - -	Common or reference voltage.
RAS	- - - - -	Row address strobe input.
CAS	- - - - -	Column address strobe input.
WRITE (W)	- - - - -	Read/write input.
DI	- - - - -	Data input.
DO	- - - - -	Data output.
A ₀ -A ₈ , ADDR, ADRS	- - - - -	Address input.
LSB	- - - - -	Least significant address bit.
MSB	- - - - -	Most significant address bit.
NC	- - - - -	No connect.
TS number	- - - - -	Timing set number.

6.3.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:



a. Signal definitions:

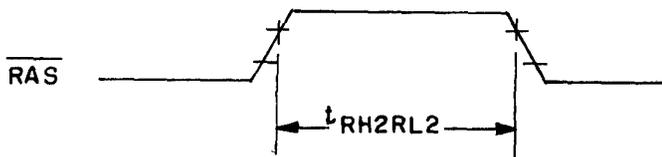
- A = Address
- D = Data in
- Q = Data out
- W = Write enable
- E = Chip enable
- O = Output enable
- P = Supply current
- R = Usually abbreviation for "Read", however, in the case of dynamic memories "R" stands for RAS.

b. Transition definitions:

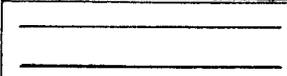
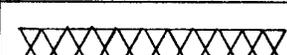
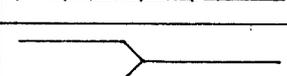
- H = Transition to high
- L = Transition to low
- V = Transition to valid
- X = Transition to invalid
- Z = Transition to off (high impedance)
- U = Up
- N = Down

A "1" (lower) and "2" (upper) are used, where appropriate to indicate position on a drop or rise.

Example:



- c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.
- d. Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	MUST BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DONT CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
		HIGH IMPEDANCE

6.4 Application and operation guidelines.

6.4.1 Initialization. The device requires a 500 μ s pause and eight pump cycles after power up before it will operate properly. Any cycle that performs refresh may be used for a pump cycle.

6.4.2 Addressing. Addressing 1 of 262,144 (2^{18}) cells requires handling an 18-bit address word. This is accomplished with minimum pin count by multiplexing two 9-bit address fields onto the nine address inputs (A_0 - A_8). The two fields are brought on chip in succession by the high to low transition of the row address and column address strobes (RAS , CAS) which activate internal timing generators and latch the address information on chip for decoding.

6.4.3 Read operation. When a valid row address is presented to the address inputs, the row address strobe (RAS) can fall and thereby clock the row address into the address latches. After a row address hold time (t_{RL1AX}), the column address can be presented to the device and the column address strobe (CAS) can fall to latch the column address onto the chip. The $WRITE$ input is held at a logic "1" (high) level. The output is in the high impedance state and will remain in that state until access time. At access time it will turn on and assume the appropriate level ("1" to "0"). A feature referred to as "Gated CAS" is simply a delayed internal signal that is gated with the external CAS signal which causes the on chip CAS clock to occur at a fixed internal after RAS . This allows CAS to become active (low) any time after row address hold time (t_{RL1AX}) has been satisfied but before the maximum RAS to CAS delay time (t_{RL1CL1}) without affecting access time referenced to RAS (t_{RL1QV}). CAS can occur later than (t_{RL1CL1}) maximum without affecting device operation but access time will be controlled exclusively by CAS which is access time referenced to CAS (t_{CL1QV}).

6.4.4 Write operation. The same procedure applies for latching the address information on chip that was explained for the read operation. Data can be written into the device in several ways. In all cases, however, writing is accomplished by the following edge of $\overline{\text{CAS}}$ or $\overline{\text{WRITE}}$ (while $\overline{\text{RAS}}$ is low) whichever occurs latest. Data is latched onto the chip.

- a. Early write: Data-In and $\overline{\text{WRITE}}$ precede the fall of $\overline{\text{CAS}}$ by a setup time (t_{DVCL2}) and (t_{WL1CL2}), respectively and remain valid for a hold time (t_{CL1DX}) and (t_{CL1WH1}). The setup and hold times are with respect to the falling edge of $\overline{\text{CAS}}$. Data-Out remains in the high impedance state for the entire cycle.
- b. Late write: The fall of $\overline{\text{WRITE}}$ occurs after Data-In and $\overline{\text{CAS}}$ by a specified time ($\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay (t_{CL1WL2}). Data-In setup and hold times are referenced to the fall of $\overline{\text{WRITE}}$. Data-Out will contain data from the selected cell at access time. If the fall of $\overline{\text{WRITE}}$ occurs prior to the $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay limit, the state of the Data-Out pin is indeterminate.

6.4.5 Refresh operations. The basic device constraint is that no cell shall be refreshed at intervals exceeding 2.0 milliseconds. There are 512 cells along each row in the storage matrix and there are 512 such rows. A refresh cycle refreshes 512 cells in each of two rows simultaneously. A row address 256 cycle "burst" every 2.0 milliseconds or a single distributed cycle every 7.812 microseconds at each of the first 256 row addresses (i.e., A₀-A₇; A₈ is a don't care but should be either a valid high or a valid low) will accomplish complete memory refreshing. A refresh cycle can be accomplished in three ways. Any normal read, write, or read-modify-write cycle, a $\overline{\text{RAS}}$ -only refresh cycle, or a $\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh cycle will accomplish refresh. The $\overline{\text{RAS}}$ -only and $\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh modes require less power than a standard $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle. The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ further simplifies refresh by eliminating the need for externally applied addresses.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver to any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>	<u>Circuit designator</u>	<u>Symbol/CAGE number</u>
01	M41256P-12/AT&T	A	CFRU/98739 6Y440
01	MT1257-12/Micron Technology	B	
02	M41256P-15/AT&T	A	---
02	MT1257-15/Micron Technology	B	---
03	M41256N-12/AT&T	A	---
03	MT1259-12/Micron Technology	B	---
04	M41256N-15/AT&T	A	---
04	MT1259-15/Micron Technology	B	---

6.7 Handling. MOS devices should be handled with certain precautions to avoid damage ~~due to~~ the accumulation of static charge. Input protection circuitry has been designed into the device to minimize the effect of this static build-up. However, the following handling practices are recommended.

- a. Devices should be handled on benches with conductive and grounded surfaces.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam or carriers.
- e. The use of plastic, rubber, or silk in MOS areas should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

10.1.1 Step 1. Step 1 of all algorithms may be performed initially and if testing is continuous (no dead time exceeding .2 ms between tests), step 1 does not have to be repeated for each algorithm.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (Pattern 1).30.1.1 Continuous read, data backgrounds = all "0".

This pattern is used to allow the maximum amount of current I_{CC} to be drawn from the V_{CC} power supply. It is performed in the following manner with normal cycle timing:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data.
- Step 3 Sequentially read entire memory.
- Step 4 Repeat step 3 as many times as necessary to achieve a reading.

30.2 Algorithm B (Pattern 2).30.2.1 Output high impedance (t_{off}).

This pattern verifies the output buffer switches to high impedance (tri-state) within the specified 40 ns after the rise of CAS . It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load minimum address with "0".
- Step 3 Read minimum address location and measure V_{OL} .
- Step 4 Raise CAS and measure $V_{OUT} \geq V_{OL} + 0.5$ V after 40 ns delay.
- Step 5 Load minimum address location with "1".
- Step 6 Read minimum address location and measure V_{OH} .
- Step 7 Raise CAS and measure $V_{OUT} \leq V_{OH} - 0.5$ V after 40 ns delay.

30.3 Algorithm C (Pattern 3).30.3.1 V_{BUMP}/V_{BOBBLE} data background = all "0" (discharged state).

This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Pause 40 μ s to 2 ms ramping V_{CC} to 4.5 V inhibiting all clocks.
- Step 3 Load memory with background data.
- Step 4 Pause 40 μ s to 2 ms ramping V_{CC} to 5.5 V inhibiting all clocks.
- Step 5 Read memory with background data.
- Step 6 Repeat steps 2 through 5 for background data complement.
- Step 7 Load memory with background data.
- Step 8 Pause 40 μ s to 2 ms ramping V_{CC} to 4.5 V inhibiting all clocks.
- Step 9 Read memory with background data.
- Step 10 Pause 40 μ s to 2 ms ramping V_{CC} to 5.5 V inhibiting all clocks.
- Step 11 Repeat steps 7 through 9 for background data complement.

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30.4 Algorithm D (Pattern 4).30.4.1 Address complement, data background = all "0".

This pattern produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data.
- Step 3 Read minimum address location.
- Step 4 Load minimum address location with "1".
- Step 5 Read maximum address location.
- Step 6 Load maximum address location with "1".
- Step 7 Read minimum address location +1.
- Step 8 Load minimum address location +1 with "1".
- Step 9 Read maximum address location -1.
- Step 10 Load maximum address location -1 with "1".
- Step 11 Repeat steps 3 through 10 until all address locations have been read and loaded with "1"s.
- Step 12 Repeat steps 3 through 11 reading "1"s and loading "0"s.
- Step 13 Read memory, all "0"s.

30.5 Algorithm E (Pattern 5).30.5.1 Marching columns, initial data background = all "0".

This pattern is a good test for sense line imbalance and response plus restore noise in addition to multiple selection. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with data background.
- Step 3 Write test column complement.
- Step 4 Read test column complement.
- Step 5 Write test columns true.
- Step 6 Repeat 3 through 6 for all columns sequentially.
- Step 7 Write background data to "1".
- Step 8 Write test column complement.
- Step 9 Read test column complement.
- Step 10 Write test columns true.
- Step 11 Repeat 8 through 10 for all columns sequentially.

30.6 Algorithm F (Pattern 6).30.6.1 March data, data background = all "0".

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data.
- Step 3 Read location 0.
- Step 4 Write data complement in location 0.
- Step 5 Read data complement in location 0.
- Step 6 Repeat steps 3 through 5 for all other locations in memory (sequentially).
- Step 7 Read data complement at minimum location.
- Step 8 Write data at minimum location.
- Step 9 Read data at minimum location.
- Step 10 Repeat steps 7 through 9 for all other locations in the memory (sequentially).
- Step 11 Repeat steps 2 through 10 with data background of all "1".

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30.7 Algorithm G (Pattern 7).30.7.1 Static refresh (periphery retention).

This pattern tests for periphery retention time by attempting to write after a lengthy pause. This test is performed at +110°C (case) only, and is not used to measure the retention time of the memory cells but to insure that the periphery circuits will hold for at least 2 ms. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with all "0"s.
- Step 3 Read memory, all "0"s.
- Step 4 Pause (stop all clocks) 2 ms.
- Step 5 Load memory with all "1"s.
- Step 6 Read memory, all "1"s.
- Step 7 Pause (stop all clocks) 2 ms.
- Step 8 Load memory with all "0"s.
- Step 9 Read memory, all "0"s.

30.8 Algorithm H (Pattern 8).30.8.1 Refresh test (cell retention).

This test is used to check the retention time of memory cells under static and dynamic conditions. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with all "0"s.
- Step 3 Pause 2 ms (stop all clocks).
- Step 4 Read memory, all "0"s.
- Step 5 Repeat steps 2 through 4 with all "1"s.
- Step 6 Read minimum address location.
- Step 7 Read maximum address location.
- Step 8 Repeat steps 6 and 7 for 2 ms.
- Step 9 Read memory, all "1"s.
- Step 10 Load memory, all "0"s.
- Step 11 Repeat steps 6 through 9 with all "0"s.
- Step 12 Read address location 131071.
- Step 13 Read address location 131072.
- Step 14 Repeat steps 12 and 13 for 2 ms.
- Step 15 Read memory, all "0"s.
- Step 16 Load memory, all "1"s.
- Step 17 Repeat steps 12 through 15 with all "1"s.

30.9 Algorithm I (Pattern 9).30.9.1 Extended cycle test (10 μ s), data background = X-bar.

This test is used to verify the 10 μ s maximum limit on $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ pulse widths. Front and back edge timing is held to normal cycle timing while the cycle is increased to allow 10 μ s of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active time (low level). It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Write data in location 0.
- Step 3 Read data in location 0.
- Step 4 Repeat steps 2 and 3 for all other locations in the memory (sequentially).
- Step 5 Repeat steps 2 through 4 with complement data.

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30.10 Algorithm J (Pattern 10).30.10.1 RAS-only refresh test.

This test is used to verify the functionality of the RAS-only mode of cell refreshing. It is done at +110°C only and is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with all "0"s.
- Step 3 Pause 2 ms ($\overline{\text{CAS}} = \overline{\text{RAS}} = \overline{\text{WE}} = V_{IH}$).
- Step 4 Perform 256 RAS-only cycles ($\overline{\text{CAS}} = \overline{\text{WE}} = V_{IH}$).
- Step 5 Repeat steps 3 and 4 for 250 ms.
- Step 6 Read memory, all "0"s.
- Step 7 Repeat steps 2 through 6 with all "1"s.

30.11 Algorithm K (Pattern 11).30.11.1 Read-modify-write (RMW), data background = all "0".

This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data.
- Step 3 Read minimum address location and load with "1" using RMW cycle.
- Step 4 Read maximum address location and load with "1" using RMW cycle.
- Step 5 Read minimum address location +1 and load with "1" using RMW cycle.
- Step 6 Read maximum address location -1 and load with "1" using RMW cycle.
- Step 7 Repeat steps 3 through 6 until all address locations have been read and loaded with "1".
- Step 8 Repeat steps 3 through 7 reading "1"s and loading "0"s.
- Step 9 Read memory, all "0"s.

30.12 Algorithm L (Pattern 12).30.12.1 CAS-before-RAS refresh test.

This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +110°C only and is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with all "0"s.
- Step 3 Pause 2 ms ($\overline{\text{CAS}} = \overline{\text{RAS}} = \overline{\text{WE}} = V_{IH}$).
- Step 4 Perform 256 CAS-before-RAS cycles.
- Step 5 Repeat steps 3 and 4 for 250 ms.
- Step 6 Read memory, all "0"s.
- Step 7 Repeat steps 2 through 6 with all "1"s.

30.13 Algorithm M (optional pattern 13, see note 1, table III).30.13.1 Output high impedance (t_{off}).

- Q test (Hi-Z output test)
- 1 Perform 8 pump cycles.
- 2 Write the entire memory to a background of all "0"s using a row fast address sequence.
- 3 Go to row and column address 0.
- 4 a. Perform a read (ignore data) followed by a write complement. Verify that the output is in the Hi-Z state during the write cycle by making the expect data the same as the write input data.
- b. Increment both the row and column address by one.
- 5 Repeat step 3 until the row and column addresses reach 511.
- 6 Repeat steps 2 through 5 with complement input and expect data.

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30.14 Algorithm N (optional pattern 14, see note 1, table III).30.14.1 Shifting 1 and 4 sparse matrix with hold time.

This pattern produces a pattern of minority bits surrounded by majority bits, and tests for sense amplifier imbalance, data-dependent response time effects, and internally-generated noise sensitivity. It also includes cell retention time to further test the memory array. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load location 0 with a "1".
- Step 3 Load the next 4 sequential locations with a "0".
- Step 4 Repeat steps 2 and 3 for all other locations in memory.
- Step 5 Pause 2 ms (stop all clocks).
- Step 6 Read the data in the entire memory.
- Step 7 Repeat steps 2 through 6, 4 more times, incrementing the starting row address by 1 each time.
- Step 8 Repeat steps 2 through 7 with complement data.

30.15 Algorithm O (optional pattern 15, see note 1, table III).

30.15.1 Up-down march, data background = all "0". This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data.
- Step 3 Read data in location 0. Do not change the address.
- Step 4 Write data complement in location 0. Increment the address.
- Step 5 Repeat steps 3 and 4 for all other locations in memory (sequentially). At the completion of this step, the memory will be loaded with all "1"s.
- Step 6 Read data complement in location 0. Do not change the address.
- Step 7 Write data in location 0. Increment the address.
- Step 8 Repeat steps 6 and 7 for all other locations in memory (sequentially). At the completion of this step, the memory will be returned to all "0" data.
- Step 9 Repeat steps 3 through 8, except decrement the address in steps 4 and 7 instead of incrementing it.

30.16 Algorithm P (optional pattern 16, see note 1, table III).30.16.1 Long cycle dual diagonal, data background = all "0".

This test is used to verify the 10 μ s maximum limit on $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ pulse widths. The background is loaded using normal cycles, while only the major diagonals are accessed with the extended 10 μ s cycle, which uses minimum RAS precharge time and a very late WRITE to test timing margins and address decoder malfunction. It is performed in the following manner:

- Step 1 Perform 8 pump cycles.
- Step 2 Load memory with background data using normal cycles.
- Step 3 Read data in location 0, writing complement data using the extended cycle.
- Step 4 Repeat step 3, incrementing both the row and column address, until the entire diagonal has been accessed. Perform a 256-cycle burst RAS-only refresh every 2 ms.
- Step 5 Read the memory, with background data everywhere but the major diagonal, using normal cycles.
- Step 6 Restore the diagonal to background data using normal cycles.
- Step 7 Read data in the minimum row and maximum column address, and write complement data using the extended cycle.
- Step 8 Repeat step 7, incrementing the row and decrementing the column address until this diagonal has been accessed. Perform a 256-cycle burst RAS-only refresh, every 2 ms.
- Step 9 Read the memory, with background data everywhere but the diagonal described in step 8, using normal cycles.
- Step 10 Repeat steps 2 through 9 with complement data.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SP, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-0879)