

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS, 512 X 9 BIT,
FIRST IN - FIRST OUT DUAL PORT MEMORY (FIFO), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, first in - first out dual port memory microcircuits. One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit organization	Access time
01	512/9 - bit FIFO	120 ns
02	512/9 - bit FIFO	100 ns
03	512/9 - bit FIFO	80 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
Y	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line package
Z	C-12 (32-terminal, .450" x .450"), leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 Vdc
Voltage on any pin (referenced to ground)	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Maximum junction temperature (T_J) ^{1/}	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Y	°C/W
Case Z	°C/W

1.4 Recommended operating conditions.

Supply voltage: V_{CC}	4.5 V dc minimum to 5.5 V dc maximum
V_{SS}	GND
Minimum high-level input voltage (V_{IH})	2.0 V dc (2.4 V dc at -55°C)
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

^{1/} Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and pin assignments. The terminal connections and pin assignments shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Functional description, terms, and symbols. The functional description, pin definitions, and expansion modes shall be specified in 6.3.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group 105 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C T_C \leq +125°C <math>v_{cc} 10\%<="" 5.0\text{="" =="" \pm="" math="" v}=""> unless otherwise specified</math>v_{cc}>	Device type	Limits		Unit
				Min	Max	
Output high voltage	V_{OH}	$I_{OH} = -1.0\text{ mA}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$ at +25, +125 $V_{IH} = 2.4\text{ V}$ at -55. $V_{CC} = 4.5\text{ V}$	A11	2.7 <u>1/</u>		V
Output low voltage	V_{OL}	$I_{OL} = 4.0\text{ mA}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$ at +25, +125 $V_{IH} = 2.4\text{ V}$ at -55. $V_{CC} = 4.5\text{ V}$	A11		0.4	V
Input leakage, all inputs	$I_{I(L)(H)}$	$V_{IN} = V_{SS}$ to V_{CC}	A11	-1.0 <u>3/</u>	1.0 <u>3/</u>	μA
Output leakage	$I_{OZ(H,L)}$	$V_{OUT} = V_{SS}$ to V_{CC} $R \geq V_{IH}$	A11	-10	10	μA
Supply current from V_{CC}	I_{CC1} <u>4/</u>	All outputs are open $R_S = V_{IH}$	A11		80 <u>5/</u>	mA
	I_{CC2} <u>4/</u>	All outputs are open Standby ($R = W = R_S = F_L/RT = V_{IH}$)	A11		8 <u>6/</u>	mA
	I_{CC3} <u>4/</u>	All outputs are open Power down (All inputs = $V_{CC} - 0.2\text{ V}$)	A11		1	mA
Input capacitance	C_{IN} <u>7/</u>		A11		7	pF
Output capacitance	C_{OUT} <u>7/</u>	Output buffer is deselected	A11		12	pF
Read cycle time	t_{RC}	$V_{CC} = 4.5\text{ V}$ and 5.5 V <u>8/</u> $C_L = 30\text{ pF}$ See figure 3	01	140		ns
			02	120		ns
			03	100		ns
Access time	t_A		01		120	ns
			02		100	ns
			03		80	ns
Read recovery time	t_{RR}		01	20		ns
			02	20		ns
			03	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Read pulse width	t _{RPW}	V _{CC} = 4.5 V and 5.5 V <u>8/</u> C _L = 30 pF See figure 3	01	120		ns
			02	100		ns
			03	80		ns
Read pulse low to data bus at low Z	t _{RL}		01	10		ns
			02, 03	10		ns
Data valid from read pulse high	t _{DV}		01, 02, 03	5		ns ns
Read pulse high to data bus at high Z	t _{RHZ}		01		35	ns
			02		35	ns
			03		35	ns
Write cycle time	t _{WC}		01	140		ns
			02	120		ns
			03	100		ns
Write pulse width	t _{WPW}		01	120		ns
			02	100		ns
			03	80		ns
Write recovery time	t _{WR}		01	20		ns
			02	20		ns
			03	20		ns
Data setup time	t _{DS}		01	40		ns
			02	35		ns
			03	25		ns
Data hold time	t _{DH}		01, 02, 03	10		ns
Reset cycle time	t _{RSC}		01	140		ns
			02	120		ns
			03	100		ns
Reset pulse width	t _{RS}		01	120		ns
			02	100		ns
			03	80		ns
Reset recovery time	t _{RSR}		01	20		ns
			02	20		ns
			03	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Retransmit cycle time	t _{RTC}	V _{CC} = 4.5 V and 5.5 V 8/ C _L = 30 pF See figure 3	01 02 03		140 120 100	ns ns ns
Retransmit pulse width	t _{RT}		01 02 03	120 100 80		ns ns ns
Retransmit recovery time	t _{RTR}		01 02 03	20 20 20		ns ns ns
Reset to empty flag low	t _{EFL}		01 02 03		140 120 80	ns ns ns
Read low to empty flag low	t _{REF}		01 02 03		115 95 75	ns ns ns
Read high to full flag high	t _{RFF}		01 02 03		110 90 70	ns ns ns
Write high to empty flag high	t _{WEF}		01 02 03		110 90 70	ns ns ns
Write low to full flag low	t _{WFF}		01 02 03		115 95 75	ns ns ns

1/ V_{OH} = 2.4 V, V_{IH} = 2.0 V over entire temperature range for circuit B devices.

2/ I_{OL} = 8.0 mA for circuit B devices.

3/ I_{IL}, I_{IH} = -10 μA and 10 μA respectively for circuit B devices.

4/ I_{CC} measurements are made with EF, FF, and X0 open and XI = V_{IL}.

5/ I_{CC1} = 100 mA maximum for circuit B devices.

6/ I_{CC2} = 15 mA maximum for circuit B devices.

7/ Capacitance measured with Boonton meter or effective capacitance calculated from the equation:

$$C = \frac{I_{\Delta t}}{\Delta V} \text{ with } \Delta V = 3 \text{ V and } V_{CC} = 5.0 \text{ V.}$$

8/ For dynamic tests; V_{IH} = 2.4 V at -55°C and 2.0 V at +25°C and +125°C for circuit A devices, V_{IH} = 2.0 V over entire temperature range for circuit B devices. V_{OL} = <1.2 V, V_{OH} = >2.2 V.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)
	Class B devices
Interim electrical parameters (method 5004)	2, 10*
Final electrical test parameters (method 5004)	2**, 3, 10, 11
Group A test requirements (method 5005)	2, 4***, 10
Group C end-point electrical parameters (method 5005)	2, 10
Group D end-point electrical parameters (method 5005)	2, 10

* Subgroup 8 is encompassed in subgroups 10 and 11.

** PDA applies to subgroup 2 only.

*** Subgroup 4 shall be done once upon qualification or when a device redesign effects input capacitance. Select 5 samples at random and measure 5 terminals of each sample as a minimum (R5, D8, Q1, Q5, and Q7 plus any redesigned pins) with an acceptance number of zero.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883).

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) $T_A = +125^\circ\text{C}$ minimum.

b. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification by extension. Successful qualification of a device type of the faster access time shall also qualify all device types with slower access times without additional qualification testing. At the manufacturer's request these additional device types shall be listed on the QPL.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

Case Y

Device types 01, 02, 03

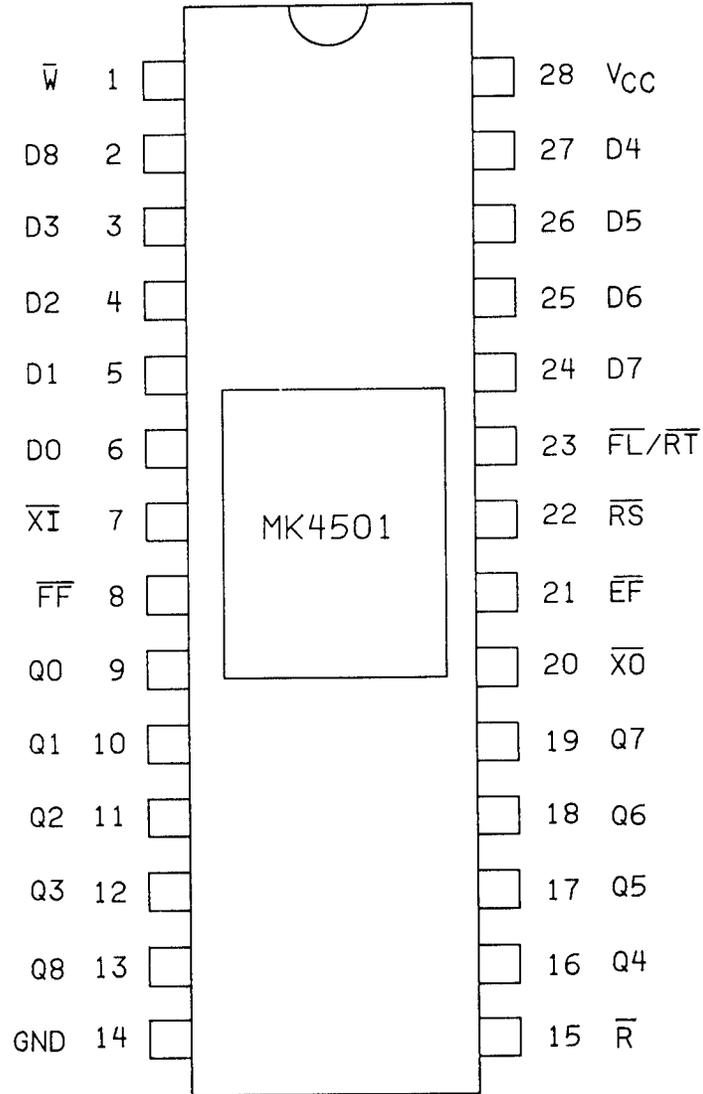


FIGURE 1. Terminal connections and pin assignments.

Case Z

Device types 01, 02, 03

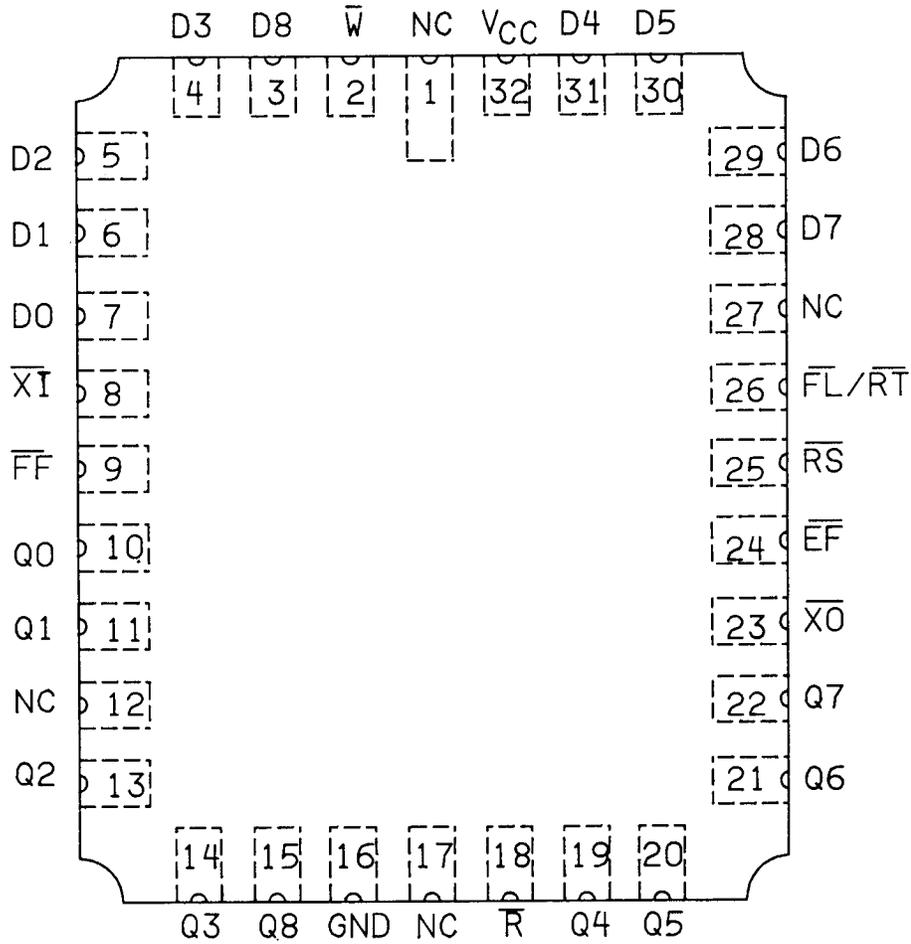


FIGURE 1. Terminal connections and pin assignments - Continued.

Device types 01, 02, 03

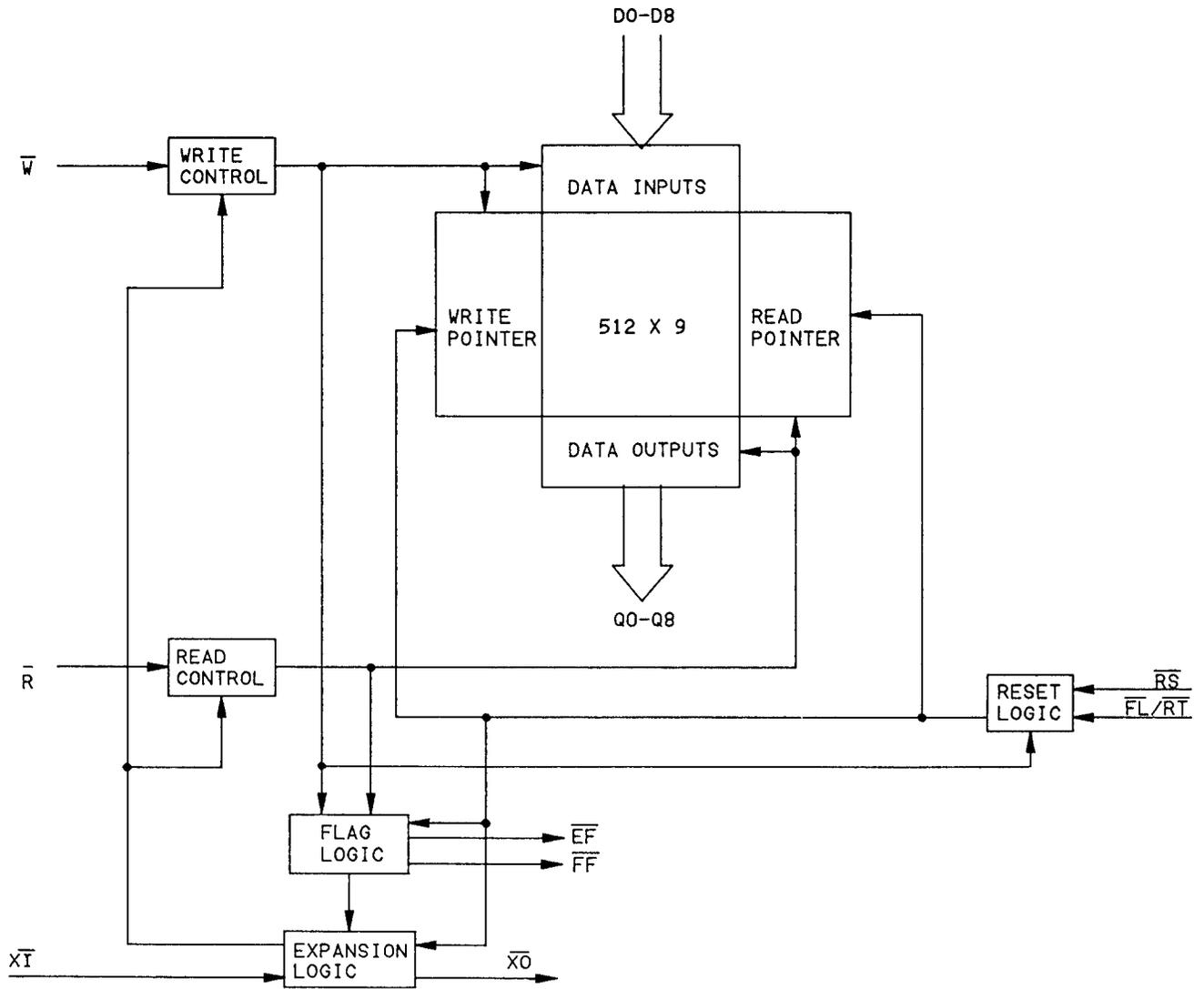
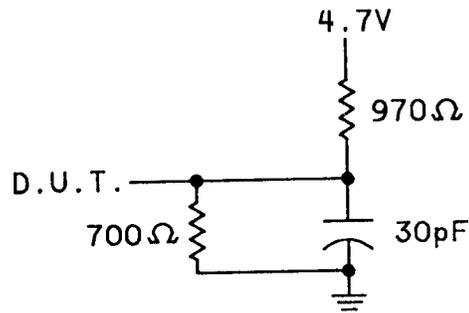


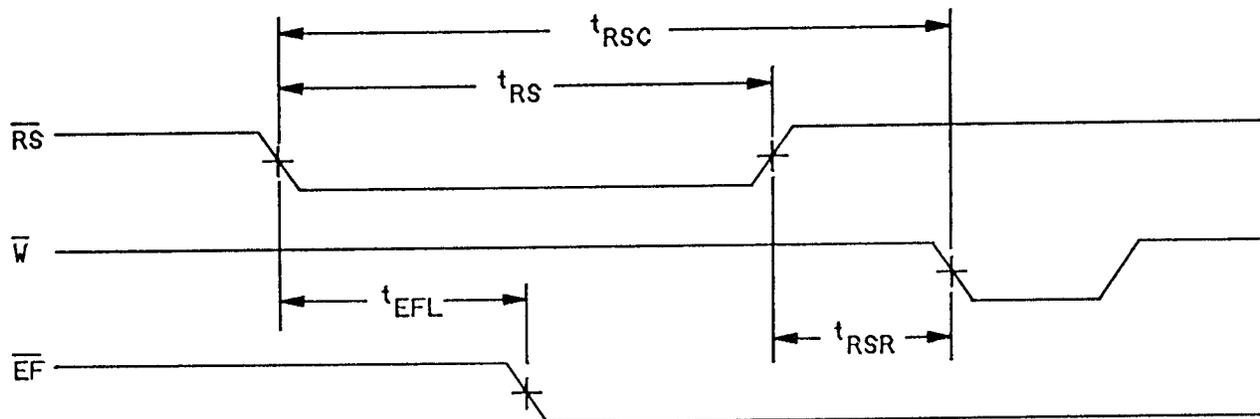
FIGURE 2. Functional block diagram.



NOTE: $C_L = 30 \text{ pF}$ minimum including jig and probe capacitance.

Output Load Circuit

FIGURE 3. Switching time load circuit, test conditions and waveforms.

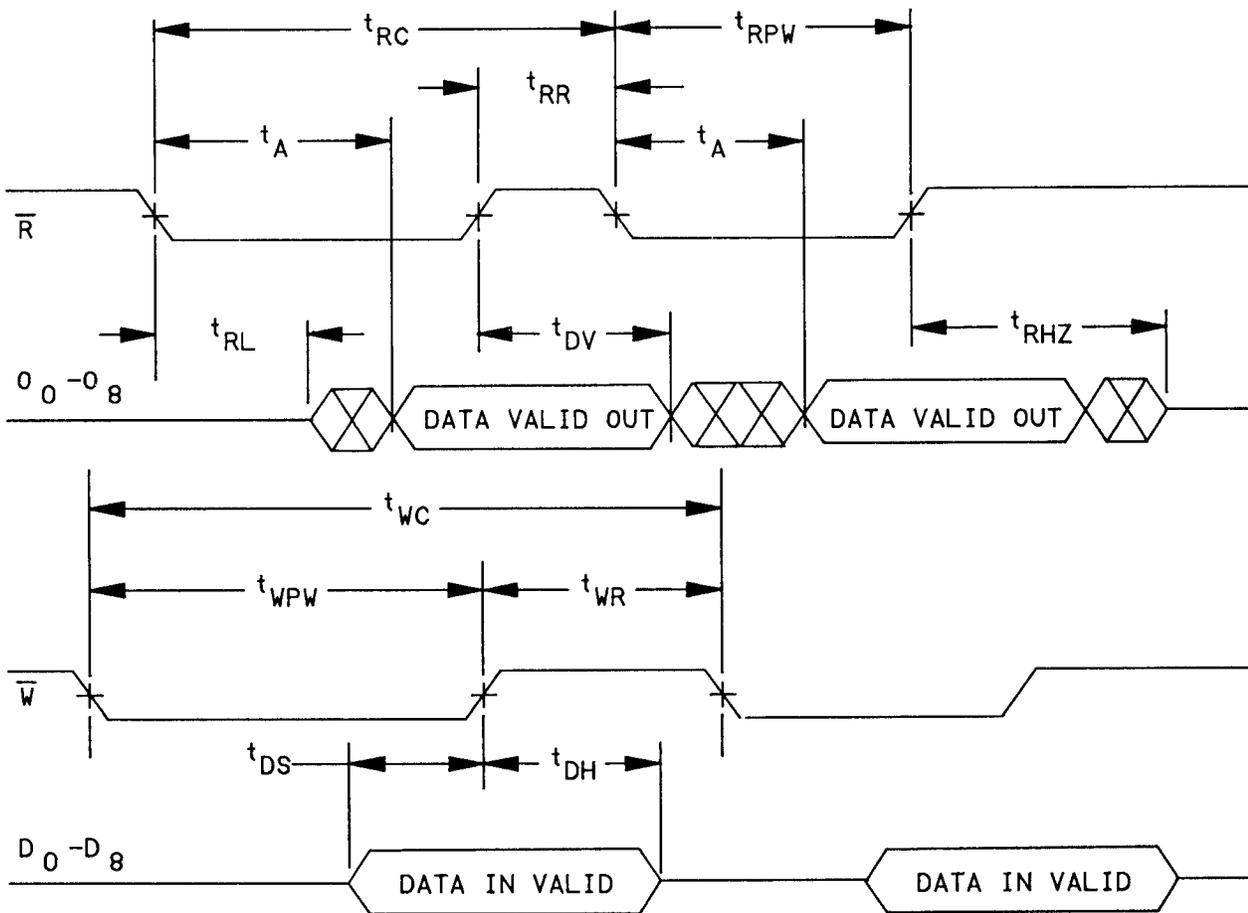


NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. \bar{W} and $R = V_{IH}$ during RESET.
3. For subgroups 10 and 11, $V_{IH} = 2.4 \text{ V}$ @ -55°C and 2.0 V @ $+25^{\circ}\text{C}$ and $+125^{\circ}\text{C}$ for circuit A devices, $V_{IH} = 2.0 \text{ V}$ over entire temperature range for circuit B devices, $V_{IL} = 0.8 \text{ V}$, $V_{OL} = < 1.2 \text{ V}$, $V_{OH} = > 2.2 \text{ V}$.
4. Timing values per table I.

Reset Cycle Timing

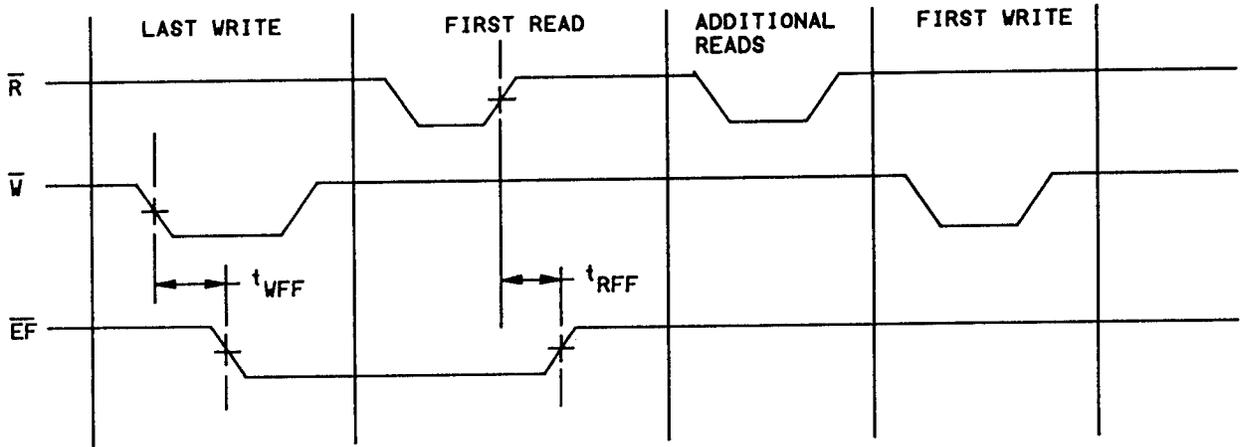
FIGURE 3. Switching time load circuit, test conditions and waveforms - Continued.



NOTES:

1. $t_{RC} = t_{RR} + t_{RPW}$.
2. $t_{WC} = t_{WR} + t_{WPW}$.
3. For subgroups 10 and 11, $V_{IH} = 2.4 \text{ V}$ @ -55°C and 2.0 V @ $+25^\circ\text{C}$ and $+125^\circ\text{C}$, for circuit A devices, $V_{IH} = 2.0 \text{ V}$ over entire temperature range for circuit B devices, $V_{IL} = 0.8 \text{ V}$, $V_{OL} = < 1.2 \text{ V}$, $V_{OH} = > 2.2 \text{ V}$.
4. Timing values per table I.

Asynchronous Read Write Cycle TimingFIGURE 3. Switching time load circuit, test conditions and waveforms - Continued.

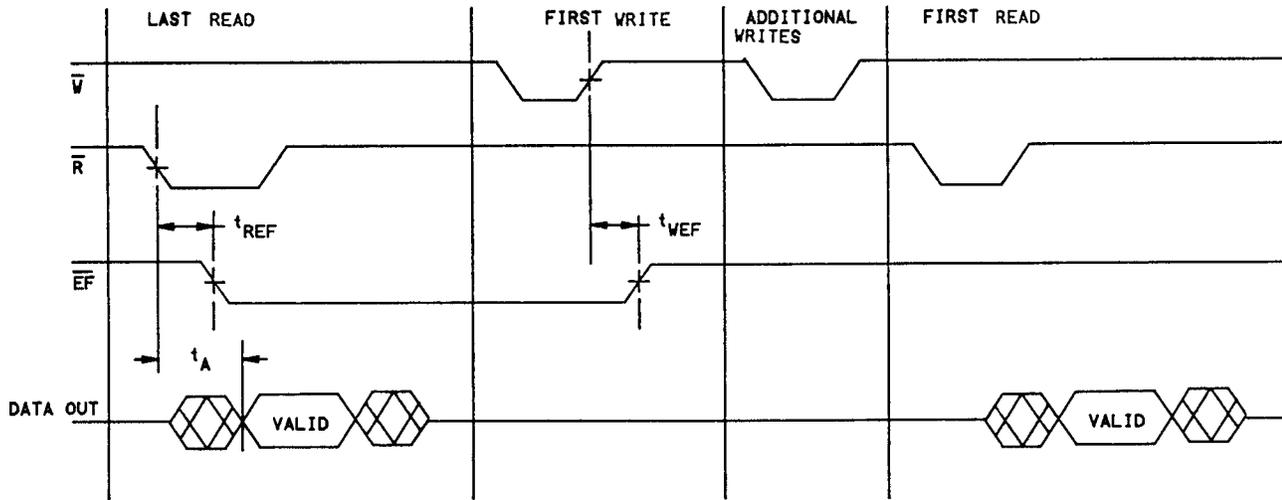


NOTES:

1. For subgroups 10 and 11, $V_{IH} = 2.4 \text{ V}$ @ -55°C and 2.0 V @ $+25^{\circ}\text{C}$ and $+125^{\circ}\text{C}$ for circuit A devices, $V_{IH} = 2.0 \text{ V}$ over entire temperature range for circuit B devices, $V_{IL} = 0.8 \text{ V}$, $V_{OL} = < 1.2 \text{ V}$, $V_{OH} = > 2.2 \text{ V}$.
2. Timing values per table I.

Full Flag Cycle Timing

FIGURE 3. Switching time load circuit, test conditions and waveforms.

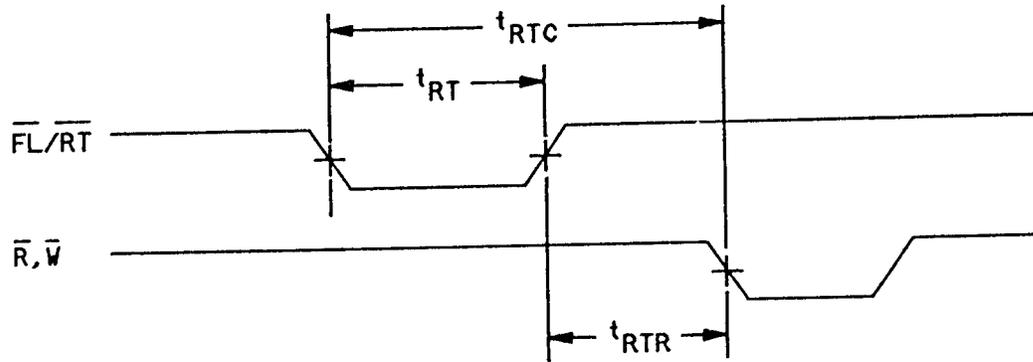


NOTES:

1. For subgroups 10 and 11, $V_{IH} = 2.4 \text{ V}$ @ -55°C and 2.0 V @ $+25^\circ\text{C}$ and $+125^\circ\text{C}$ for circuit A devices, $V_{IH} = 2.0 \text{ V}$ over entire temperature range for circuit B devices, $V_{IL} = 0.8 \text{ V}$, $V_{OL} = < 1.2 \text{ V}$, $V_{OH} = > 2.2 \text{ V}$.
2. Timing values per table I.

Empty Flag Cycle Timing

FIGURE 3. Switching time load circuit, test conditions and waveforms - Continued.



NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. EF and FF may change state during retransmit as a result of the read and write pointers, but flags will be valid at t_{RTC} .
3. For subgroups 10 and 11, $V_{IH} = 2.4 \text{ V}$ @ -55°C and 2.0 V @ $+25^{\circ}\text{C}$ and $+125^{\circ}\text{C}$ for circuit A devices, $V_{IH} = 2.0 \text{ V}$ over entire temperature range for circuit B devices, $V_{IL} = 0.8 \text{ V}$, $V_{OL} = < 1.2 \text{ V}$, $V_{OH} = > 2.2 \text{ V}$.
4. Timing values per table I.

Retransmit Cycle TimingFIGURE 3. Switching time load circuit, test conditions and waveforms - Continued.

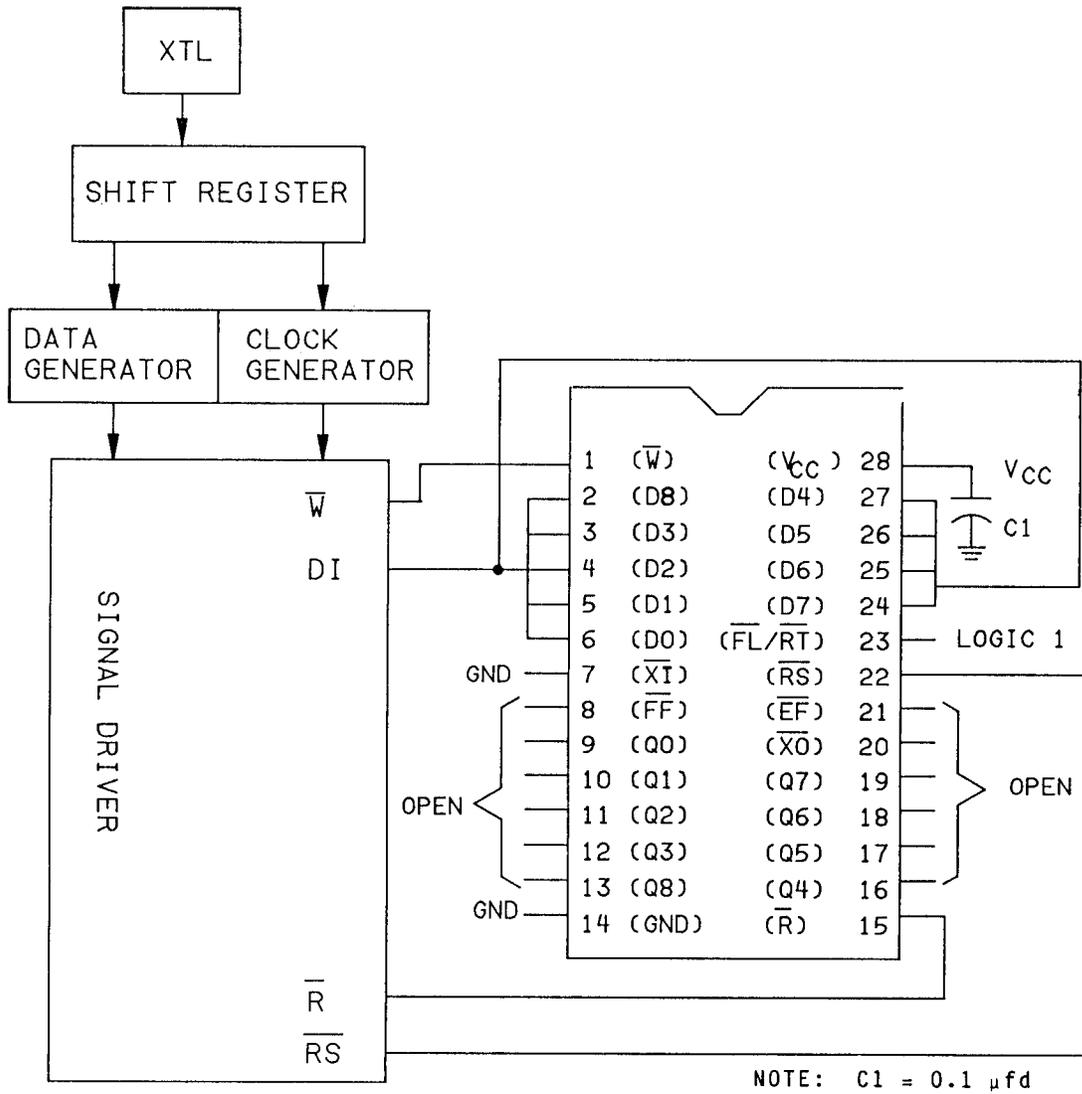
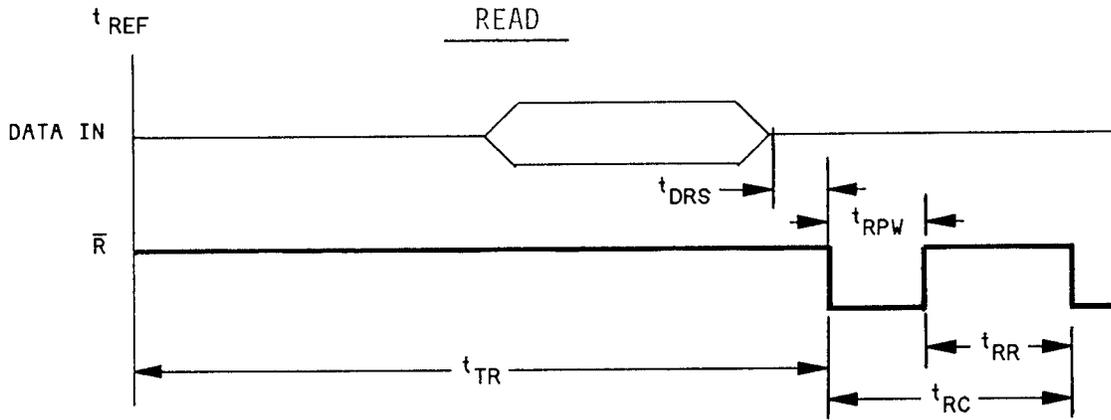
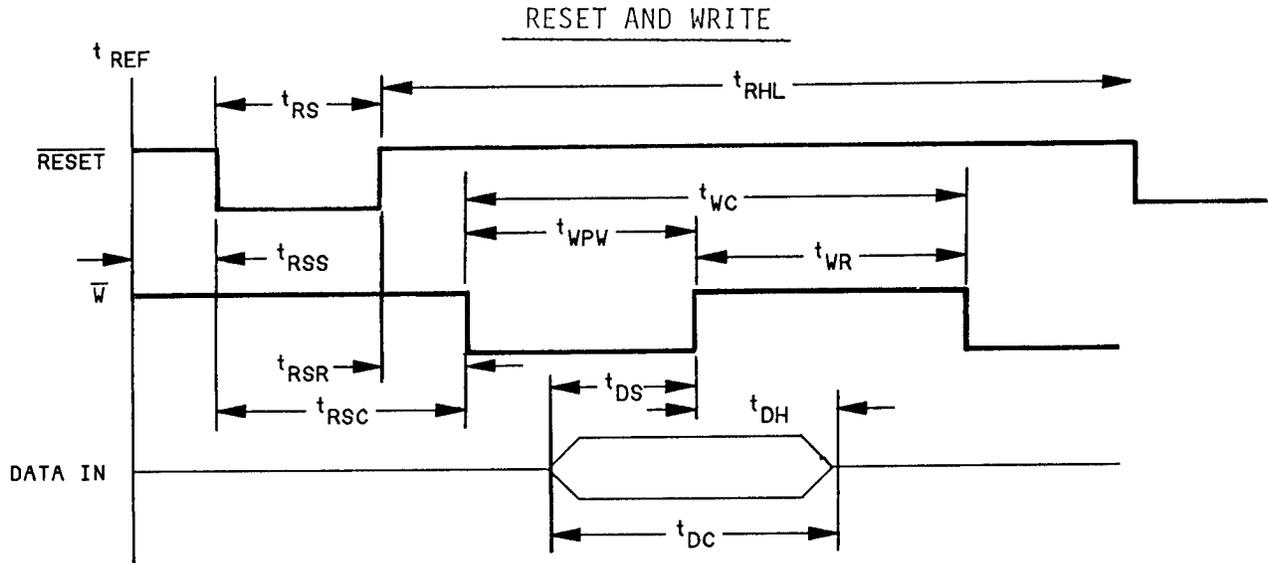


FIGURE 4. Burn-in and life test circuit and timing waveforms.



- | | |
|---------------------------------------|------------------------------------|
| $t_{REF} = 0$ | $t_{RS} = 120 \text{ ns minimum}$ |
| * $t_{DC} = 1 \mu\text{s maximum}$ | $t_{RSC} = 140 \text{ ns minimum}$ |
| $t_{DH} = 10 \text{ ns minimum}$ | $t_{RSR} = 20 \text{ ns minimum}$ |
| ∅ $t_{DRS} = 0 \text{ ns minimum}$ | $t_{RSS} = 0 \text{ ns minimum}$ |
| $t_{DS} = 40 \text{ ns minimum}$ | $t_{TR} = 512 \mu\text{s minimum}$ |
| * $t_{RC} = 1 \mu\text{s maximum}$ | * $t_{WC} = 1 \mu\text{s maximum}$ |
| $t_{RHL} = 1,024 \mu\text{s maximum}$ | $t_{WPW} = 120 \text{ ns minimum}$ |
| $t_{RPW} = 120 \text{ ns minimum}$ | $t_{WR} = 20 \text{ ns minimum}$ |
| $t_{RR} = 20 \text{ ns minimum}$ | |

NOTES:

1. * = First pulse of 512 shown.
2. ∅ = Occurs after 512 data pulses and prior to the occurrence of the first read pulse.

FIGURE 4. Burn-in and life test circuit and timing waveforms - Continued.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 1, 3, 5 through 9, and 11 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. A special subgroup shall be added using an LTPD of 15 for class B. This subgroup should consist of a high-voltage test of the input protection circuits, and should be tested in accordance with method 3015 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. Acquisition documents should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government. These requirements should not affect the part number.
- h. Requirements for "JAN" marking.

6.3 Terminal and pin definition. The input and output signals can be functionally organized into groups as shown on figure 5.

Reset (\overline{RS}). This input signal acts to reset the device in response to an external reset signal. During a Reset, both the internal read and write pointers are set to the first location. A reset is required after power up before a write operation can begin. Both \overline{W} and \overline{R} must be in a high state during a Reset. Refer to figure 3 for reset cycle timing.

Empty flag (\overline{EF}). This output signal is set to a low state whenever a Reset signal occurs (refer to figure 3) or after all data has been read from the device. If \overline{EF} is in a low state, all further read operations will be inhibited until the completion of a valid write operation where after t_{WEF} , \overline{EF} will go high. Refer to figure 3 for empty flag cycle timing.

Full flag (\overline{FF}). This output signal is set to a low state after the last write cycle to prevent a data overflow condition. With \overline{FF} in a low state, all further Write operations are inhibited until a valid Read operation occurs where after t_{RFF} , \overline{FF} will go high. Refer to figure 3 for Full Flag cycle timing.

Write (\overline{W}). The falling edge of this input signal initiates a write cycle as long as Full Flag (\overline{FF}) is not in a low state. Data set-up (t_{DS}) and hold time (t_{DH}) requirements must be satisfied with respect to the rising edge of \overline{W} . The data is stored sequentially and independent of any ongoing Read operations. Refer to figure 3 for Write cycle timing.

Read (\overline{R}). The falling edge of this input signal initiates a read cycle as long as Full Flag (\overline{FF}) is not set. The data is accessed on a First in First Out basis independent of any ongoing write operations. Refer to figure 3 for read cycle timing.

Data input bus (D0 through D8). This 9 bit input data bus provides a path to transfer the input data into the memory of the FIFO during a Write cycle.

Data output bus (Q0 through Q8). This 9 bit, three state data output bus provides a path for the memory to be read during a Read operation. After \overline{R} goes high, the data outputs will return to a high impedance condition until the next read operation.

First Load/Retransmit ($\overline{FL/RT}$). When this input signal is pulsed low, data can be retransmitted to the output data bus. A Retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. \overline{R} and \overline{W} must be in the high state during Retransmit. Refer to figure 3 for Retransmit timing. In the depth expansion mode of two or more devices, the retransmit operation is not compatible. Instead, $\overline{FL/RT}$ of the first device in the chain is connected to ground and $\overline{FL/RT}$ of the other devices is connected to V_{CC} .

Expansion In (\overline{XI}) and Expansion Out (\overline{XO}). These signals are used when two or more devices are used together for depth expansion. The Expansion Out (\overline{XO}) pin of each device must be connected to the Expansion In (\overline{XI}) pin of the next device. In single chip operation, \overline{XI} must be tied to ground.

6.4 Logistic support. Lead material and finish (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS devices should be handled with certain precautions to avoid damage due to the accumulation of static charge. These CMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam, or carriers.
- e. The uses of plastic, rubber, or silk in MOS areas should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

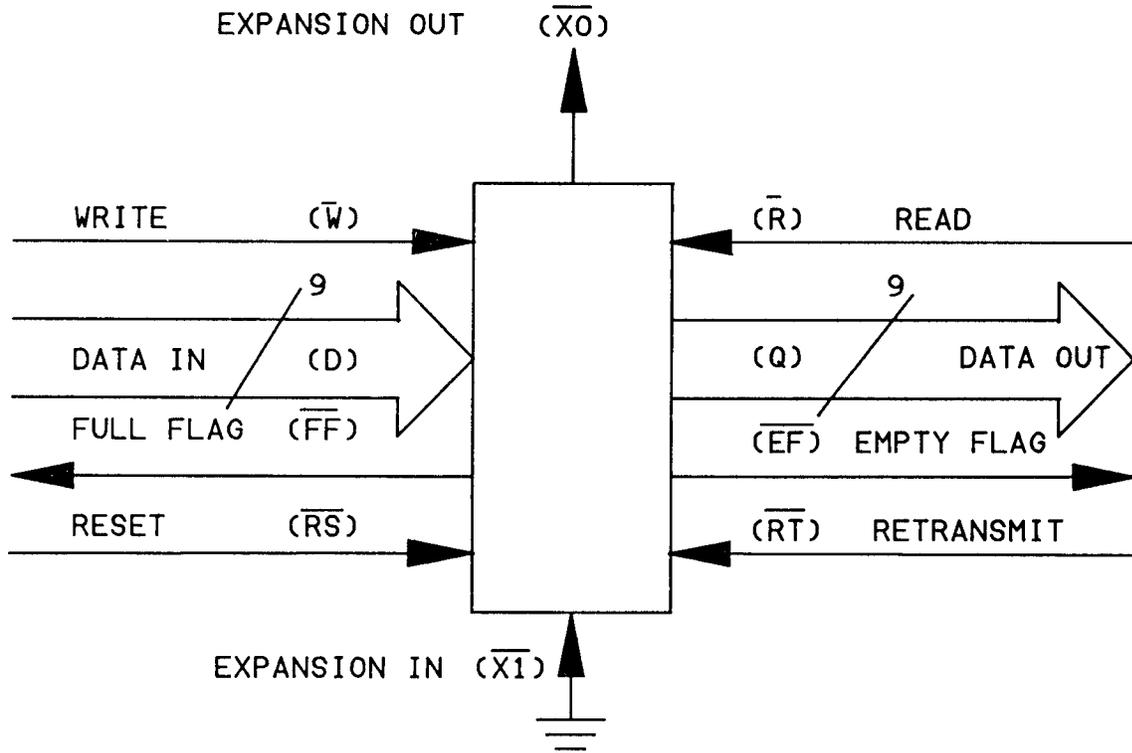


FIGURE 5. Input and output signals.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver to any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>	<u>Circuit designator</u>
01	MKB4501-81/MOSTEK	A
02	MKB4501-80/MOSTEK	A
03	MKB4501-88/MOSTEK	A
01	7C412-12/CYPRESS	B
02	7C412-10/CYPRESS	B
03	7C412-80/CYPRESS	B

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a first-in/first-out memory. Each algorithm serves a specific purpose for testing the different modes of operation of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 ALGORITHM A

30.1.1 Single chip mode.

This algorithm verifies the proper operation of the device in single chip operation ($\overline{X}T = 0.0 V$).

	FLAGS	
	EF	FF
Step 1 - Reset, check proper flag operation, and verify that the outputs are tristate.	0	1
Step 2 - Write DATA 511 times and verify proper flag operation.	1	1
Step 3 - Write DATA and verify proper flag operation.	1	0
Step 4 - Write DATA complement 512 times (further write operations are ignored).	1	0
Step 5 - Read DATA 511 times and verify proper flag operation.	1	1
Step 6 - Read DATA and verify proper flag operation.	0	1
Step 7 - Retransmit and verify proper flag operation.	1	0
Step 8 - Read DATA 511 times and verify proper flag operation.	1	1
Step 9 - Read DATA and verify proper flag operation.	0	1
Step 10 - Write DATA and verify proper flag operation.	1	1
Step 11 - Simultaneously read and write DATA 511 times and check proper flag operation.	1	1
Step 12 - Read DATA and verify proper flag operation.	0	1
Step 13 - Repeat step 2 through 12 with DATA complement.		

DATA is referenced as "PATTERNS" in table III.

30.2 ALGORITHM B

30.2.1 Multichip mode - first chip.

This algorithm verifies the proper operation of the device in multichip - first chip mode ($\overline{F}C = 0.0 V$).

	FLAGS	
	EF	FF
Step 1 - Reset.	0	1
Step 2 - Write DATA 511 times.	1	1
Step 3 - Write DATA and verify that $\overline{X}O$ pulses.	1	0
Step 4 - Read DATA 511 times.	1	1
Step 5 - Read DATA and verify that $\overline{X}O$ pulses.	0	1
Step 6 - Write DATA complement (this write operation will be ignored).	0	1
Step 7 - Read TRISTATE (this read operation will be ignored).	0	1
Step 8 - Pulse $\overline{X}T$ (simulates the last write operation of the previous chip).	0	1
Step 9 - Write DATA and verify proper flag operation.	1	1
Step 10 - Read TRISTATE (Read cycles will be ignored).	1	1
Step 11 - Pulse $\overline{X}T$ (simulates the last read operation of the previous chip).	1	1
Step 12 - Read DATA and verify proper flag operation.	0	1

DATA is referenced as "PATTERNS" in table III.

APPENDIX

30.3 ALGORITHM C

30.3.1 Multichip mode - not first chip.

This algorithm verifies the proper operation of the device in multichip - not first chip mode ($\overline{FL} = 5.0 \text{ V}$).

	FLAGS	
	\overline{EF}	\overline{FF}
Step 1 - Reset.	0	1
Step 2 - Write DATA (this write operation will be ignored).	0	1
Step 3 - Read TRISTATE.	0	1
Step 4 - Pulse \overline{XI} (simulates the last write operation of the previous chip).	0	1
Step 5 - Write DATA and verify proper flag operation.	1	1
Step 6 - Read TRISTATE.	1	1
Step 7 - Pulse \overline{XI} (simulates the last read operation of the previous chip).	1	1
Step 8 - Read DATA.	0	1

DATA is referenced as "PATTERNS" in table III.

Custodians:

Air Force - 17
Army - ER
Navy - EC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

Review activities:

Air Force - 11, 19, 85, 99
Army - AR, MI
Navy - OS, SH, TD
DLA - ES

(Project 5962-0967)

User activities:

Army - SM
Navy - AS, CG, MC