

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS
4096 BIT STATIC RANDOM ACCESS MEMORY (RAM)
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS static, 4096-bit random access memories. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510 and as specified herein.

1.2.1 Device type. The device types shall be as follows:

<u>Device type</u>	<u>Circuit organization</u>	<u>Address access time</u>
01, 03 ($T_C = -55^{\circ}\text{C}$ "instant-on" to $+125^{\circ}\text{C}$) 1/	4096 words/1-bit	$t_{AVQV} = 35 \text{ ns}, 55 \text{ ns}$
02, 04 ($T_C = -55^{\circ}\text{C}$ "instant-on" to $+125^{\circ}\text{C}$) 1/	1024 words/4-bit	$t_{AVQV} = 35 \text{ ns}, 55 \text{ ns}$

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
V	D-6 (18-lead, $1/4"$ x $15/16"$), dual-in-line package
X	See figure 1 (18-lead, $1/4"$ x $1/2"$), flat package
3	C-10 (18 terminal RECT.CCP - .285" x /425")

1.3 Absolute maximum ratings.

Voltage on any pin with respect to ground 2/	-0.5 V to +7.0 V
Storage temperature range-	-65°C to $+150^{\circ}\text{C}$
Power dissipation (P_D)	1.0 mW
Lead temperature (soldering, 5 seconds)-	270°C
Maximum junction temperature (T_J) 3/	150°C
Thermal resistance, junction-to-case: θ_{JC}	
Case V	(See MIL-M-38510, appendix C)
Cases 3, X	55°C/W 4/
Maximum dc output current-	20 mA

- 1/ $T_C = T_A$ at test time equals zero. "Instant-on" is defined as all functional characteristics guaranteed at all temperatures 50 ms after power is applied.
2/ Under absolute maximum ratings, the voltage values are with respect to the most negative supply voltage, V_{SS} . Throughout the remainder of this specification, the voltage values are with respect to V_{SS} .
3/ Maximum junction temperature (T_J) may be increased to 175°C during the burn-in and steady state life test.
4/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC} - V_{SS}) - - - - -	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH}) (all inputs) - - - -	2.0 V dc to 6.0 V dc (device 01, 02)
High level input voltage (V_{IH}) (all inputs) - - - -	2.0 V dc to V_{CC} (device 03, 04)
Low-level input voltage (V_{IL}) (all inputs) - - - -	-3.0 V dc to +0.8 V dc
Operating case temperature (T_C) - - - - -	-55°C to +125°C

	Min	Max	Units
Device type 01:			
Read cycle time (tAVAV) - - - - -	35		ns
Address access time (tAVQV) - - - - -		35	ns
CS access time (tELQV) - - - - -		35	ns
Output hold time from address change (tAVQX) - - -	5		ns
Chip select to output in low-Z (tELQL) 5/ 6/-	5		ns
Chip deselect to output in high-Z (tEHQZ) 5/ 6/-	0	30	ns
Chip select to power-up time (tEHPU) - - - - -	0		ns
Chip deselect to power-down time (tEHPD) - - - - -		20	ns
Write cycle time (tAVAV) - - - - -	35		ns
Pulse width, chip select to end of write (tELWH) 7/-	35		ns
Address valid to end of write (tAVWH) - - - - -	35		ns
Pulse width, write (tWLWH) - - - - -	20		ns
Data valid to end of write (tDVWH) - - - - -	20		ns
Address set-up to write start (tAVWL) - - - - -	0		ns
Write recovery time (tWHDAX) - - - - -	0		ns
Data hold from write end (tWHDX) - - - - -	10		ns
Write enabled to output in high-Z (tWLQZ) 6/- - -	0	20	ns
Output active from end of write (tWHQX) 6/- / - -	0		ns
Device type 02:			
Read cycle time (tAVAV) - - - - -	35		ns
Address access time (tAVQV) - - - - -		35	ns
Chip select access time (tELQV) - - - - -		35	ns
Output hold time from address change (tAVQX) - - -	0		ns
Chip select to output in low-Z (tELQL) 5/ 6/-	10		ns
Chip deselect to output in high-Z (tEHQZ) 5/ 6/-	0	20	ns
Chip select to power-up time (tEHPU) - - - - -	0		ns
Chip deselect to power-down time (tEHPD) - - - - -		30	ns
Write cycle time (tAVAV) - - - - -	35		ns
Pulse width, chip select to end of write (tELWH) 7/-	30		ns
Address valid to end of write (tAVWH) - - - - -	30		ns
Pulse width, write (tWLWH) - - - - -	30		ns
Data valid to end of write (tDVWH) - - - - -	20		ns
Address set-up to write start (tAVWL) - - - - -	0		ns
Write recovery time (tWHDAX) - - - - -	5		ns
Data hold from write end (tWHDX) - - - - -	0		ns
Write enabled to output in high-Z (tWLQZ) 6/- - -	0	10	ns
Output active from end of write (tWHQX) 6/- / - -	0		ns
Device type 03:			
Read cycle time (tAVAV) - - - - -	55		ns
Address access time (tAVQV) - - - - -		55	ns
Chip select access time (tELQV) - - - - -		55	ns
Output hold time from address change (tAVQX) - - -	5		ns
Chip select to output in low-Z (tELQL) 5/ 6/- -	5		ns
Chip deselect to output in high-Z (tEHQZ) 5/ 6/-	0	30	ns
Chip select to power-up time (tEHPU) - - - - -	0		ns
Chip deselect to power-down time (tEHPD) - - - - -		20	ns
Write cycle time (tAVAV) - - - - -	55		ns
Pulse width, chip select to end of write (tELWH) 7/-	45		ns
Address valid to end of write (tAVWH) - - - - -	45		ns
Pulse width, write (tWLWH) - - - - -	25		ns
Data valid to end of write (tDVWH) - - - - -	25		ns
Address set-up to write start (tAVWL) - - - - -	0		ns
Write recovery time (tWHDAX) - - - - -	10		ns
Data hold from write end (tWHDX) - - - - -	10		ns
Write enabled to output in high-Z (tWLQZ) 6/- - -	0	25	ns
Output active from end of write (tWHQX) 6/- / - -	0		ns

Device type 04:		Min	Max	Units
Read cycle time (tAVAV)	- - - - -	55		ns
Address access time (tAVQV)	- - - - -		55	ns
Chip select access time (tELQV)	8/- - - - -		65	ns
Output hold time from address change (tAVQX)	- - -	5		ns
Chip select to output in low-Z (tELQL)	5/ 6/- - -		10	ns
Chip deselect to output in high-Z (tEHQZ)	5/ 6/ -	0	20	ns
Chip select to power-up time (tELPU)	- - - - -		0	ns
Chip deselect to power-down time (tEHPD)	- - - - -		30	ns
Write cycle time (tAVAV)	- - - - -	55		ns
Pulse width, chip select to end of write (tELWH)	7/	50		ns
Address valid to end of write (tAVWH)	- - - - -	50		ns
Pulse width, write (tWLWH)	- - - - -	40		ns
Data valid to end of write (tDVWH)	- - - - -	20		ns
Address set-up to write start (tAVNL)	- - - - -	0		ns
Write recovery time (tWHAX)	- - - - -	5		ns
Data hold from write end (tWHDX)	- - - - -	0		ns
Write enabled to output in high-Z (tWLQZ)	6/- - -	0	20	ns
Output active from end of write (tWHQX)	6/-7/ - -	0		ns

- 5/ At any given temperature and voltage condition, tELQL maximum is less than tEHQZ minimum both for a given device and from device to device.
- 6/ Transition is measured ± 500 mV from steady state voltage with specified loading.
- 7/ The internal write time of the memory is defined by the overlap of CS low and WE low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 8/ Chip deselected less than 55 ns prior to selection.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standards required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

- 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.
- 3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.
- 3.2.3 Functional tests. The functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.
- 3.2.4 Truth table. The truth table shall be as specified on figure 4.
- 3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3.
- 3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.
- 3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/	Device	Limits	Unit
				Min	Max
Low level input leakage current (all input pins)	I _{IL}	V _{CC} = 5.5 V V _{IN} = GND	A11	-10	μA
High level input leakage current (all input pins)	I _{IH}	V _{CC} = 5.5 V V _{IN} = 5.5 V	A11	10	μA
Output leakage current	I _{LO}	CS = V _{IH} , V _{CC} = 5.5 V V _{OUT} = GND to 5.5 V	A11	±50	μA
Power supply current	I _{CC}	V _{CC} = 5.5 V CS = V _{IL} , outputs open	01,02 03,04	110 140	mA
Standby current	I _{S8}	V _{CC} = 4.5 V to 5.5 V CS = V _{IH}	01,02 03 04	10 25 30	mA
Output low voltage	V _{OL}	I _{OL} = 12.0 mA V _{IL} = 0.8 V V _{IH} = 2.0 V V _{CC} = 4.5 V I _{OL} = 8.0 mA	01,03 02,04	0.4 0.4	V
Output high voltage	V _{OH}	V _{IL} = 0.8 V V _{IH} = 2.0 V V _{CC} = 4.5 V I _{OH} = -4.0 mA	A11	2.4	V
Output short circuit current 4/, 5/	I _{OS}	V _{CC} = 5.5 V, V _{OUT} = GND	A11	-350	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device	Limits		
				1/	2/	3/
Input capacitance	C_{IN}	$V_{IN} = 0 \text{ V}$, $f = 1 \text{ MHz}$ $T_C = 25^\circ\text{C}$	A11		5	pF
Output capacitance	C_O	$V_{IN} = 0 \text{ V}$, $f = 1 \text{ MHz}$ $T_C = 25^\circ\text{C}$	A11		7	pF
Peak power on 5/	I_{PO}	$V_{CC} = 4.5 \text{ V}$, $CS = 2.4 \text{ V}$	A11		10	mA
Read cycle time 2/	tAVAV	See table III and figure 6	01,02 03,04	35 55		ns
Address access time	tAVQV		01,02 03,04		35 55	ns
Chip select access time 3/	tELQV		01,02 03 04 6/		35 55 65	ns
Chip select to output in low-Z 5/ 7/	tELQX		01,03 02,04	5 10		ns
Chip deselect to output in high-Z 5/ 7/	tEHQZ		01,03 02,04	0 0	30 20	ns
Output hold from address change	tAVQX		01,03,04 02	5 0		ns
Chip select to power up time 5/	tELPU		A11	0		ns
Chip deselect to power down time 5/	tEHPD		01,03 02,04		20 30	ns
Write cycle time	tAVAV		01,02 03,04	35 55		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Device	Limits
				Min Max Unit
Chip select to end of write	tELWH	See table III and figure 6	01 02 03 04	35 30 45 50 ns
Address valid to end of write	tAVWH		01 02 03 04	35 30 45 50 ns
Address setup time	tAVWL		All	0 ns
Write pulse width	twLWH		03 04 01 02	25 40 20 30 ns
Write recovery time	twHAX		01 02,04 03	0 5 10 ns
Data valid to end of write	tUVWH		01,02,04 03	20 25 ns
Data hold time	tWHDX		01,03 02,04	10 0 ns
Write enable to output in high-Z 7/, 5/	twLQZ		01,04 02 03	0 10 25 20 10 25 ns
Output active from end of write 7/, 5/	tWHQX		All	0 ns

- 1/ Output levels are tested in static state and are specified over voltage range of V_{CC}.
- 2/ Unless otherwise specified, the dynamic load shall be in accordance with figure 6 (load A).
- 3/ Complete terminal conditions are as specified in table III.
- 4/ Duration not to exceed 1 second.
- 5/ Not tested.
- 6/ Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
- 7/ Transition is measured ± 500 mV from steady state voltage using figure 6 (load B).

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B 1/ devices
Initial electrical parameters (method 5004)	2,8*	2,8*,10
Final electrical test parameters (method 5004)	1**,2,3,7**, 8	1**,2,3,7**, 8*,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11	1,2,3,4,7, 8*,9,10,11
Group B end-point electrical parameters (method 5005)	1,2,3,7,8 9,10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	2,10
Group D end-point electrical parameters (method 5005)	1,2,3,7,8	2,10

* Maximum temperature only.

** PDA applies to subgroups 1 and 7 (see 4.2d).

1/ For subgroup 4, see 4.4.1c).

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. A cell bit stress test may be used for the special electrical screen test of method 5004. The cell bit stress test shall be conducted per table III test number 42 for device types 01, 03 and test number 54 for device types 02, 04. The functional test shall be the checkerboard/checkboard algorithm of the appendix. This test shall be performed once at the first high temperature (125°C) functional test only.
- b. Burn-in (method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.

- c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- d. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type of this specification, the slower device type may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be in accordance with table II herein.
- b. Subgroups 5 and 6 shall be omitted.
- c. Subgroup 4 (C_i , C_o measurement) shall be measured only for initial qualification and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz and a signal amplitude ± 50 mV rms. Perform C_{in} and C_o parameter measurements to table I limits.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883 method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using method 3015 modified as follows:
 - (1) For use in this specification method 3015 table I pin combination number (4) shall be "input (B) to V₊ (A)" and combination number (5) shall be "output (B) to V₊ (A)".
 - (2) The reverse polarity procedure shall be applicable to all pin combinations.
 - (3) Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.
- b. Steady-state life test for class S devices shall be in accordance with table IIA (subgroup 5) of method 5005 of MIL-STD-883, using the circuit on figure 5 or equivalent.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration, 1,000 hours except as permitted by method 1005 of MIL-STD-883.

Device types 01, 02, 03 and 04

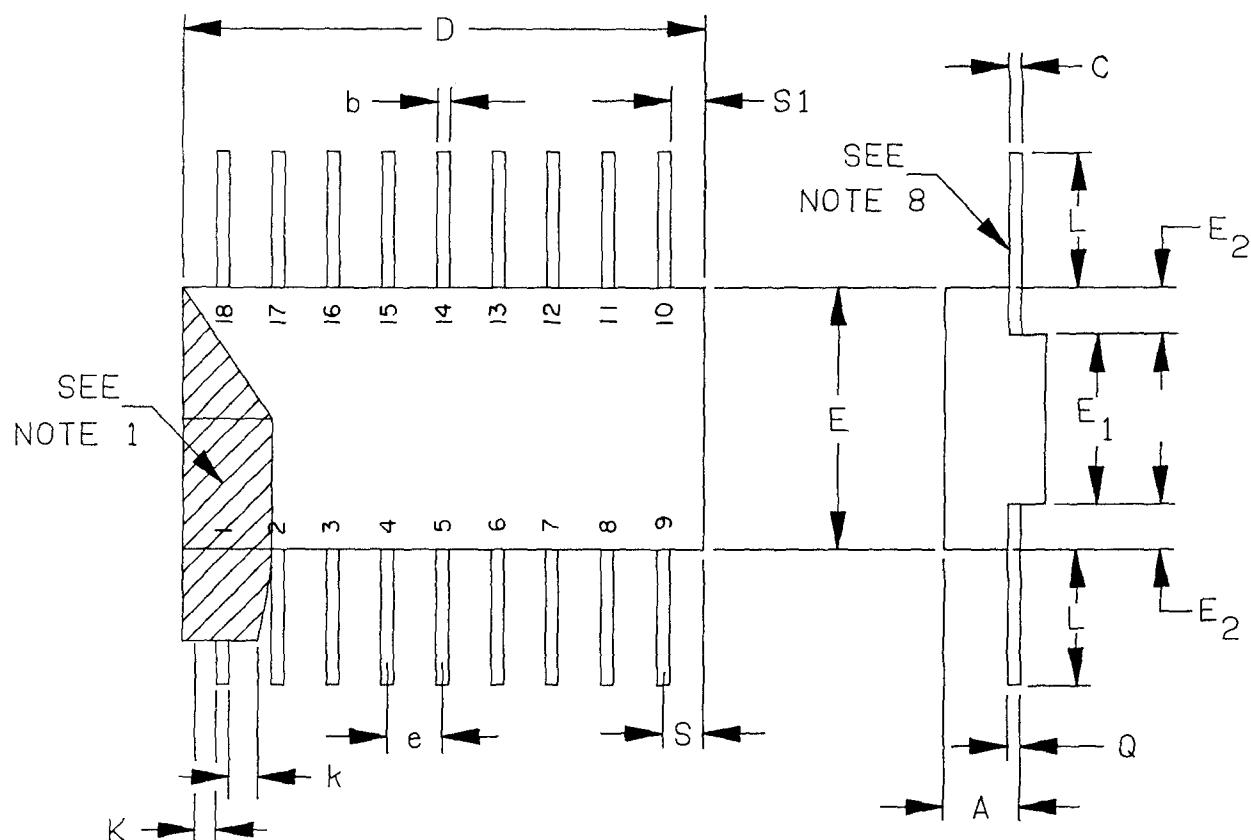


FIGURE 1. Case outline X (18 lead, 1/4" x 1/2" flat package).

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.092	1.14	2.34	
b	.015	.019	0.38	0.48	5
c	.003	.007	0.08	0.18	5
D		.455		11.56	3
E	.295	.320	7.49	8.13	
E ₁	.130	.150	3.30	3.81	
E ₂	.030		10.76		
e	.050 BSC		1.27 BSC		4, 6
k	.005	.018	0.13	0.46	9
L	.250	.370	6.35	9.40	
Q	.010	.040	0.25	1.02	2
S		.045		1.14	7
S ₁	.005		0.13		

FIGURE 1. Case outline X (18 lead, 1/4" x 1/2") - Continued.

NOTES:

1. Index area, A notch or A pin identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim k) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body. Dimension Q shall be .0085 inch (0.22 mm) minimum when lead finish A is applied.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 18.
5. All leads - increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads number 1, 9, 10 and 18).
8. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
9. Optional, see note 1. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

FIGURE 1. Case outline X (18 lead, 1/4" x 1/2" flat package) - Continued.

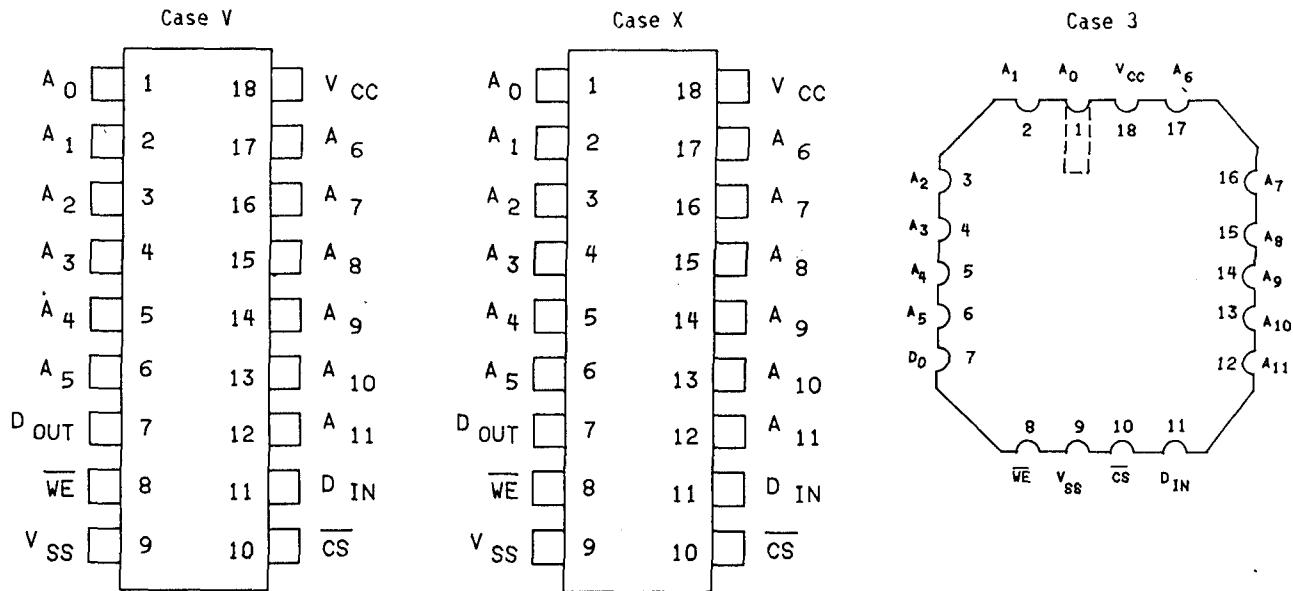
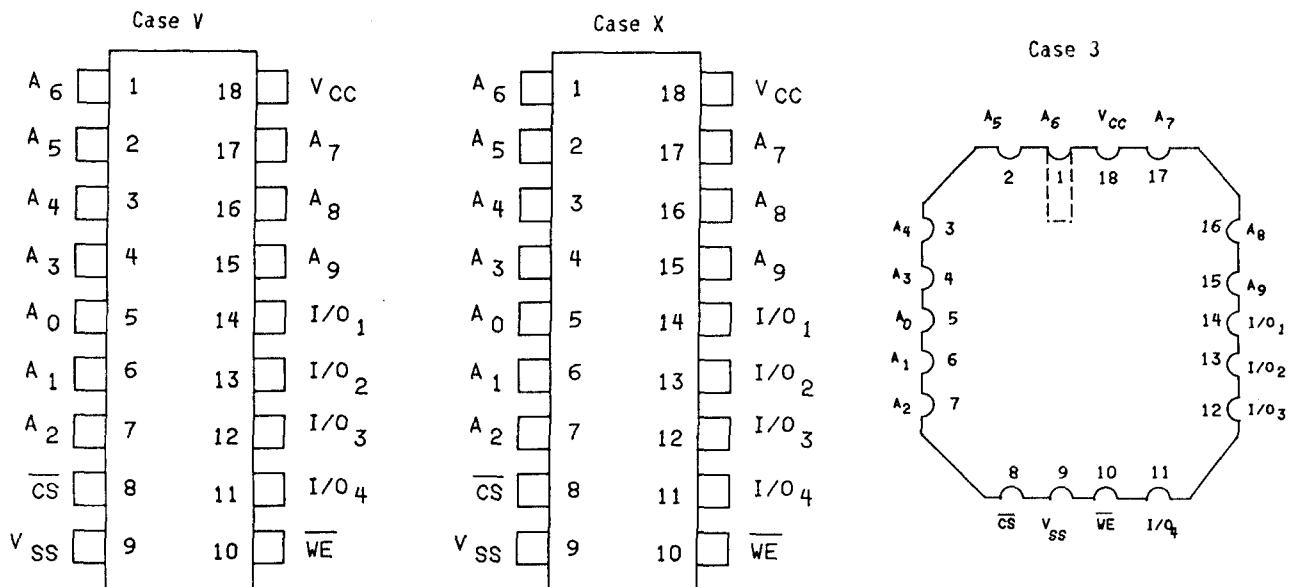
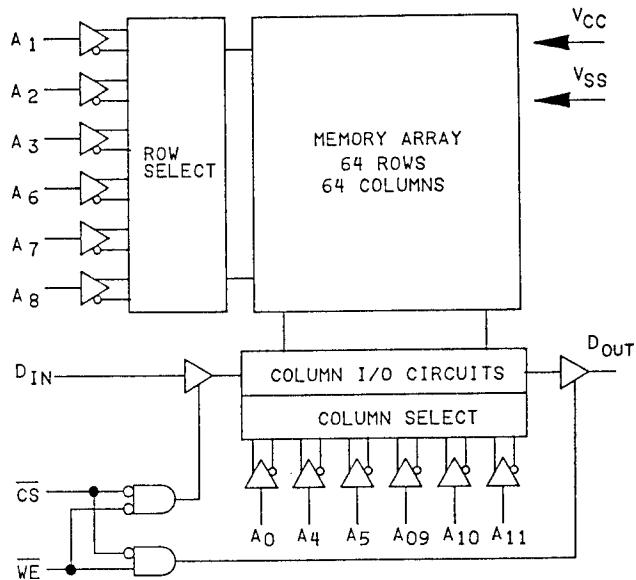
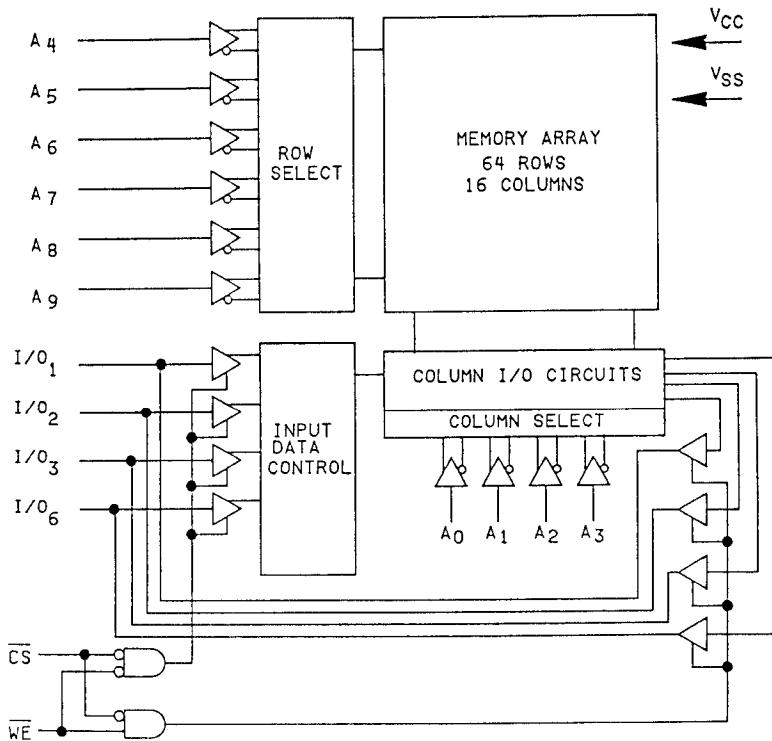
Device types 01 and 03Device types 02 and 04

FIGURE 2. Terminal connections.

Device types 01 and 03Device types 02 and 04

NOTE: Address numbering may vary between vendors.

FIGURE 3. Block diagrams.

Device types 01, 02, 03 and 04

<u>CS</u>	<u>WE</u>	Mode	Output	Power	I/O
H	X	Not selected	High Z	Stand by	High Z
L	L	Write	High Z	Active	DIN
L	H	Read	D _{OUT}	Active	D _{OUT}

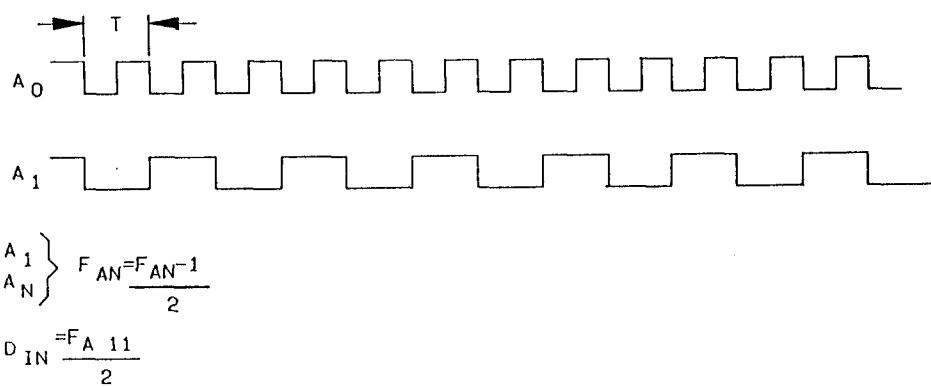
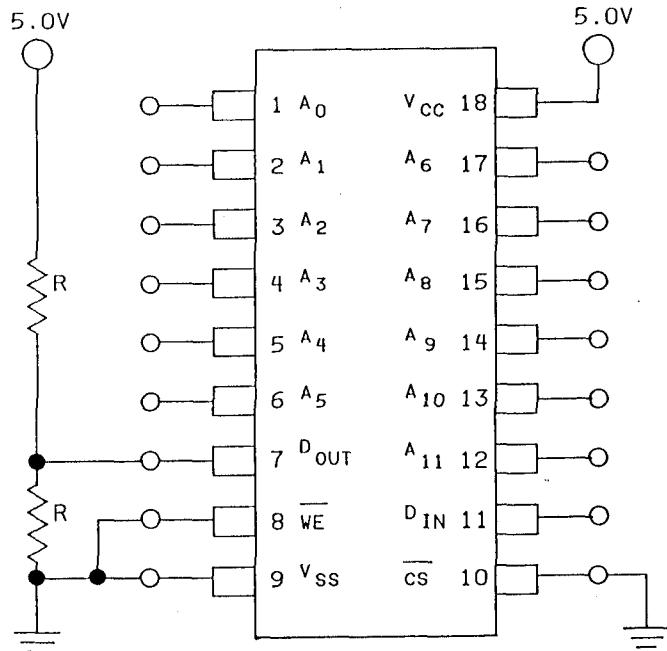
H = High voltage level.

L = Low voltage level.

X = Don't care (high or low).

FIGURE 4. Truth table.

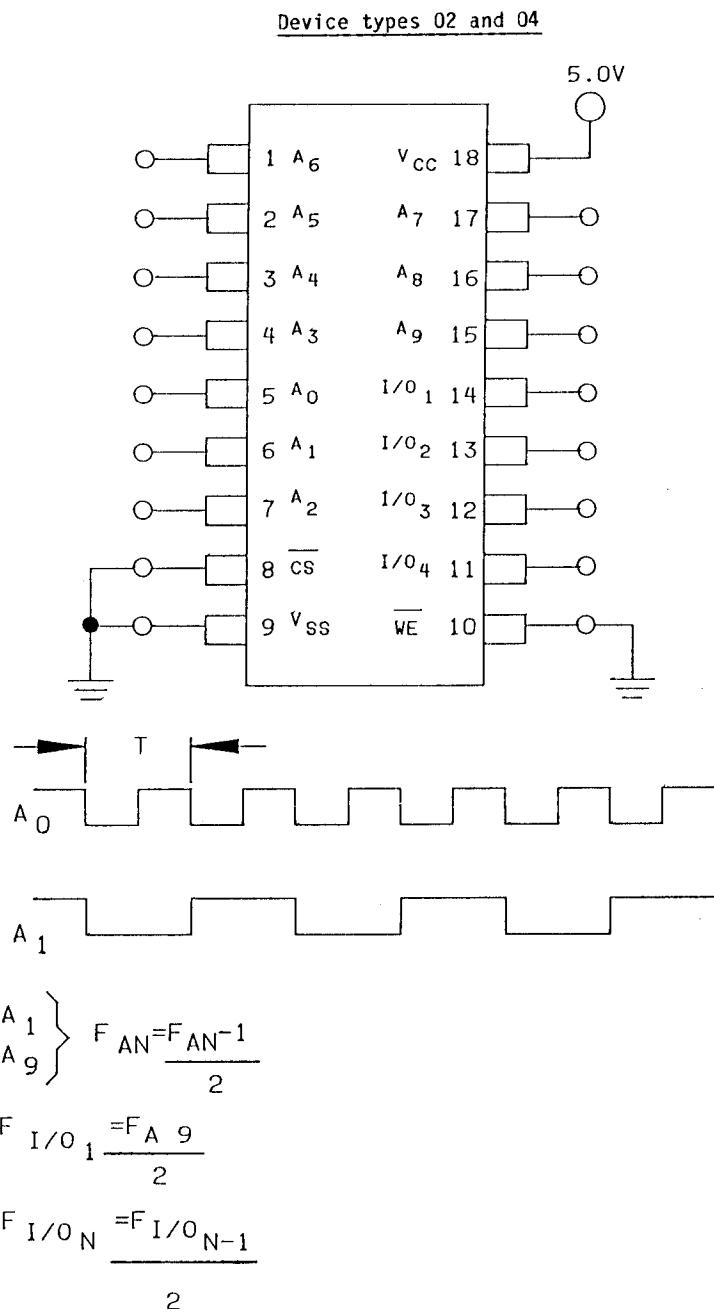
Device types 01 and 03



NOTES:

1. $T = 20 \mu s$, 50% duty cycle, $t_{TLH} = t_{THL} \leq 150 \text{ ns}$.
 2. $R = 200\Omega \pm 5\%$. *For 12V, this resistance.*
 3. Address to be cycled in a binary sequence where A_0 is least significant and A_{11} is most significant.

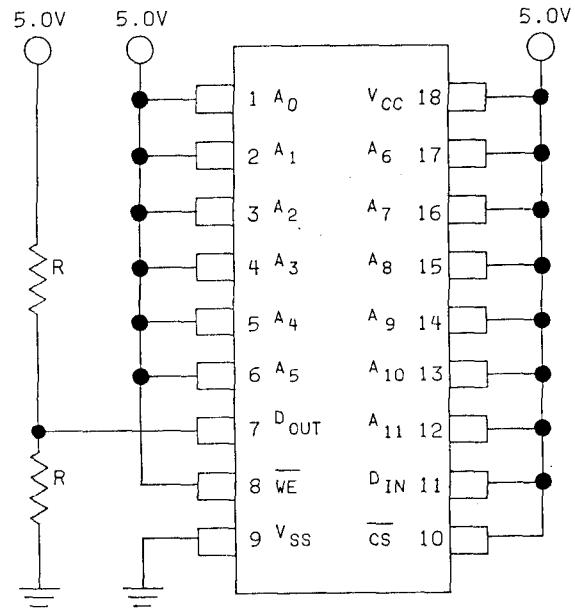
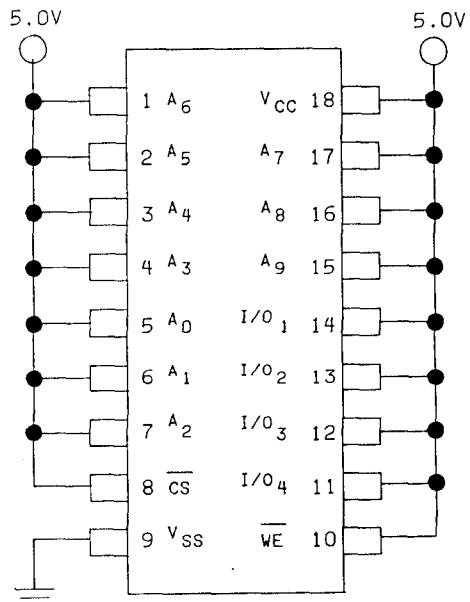
FIGURE 5. Burn-in and steady state life test circuit and waveform.



NOTES:

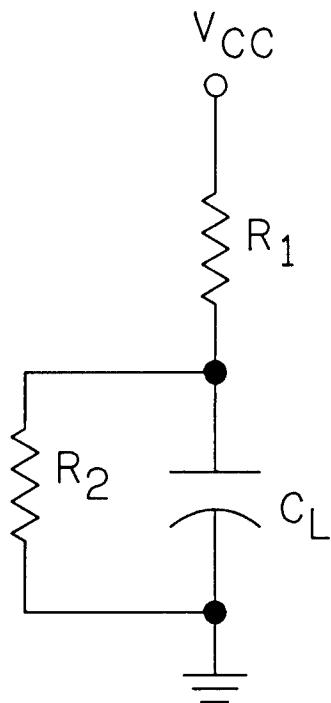
1. T = 20 μ s, 50% duty cycle, $t_{TLH} = t_{THL} \leq 150$ ns.
2. Address to be cycled in a binary sequence where A_0 is least significant and A_q is most significant.

FIGURE 5. Burn-in and steady state life test circuit and waveform - Continued.

Device types 01 and 03Device types 02 and 04

NOTE: $R = 1 \text{ k}\Omega \pm 5\%$.

FIGURE 5. Optional steady state life test circuit - Continued.

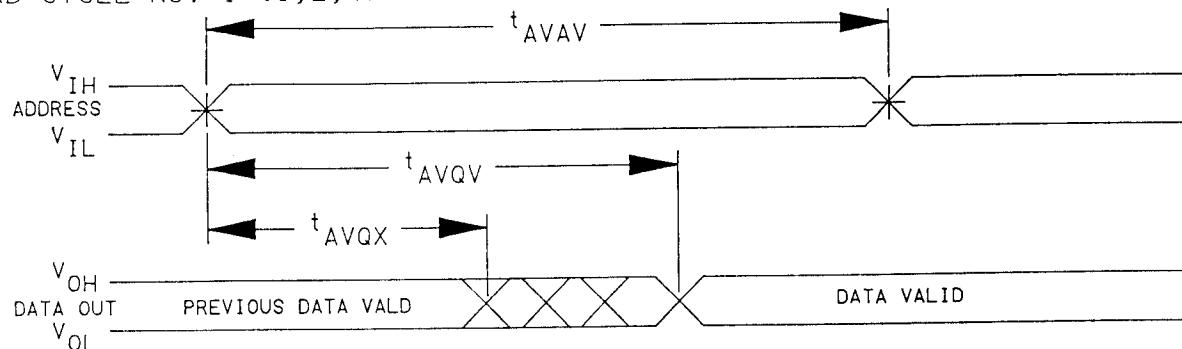
Device types 01, 02, 03 and 04

NOTES:

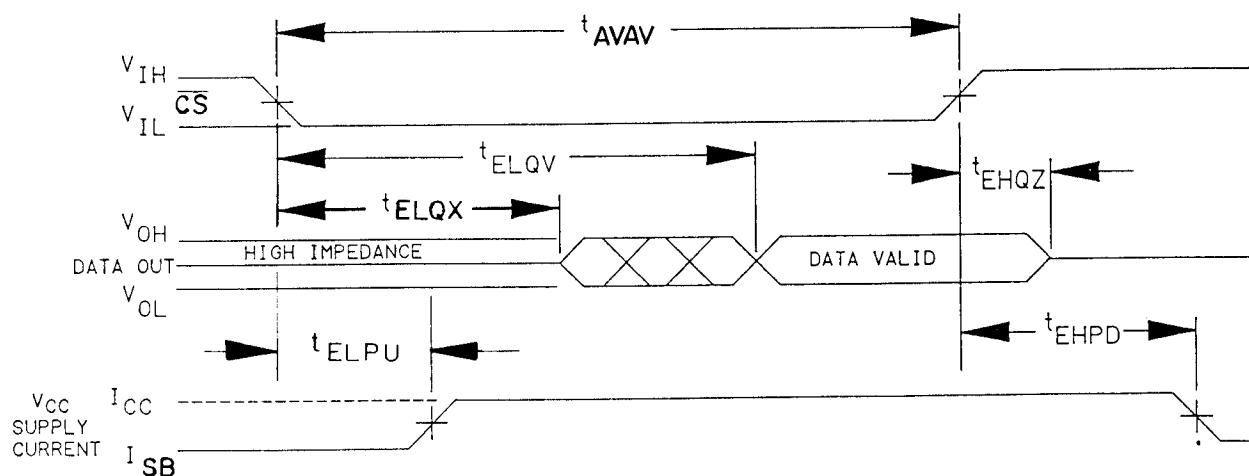
1. V_{CC} is defined in table III.
2. Load A: (including probe and jig capacitance)
 $R_1 = 481\Omega \pm 5\%$; $R_2 = 255\Omega \pm 5\%$; $C_L = 30 \text{ pF}$ (device 02 and 04)
 $R_1 = 329\Omega \pm 5\%$; $R_2 = 202\Omega \pm 5\%$; $C_L = 30 \text{ pF}$ (device 01 and 03)
3. Load B: (Including probe and jig capacitance)
 $R_1 = 481\Omega \pm 5\%$; $R_2 = 255\Omega \pm 5\%$; $C_L = 5 \text{ pF}$ (device 02 and 04)
 $R_1 = 329\Omega \pm 5\%$; $R_2 = 202\Omega \pm 5\%$; $C_L = 5 \text{ pF}$ (device 01 and 03).

FIGURE 6. Load circuit and timing diagram.

READ CYCLE NO. 1 (1,2,4)



READ CYCLE NO. 2 (1,3,4)

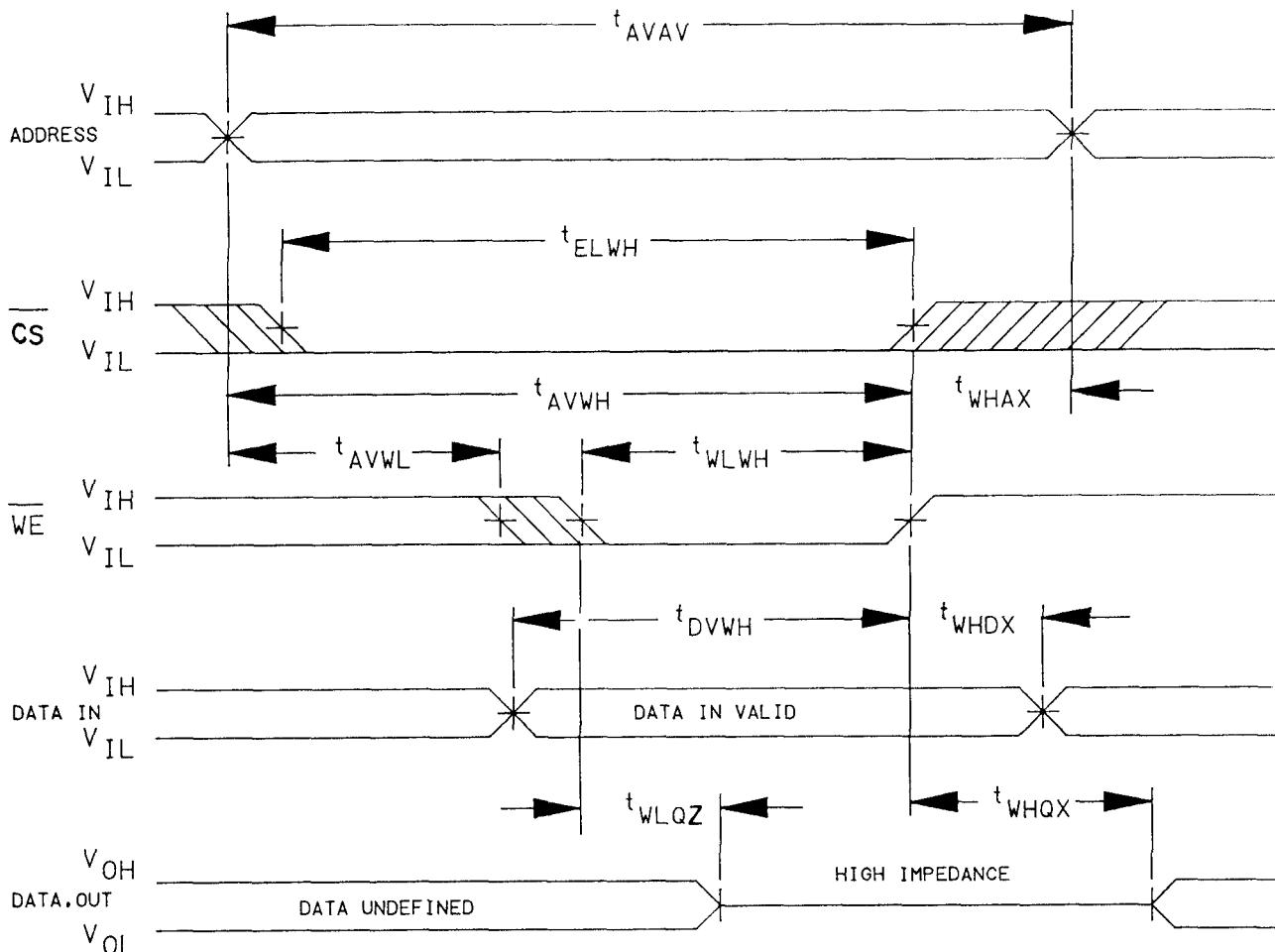
WAVEFORMS

NOTES:

1. WE is high for read cycles.
2. Device is continuously selected, CS transition low.
3. Addresses valid prior to or coincident with CS transition low.
4. See table 1 for limits and complete terminal conditions.
5. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
6. t_{ELQX} and t_{EHQZ} are measured at ±500 mV from steady state with 5 pF load.

Read cycle waveforms and test conditions for device types 01, 02, 03 and 04

FIGURE 6. Load circuit and timing diagram - Continued.

WE CONTROLLEDWAVEFORMS

NOTES:

1. See table I for limits and complete terminal conditions.
2. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
3. t_{WHQX} and t_{WLQZ} are measured at ± 500 mV from steady state with 5 pF load.

Write cycle waveforms and test conditions for device types 01, 02, 03 and 04

FIGURE 6. Load circuit and timing diagram - Continued.

TABLE III. Terminal conditions (outputs not designated) for device types 01 and 03. Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open.

2 Same tests, terminal conditions, and limits as subgroup 1, except $T_C = 125^\circ C$.

3 Same tests, terminal conditions, and limits as subgroup 1, except $T_C = -55^\circ C$.

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See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (outputs not designated are open V or open).
Inputs not designated are high > 2.0 V or low < 0.8 V or open.

8 Same tests, terminal conditions, and limits as subgroup 7, except $T_C = 125^\circ\text{C}$ and -55°C .

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
 Terminal conditions (outputs not designated are open or resistive coupled to ground or voltages;
 Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883	Cases 1 3, YX	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algo. limits	Measured terminal	Test limits	Unit	
		Method	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	I _{DUT}	V _E	V _{SS}	CS	I _{D14}	I _{A11}	I _{A10}	I _{A9}	I _{A8}	I _{A7}	I _G	V _{CC}					
9	tHDX	Fig. 6	79	15/ $\frac{V}{W}$	"	"	"	"	15/ $\frac{V}{W}$	4.5 V	GALP1 and GALP2	D _{OUT}	10	ns											
T _C = +25°C		80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V				
	CAVX		81	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	4.5 V	GALPA1 and GALPA2	D _{OUT}	5	"
			82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V	GALP1 and GALP2	D _{OUT}	5	"
10	Same tests, terminal conditions, and limits as subgroup 9, except T _C = 125°C.																								
11	Same tests, terminal conditions, and limits as subgroup 9, except T _C = -55°C.																								

See footnotes at end of device types 01 and 03.

- 1/ See appendix for description of algorithms.
- 2/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels during measurement shall be: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$
- 3/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels during measurement shall be:

	V_{IL}	V_{IH}	I_{OL}
Types 01, 03	0.8 V	2.0 V	12.0 mA

- 4/ $I_{SB} = 10 \text{ mA}$ for device type 01; 25 mA for device type 03. The device manufacturer may at his option do either test or both tests.
 - 5/ $I_{CC} = 110 \text{ mA}$ for device type 01, 140 mA for device type 03.
 - 6/ See 4.4.1c.
 - 7/ $V_{IL} = \text{GND}$, $V_{IH} = 6.0 \text{ V}$, pause time = 250 ms/loop max, $\overline{CS} = \text{high}$, only performed once at 125°C , and $V_{CC} = 7.0 \text{ V}$ min.
 - 8/ $V_{IL} = 0.8 \text{ V}$ and $V_{IH} = 2.0 \text{ V}$.
 - 9/ Algorithm has 60 ns where chip is deselected between the write.
 - 10/ $V_{IL} = \text{GND}$, $V_{IH} = 3.0 \text{ V}$, and all address setup times are at minimums.
 - 11/ $V_{IL} = \text{GND}$, $V_{IH} = 3.0 \text{ V}$, and all write pulse timing are at minimums.
 - 12/ $V_{IL} = \text{GND}$, $V_{IH} = 3.0 \text{ V}$, and all address ending times are at minimums.
 - 13/ $V_{IL} = \text{GND}$, $V_{IH} = 3.0 \text{ V}$, and $tAVQV$ is measured at minimum timing.
 - 14/ $V_{IL} = \text{GND}$, $V_{IH} = 3.0 \text{ V}$, $tELQV1$ and $tELQV2$ are measured at minimum timing.
 - 15/ $V_{IL} = 0.0 \text{ V}$, $V_{IH} = 3.0 \text{ V}$, and all parameters are measured at minimum timing.
 - 16/ $tAVQV = 35 \text{ ns}$ for device type 01; 55 ns for device type 03.
 - 17/ $tELQV1 = 35 \text{ ns}$ for device type 01; 55 ns for device type 03.
 - 18/ $tELQV2 = 35 \text{ ns}$ for device type 01; 55 ns for device type 03.
 - 19/ $tAVAV = 35 \text{ ns}$ for device type 01; 55 ns for device type 03.
 - 20/ $tELWH = 35 \text{ ns}$ for device type 01; 45 ns for device type 03.
 - 21/ $tAVWH = 35 \text{ ns}$ for device type 01; 45 ns for device type 03.
 - 22/ $tWLWH = 35 \text{ ns}$ for device type 01; 25 ns for device type 03.
 - 23/ $tWHAX = 20 \text{ ns}$ for device type 01; 10 ns for device type 03.
 - 24/ $tDVWH = 20 \text{ ns}$ for device type 01; 25 ns for device type 03.
- * The device manufacturer may at his option, do either test or both tests.

TABLE III. Group A inspection for device types 02 and 04. Terminal conditions (outputs not designated are open or shorted to ground or voltages; inputs not designated are high > 2.0 V low < 0.8 V or open).

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TABLE III. Group A inspection for Terminal conditions (Outputs not designated are open or inputs not designated are high ≥ 2.0 V). Device types 02 and 04 - Continued
Resistive coupled to ground or voltages; low ≤ 0.8 V or open.

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See footnotes at end of device types Q2 and Q4.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
 Terminal conditions (outputs not designated are open or resistive coupled to GND or voltages;
 Inputs not designated are high ≥ 2.0 , low ≤ 0.8 V or open).

Subgroup	Symbol	MLT- STD-83 method	Cases			V _X	I	2	3	4	5	6	7	d	9	10	11	12	13	14	15	16	17	18	Algorithms 1/ A ₁ A ₂ A ₃ A ₄ A ₅ A ₆	Measured terminal 1/ A ₉ A ₈ A ₇ V _{CC}	Test limits	Unit
			A ₀	A ₁	A ₂																							
9 $T_C = +25^\circ C$	LMHDX Fig. 6	91	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	
	LMHDX	92	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	
	LAVOX	93	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	
	LAVOX	94	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	15/	
10	Same tests, terminal conditions, and limits as subgroup 9, except $T_C = 125^\circ C$.																											
11	Same tests, terminal conditions, and limits as subgroup 9, except $T_C = -55^\circ C$.																											

- 1/ See appendix for description of algorithms.
- 2/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels during measurement shall be: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V. Forcing current I_{OL} shall be -4.0 mA.
- 3/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels during measurement shall be:

	V_{IL}	V_{IH}	I_{OL}
Types 02, 04	0.8 V	2.0 V	-8.0 mA

- 4/ $I_{CC} = 110$ mA for device type 02, 140 mA for device type 04.
- 5/ $I_{SB} = 10$ mA for device type 02; 30 mA for device type 04. The device manufacturer, may at his option, do either test or both tests.
- 6/ See 4.4.1c.
- 7/ $V_{IL} = GND$, $V_{IH} = 6.0$ V, pause time = 250 ms/loop max, \overline{CS} = high, only performed once at 125 °C, and $V_{CC} = 0.7$ V min.
- 8/ $V_{IL} = 0.8$ V and $V_{IH} = 2.0$ V.
- 9/ Algorithm has 60 ns where chip is deselected between the write.
- 10/ $V_{IL} = GND$, $V_{IH} = 3.0$ V, and all address setup times are at a minimum.
- 11/ $V_{IL} = GND$, $V_{IH} = 3.0$ V, and all write pulse timing are at minimums.
- 12/ $V_{IL} = GND$, $V_{IH} = 3.0$ V, and all address ending timing are at minimums.
- 13/ $V_{IL} = GND$, $V_{IH} = 3.0$ V, and tAVQV measured at minimum timing.
- 14/ $V_{IL} = GND$, $V_{IH} = 3.0$ V, tELQV1 and tELQV2 are measured at minimum timing.
- 15/ $V_{IL} = 0.0$ V, $V_{IH} = 3.0$ V, and all parameters are measured at minimum timing.
- 16/ tAVQV = 35 ns for device type 02; 55 ns for device type 04.
- 17/ tELQV1 and tELQV2 = 35 ns for device type 02; 65 ns for device type 04.
- 18/ tAVAV = 35 ns for device type 02; 55 ns for device type 04.
- 19/ tWLWH = 30 ns for device type 02; 40 ns for device type 04.
- 20/ tWHAX = 5 ns for device type 02; 5 ns for device type 04.
- 21/ tDVWH = 20 ns for device type 02; 20 ns for device type 04.
- 22/ tELWH = 30 ns for device type 02; 50 ns for device type 04.
- 23/ tAVWH = 30 ns for device type 02; 50 ns for device type 04.
- 24/ tAVWL = 30 ns for device type 02; 50 ns for device type 04.
- 25/ tAVQX is 0 ns for device type 02; 5 ns for device type 04.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown and electrical test procedure. When devices are measured at 25°C following application of the life or burn-in test condition, all devices shall be cooled to 35°C prior to removal of bias voltages.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

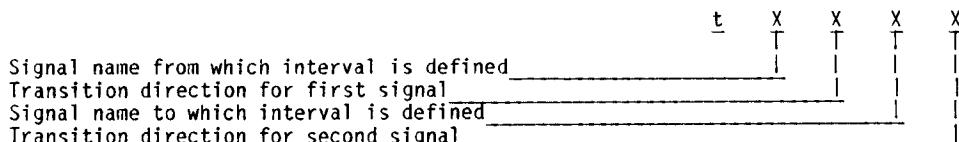
- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

V _{CC} - - - - - - - - - - -	Supply voltage
V _{SS} - - - - - - - - - - -	Common or reference voltage node
C _E - - - - - - - - - - -	Chip-selection, input
D _{IN} - - - - - - - - - - -	Data input
D _{OUT} - - - - - - - - - - -	Data output
A ₀ thru A ₁₁ - - - - - - - - -	Address input

WE - - - - -	Read or write input
I _{OHZ} - - - - -	High-impedance-state high output current
I _{OLZ} - - - - -	High-impedance-state low output current
I _{CC} - - - - -	Supply current from V _{CC} supply
tAVAV- - - - -	Read cycle time
tAVWL- - - - -	Address set-up time
tWLWH- - - - -	Write pulse width
tWHAX- - - - -	Write recovery time
tDVWH- - - - -	Data valid to end of write
tWHDX- - - - -	Data hold time
tAVQX- - - - -	Output hold time from address change
tAVQV- - - - -	Address access time
tELQV- - - - -	Chip selection to output valid
tAVAV- - - - -	Write cycle time
tELWH- - - - -	Chip selection to end of write
tAVWH- - - - -	Address valid to end of write
tELQX- - - - -	Chip selection to output active
tEHQZ- - - - -	Chip deselection to output in high impedance
tELPU- - - - -	Chip selection to power up time
tEHPD- - - - -	Chip deselection to power down time
tWLQZ- - - - -	Write enabled to output in high impedance
tWHQX- - - - -	Output active from end of write
I _{OZH} , I _{OZL} - - - - -	Output leakage current
T _C - - - - -	Case temperature
T _A - - - - -	Ambient temperature

6.3.1 Timing parameter abbreviations. All timing abbreviations used lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:

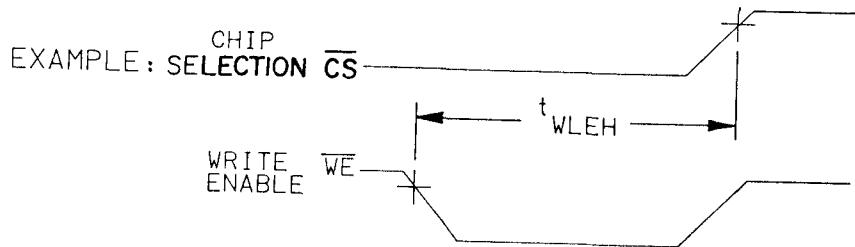


- a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output current
P = Supply current

- b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid
Z = Transition to off (high impedance)
U = Up
N = Down



The example shows Write pulse setup time defined as tWLEH-time from Write Enable to low to Chip Enable High.

- c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

- #### d. Waveforms

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
		HIGH IMPEDANCE

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type	CAGE number
01	7C147/Cypress Semiconductor	65786
02	7C148/Cypress Semiconductor	---
03	2147/Cypress Semiconductor	---
04	2148/Cypress Semiconductor	---

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static build up. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam or carriers.
- e. The use of plastic, rubber, or silk in MOS areas should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

APPENDIX

FUNCTIONAL ALGORITHMS

Functional algorithms are test patterns which define the exact sequence of tests used to verify proper operation of a random access memory (RAM). Each algorithm serves a specified purpose for the testing of the device.

10. FUNCTIONAL PATTERNS.

10.1 Pattern 1.CKBD

- a. Write a checkerboard pattern into memory (0 in address 0) from address 0 to N.
- b. When the CS off test is performed, attempt to write the complement pattern into cell memory with the device not selected.
- c. Read checkerboard pattern in the memory.

10.2 Pattern 2.

CKBD. Same as CKBD only with data complemented.

10.3 Pattern 3.MARCH

- a. Write test word into every location.
- b. The addressing is then scanned from location "0" to location "N".
- c. At each address, the test word is read and a complemented test word is written back into the same location.
- d. The addressing is then scanned in reverse from location "N" to location "0".
- e. At each address, the complemented test word is read and the test word is written back in.

10.4 Pattern 4.

GALPAT. This program will test all bits in the array. The addressing and interaction between bits for ac performance. The memory is initialized by writing a field of "1" and then a field of "0" into the cell memory.

- a. Write a "1" in word location 0 (reference location).
- b. Word 0 is read.
- c. Word 1 is read.
- d. Word 0 is read.
- e. Word 2 is read.
- f. Word 0 is read.
- g. The reading procedure continues back and forth between word 0 and the next higher number word until word 4095(01,03) or 1023(02,04) is reached. Then increment to the next word which becomes the reference location and then step a through g again until all the words in the memory are used at least once as a reference.

APPENDIX

10.5 Pattern 5.

Diagonal GALRESH (with row column ping pong read GG II). This pattern will test all bits in the array for writing interaction for switching performance.

- a. Initialize the memory by writing a field of 0's.
 - b. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping pong fashion:

R0 = Read "0"

WI = Write "1" etc.

	STEP								
	1	2	3	4	5	6	7	8	9
BACKGROUND BIT		RO		RO		RO		RO	
TEST BIT	RO		WI		RI		WO		RO

- c. Reinitialize the memory by writing a field of 1's.
 - b. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping pong fashion:

	STEP								
	1	2	3	4	5	6	7	8	9
BACKGROUND BIT		RI		RI		RI		RI	
TEST BIT	RI		WO		RO		WI		RI

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC
DLA - ES

**Preparing activity:
Air Force - 17**

Agent:

(Project 5962-0818)