INCH-POUND

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12 September 1988
SUPERSEDING
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25 July 1985

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS
16,384-BIT STATIC RANDOM ACCESS MEMORY (RAM)
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 16,384-bit static random access memory microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assured (RHA) products are reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as shown in the following:

Device type	Circuit organization	Access time
01	2,048 words/8 bits	150 ns
02	2,048 words/8 bits	210 ns (synchronous)
03	16,384 words/1 bit	85 ns
04	2,048 words/8 bits	90 ns
05	2,048 words/8 bits	200 ns
06	16,384 words/1 bit	45 ns
07 (RHA)	16,384 words/1 bit	150 ns
08 (RHA)	16,384 words/1 bit	175 ns
09	16,384 words/1 bit	70 ns
10	2,048 words/8 bits	70 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
X	C-12 (32-terminal, .560" x .458" x .120" maximum), leadless chip carrier package
Y	C-13 (20-terminal, .440" x .305" x .120" maximum), leadless chip carrier package
Z	F-6A (24-lead, .640" x .420" x .115" maximum) flat package

1.2.4 RHA level. Radiation hardness levels shall be as defined in MIL-M-38510.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.3 Absolute maximum ratings (device types 01 through 10).

Supply voltage range (V_{CC}-V_{SS})	-0.3 V dc to +7.0 V dc
Input voltage range	(V_{SS} -0.3 V) $\leq V_I \leq$ (V_{CC} +0.3 V)
Storage temperature range	-65°C to +150°C
Maximum dc output current	50 mA
Maximum power dissipation (P_D)	1 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J) 1/	+150°C
Thermal resistance, junction-to-case (θ_{JC}) 2/:	
Cases J, R, and Z	See MIL-M-38510, appendix C
Cases X and Y	14°C/W

1.4 Recommended operating conditions.

Supply voltages:	
V_{CCDR} (data retention supply voltage):	
Device types 01 through 06 and device types 09 and 10	2.0 V dc
Device types 07 and 08	3.0 V dc
V_{CC}	4.5 V dc minimum to 5.5 V dc maximum
V_{SS}	0 V dc
High level input voltage (V_{IH}) (all inputs):	
Device types 01, 03 through 06 and device types 09 and 10	V_{CC} -2.3 V to V_{CC} +0.3 V
Device type 02	V_{CC} -2.1 V to V_{CC} +0.3 V
Device type 07	V_{CC} -1.5 V to V_{CC} +0.3 V
Device type 08	2.3 V to V_{CC} +0.3 V
Low level input voltage (V_{IL}) (all inputs):	
All device types	V_{SS} -0.3 V to +0.8 V
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard, form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein. Die bonding may be performed using conductive silver paste or other epoxy. However, upon implementation of test method 5011 of MIL-STD-883, all epoxies must be qualified to this test method. Laser scribing shall be allowed only for SOS technology product and only to the backside of the wafer.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagrams. The block diagrams shall be as specified on figure 2.

3.2.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2.4 Truth tables. The truth tables shall be as specified on figure 3.

3.2.5 Functional tests. The functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.2.6 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.4.1 Post-irradiation performance characteristics. The electrical performance characteristics of the RHA devices at the RHA level are as specified in table I and apply at an ambient temperature of +25°C ±5°C.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.6.1 Serialization. All class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10).

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified		Device types	Limits Min	Limits Max	Unit
Operating supply current	I_{CC1}	Addresses cycling f = 1 MHz $\overline{CE}$ = V_{IL}, I_O = 0 (outputs are open)		01,04,05, 10		70	mA
				02		10	
				03,09		50	
				06		100	
Standby supply current	I_{CC2}	Addresses stable $\overline{CE}$ = V_{CC} -0.3 V, I_O = 0		01,02,03, 04,05,09, 10		100	µA
				03,09		5	mA
	I_{CC3}	Address stable $\overline{CE}$ = V_{IH}, I_O = 0		01,04,05, 06,10		10	
Data retention supply current	I_{CC4}	V_{CC} = 2.0 V, I_O = 0 $\overline{CE}$ = V_{CC} -0.3 V		01,02,03, 04,05,09, 10		50	µA
Low level output voltage	V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4.0 mA	01,04,05,06 10		0.4	V
			I_{OL} = 3.2 mA	02		0.4	
			I_{OL} = 8.0 mA	03,09		0.4	
High level output voltage	V_{OH}	V_{CC} = 4.5 V	I_{OH} = -1.0 mA	01,02,04, 05,06,10	2.4		V
			I_{OH} = -4.0 mA	03,09	2.4		
Input leakage current	I_{IL}	V_{IN} = GND		01,04,05, 10	-1	1	µA
	I_{IH}	V_{IN} = 5.5 V		02,03,09	-1	1	
				06	-10	10	
High impedance output leakage current	I_{OLZ}	V_{OUT} = GND	$\overline{CE}$ = V_{IH}	01,03,04, 05,09,10	-1	1	µA
	I_{OHZ}	V_{OUT} = 5.5 V		02	-1	1	
				06	-20	20	
Input capacitance	C_I	T_C = +25°C, V_{CC} = GND V_{IN} = GND, f = 1 MHz		01,03,04, 05,06,09,10		10	pF
				02		12	

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10) - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Output capacitance	C_O	T_C = +25°C, V_{CC} = GND V_{IN} = GND, f = 1 MHz	01,03,04, 05,06,09,10		12	pF
			02		14	
Read or write cycle time	t_{AVAV}	V_{CC} = 4.5 V to 5.5 V See figure 5	01	150		ns
			03	85		
			04	90		
			05	200		
			06	45		
			09	70		
			10	70		
Address access time	t_{AVQV}		01		150	ns
			02		200	
			03		85	
			04		90	
			05		200	
			06		45	
			09		70	
			10		70	
Chip enable access time	t_{ELQV}		01		150	ns
			02		200	
			03		85	
			04		90	
			05		200	
			06		45	
			09		70	
			10		70	
Chip disable to output disable time	t_{EHQZ}		01,04		50	ns
			02		80	
			03		40	
			05		60	
			06		25	
			09		40	
			10		40	
Output hold after address change	t_{AVQX}		01,05	0		ns
			06	3		
			03,04, 09,10	5		
Chip enable to output active	t_{ELQX}		01,05	0		ns
			02	10		
			06	3		
			03,04, 09,10	5		

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10) - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Write pulse width	t_{WLWH}	V_{CC} = 4.5 V to 5.5 V See figure 5	01	90		ns
			02	200		
			03	45		
			04	55		
			05	120		
			06	30		
			09	40		
			10	40		
Chip enable to end-of-write	t_{ELWH}		01	90		ns
			02	200		
			03	65		
			04	55		
			05	120		
			06	35		
			09	55		
			10	45		
Data setup to end-of-write	t_{DVWH}		01	50		ns
			02	80		
			03	35		
			04	30		
			05	70		
			06	25		
			09	30		
			10	30		
Data hold after end-of-write	t_{WHDX}		01,04,05	15		ns
			02	10		
			03,09	0		
			06	5		
			10	10		
Address setup before write low	t_{AVWL}		01,04,05, 10	10		ns
			06	5		
			03,09	0		
Address setup to end-of-write	t_{AVWH}		01	120		ns
			03	65		
			04	80		
			05	140		
			06	35		
			09	55		
			10	50		
Write recovery time	t_{WHAX}		01,04,05, 10	10		ns
			06	5		
			03,09	0		

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10) - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Output enable access time	t_{OLQV}	V_{CC} = 4.5 V to 5.5 V See figure 5	01		75	ns
			02		80	
			04		65	
			05		100	
			10		50	
Output enable to output active	t_{OLQX}		01,04,05	0		ns
			02	10		
			10	5		
Output enable to output active	t_{OHQZ}		01,05		60	ns
			02		80	
			04		40	
			10		35	
Address to chip enable setup time	t_{AVEL}		02	0		ns
Address to chip enable hold time	t_{ELAX}		02	50		ns
Chip enable pulse negative width	t_{ELEH}		02	200		ns
Chip enable pulse positive width	t_{EHEL}		02	80		ns
Write enable pulse setup time	t_{WLEH}		02	200		ns
Read or write cycle time	t_{ELEL}		02	280		ns

TABLE I. Electrical performance characteristics (device types 07 and 08).

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Low level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 5.0 mA	07 08		0.4 0.4	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -5.0 mA	07 08	4.0 4.0		V
Input leakage current	I_{IH}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	07 08		1.0 1.0	µA
Input leakage current	I_{IL}	V_{CC} = 5.5 V; V_{IN} = GND	07 08		-1.0 -1.0	µA
High impedance output leakage	I_{OHZ}	V_{CC} = 5.5 V	07 08		10.0 10.0	µA
High impedance	I_{OLZ}	V_{CC} = 5.5 V	07 08		-10.0 -10.0	µA
Standby supply	I_{CC}	V_{CC} = 5.5 V	07 08		200 5	µA mA
Data retention supply voltage	V_{CCDR}	V_{CC} = 3.0 V minimum (see power down test in table III)	07 08	3.0 3.0		V
Operating current	I_{CCOP}	T_C = +25°C, V_{CC} = 5.5 V f = 1 MHz	07 08		6 6	mA
Data retention quiescent supply current	I_{CCDR}	V_{CC} = 3.0 V; I_O = 0; V_I = V_{CC} or GND	07 08		100 100	µA
Input capacitance	C_i	V_{CC} = 5.5 V; V_{IN} = V_{CC} or GND f = 1 MHz	07 08		8 8	pF
Address access time	t_{AVQV}	See table III	07 08		150 175	ns
Chip enable access	t_{ELQV}		07 08		150 175	ns
Read cycle time	t_{AVAV}		07 08	150 175		ns
Chip enable output time	t_{ELQX}		07 08	20 40		ns

TABLE I. Electrical performance characteristics (device types 07 and 08) - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Chip enable output disable	t_{EHQZ} 1/	See table III	07 08		25 50	ns
Chip enable pulse negative width	t_{ELEH}		07 08	100 125		ns
Chip disable output hold time	t_{EHQX} 1/		07 08	20 40		ns
Address setup time	t_{AVEL}		07 08	0 0		ns
Address invalid output hold time	t_{AXQX} 1/		07 08	40 60		ns
Write enable pulse width	t_{WLWH}		07 08	75 100		ns
Write enable pulse setup time	t_{WLEH}		07 08	100 125		ns
Address setup time	t_{AVWL}		07 08	10 10		ns
Chip enable to end-of-write	t_{ELWH}	See table III I_O = 0; V_I = V_{CC} or GND	07 08	100 125		ns
Write disable output enable time	t_{WHQX} 1/	See table III	07 08	0 0		ns
Address valid to end-of-write	t_{AVWH}		07 08	100 125		ns
Address hold time	t_{WHAX}		07 08	20 25		ns
Address hold time	t_{EHAX}		07 08	0 0		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics (device types 07 and 08) - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, V_{CC} = 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Address valid to end-of-write	t_{AVEH}	See table III	07 08	100 125		ns
Write enable output disable time	t_{WLQZ} 1/		07 08		25 50	ns
Data setup time	t_{DVWH}		07 08	75 100		ns
Data hold time	t_{WHDX}		07 08	20 20		ns
Data setup time	t_{DVEH}		07 08	75 100		ns
Data hold time	t_{EHDX}		07 08	0 0		ns

1/ This parameter is guaranteed but not tested.

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Class S devices 1/ 2/ Reference paragraph	Table III 3/ sub-groups	Table IV 4/ delta limits	Test circuit figure	Table V 5/ sub-groups	Class B devices 1/ 2/ Reference paragraph	Table III 3/ sub-groups	Table IV 4/ delta limits	Test circuit figure	Table V 5/ sub-groups
1	Interim electrical parameters, method 5004		1					2,8* (hot only) 10			
2	Static burn-in, method 1015	4.2b 4.5.2			4						
3	Same as 6/ line 1		1*	Δ							
4	Dynamic burn-in, method 1015	4.2b 4.5.2	7/		4		4.2b 4.5.2	7/		4	
5	Same as line 1	4.2d	1*	Δ			4.2d	1*	Δ		
6	Final electrical parameters, method 5004		1*,2, 3,8,9, 10,11					1*,2, 3,7,8, 9,10 11			

See footnotes at end of table.

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Class S devices 1/ 2/					Class B devices 1/ 2/				
		Reference paragraph	Table III 3/ sub-groups	Table IV 4/ delta limits	Test circuit figure	Table V 5/ sub-groups	Reference paragraph	Table III 3/ sub-groups	Table IV 4/ delta limits	Test circuit figure	Table V 5/ sub-groups
7	Group A test requirements, method 5005	4.4.1	1,2,3, 4,8,9, 10,11, 12				4.4.1	1,2,3, 4,7,8, 9,10, 11			
8	Group B test requirements method 5005	4.4.2	1,2,4, 8,9, 10,11	Δ			4.4.2 4.5.3	1 8/			
9	Group C end-point electrical parameters, method 5005						4.4.3	1,7,9	Δ		
10	Group D end-point electrical parameters, method 5005	4.4.4	1,2,3				4.4.4	1,7,9			
11	Group E end-point electrical parameters, method 5005	4.5.6			Table V	1,2	4.5.6				1,2

1/ Blank spaces indicate tests are not applicable.
2/ For subgroups 9, 10, and 11, only the worst value measured per device need be recorded when variables data is required (e.g., during qualification).
3/ (*) indicates PDA applies to subgroup 1 (see 4.2.1).
4/ (Δ) indicates delta limit shall be required, and delta values shall be computed with reference to the previous interim electrical parameters (see 4.5.3).
5/ As applicable in group E of MIL-STD-883.
6/ The device manufacturer may, at his option, delete line number 3.
7/ The device manufacturer may, at his option, either perform delta measurements, or within 24 hours after burn-in (removal of temperature or bias), perform the final electrical parameter measurements, subgroup A1.
8/ Applies to electrostatic discharge sensitivity tests.

TABLE III. Group A inspection for device types 01 and 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DQ_0	DQ_1	DQ_2	V_{SS}	DQ_3
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	GND	3/
	I_{CC2}		2	4/	4/	4/	4/	4/	4/	4/	4/	"	"	"	"	"
	I_{CC3}		3	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"
	I_{CC4}		4	6/	6/	6/	6/	6/	6/	6/	6/	"	"	"	"	"
	I_{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V
			6	5.5 V	GND	5.5 V	"	"	"	"	"	"	"	"	"	"
			7	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"
			8	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"
			9	"	"	"	5.5 V	GND	"	"	"	"	"	"	"	"
			10	"	"	"	"	5.5 V	GND	"	"	"	"	"	"	"
			11	"	"	"	"	"	5.5 V	GND	"	"	"	"	"	"
			12	"	"	"	"	"	"	5.5 V	GND	"	"	"	"	"
			13	"	"	"	"	"	"	"	5.5 V	GND	"	"	"	"
			14	"	"	"	"	"	"	"	"	5.5 V	GND	"	"	"
			15	"	"	"	"	"	"	"	"	"	5.5 V	GND	"	"
			16	"	"	"	"	"	"	"	"	"	"	5.5 V	"	GND
			17	"	"	"	"	"	"	"	"	"	"	"	"	5.5 V
			18	"	"	"	"	"	"	"	"	"	"	"	"	"
			19	"	"	"	"	"	"	"	"	"	"	"	"	"
			20	"	"	"	"	"	"	"	"	"	"	"	"	"
			21	"	"	"	"	"	"	"	"	"	"	"	"	"
			22	"	"	"	"	"	"	"	"	"	"	"	"	"
			23	"	"	"	"	"	"	"	"	"	"	"	"	"
			24	"	"	"	"	"	"	"	"	"	"	"	"	"
			25	"	"	"	"	"	"	"	"	"	"	"	"	"
			26	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{IH}	3010	27	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	GND
			28	GND	5.5 V	GND	"	"	"	"	"	"	"	"	"	"
			29	"	GND	5.5 V	"	"	"	"	"	"	"	"	"	"
			30	"	"	GND	5.5 V	"	"	"	"	"	"	"	"	"
			31	"	"	"	GND	5.5 V	"	"	"	"	"	"	"	"
			32	"	"	"	"	GND	5.5 V	"	"	"	"	"	"	"
			33	"	"	"	"	"	GND	5.5 V	"	"	"	"	"	"
			34	"	"	"	"	"	"	GND	5.5 V	"	"	"	"	"
			35	"	"	"	"	"	"	"	GND	5.5 V	"	"	"	"
			36	"	"	"	"	"	"	"	"	GND	5.5 V	"	"	"
			37	"	"	"	"	"	"	"	"	"	GND	5.5 V	"	"
			38	"	"	"	"	"	"	"	"	"	"	GND	"	5.5 V
			39	"	"	"	"	"	"	"	"	"	"	"	"	GND
			40	"	"	"	"	"	"	"	"	"	"	"	"	"
			41	"	"	"	"	"	"	"	"	"	"	"	"	"
			42	"	"	"	"	"	"	"	"	"	"	"	"	"
			43	"	"	"	"	"	"	"	"	"	"	"	"	"
			44	"	"	"	"	"	"	"	"	"	"	"	"	"
			45	"	"	"	"	"	"	"	"	"	"	"	"	"
			46	"	"	"	"	"	"	"	"	"	"	"	"	"
			47	"	"	"	"	"	"	"	"	"	"	"	"	"
			48	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of device types 01 and 05.

TABLE III. Group A inspection for device types 01 and 05 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	19	20	21	22	23	24	25	26	28	29	32	Measured terminal	Test limits		Unit
			Case J	14	15	16	17	18	19	20	21	22	23	24		Min	Max	
			Test no.	DQ_4	DQ_5	DQ_6	DQ_7	$\overline{CE}$	A_{10}	$\overline{OE}$	$\overline{WE}$	A_9	A_8	V_{CC}				
1 T_C = +25°C	I_{CC1}	3005	1	3/	3/	3/	3/	2/	2/	2/	2/	2/	2/	5.5 V	V_{CC}		90	mA
	I_{CC2}		2	"	"	"	"	4/	4/	4/	4/	4/	4/	"	"		100	µA
	I_{CC3}		3	"	"	"	"	5/	5/	5/	5/	5/	5/	"	"		10	mA
	I_{CC4}		4	"	"	"	"	6/	6/	6/	6/	6/	6/	2.0 V	"		100	µA
	I_{IL}	3009	5	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A_7		-2	µA
			6	"	"	"	"	"	"	"	"	"	"	"	A_6		"	"
			7	"	"	"	"	"	"	"	"	"	"	"	A_5		"	"
			8	"	"	"	"	"	"	"	"	"	"	"	A_4		"	"
			9	"	"	"	"	"	"	"	"	"	"	"	A_3		"	"
			10	"	"	"	"	"	"	"	"	"	"	"	A_2		"	"
			11	"	"	"	"	"	"	"	"	"	"	"	A_1		"	"
			12	"	"	"	"	"	"	"	"	"	"	"	A_0		"	"
			13	"	"	"	"	GND	"	"	"	"	"	"	DQ_0		"	"
			14	"	"	"	"	"	"	"	"	"	"	"	DQ_1		"	"
			15	"	"	"	"	"	"	"	"	"	"	"	DQ_2		"	"
			16	"	"	"	"	"	"	"	"	"	"	"	DQ_3		"	"
			17	GND	"	"	"	"	"	"	"	"	"	"	DQ_4		"	"
			18	5.5 V	GND	"	"	"	"	"	"	"	"	"	DQ_5		"	"
			19	"	5.5 V	GND	"	"	"	"	"	"	"	"	DQ_6		"	"
			20	"	"	5.5 V	GND	"	"	"	"	"	"	"	DQ_7		"	"
			21	"	"	"	5.5 V	"	"	"	"	"	"	"	$\overline{CE}$		"	"
			22	"	"	"	"	5.5 V	GND	"	"	"	"	"	A_{10}		"	"
			23	"	"	"	"	"	5.5 V	GND	"	"	"	"	$\overline{OE}$		"	"
			24	"	"	"	"	"	"	5.5 V	GND	"	"	"	$\overline{WE}$		"	"
			25	"	"	"	"	"	"	"	5.5 V	GND	"	"	A_9		"	"
			26	"	"	"	"	"	"	"	5.5 V	5.5 V	GND	"	A_8		"	"
	I_{IH}	3010	27	GND	GND	GND	GND	GND	GND	GND	GND	"	GND	"	A_7		2	"
			28	"	"	"	"	"	"	"	"	"	"	"	A_6		"	"
			29	"	"	"	"	"	"	"	"	"	"	"	A_5		"	"
			30	"	"	"	"	"	"	"	"	"	"	"	A_4		"	"
			31	"	"	"	"	"	"	"	"	"	"	"	A_3		"	"
			32	"	"	"	"	"	"	"	"	"	"	"	A_2		"	"
			33	"	"	"	"	"	"	"	"	"	"	"	A_1		"	"
			34	"	"	"	"	"	"	"	"	"	"	"	A_0		"	"
			35	"	"	"	"	"	"	2.2 V	"	"	"	"	DQ_0		"	"
			36	"	"	"	"	"	"	"	"	"	"	"	DQ_1		"	"
			37	"	"	"	"	"	"	"	"	"	"	"	DQ_2		"	"
			38	"	"	"	"	"	"	"	"	"	"	"	DQ_3		"	"
			39	5.5 V	"	"	"	"	"	"	"	"	"	"	DQ_4		"	"
			40	GND	5.5 V	"	"	"	"	"	"	"	"	"	DQ_5		"	"
			41	"	GND	5.5 V	"	"	"	"	"	"	"	"	DQ_6		"	"
			42	"	"	GND	5.5 V	"	"	"	"	"	"	"	DQ_7		"	"
			43	"	"	"	GND	2.2 V	"	GND	"	"	"	"	$\overline{CE}$		"	"
			44	"	"	"	"	GND	5.5 V	GND	"	"	"	"	A_{10}		"	"
			45	"	"	"	"	"	GND	5.5 V	"	"	"	"	$\overline{OE}$		"	"
			46	"	"	"	"	"	"	GND	5.5 V	"	"	"	$\overline{WE}$		"	"
			47	"	"	"	"	"	"	"	GND	5.5 V	"	"	A_9		"	"
			48	"	"	"	"	"	"	"	GND	GND	5.5 V	"	A_8		"	"

TABLE III. Group A inspection for device types 01 and 05 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DQ_0	DQ_1	DQ_2	V_{SS}	DQ_3
1 T_C = +25°C	I_{OLZ}	3020	49									GND	5.5 V	5.5 V	GND	5.5 V
			50									5.5 V	GND	5.5 V	"	"
			51									"	5.5 V	GND	"	"
			52									"	"	5.5 V	"	GND
			53									"	"	"	"	5.5 V
			54									"	"	"	"	"
			55									"	"	"	"	"
			56									"	"	"	"	"
	I_{OHZ}	3021	57									"	GND	GND	"	GND
			58									GND	5.5 V	GND	"	"
			59									"	GND	5.5 V	"	"
			60									"	"	GND	"	5.5 V
			61									"	"	"	"	GND
			62									"	"	"	"	"
			63									"	"	"	"	"
			64									"	"	"	"	"
	V_{OL} 7/	3007	65	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	8/
			66	"	"	"	"	"	"	"	"	"	"	"	"	"
			67	"	"	"	"	"	"	"	"	"	"	"	"	"
			68	"	"	"	"	"	"	"	"	"	"	"	"	"
			69	"	"	"	"	"	"	"	"	"	"	"	"	"
			70	"	"	"	"	"	"	"	"	"	"	"	"	"
			71	"	"	"	"	"	"	"	"	"	"	"	"	"
			72	"	"	"	"	"	"	"	"	"	"	"	"	"
	V_{OH} 7/	3006	73	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	"	9/
			74	"	"	"	"	"	"	"	"	"	"	"	"	"
			75	"	"	"	"	"	"	"	"	"	"	"	"	"
			76	"	"	"	"	"	"	"	"	"	"	"	"	"
			77	"	"	"	"	"	"	"	"	"	"	"	"	"
			78	"	"	"	"	"	"	"	"	"	"	"	"	"
			79	"	"	"	"	"	"	"	"	"	"	"	"	"
			80	"	"	"	"	"	"	"	"	"	"	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.															
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.															
4 T_C = +25°C	C_i	3012	81	10/	10/	10/	10/	10/	10/	10/	10/				GND	
	C_o		82									10/	10/	10/	"	10/
9 T_C = +25°C	NOT WRITE	See fig. 8	83	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	"	11/
			84	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	"	11/
	WRITE/ WRITE	See fig. 9	85	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	"	12/
			86	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	"	12/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.															
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.															

See footnotes at end of device types 01 and 05.

TABLE III. Group A inspection for device types 01 and 05 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X / Case J / Test no.	19 / 14 / DQ_4	20 / 15 / DQ_5	21 / 16 / DQ_6	22 / 17 / DQ_7	23 / 18 / $\overline{CE}$	24 / 19 / A_{10}	25 / 20 / $\overline{OE}$	26 / 21 / $\overline{WE}$	28 / 22 / A_9	29 / 23 / A_8	32 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{OLZ}	3020	49	5.5 V	5.5 V	5.5 V	5.5 V	2.2 V		2.2 V	5.5 V			5.5 V	DQ_0		-10	µA
			50	"	"	"	"	"		"	"			"	DQ_1		"	"
			51	"	"	"	"	"		"	"			"	DQ_2		"	"
			52	"	"	"	"	"		"	"			"	DQ_3		"	"
			53	GND	"	"	"	"		"	"			"	DQ_4		"	"
			54	5.5 V	GND	"	"	"		"	"			"	DQ_5		"	"
			55	"	5.5 V	GND	"	"		"	"			"	DQ_6		"	"
			56	"	5.5 V	5.5 V	GND	"		"	"			"	DQ_7		"	"
	I_{OHZ}	3021	57	GND	GND	GND	"	"		"	"			"	DQ_0		10	"
			58	"	"	"	"	"		"	"			"	DQ_1		"	"
			59	"	"	"	"	"		"	"			"	DQ_2		"	"
			60	"	"	"	"	"		"	"			"	DQ_3		"	"
			61	5.5 V	"	"	"	"		"	"			"	DQ_4		"	"
			62	GND	5.5 V	"	"	"		"	"			"	DQ_5		"	"
			63	"	GND	5.5 V	"	"		"	"			"	DQ_6		"	"
			64	"	GND	GND	5.5 V	"		"	"			"	DQ_7		"	"
	V_{OL} 7/	3007	65	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	DQ_0		0.4	V
			66	"	"	"	"	"	"	"	"	"	"	"	DQ_1		"	"
			67	"	"	"	"	"	"	"	"	"	"	"	DQ_2		"	"
			68	"	"	"	"	"	"	"	"	"	"	"	DQ_3		"	"
			69	"	"	"	"	"	"	"	"	"	"	"	DQ_4		"	"
			70	"	"	"	"	"	"	"	"	"	"	"	DQ_5		"	"
			71	"	"	"	"	"	"	"	"	"	"	"	DQ_6		"	"
			72	"	"	"	"	"	"	"	"	"	"	"	DQ_7		"	"
	V_{OH} 7/	3006	73	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	"	DQ_0	2.4		"
			74	"	"	"	"	"	"	"	"	"	"	"	DQ_1	"		"
			75	"	"	"	"	"	"	"	"	"	"	"	DQ_2	"		"
			76	"	"	"	"	"	"	"	"	"	"	"	DQ_3	"		"
			77	"	"	"	"	"	"	"	"	"	"	"	DQ_4	"		"
			78	"	"	"	"	"	"	"	"	"	"	"	DQ_5	"		"
			79	"	"	"	"	"	"	"	"	"	"	"	DQ_6	"		"
			80	"	"	"	"	"	"	"	"	"	"	"	DQ_7	"		"
2																		
3																		
4 T_C = +25°C	C_i	3012	81					10/	10/	10/	10/	10/	10/	10/	All inputs		8	pF
	C_o		82	10/	10/	10/	10/								All outputs		10	pF
9 T_C = +25°C	NOT WRITE	See fig. 8	83	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	All outputs	11/	11/	ns
			84	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	5.5 V		11/	11/	ns
	WRITE/ WRITE	See fig. 9	85	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	4.5 V	All outputs	12/	12/	ns
			86	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V		12/	12/	ns
10																		
11																		

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.

2/ All inputs levels and timing edges are set to table I limits with read cycle timing; V_{IL} = 0.4 V and V_{IH} = 2.2 V for device types 01 and 05.

3/ Outputs loaded with load as specified on figure 6.

4/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = 2.2 V for device types 01 and 05.

5/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = V_{CC} -0.3 V.

6/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

7/ For V_{OL} or V_{OH}, testing all terminals, only the worst case variables data shall be recorded, and variables data for each failed terminal. Attributes data otherwise.

8/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IL} = 0.8 V, I_{OL} = 2.0 mA.

9/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IH} = 2.2 V, I_{OH} = -1.0 mA.

10/ See 4.4.1c.

11/ Since the object of the NOT WRITE pattern (see figure 8) is to verify that the device may not be written into when it is disabled, the waveforms shown on figure 5 may be applied using nominal timing. The outputs shall be loaded with the load specified on figure 6.

12/ Timing waveforms shown on figure 5 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 9). This procedure ensures that the following parameters meet the specified limits:

Parameter	Limits				Unit
	Device type 01		Device type 05		
	Min	Max	Min	Max	
t_{AVAV}	150	---	200	---	ns
t_{AVQV}	---	150	---	200	"
t_{AVQX}	0	---	0	---	"
t_{OLQX}	0	---	0	---	"
t_{OLQV}	---	75	100	---	"
t_{OHQZ}	---	60	---	60	"
t_{ELQV}	150	---	---	200	"
t_{ELQX}	0	---	0	---	"
t_{EHQZ}	---	50	---	60	"
t_{AVEL}	---	---	---	---	"
t_{ELAX}	---	---	---	---	"
t_{ELEH}	---	---	---	---	"
V_{IL}	0.0		0.0		V
V_{IH}	2.2		2.2		"
Output compare level V_{OL}	0.4		0.4		"
Output compare level V_{OH}	2.4		2.4		"
Read cycle timing					

Parameter	Limits				Unit
	Device type 01		Device type 05		
	Min	Max	Min	Max	
t_{WHAV}	10	---	10	---	ns
t_{ELWH}	90	---	120	---	"
t_{AVWH}	120	---	140	---	"
t_{AVWL}	10	---	10	---	"
t_{WLWH}	90	---	120	---	"
t_{DVWH}	50	---	70	---	"
t_{WHDX}	15	---	15	---	"
t_{WLEH}	---	---	---	---	"
V_{IL}	0.0		0.0		V
V_{IH}	2.2		2.2		"
Output compare level V_{OL}	0.4		0.4		"
Output compare level V_{OH}	2.4		2.4		"
Write cycle timing					

The output shall be loaded with the load specified on figure 6. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X / Case J / Test no.	4 / 1 / A_7	5 / 2 / A_6	6 / 3 / A_5	7 / 4 / A_4	8 / 5 / A_3	9 / 6 / A_2	10 / 7 / A_1	11 / 8 / A_0	13 / 9 / DQ_0	14 / 10 / DQ_1	15 / 11 / DQ_2	16 / 12 / V_{SS}	18 / 13 / DQ_3	19 / 14 / DQ_4	20 / 15 / DQ_5
1 T_C = +25°C	I_{CC1} I_{CC2} I_{CC4}	3005	1 2 3	2/ GND "	2/ GND GND	2/ GND GND	2/ GND GND	2/ GND GND	2/ GND GND	2/ GND GND	2/ GND GND	3/ " "	3/ " "	3/ " "	GND " "	3/ " "	3/ " "	3/ " "
	I_{IL}	3009	4 5 6 7 8 9 10 11 12 13 14 15 16 17	" V_{CC} " " " " " " " " " " " "	V_{CC} GND V_{CC} " " " " " " " " " "	V_{CC} V_{CC} GND V_{CC} " " " " " " " " "	V_{CC} " GND V_{CC} " " " " " " " " "	V_{CC} " " GND V_{CC} " " " " " " " "	V_{CC} " " " GND V_{CC} " " " " " " "	V_{CC} " " " " GND V_{CC} " " " " " "	V_{CC} " " " " " GND V_{CC} " " " " "				" " " " " " " " " " " " "			
	I_{IH}	3010	18 19 20 21 22 23 24 25 26 27 28 29 30 31	" GND " " " " " " " " " " " "	GND V_{CC} GND " " " " " " " " " "	GND GND V_{CC} GND " " " " " " " " "	GND " " V_{CC} GND " " " " " " " "	GND " " " V_{CC} GND " " " " " " "	GND " " " " V_{CC} GND " " " " " "	GND " " " " " V_{CC} GND " " " " "	GND " " " " " " V_{CC} GND " " " "				" " " " " " " " " " " " "			
	I_{OLZ}	3020	32 33 34 35 36 37 38 39									GND V_{CC} " " " " " "	V_{CC} GND V_{CC} " " " " "	V_{CC} V_{CC} GND V_{CC} " " " "	" " " " " " " "	V_{CC} " GND V_{CC} " " " "	V_{CC} " " GND V_{CC} " " "	V_{CC} " " " GND V_{CC} V_{CC}
	I_{OHZ}	3021	40 41 42 43 44 45 46 47									" GND " " " " " "	GND V_{CC} GND " " " " "	GND GND V_{CC} GND " " " "	" " " " " " " "	GND " " V_{CC} GND " " "	GND " " " V_{CC} GND " "	GND " " " " V_{CC} GND GND
	V_{OL} V_{OH}	3007 3006	48-55 56-63	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	" "	4/ 5/	4/ 5/	4/ 5/

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X / Case J / Test no.	21 / 16 / DQ_6	22 / 17 / DQ_7	23 / 18 / $\overline{CE}$	24 / 19 / A_{10}	25 / 20 / $\overline{OE}$	26 / 21 / $\overline{WE}$	28 / 22 / A_9	29 / 23 / A_8	32 / 24 / V_{CC}	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{CC1}	3005	1	3/	3/	2/	2/	2/	GND	2/	2/	5.5 V	1 MHz	V_{CC}		10	mA
	I_{CC2}		2	"	"	5.2 V	GND	GND	GND	GND	GND	5.5 V				100	µA
	I_{CC4}		3	"	"	1.7 V	GND	GND	GND	GND	GND	2.0 V		"		50	"
	I_{IL}	3009	4			V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	5.5 V		A_7	-1	1	"
			5			"	"	"	"	"	"	"		A_6	"	"	"
			6			"	"	"	"	"	"	"		A_5	"	"	"
			7			"	"	"	"	"	"	"		A_4	"	"	"
			8			"	"	"	"	"	"	"		A_3	"	"	"
			9			"	"	"	"	"	"	"		A_2	"	"	"
			10			"	"	"	"	"	"	"		A_1	"	"	"
			11			"	"	"	"	"	"	"		A_0	"	"	"
			12			GND	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			13			V_{CC}	GND	"	"	"	"	"		A_{10}	"	"	"
			14				V_{CC}	GND	"	"	"	"		$\overline{OE}$	"	"	"
			15			"	"	V_{CC}	GND	"	"	"		$\overline{WE}$	"	"	"
			16			"	"	"	V_{CC}	GND	"	"		A_9	"	"	"
			17			"	"	"	V_{CC}	V_{CC}	GND	"		A_8	"	"	"
	I_{IH}	3010	18			GND	GND	GND	GND	GND	"	"		A_7	"	"	"
			19			"	"	"	"	"	"	"		A_6	"	"	"
			20			"	"	"	"	"	"	"		A_5	"	"	"
			21			"	"	"	"	"	"	"		A_4	"	"	"
			22			"	"	"	"	"	"	"		A_3	"	"	"
			23			"	"	"	"	"	"	"		A_2	"	"	"
			24			"	"	"	"	"	"	"		A_1	"	"	"
			25			"	"	"	"	"	"	"		A_0	"	"	"
			26			V_{CC}	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			27			GND	V_{CC}	"	"	"	"	"		A_{10}	"	"	"
			28			"	GND	V_{CC}	"	"	"	"		$\overline{OE}$	"	"	"
			29			"	"	GND	V_{CC}	"	"	"		$\overline{WE}$	"	"	"
			30			"	"	"	GND	V_{CC}	"	"		A_9	"	"	"
			31			"	"	"	GND	GND	V_{CC}	"		A_8	"	"	"
	I_{OLZ}	3020	32	V_{CC}	V_{CC}	2.2 V		2.2 V				"		DQ_0	"	"	"
			33	"	"	"		"				"		DQ_1	"	"	"
			34	"	"	"		"				"		DQ_2	"	"	"
			35	"	"	"		"				"		DQ_3	"	"	"
			36	"	"	"		"				"		DQ_4	"	"	"
			37	"	"	"		"				"		DQ_5	"	"	"
			38	GND	"	"		"				"		DQ_6	"	"	"
			39	V_{CC}	GND	"		"				"		DQ_7	"	"	"
	I_{OHZ}	3021	40	GND	"	"		"				"		DQ_0	"	"	"
			41	"	"	"		"				"		DQ_1	"	"	"
			42	"	"	"		"				"		DQ_2	"	"	"
			43	"	"	"		"				"		DQ_3	"	"	"
			44	"	"	"		"				"		DQ_4	"	"	"
			45	"	"	"		"				"		DQ_5	"	"	"
			46	V_{CC}	"	"		"				"		DQ_6	"	"	"
			47	GND	V_{CC}	"		"				"		DQ_7	"	"	"
	V_{OL}	3007	48-55	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V		DQ_0-DQ_7		0.4	V
	V_{OH}	3006	56-63	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V		DQ_0-DQ_7	2.4		V

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DQ_0	DQ_1	DQ_2	V_{SS}	DQ_3	DQ_4	DQ_5
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.																	
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																	
4 T_C = +25°C	C_{in} C_{out}	3012	64 65	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND "	6/	6/	6/
7 T_C = +25°C	I/O V_{DR}	Function tests	66 67	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	" "	7/ 8/	7/ 8/	7/ 8/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																	
9 T_C = +25°C	Functional tests		68 69	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	GND "	9/ 9/	9/ 9/	9/ 9/
	t_{ELQV}		70 71												" "			
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.																	
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X / Case J / Test no.	21 / 16 / DQ_6	22 / 17 / DQ_7	23 / 18 / $\overline{CE}$	24 / 19 / A_{10}	25 / 20 / $\overline{OE}$	26 / 21 / $\overline{WE}$	28 / 22 / A_9	29 / 23 / A_8	32 / 24 / V_{CC}	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
2																	
3																	
4 T_C = +25°C	C_{in} C_{out}	3012	64 65	6/	6/	6/	6/	6/	6/	6/	6/			Input Output		12 14	pF pF
7 T_C = +25°C	I/O V_{DR}	Function tests	66 67	7/ 10/	7/ 10/	7/	7/	7/	7/	7/	7/	4.5 V 2.0 V	Pattern 5 Pattern 4				
8																	
9 T_C = +25°C	Func-tional tests		68 69	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	4.5 V 5.5 V	Patterns 1,3,5 Patterns 1,3,5	DQ DQ			
	t_{ELQV}		70 71									4.5 V 5.5 V	Pattern 3 Pattern 3	DQ DQ		200 200	ns ns
10																	
11																	

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.

2/ All inputs levels and timing edges are set to table I limits with read cycle timing: For device type 02, outputs are open. I_O = 0 mA. Device type 02 inputs = GND and V_{CC}.

3/ Outputs loaded with load as specified on figure 6.

4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IL} = 0.8 V, I_{OL} = 3.2 mA.

5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IH} = 2.4 V, I_{OH} = -1.0 mA.

6/ See 4.4.1c.

7/ Tested as follows: f = 2 MHz, V_{IL} = 0.4 V, V_{IH} = 2.4 V, I_{OL} = -4 mA, I_{OH} = +4.0 µA, $V_{OH} \geq$ 1.5 V and $V_{OL} \leq$ 1.5 V.

8/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

9/ Timing waveforms shown on figure 5 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 9). Device type 02 uses patterns 1, 3, 5 (see appendix). A combination of test patterns is used to verify all of the ac parameters. Each pattern does not test all ac parameters inclusive. This procedure ensures that the following parameters meet the specified limits:

Parameter	Limits Device type 02 Min	Limits Device type 02 Max	Unit
t_{AVAV}	210	---	ns
t_{AVQV}	---	210	"
t_{AVQX}	---	---	"
t_{OLQX}	---	---	"
t_{OLQV}	---	---	"
t_{OHQZ}	---	---	"
t_{ELQV}	210	---	"
t_{ELQX}	---	---	"
t_{EHQZ}	---	---	"
t_{AVEL}	10	---	"
t_{ELAX}	50	---	"
t_{ELEH}	200	---	"
V_{IL}	0.0		V
V_{IH}	3.0		"
Output compare level V_{OL}	1.5		"
Output compare level V_{OH}	1.5		"
Read cycle timing			

Parameter	Limits Device type 02 Min	Limits Device type 02 Max	Unit
t_{WHAV}	---	---	ns
t_{ELWH}	200	---	"
t_{AVWH}	---	---	"
t_{AVWL}	---	---	"
t_{WLWH}	200	---	"
t_{DVWH}	80	---	"
t_{WHDX}	10	---	"
t_{WLEH}	200	---	"
V_{IL}	0.0		V
V_{IH}	3.0		"
Output compare level V_{OL}	1.5		"
Output compare level V_{OH}	1.5		"
Write cycle timing			

The output shall be loaded with the load specified on figure 6. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device types 03 and 09. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R, Y Test no.	1 A_0	2 A_1	3 A_2	4 A_3	5 A_4	6 A_5	7 A_6	8 D_Q	9 $\overline{WE}$	10 V_{SS}	11 $\overline{CE}$	12 D_{IN}	13 A_7
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	0.8 V	2/	2/
	I_{CC2}		2	GND	GND	GND	GND	GND	GND	GND	"	GND	"	5.2 V	GND	GND
	I_{CC3}		3	"	"	"	"	"	"	"	"	"	"	2.2 V	"	"
	I_{CC4}		4	"	"	"	"	"	"	"	"	"	"	1.7 V	"	"
	I_{IL}	3009	5	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}		V_{CC}	"	V_{CC}	V_{CC}	V_{CC}
			6	V_{CC}	GND	V_{CC}	"	"	"	"		"	"	"	"	"
			7	"	V_{CC}	GND	"	"	"	"		"	"	"	"	"
			8	"	"	V_{CC}	GND	"	"	"		"	"	"	"	"
			9	"	"	"	V_{CC}	GND	"	"		"	"	"	"	"
			10	"	"	"	"	V_{CC}	GND	"		"	"	"	"	"
			11	"	"	"	"	"	V_{CC}	GND		"	"	"	"	"
			12	"	"	"	"	"	"	V_{CC}		GND	"	"	"	"
			13	"	"	"	"	"	"	"		V_{CC}	"	GND	"	"
			14	"	"	"	"	"	"	"		"	"	V_{CC}	GND	"
			15	"	"	"	"	"	"	"		"	"	"	V_{CC}	GND
			16	"	"	"	"	"	"	"		"	"	"	"	V_{CC}
			17	"	"	"	"	"	"	"		"	"	"	"	"
			18	"	"	"	"	"	"	"		"	"	"	"	"
			19	"	"	"	"	"	"	"		"	"	"	"	"
			20	"	"	"	"	"	"	"		"	"	"	"	"
			21	"	"	"	"	"	"	"		"	"	"	"	"
	I_{IH}	3010	22	"	GND	GND	GND	GND	GND	GND		GND	"	GND	GND	GND
			23	GND	V_{CC}	GND	"	"	"	"		"	"	"	"	"
			24	"	GND	V_{CC}	"	"	"	"		"	"	"	"	"
			25	"	"	GND	V_{CC}	"	"	"		"	"	"	"	"
			26	"	"	"	GND	V_{CC}	"	"		"	"	"	"	"
			27	"	"	"	"	GND	V_{CC}	"		"	"	"	"	"
			28	"	"	"	"	"	GND	V_{CC}		"	"	"	"	"
			29	"	"	"	"	"	"	GND		V_{CC}	"	"	"	"
			30	"	"	"	"	"	"	"		GND	"	V_{CC}	"	"
			31	"	"	"	"	"	"	"		"	"	GND	V_{CC}	"
			32	"	"	"	"	"	"	"		"	"	"	GND	V_{CC}
			33	"	"	"	"	"	"	"		"	"	"	"	GND
			34	"	"	"	"	"	"	"		"	"	"	"	"
			35	"	"	"	"	"	"	"		"	"	"	"	"
			36	"	"	"	"	"	"	"		"	"	"	"	"
			37	"	"	"	"	"	"	"		"	"	"	"	"
			38	"	"	"	"	"	"	"		"	"	"	"	"
	I_{OLZ}	3020	39								GND		"	2.2 V		
	I_{OHZ}	3021	40								V_{CC}		"	2.2 V		
	V_{OL}	3007	41	4/	4/	4/	4/	4/	4/	4/	4/	4/	"	4/	4/	4/
	V_{OH}	3006	42	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	5/	5/	5/
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.															
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.															

See footnotes at end of device type 03.

TABLE III. Group A inspection for device types 03 and 09 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y / Test no.	14 / A_8	15 / A_9	16 / A_{10}	17 / A_{11}	18 / A_{12}	19 / A_{13}	20 / V_{CC}	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	5.5 V	1 MHz	V_{CC}		50	mA
	I_{CC2}		2	GND	GND	GND	GND	GND	GND	"				100	µA
	I_{CC3}		3	"	"	"	"	"	"	"		"		5	mA
	I_{CC4}		4	"	"	"	"	"	"	2.0 V		"		50	µA
	I_{IL}	3009	5	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	5.5 V		A_0	-1	1	"
			6							"		A_1	"	"	"
			7	"	"	"	"	"	"	"		A_2	"	"	"
			8	"	"	"	"	"	"	"		A_3	"	"	"
			9	"	"	"	"	"	"	"		A_4	"	"	"
			10	"	"	"	"	"	"	"		A_5	"	"	"
			11	"	"	"	"	"	"	"		A_6	"	"	"
			12	"	"	"	"	"	"	"		$\overline{WE}$	"	"	"
			13	"	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			14	"	"	"	"	"	"	"		D_{IN}	"	"	"
			15	"	"	"	"	"	"	"		A_7	"	"	"
			16	GND	"	"	"	"	"	"		A_8	"	"	"
			17	V_{CC}	GND	"	"	"	"	"		A_9	"	"	"
			18		V_{CC}	GND	"	"	"	"		A_{10}	"	"	"
			19	"	"	V_{CC}	GND	"	"	"		A_{11}	"	"	"
			20	"	"	"	V_{CC}	GND	"	"		A_{12}	"	"	"
			21	"	"	"	V_{CC}	V_{CC}	GND	"		A_{13}	"	"	"
	I_{IH}	3010	22	GND	GND	GND	GND	GND	"	"		A_0	"	"	"
			23	"	"	"	"	"	"	"		A_1	"	"	"
			24	"	"	"	"	"	"	"		A_2	"	"	"
			25	"	"	"	"	"	"	"		A_3	"	"	"
			26	"	"	"	"	"	"	"		A_4	"	"	"
			27	"	"	"	"	"	"	"		A_5	"	"	"
			28	"	"	"	"	"	"	"		A_6	"	"	"
			29	"	"	"	"	"	"	"		$\overline{WE}$	"	"	"
			30	"	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			31	"	"	"	"	"	"	"		D_{IN}	"	"	"
			32	"	"	"	"	"	"	"		A_7	"	"	"
			33	V_{CC}	"	"	"	"	"	"		A_8	"	"	"
			34	GND	V_{CC}	"	"	"	"	"		A_9	"	"	"
			35	"	GND	V_{CC}	"	"	"	"		A_{10}	"	"	"
			36	"	"	GND	V_{CC}	"	"	"		A_{11}	"	"	"
			37	"	"	"	GND	V_{CC}	"	"		A_{12}	"	"	"
			38	"	"	"	GND	GND	V_{CC}	"		A_{13}	"	"	"
	I_{OLZ}	3020	39							"		D_Q	"	"	"
	I_{OHZ}	3021	40							"		D_Q	"	"	"
	V_{OL}	3007	41	4/	4/	4/	4/	4/	4/	4.5 V		D_Q		0.4	V
	V_{OH}	3006	42	5/	5/	5/	5/	5/	5/	4.5 V		D_Q	2.4		V
2															
3															

TABLE III. Group A inspection for device types 03 and 09 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	1 A_0	2 A_1	3 A_2	4 A_3	5 A_4	6 A_5	7 A_6	8 D_Q	9 $\overline{WE}$	10 V_{SS}	11 $\overline{CE}$	12 D_{IN}	13 A_7
4 T_C = +25°C	C_{in} C_{out}	3012	43 44	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND "	6/	6/	6/
7 T_C = +25°C	I/O V_{DR}	Function tests	45 46	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	" "	7/ 8/	7/ 8/	7/ 8/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.															
9 T_C = +25°C	Functional tests		47 48	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	GND "	9/ 9/	9/ 9/	9/ 9/
	t_{ELQV} t_{ELQV} t_{AVQV} t_{AVQV}		49 50 51 52										" " " "			
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.															
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.															

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.

2/ All input levels and timing edges are set to table I limits with read cycle timing: Inputs = GND and V_{CC}, outputs = open, I_O = 0 mA.

3/ Outputs loaded with load as specified on figure 6.

4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, I_{OL} = 8.0 mA.

5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IH} = 2.2 V, I_{OH} = -4.0 mA.

6/ See 4.4.1c.

7/ Tested as follows: f = 2 MHz, V_{IL} = 0.4 V, V_{IH} = 2.2 V, I_{OL} = -4 mA, I_{OH} = +4.0 μA, $V_{OH} \geq$ 1.5 V and $V_{OL} \leq$ 1.5 V.

8/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

TABLE III. Group A inspection for device types 03 and 09 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	14 A_8	15 A_9	16 A_{10}	17 A_{11}	18 A_{12}	19 A_{13}	20 V_{CC}	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
4 T_C = +25°C	C_{in} C_{out}	3012	43 44	6/	6/	6/	6/	6/	6/	6/		Input Output		10 12	pF pF
7 T_C = +25°C	I/O VDR	Function tests	45 46	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	5.5 V 2.0 V	Pattern 5 Pattern 4				
8															
9 T_C = +25°C 10/	Func-tional tests		47 48	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	4.5 V 5.5 V	Patterns 1,3,5 Patterns 1,3,5	D_Q D_Q			
	t_{ELQV} t_{ELQV} t_{AVQV} t_{AVQV}		49 50 51 52							4.5 V 5.5 V 4.5 V 5.5 V	Pattern 3 Pattern 3 Pattern 3 Pattern 3	D_Q D_Q D_Q D_Q		85 " " "	ns " " "
10															
11															

9/ Timing waveforms shown on figure 5 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 9). This procedure ensures that the following parameters meet the specified limits:

Parameter	Limits: Device type 03 Min	Device type 03 Max	Device type 09 Min	Device type 09 Max	Unit
t_{AVAV}	85	---	70	---	ns
t_{AVQV}	---	85	---	70	"
t_{ELQV}	---	85	---	70	"
V_{IL}	0.0		0.0		V
V_{IH}	3.0		3.0		"
Output compare level V_{OL}	1.5		1.5		"
Output compare level V_{OH}	1.5		1.5		"
Read cycle timing					

Parameter	Limits: Device type 03 Min	Device type 03 Max	Device type 09 Min	Device type 09 Max	Unit
t_{AVWH}	65	---	55	---	ns
t_{WHAV}	0	---	0	---	"
t_{ELWH}	65	---	55	---	"
t_{AVWL}	0	---	0	---	"
t_{WLWH}	45	---	40	---	"
t_{WHDX}	0	---	0	---	"
t_{DVWH}	35	---	30	---	"
t_{ELQX}	---	---	---	---	"
t_{WHQZ}	---	---	---	---	"
V_{IL}	0.0		0.0		V
V_{IH}	3.0		3.0		"
Output compare level V_{OL}	1.5		1.5		"
Output compare level V_{OH}	1.5		1.5		"
Write cycle timing					

The output shall be loaded with the load specified on figure 6. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

10/ When testing subgroup 9, device type 09 will have the same test conditions as device type 03, except for the following:

a. t_{ELQV} = 70 ns maximum.
b. t_{ELQV} = 70 ns maximum.
c. t_{AVQV} = 70 ns maximum.
d. t_{AVQV} = 70 ns maximum.

TABLE III. Group A inspection for device types 04 and 10. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X / Case J / Test no.	4 / 1 / A_7	5 / 2 / A_6	6 / 3 / A_5	7 / 4 / A_4	8 / 5 / A_3	9 / 6 / A_2	10 / 7 / A_1	11 / 8 / A_0	13 / 9 / DQ_0	14 / 10 / DQ_1	15 / 11 / DQ_2	16 / 12 / V_{SS}	18 / 13 / DQ_3	19 / 14 / DQ_4	20 / 15 / DQ_5
1 T_C = +25°C	I_{CC1} I_{CC2} I_{CC3} I_{CC4}	3005	1 2 3 4	2/ GND " "	2/ GND " "	2/ GND " "	2/ GND " "	2/ GND " "	2/ GND " "	2/ GND " "	2/ GND " "	3/ " " "	3/ " " "	3/ " " "	GND " " "	3/ " " "	3/ " " "	3/ " " "
	I_{IL}	3009	5 6 7 8 9 10 11 12 13 14 15 16 17 18	" V_{CC} " " " " " " " " " " " "	V_{CC} GND V_{CC} " " " " " " " " " " "	V_{CC} V_{CC} GND V_{CC} " " " " " " " " " "	V_{CC} " GND V_{CC} " " " " " " " " " "	V_{CC} " " GND V_{CC} " " " " " " " " "	V_{CC} " " " GND V_{CC} " " " " " " " "	V_{CC} " " " " " GND V_{CC} " " " " " "	V_{CC} " " " " " " " GND V_{CC} " " " "				" " " " " " " " " " " " " "			
	I_{IH}	3010	19 20 21 22 23 24 25 26 27 28 29 30 31 32	" GND " " " " " " " " " " " "	GND V_{CC} GND " " " " " " " " " " "	GND GND V_{CC} GND " " " " " " " " " "	GND " " V_{CC} GND " " " " " " " " "	GND " " " V_{CC} GND " " " " " " " "	GND " " " " V_{CC} GND " " " " " " "	GND " " " " " V_{CC} GND " " " " " "	GND " " " " " " " V_{CC} GND " " " "				" " " " " " " " " " " " " "			
	I_{OLZ}	3009	33 34 35 36 37 38 39 40									GND V_{CC} " " " " " "	V_{CC} GND V_{CC} " " " " "	V_{CC} V_{CC} GND V_{CC} " " " "	" " " " " " " "	V_{CC} " GND V_{CC} " " " "	V_{CC} " " GND V_{CC} " " "	V_{CC} " " " GND V_{CC} " "
	I_{OHZ}	3010	41 42 43 44 45 46 47 48									V_{CC} GND " " " " " "	GND V_{CC} GND " " " " "	GND GND V_{CC} GND " " " "	" " " " " " " "	GND " " V_{CC} GND " " "	GND " " " V_{CC} GND " "	GND " " " " V_{CC} GND "
	V_{OL} V_{OH}	3007 3006	49-56 57-64	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	" "	4/ 5/	4/ 5/	4/ 5/

See footnotes at end of device type 04.

TABLE III. Group A inspection for device types 04 and 10 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases X	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
			J	16	17	18	19	20	21	22	23	24					
			Test no.	DQ_6	DQ_7	$\overline{CE}$	A_{10}	$\overline{OE}$	$\overline{WE}$	A_9	A_8	V_{CC}					
1 T_C = +25°C	I_{CC1}	3005	1	3/	3/	0.8 V	2/	2/	2/	2/	2/	5.5 V	1 MHz	V_{CC}		70	mA
	I_{CC2}		2	"	"	5.2 V	GND	GND	GND	GND	GND	"				100	µA
	I_{CC3}		3	"	"	2.2 V	"	"	"	"	"	"		"		8	mA
	I_{CC4}		4	"	"	1.7 V	"	"	"	"	"	2.0 V		"		50	µA
	I_{IL}	3009	5			V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	5.5 V		A_7	-1	1	"
			6			"	"	"	"	"	"	"		A_6	"	"	"
			7			"	"	"	"	"	"	"		A_5	"	"	"
			8			"	"	"	"	"	"	"		A_4	"	"	"
			9			"	"	"	"	"	"	"		A_3	"	"	"
			10			"	"	"	"	"	"	"		A_2	"	"	"
			11			"	"	"	"	"	"	"		A_1	"	"	"
			12			"	"	"	"	"	"	"		A_0	"	"	"
			13			GND	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			14			V_{CC}	GND	"	"	"	"	"		A_{10}	"	"	"
			15			"	V_{CC}	GND	"	"	"	"		$\overline{OE}$	"	"	"
			16			"	"	V_{CC}	GND	"	"	"		$\overline{WE}$	"	"	"
			17			"	"	"	V_{CC}	GND	"	"		A_9	"	"	"
			18			"	"	"	V_{CC}	V_{CC}	GND	"		A_8	"	"	"
	I_{IH}	3010	19			GND	GND	GND	GND	GND	"	"		A_7	"	"	"
			20			"	"	"	"	"	"	"		A_6	"	"	"
			21			"	"	"	"	"	"	"		A_5	"	"	"
			22			"	"	"	"	"	"	"		A_4	"	"	"
			23			"	"	"	"	"	"	"		A_3	"	"	"
			24			"	"	"	"	"	"	"		A_2	"	"	"
			25			"	"	"	"	"	"	"		A_1	"	"	"
			26			"	"	"	"	"	"	"		A_0	"	"	"
			27			V_{CC}	"	"	"	"	"	"		$\overline{CE}$	"	"	"
			28			GND	V_{CC}	"	"	"	"	"		A_{10}	"	"	"
			29			"	GND	V_{CC}	"	"	"	"		$\overline{OE}$	"	"	"
			30			"	"	GND	V_{CC}	"	"	"		$\overline{WE}$	"	"	"
			31			"	"	"	GND	V_{CC}	"	"		A_9	"	"	"
			32			"	"	"	GND	GND	V_{CC}	"		A_8	"	"	"
	I_{OLZ}	3009	33	V_{CC}	V_{CC}	2.2 V		2.2 V				5.5 V		DQ_0	"	"	"
			34	"	"	"		"				"		DQ_1	"	"	"
			35	"	"	"		"				"		DQ_2	"	"	"
			36	"	"	"		"				"		DQ_3	"	"	"
			37	"	"	"		"				"		DQ_4	"	"	"
			38	"	"	"		"				"		DQ_5	"	"	"
			39	GND	"	"		"				"		DQ_6	"	"	"
			40	V_{CC}	GND	"		"				"		DQ_7	"	"	"
	I_{OHZ}	3010	41	GND	"	"		"				"		DQ_0	"	"	"
			42	"	"	"		"				"		DQ_1	"	"	"
			43	"	"	"		"				"		DQ_2	"	"	"
			44	"	"	"		"				"		DQ_3	"	"	"
			45	"	"	"		"				"		DQ_4	"	"	"
			46	"	"	"		"				"		DQ_5	"	"	"
			47	V_{CC}	"	"		"				"		DQ_6	"	"	"
			48	GND	V_{CC}	"		"				"		DQ_7	"	"	"
	V_{OL}	3007	49-56	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V		DQ_0-DQ_7		0.4	V
	V_{OH}	3006	57-64	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V		DQ_0-DQ_7	2.4		V

TABLE III. Group A inspection for device types 04 and 10 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DQ_0	DQ_1	DQ_2	V_{SS}	DQ_3	DQ_4	DQ_5
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.																	
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																	
4 T_C = +25°C	C_{in} C_{out}	3012	65 66	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND "	6/	6/	6/
7 T_C = +25°C	I/O V_{DR}	Function tests	67 68	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	" "	7/ 8/	7/ 8/	7/ 8/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																	
9 T_C = +25°C	Functional tests		69 70	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	GND "	9/ 9/	9/ 9/	9/ 9/
	t_{ELQV} t_{ELQV} t_{AVQV} t_{AVQV}		71 72 73 74												" " " "			
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.																	
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																	

See footnotes at end of device type 04.

TABLE III. Group A inspection for device types 04 and 10 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases X	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits Min	Test limits Max	Unit
			J	16	17	18	19	20	21	22	23	24					
			Test no.	DQ_6	DQ_7	$\overline{CE}$	A_{10}	$\overline{OE}$	$\overline{WE}$	A_9	A_8	V_{CC}					
2																	
3																	
4 T_C = +25°C	C_{in} C_{out}	3012	65 66	6/	6/	6/	6/	6/	6/	6/	6/			Input Output		10 12	pF pF
7 T_C = +25°C	I/O V_{DR}	Function tests	67 68	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	4.5 V 2.0 V	Pattern 5 Pattern 4				
8																	
9 T_C = +25°C 10/	Func-tional tests		69 70	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	4.5 V 5.5 V	Patterns 1,3,5 Patterns 1,3,5	DQ DQ			
	t_{ELQV} t_{ELQV} t_{AVQV} t_{AVQV}		71 72 73 74									4.5 V 5.5 V 4.5 V 5.5 V	Pattern 3 Pattern 3 Pattern 3 Pattern 3	DQ DQ DQ DQ		90 " " "	ns " " "
10																	
11																	

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.

2/ All input levels and timing edges are set to table I limits with read cycle timing: Input = GND and V_{CC}, outputs = open, I_O = 0 mA.

3/ Outputs loaded with load as specified on figure 6.

4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IL} = 0.8 V, I_{OL} = 2.0 mA.

5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be V_{IH} = 2.2 V, I_{OH} = -1.0 mA.

6/ See 4.4.1c.

7/ Tested as follows: f = 2 MHz, V_{IL} = 0.4 V, V_{IH} = 2.2 V, I_{OL} = -4 mA, I_{OH} = +4.0 μA, $V_{OH} \geq$ 1.5 V and $V_{OL} \leq$ 1.5 V.

8/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

9/ Timing waveforms shown on figure 5 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 9). Device types 04 and 10 use patterns 1, 3, 5 (see appendix). A combination of test patterns is used to verify all of the ac parameters. Each pattern does not test all ac parameters inclusive. This procedure ensures that the following parameters meet the specified limits:

Parameter	Limits				Unit
	Device type 04		Device type 10		
	Min	Max	Min	Max	
t_{AVAV}	90	---	70	---	ns
t_{AVQV}	---	90	---	70	"
t_{AVQX}	0	---	5	---	"
t_{OLQX}	---	---	---	---	"
t_{OLQV}	65	---	---	---	"
t_{OHQZ}	---	---	---	50	"
t_{ELQV}	90	---	70	---	"
t_{ELQX}	---	---	---	---	"
t_{EHQZ}	---	---	---	---	"
t_{AVEL}	---	---	---	---	"
t_{ELAX}	---	---	---	---	"
t_{ELEH}	---	---	---	---	"
V_{IL}	0.0		0.0		V
V_{IH}	3.0		3.0		"
Output compare level V_{OL}	1.5		1.5		"
Output compare level V_{OH}	1.5		1.5		"
Read cycle timing					

Parameter	Limits				Unit
	Device type 04		Device type 10		
	Min	Max	Min	Max	
t_{WHAV}	10	---	10	---	ns
t_{ELWH}	55	---	45	---	"
t_{AVWH}	80	---	50	---	"
t_{AVWL}	10	---	10	---	"
t_{WLWH}	55	---	40	---	"
t_{DVWH}	30	---	30	---	"
t_{WHDX}	15	---	10	---	"
t_{WLEH}	---	---	40	---	"
V_{IL}	0.0		0.0		V
V_{IH}	3.0		3.0		"
Output compare level V_{OL}	1.5		1.5		"
Output compare level V_{OH}	1.5		1.5		"
Write cycle timing					

The output shall be loaded with the load specified on figure 6. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

10/ When testing subgroup 9, device type 10 will have the same test conditions as device type 04, except for the following:

a. t_{ELQV} = 70 ns maximum.
b. t_{ELQV} = 70 ns maximum.
c. t_{AVQV} = 70 ns maximum.
d. t_{AVQV} = 70 ns maximum.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	1 A_0	2 A_1	3 A_2	4 A_3	5 A_4	6 A_5	7 A_6	8 D_Q	9 $\overline{WE}$	10 V_{SS}	11 $\overline{CE}$	12 D_{IN}
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	2/	2/
	I_{CC2}		2	4/	4/	4/	4/	4/	4/	4/	"	4/	"	4/	4/
	I_{CC3}		3	5/	5/	5/	5/	5/	5/	5/	"	5/	"	5/	5/
	I_{CC4}		4	6/	6/	6/	6/	6/	6/	6/	"	6/	"	6/	6/
	I_{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	"	5.5 V	5.5 V
			6	5.5 V	GND	5.5 V	"	"	"	"		"	"	"	"
			7	"	5.5 V	GND	"	"	"	"		"	"	"	"
			8	"	"	5.5 V	GND	"	"	"		"	"	"	"
			9	"	"	"	5.5 V	GND	"	"		"	"	"	"
			10	"	"	"	"	5.5 V	GND	"		"	"	"	"
			11	"	"	"	"	"	5.5 V	GND		"	"	"	"
			12	"	"	"	"	"	"	5.5 V		GND	"	"	"
			13	"	"	"	"	"	"	"		5.5 V	"	GND	"
			14	"	"	"	"	"	"	"		"	"	5.5 V	GND
			15	"	"	"	"	"	"	"		"	"	"	5.5 V
			16	"	"	"	"	"	"	"		"	"	"	"
			17	"	"	"	"	"	"	"		"	"	"	"
			18	"	"	"	"	"	"	"		"	"	"	"
			19	"	"	"	"	"	"	"		"	"	"	"
			20	"	"	"	"	"	"	"		"	"	"	"
			21	"	"	"	"	"	"	"		"	"	"	"
	I_{IH}	3010	22	"	GND	GND	GND	GND	GND	GND		GND	"	GND	GND
			23	GND	5.5 V	GND	"	"	"	"		"	"	"	"
			24	"	GND	5.5 V	"	"	"	"		"	"	"	"
			25	"	"	GND	5.5 V	"	"	"		"	"	"	"
			26	"	"	"	GND	5.5 V	"	"		"	"	"	"
			27	"	"	"	"	GND	5.5 V	"		"	"	"	"
			28	"	"	"	"	"	GND	5.5 V		"	"	"	"
			29	"	"	"	"	"	"	GND		5.5 V	"	"	"
			30	"	"	"	"	"	"	"		GND	"	5.5 V	"
			31	"	"	"	"	"	"	"		"	"	GND	5.5 V
			32	"	"	"	"	"	"	"		"	"	"	GND
			33	"	"	"	"	"	"	"		"	"	"	"
			34	"	"	"	"	"	"	"		"	"	"	"
			35	"	"	"	"	"	"	"		"	"	"	"
			36	"	"	"	"	"	"	"		"	"	"	"
			37	"	"	"	"	"	"	"		"	"	"	"
			38	"	"	"	"	"	"	"		"	"	"	"
	I_{OLZ}	3020	39								GND		"	2.2 V	
	I_{OHZ}	3021	40								5.5 V		"	2.2 V	
	V_{OL}	3007	41	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	7/
	V_{OH}	3006	42	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	8/	8/
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.														

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	13 A_7	14 A_8	15 A_9	16 A_{10}	17 A_{11}	18 A_{12}	19 A_{13}	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	5.5 V	V_{CC}		100	mA
	I_{CC2}		2	4/	4/	4/	4/	4/	4/	4/	"	"			
	I_{CC3}		3	5/	5/	5/	5/	5/	5/	5/	"	"		10	mA
	I_{CC4}		4	6/	6/	6/	6/	6/	6/	6/	"	"			
	I_{IL}	3009	5	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		A_0		-10	µA
			6	"	"	"	"	"	"	"		A_1		"	"
			7	"	"	"	"	"	"	"		A_2		"	"
			8	"	"	"	"	"	"	"		A_3		"	"
			9	"	"	"	"	"	"	"		A_4		"	"
			10	"	"	"	"	"	"	"		A_5		"	"
			11	"	"	"	"	"	"	"		A_6		"	"
			12	"	"	"	"	"	"	"		$\overline{WE}$		"	"
			13	"	"	"	"	"	"	"		$\overline{CE}$		"	"
			14	"	"	"	"	"	"	"		D_{IN}		"	"
			15	GND	"	"	"	"	"	"		A_7		"	"
			16	5.5 V	GND	"	"	"	"	"		A_8		"	"
			17	"	5.5 V	GND	"	"	"	"		A_9		"	"
			18	"	"	5.5 V	GND	"	"	"		A_{10}		"	"
			19	"	"	"	5.5 V	GND	"	"		A_{11}		"	"
			20	"	"	"	"	5.5 V	GND	"		A_{12}		"	"
			21	"	"	"	"	5.5 V	5.5 V	GND		A_{13}		"	"
	I_{IH}	3010	22	GND	GND	GND	GND	GND	"	"		A_0		+10	"
			23	"	"	"	"	"	"	"		A_1		"	"
			24	"	"	"	"	"	"	"		A_2		"	"
			25	"	"	"	"	"	"	"		A_3		"	"
			26	"	"	"	"	"	"	"		A_4		"	"
			27	"	"	"	"	"	"	"		A_5		"	"
			28	"	"	"	"	"	"	"		A_6		"	"
			29	"	"	"	"	"	"	"		$\overline{WE}$		"	"
			30	"	"	"	"	"	"	"		$\overline{CE}$		"	"
			31	"	"	"	"	"	"	"		D_{IN}		"	"
			32	5.5 V	"	"	"	"	"	"		A_7		"	"
			33	GND	5.5 V	"	"	"	"	"		A_8		"	"
			34	"	GND	5.5 V	"	"	"	"		A_9		"	"
			35	"	"	GND	5.5 V	"	"	"		A_{10}		"	"
			36	"	"	"	GND	5.5 V	"	"		A_{11}		"	"
			37	"	"	"	"	GND	5.5 V	"		A_{12}		"	"
			38	"	"	"	"	GND	GND	5.5 V		A_{13}		"	"
	I_{OLZ}	3020	39							"		0		-20	"
	I_{OHZ}	3021	40							"		0		+20	"
	V_{OL}	3007	41	7/	7/	7/	7/	7/	7/	4.5 V		0		0.4	V
	V_{OH}	3006	42	8/	8/	8/	8/	8/	8/	4.5 V		0	2.4		V
2															
3															

TABLE III. Group A inspection for device type 06 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	1	2	3	4	5	6	7	8	9	10	11	12
				A_0	A_1	A_2	A_3	A_4	A_5	A_6	D_Q	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}
4 T_C = +25°C	C_{in} C_{out}	3012	43 44	9/	9/	9/	9/	9/	9/	9/	9/	9/		9/	9/
9 T_C = +25°C	NOT WRITE	See fig. 8	45 46	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/
	WRITE/ WRITE	See fig. 9	47 48	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.														

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.

2/ All input levels and timing edges are set to table I limits with read cycle timing: V_{IL} = 0.4 V and V_{IH} = 2.2 V for device type 06.

3/ Outputs loaded with load as specified on figure 6.

4/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = 2.2 V for device type 06.

5/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = V_{CC} -0.3 V.

6/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

7/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, I_{OL} = 8.0 mA.

8/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IH} = 2.2 V, I_{OH} = -4.0 mA.

9/ See 4.4.1c.

10/ Since the object of the NOT WRITE pattern (see figure 8) is to verify that the device may not be written into when it is disabled, the waveforms shown on figure 5 may be applied using nominal timing. The outputs shall be loaded with the load specified on figure 6.

TABLE III. Group A inspection for device type 06 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	13 A_7	14 A_8	15 A_9	16 A_{10}	17 A_{11}	18 A_{12}	19 A_{13}	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
4 T_C = +25°C	C_{in}	3012	43	9/	9/	9/	9/	9/	9/	9/		Each input		8	pF
	C_{out}		44									Each output		10	pF
9 T_C = +25°C	NOT WRITE	See fig. 8	45	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	10/ 10/	4.5 V	D_{IN}	10/ 10/	10/ 10/	ns
			46								5.5 V	D_{IN}			"
	WRITE/ WRITE	See fig. 9	47	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	11/ 11/	4.5 V	D_{IN}	11/ 11/	11/ 11/	"
			48								5.5 V	D_{IN}			"
10															
11															

9/ Timing waveforms shown on figure 5 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 9). This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits Device type 06 Min	Limits Device type 06 Max	Unit
t_{AVAV}		45	---	ns
t_{AVQV}		---	45	"
t_{ELQV}		---	45	"
V_{IL}		0.0		V
V_{IH}		2.2		"
Output compare level	V_{OL}	0.4		"
	V_{OH}	2.4		"
Read cycle timing				

Parameter		Limits Device type 06 Min	Limits Device type 06 Max	Unit
t_{AVWH}		35	---	ns
t_{WHAV}		5	---	"
t_{ELWH}		35	---	"
t_{AVWL}		5	---	"
t_{WLWH}		30	---	"
t_{WHDX}		5	---	"
t_{DVWH}		25	---	"
t_{ELQX}		3	---	"
t_{WHQZ}		---	25	"
V_{IL}		0.0		V
V_{IH}		2.2		"
Output compare level	V_{OL}	0.4		"
	V_{OH}	2.4		"
Write cycle timing				

The output shall be loaded with the load specified on figure 6. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device type 07. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	D_Q	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}
1 T_C = +25°C	V_{IC} (pos)	3022	1	50 μA											
			2		50 μA										
			3			50 μA									
			4				50 μA								
			5					50 μA							
			6						50 μA						
			7							50 μA					
			8									50 μA			
			9											50 μA	
			10												50 μA
			11												
			12												
			13												
			14												
			15												
			16												
			17												
	V_{IC} (neg)	3022	18	-50 μA									GND		
			19		-50 μA								"		
			20			-50 μA							"		
			21				-50 μA						"		
			22					-50 μA					"		
			23						-50 μA				"		
			24							-50 μA			"		
			25									-50 μA	"		
			26										"	-50 μA	
			27										"		-50 μA
			28										"		
			29										"		
			30										"		
			31										"		
			32										"		
			33										"		
			34										"		
	V_{OL} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	4.5 V	"	GND	4.5 V
	V_{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	5/	4.5 V	"	"	4.5 V
	I_{IH} 6/	3010	37	5.5 V	GND	GND	GND	GND	GND	GND		GND	"	"	GND
			38	GND	5.5 V	GND	"	"	"	"		"	"	"	"
			39	"	GND	5.5 V	"	"	"	"		"	"	"	"
			40	"	"	GND	5.5 V	"	"	"		"	"	"	"
			41	"	"	"	GND	5.5 V	"	"		"	"	"	"
			42	"	"	"	"	GND	5.5 V	"		"	"	"	"
			43	"	"	"	"	"	GND	5.5 V		"	"	"	"
			44	"	"	"	"	"	"	GND		5.5 V	"	"	"
			45	"	"	"	"	"	"	"		GND	"	5.5 V	"
			46	"	"	"	"	"	"	"		"	"	GND	5.5 V
			47	"	"	"	"	"	"	"		"	"	"	GND
			48	"	"	"	"	"	"	"		"	"	"	"
			49	"	"	"	"	"	"	"		"	"	"	"
			50	"	"	"	"	"	"	"		"	"	"	"
			51	"	"	"	"	"	"	"		"	"	"	"
			52	"	"	"	"	"	"	"		"	"	"	"
			53	"	"	"	"	"	"	"		"	"	"	"

See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	13 / 15 / A_7	14 / 16 / A_8	15 / 17 / A_9	16 / 20 / A_{10}	17 / 21 / A_{11}	18 / 22 / A_{12}	19 / 23 / A_{13}	20 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	V_{IC} (pos)	3022	1								GND	A_0	0.1	2.0	V
			2								"	A_1	"	"	"
			3								"	A_2	"	"	"
			4								"	A_3	"	"	"
			5								"	A_4	"	"	"
			6								"	A_5	"	"	"
			7								"	A_6	"	"	"
			8								"	$\overline{WE}$	"	"	"
			9								"	$\overline{CE}$	"	"	"
			10								"	D_{IN}	"	"	"
			11	50 μA							"	A_7	"	"	"
			12		50 μA						"	A_8	"	"	"
			13			50 μA					"	A_9	"	"	"
			14				50 μA				"	A_{10}	"	"	"
			15					50 μA			"	A_{11}	"	"	"
			16						50 μA		"	A_{12}	"	"	"
			17							50 μA	"	A_{13}	"	"	"
	V_{IC} (neg)	3022	18									A_0	-0.1	-2.0	"
			19									A_1	"	"	"
			20									A_2	"	"	"
			21									A_3	"	"	"
			22									A_4	"	"	"
			23									A_5	"	"	"
			24									A_6	"	"	"
			25									$\overline{WE}$	"	"	"
			26									$\overline{CE}$	"	"	"
			27									D_{IN}	"	"	"
			28	-50 μA								A_7	"	"	"
			29		-50 μA							A_8	"	"	"
			30			-50 μA						A_9	"	"	"
			31				-50 μA					A_{10}	"	"	"
			32					-50 μA				A_{11}	"	"	"
			33						-50 μA			A_{12}	"	"	"
			34							-50 μA		A_{13}	"	"	"
	V_{OL} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D_Q		0.4	"
	V_{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D_Q	4.0		"
	I_{IH}	3010	37	GND	GND	GND	GND	GND	GND	GND	5.5 V	A_0		1.0	μA
			38	"	"	"	"	"	"	"	"	A_1		"	"
			39	"	"	"	"	"	"	"	"	A_2		"	"
			40	"	"	"	"	"	"	"	"	A_3		"	"
			41	"	"	"	"	"	"	"	"	A_4		"	"
			42	"	"	"	"	"	"	"	"	A_5		"	"
			43	"	"	"	"	"	"	"	"	A_6		"	"
			44	"	"	"	"	"	"	"	"	$\overline{WE}$		"	"
			45	"	"	"	"	"	"	"	"	$\overline{CE}$		"	"
			46	"	"	"	"	"	"	"	"	D_{IN}		"	"
			47	5.5 V	"	"	"	"	"	"	"	A_7		"	"
			48	GND	5.5 V	"	"	"	"	"	"	A_8		"	"
			49	"	GND	5.5 V	"	"	"	"	"	A_9		"	"
			50	"	"	GND	5.5 V	"	"	"	"	A_{10}		"	"
			51	"	"	"	GND	5.5 V	"	"	"	A_{11}		"	"
			52	"	"	"	"	GND	5.5 V	"	"	A_{12}		"	"
			53	"	"	"	"	GND	GND	5.5 V	"	A_{13}		"	"

TABLE III. Group A inspection for device type 07 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	1 / 1 / A_0	2 / 2 / A_1	3 / 3 / A_2	4 / 4 / A_3	5 / 5 / A_4	6 / 8 / A_5	7 / 9 / A_6	8 / 10 / D_Q	9 / 11 / $\overline{WE}$	10 / 12 / V_{SS}	11 / 13 / $\overline{CE}$	12 / 14 / D_{IN}
1 T_C = +25°C	I_{IL} 6/	3009	54	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	5.5 V
			55	5.5 V	GND	5.5 V	"	"	"	"		"	"	"	"
			56	"	5.5 V	GND	"	"	"	"		"	"	"	"
			57	"	"	5.5 V	GND	"	"	"		"	"	"	"
			58	"	"	"	5.5 V	GND	"	"		"	"	"	"
			59	"	"	"	"	5.5 V	GND	"		"	"	"	"
			60	"	"	"	"	"	5.5 V	GND		"	"	"	"
			61	"	"	"	"	"	"	5.5 V		"	GND	"	"
			62	"	"	"	"	"	"	"		"	5.5 V	GND	"
			63	"	"	"	"	"	"	"		"	"	5.5 V	GND
			64	"	"	"	"	"	"	"		"	"	"	5.5 V
			65	"	"	"	"	"	"	"		"	"	"	"
			66	"	"	"	"	"	"	"		"	"	"	"
			67	"	"	"	"	"	"	"		"	"	"	"
			68	"	"	"	"	"	"	"		"	"	"	"
			69	"	"	"	"	"	"	"		"	"	"	"
			70	"	"	"	"	"	"	"		"	"	"	"
	I_{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	GND	5.5 V	5.5 V	GND	5.5 V	GND
	I_{OHZ}	3021	72	GND	GND	GND	GND	GND	GND	GND	5.5 V	GND	"	GND	GND
	I_{OLZ}	3020	73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	"	5.5 V	5.5 V
	I_{OLZ}	3020	74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	"	GND	5.5 V
	I_{CC1}	3005	75	GND	GND	GND	GND	GND	GND	GND		"	"	5.5 V	GND
	I_{CC2}		76	"	"	"	"	"	"	"		"	"	"	"
	I_{CC3}		77	"	"	"	"	"	"	"		"	"	"	"
	I_{CC4}		78	"	"	"	"	"	"	"		"	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.														
4 T_C = +25°C	C_{in}	3012	79	10/	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/
8 T_C = +125°C	Power down		80	11/	11/	11/	11/	11/	11/	11/		11/	"	11/	11/
	Functional tests		81	12/	12/	12/	12/	12/	12/	12/		12/	"	12/	12/

See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	13 / 15 / A_7	14 / 16 / A_8	15 / 17 / A_9	16 / 20 / A_{10}	17 / 21 / A_{11}	18 / 22 / A_{12}	19 / 23 / A_{13}	20 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{IL} 6/	3009	54	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A_0		-1.0	µA
			55	"	"	"	"	"	"	"	"	A_1		"	"
			56	"	"	"	"	"	"	"	"	A_2		"	"
			57	"	"	"	"	"	"	"	"	A_3		"	"
			58	"	"	"	"	"	"	"	"	A_4		"	"
			59	"	"	"	"	"	"	"	"	A_5		"	"
			60	"	"	"	"	"	"	"	"	A_6		"	"
			61	"	"	"	"	"	"	"	"	$\overline{WE}$		"	"
			62	"	"	"	"	"	"	"	"	$\overline{CE}$		"	"
			63	"	"	"	"	"	"	"	"	D_{IN}		"	"
			64	GND	"	"	"	"	"	"	"	A_7		"	"
			65	5.5 V	GND	"	"	"	"	"	"	A_8		"	"
			66	"	5.5 V	GND	"	"	"	"	"	A_9		"	"
			67	"	"	5.5 V	GND	"	"	"	"	A_{10}		"	"
			68	"	"	"	5.5 V	GND	"	"	"	A_{11}		"	"
			69	"	"	"	"	5.5 V	GND	"	"	A_{12}		"	"
			70	"	"	"	"	5.5 V	5.5 V	GND	"	A_{13}		"	"
	I_{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	"	"	D_Q		10	"
	I_{OHZ}	3021	72	GND	GND	GND	GND	GND	GND	"	"	D_Q		10	"
	I_{OLZ}	3020	73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	D_Q		-10	"
	I_{OLZ}	3020	74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	D_Q		-10	"
	I_{CC1}	3005	75	GND	GND	GND	GND	GND	GND	GND	"	V_{CC} 7/		200	"
	I_{CC2}		76	"	"	"	"	"	"	"	"	V_{CC} 8/		"	"
	I_{CC3}		77	"	"	"	"	"	"	"	"	V_{CC} 9/		"	"
	I_{CC4}		78	"	"	"	"	"	"	"	"	V_{CC} 2/		"	"
2															
3															
4 T_C = +25°C	C_{in}	3012	79	10/	10/	10/	10/	10/	10/	10/	5.5 V	All inputs		8	pF
8 T_C = +125°C	Power down		80	11/	11/	11/	11/	11/	11/	11/	11/	V_{CC}		3.0	V
	Functional tests		81	12/	12/	12/	12/	12/	12/	12/	12/	D_Q	12/	12/	V

TABLE III. Group A inspection for device type 07 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	D_Q	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}
9 $T_C = +25°C$	t_{AVQV}	See fig. 8	82	13/	13/	13/	13/	13/	13/	13/	13/	13/	GND	13/	13/
10	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = +125°C$.														
11	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55°C$.														
12 $T_C = +25°C$	I_{CCOP}		83	14/	14/	14/	14/	14/	14/	14/	14/	14/	GND	14/	14/

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are as follows: V_{IC}(pos) tests, the V_{SS} terminals shall be open; V_{IC}(neg) tests, the V_{CC} terminal shall be open; I_{SS} tests, the output terminals shall be open.

2/ $V_{IL} = 0.8$ V; $V_{IH} = 4.0$ V.

3/ Contents of addressed cell shall be = data "0", $I_{OL} = 5$ mA.

4/ $V_{IL} = 0.8$ V; $V_{IH} = 3.0$ V.

5/ Contents of addressed cell shall be = data "1", $I_{OH} = -5$ mA.

6/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at +25°C for each individual input or measure all inputs together.

7/ Random data pattern (data in memory established by power turn-on).

8/ All data are "1's" in memory.

9/ All data are "0's" in memory.

10/ See 4.4.1c.

11/ Power down test (PWRDWN) terminal conditions shall be as follows:

a. Use timing parameters and limits specified on figure 5.

b. $V_{OL} < \frac{V_{CC}}{2}$; $V_{OH} > \frac{V_{CC}}{2}$

c. Use load specified on figure 6.

d. $V_{IL} = 0$ V; $V_{IH} = 4.5$ V.

e. The power down test shall be performed as follows:

(1) Power up RAM to $V_{CC} = 4.5$ V.

(2) Write topologically true checkerboard pattern into RAM memory array (see figure 4 and appendix).

(3) Reduce V_{CC} to 3.0 V. All device inputs shall be reduced along with V_{CC} exercising special care to avoid latch-up.

(4) Maintain RAM at reduced voltage for 500 ms (0.5 second) minimum.

(5) Raise V_{CC} to 4.5 V.

(6) Verify RAM contents to be unchanged from pattern written in (2) above.

(7) Repeat steps (1) through (6), except use the complement of the first checkerboard pattern.

TABLE III. Group A inspection for device type 07 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	13 / 15 / A_7	14 / 16 / A_8	15 / 17 / A_9	16 / 20 / A_{10}	17 / 21 / A_{11}	18 / 22 / A_{12}	19 / 23 / A_{13}	20 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
9 T_C = +25°C	tAVQV	See fig. 8	82	13/	13/	13/	13/	13/	13/	13/	4.5 V	D_Q		150	ns
10															
11															
12 T_C = +25°C	I_{CCOP}		83	14/	14/	14/	14/	14/	14/	14/	5.5 V	V_{CC}		6	mA

12/ Functional test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 5.

b. The output voltages shall be:

$$V_{OL} < \frac{V_{CC}}{2};\ V_{OH} > \frac{V_{CC}}{2}$$

c. Use CK, $\overline{CK}$, butterfly, spiral complement patterns.

d. Use load specified on figure 6.

e. V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = V_{CC} - 1.5 V.

13/ Timing test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 5.

b. $$V_{OL} < \frac{V_{CC}}{2};\ V_{OH} > \frac{V_{CC}}{2}$$

c. Use CK, $\overline{CK}$ patterns.

d. Use load specified on figure 6.

e. V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = V_{CC} - 1.5 V.

14/ Operating current test (I_{CCOP}) terminal conditions shall be as follows:

a. Use timing parameters and limits specified on figure 5.

b. Use topologically true checkerboard pattern (see figure 4 and appendix).

c. Use load specified on figure 6.

d. V_{IL} = 0 V; V_{IH} = 5.5 V.

TABLE III. Group A inspection for device type 08. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	D_Q	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}
1 T_C = +25°C	V_{IC} (pos)	3022	1	50 μA											
			2		50 μA										
			3			50 μA									
			4				50 μA								
			5					50 μA							
			6						50 μA						
			7							50 μA					
			8									50 μA			
			9											50 μA	
			10												50 μA
			11												
			12												
			13												
			14												
			15												
			16												
			17												
	V_{IC} (neg)	3022	18	-50 μA									GND		
			19		-50 μA								"		
			20			-50 μA							"		
			21				-50 μA						"		
			22					-50 μA					"		
			23						-50 μA				"		
			24							-50 μA			"		
			25									-50 μA	"		
			26										"	-50 μA	
			27										"		-50 μA
			28										"		
			29										"		
			30										"		
			31										"		
			32										"		
			33										"		
			34										"		
	V_{OL} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	4.5 V	"	GND	4.5 V
	V_{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	5/	4.5 V	"	"	4.5 V
	I_{IH} 6/	3010	37	5.5 V	GND	GND	GND	GND	GND	GND		GND	"	"	GND
			38	GND	5.5 V	"	"	"	"	"		"	"	"	"
			39	"	GND	5.5 V	"	"	"	"		"	"	"	"
			40	"	"	GND	5.5 V	"	"	"		"	"	"	"
			41	"	"	"	GND	5.5 V	"	"		"	"	"	"
			42	"	"	"	"	GND	5.5 V	"		"	"	"	"
			43	"	"	"	"	"	GND	5.5 V		"	"	"	"
			44	"	"	"	"	"	"	GND		5.5 V	"	"	"
			45	"	"	"	"	"	"	"		GND	"	5.5 V	"
			46	"	"	"	"	"	"	"		"	"	GND	5.5 V
			47	"	"	"	"	"	"	"		"	"	"	GND
			48	"	"	"	"	"	"	"		"	"	"	"
			49	"	"	"	"	"	"	"		"	"	"	"
			50	"	"	"	"	"	"	"		"	"	"	"
			51	"	"	"	"	"	"	"		"	"	"	"
			52	"	"	"	"	"	"	"		"	"	"	"
			53	"	"	"	"	"	"	"		"	"	"	"

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	13 / 15 / A_7	14 / 16 / A_8	15 / 17 / A_9	16 / 20 / A_{10}	17 / 21 / A_{11}	18 / 22 / A_{12}	19 / 23 / A_{13}	20 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	V_{IC} (pos)	3022	1								GND	A_0	0.1	2.0	V
			2								"	A_1	"	"	"
			3								"	A_2	"	"	"
			4								"	A_3	"	"	"
			5								"	A_4	"	"	"
			6								"	A_5	"	"	"
			7								"	A_6	"	"	"
			8								"	$\overline{WE}$	"	"	"
			9								"	$\overline{CE}$	"	"	"
			10								"	D_{IN}	"	"	"
			11	50 μA							"	A_7	"	"	"
			12		50 μA						"	A_8	"	"	"
			13			50 μA					"	A_9	"	"	"
			14				50 μA				"	A_{10}	"	"	"
			15					50 μA			"	A_{11}	"	"	"
			16						50 μA		"	A_{12}	"	"	"
			17							50 μA	"	A_{13}	"	"	"
	V_{IC} (neg)	3022	18									A_0	-0.1	-2.0	"
			19									A_1	"	"	"
			20									A_2	"	"	"
			21									A_3	"	"	"
			22									A_4	"	"	"
			23									A_5	"	"	"
			24									A_6	"	"	"
			25									$\overline{WE}$	"	"	"
			26									$\overline{CE}$	"	"	"
			27									D_{IN}	"	"	"
			28	-50 μA								A_7	"	"	"
			29		-50 μA							A_8	"	"	"
			30			-50 μA						A_9	"	"	"
			31				-50 μA					A_{10}	"	"	"
			32					-50 μA				A_{11}	"	"	"
			33						-50 μA			A_{12}	"	"	"
			34							-50 μA		A_{13}	"	"	"
	V_{OL} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D_Q		0.4	"
	V_{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D_Q			"
	I_{IH} 6/	3010	37	GND	GND	GND	GND	GND	GND	GND	5.5 V	A_0		1.0	μA
			38	"	"	"	"	"	"	"	"	A_1		"	"
			39	"	"	"	"	"	"	"	"	A_2		"	"
			40	"	"	"	"	"	"	"	"	A_3		"	"
			41	"	"	"	"	"	"	"	"	A_4		"	"
			42	"	"	"	"	"	"	"	"	A_5		"	"
			43	"	"	"	"	"	"	"	"	A_6		"	"
			44	"	"	"	"	"	"	"	"	$\overline{WE}$		"	"
			45	"	"	"	"	"	"	"	"	$\overline{CE}$		"	"
			46	"	"	"	"	"	"	"	"	D_{IN}		"	"
			47	5.5 V	"	"	"	"	"	"	"	A_7		"	"
			48	GND	5.5 V	"	"	"	"	"	"	A_8		"	"
			49	"	GND	5.5 V	"	"	"	"	"	A_9		"	"
			50	"	"	GND	5.5 V	"	"	"	"	A_{10}		"	"
			51	"	"	"	GND	5.5 V	"	"	"	A_{11}		"	"
			52	"	"	"	"	GND	5.5 V	"	"	A_{12}		"	"
			53	"	"	"	"	GND	GND	5.5 V	"	A_{13}		"	"

TABLE III. Group A inspection for device type 08 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	1 / 1 / A_0	2 / 2 / A_1	3 / 3 / A_2	4 / 4 / A_3	5 / 5 / A_4	6 / 8 / A_5	7 / 9 / A_6	8 / 10 / D_Q	9 / 11 / $\overline{WE}$	10 / 12 / V_{SS}	11 / 13 / $\overline{CE}$	12 / 14 / D_{IN}
1 T_C = +25°C	I_{IL} 6/	3009	54	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	5.5 V
			55	5.5 V	GND	5.5 V	"	"	"	"		"	"	"	"
			56	"	5.5 V	GND	"	"	"	"		"	"	"	"
			57	"	"	5.5 V	GND	"	"	"		"	"	"	"
			58	"	"	"	5.5 V	GND	"	"		"	"	"	"
			59	"	"	"	"	5.5 V	GND	"		"	"	"	"
			60	"	"	"	"	"	5.5 V	GND		"	"	"	"
			61	"	"	"	"	"	"	5.5 V		"	GND	"	"
			62	"	"	"	"	"	"	"		"	5.5 V	GND	"
			63	"	"	"	"	"	"	"		"	"	5.5 V	GND
			64	"	"	"	"	"	"	"		"	"	"	5.5 V
			65	"	"	"	"	"	"	"		"	"	"	"
			66	"	"	"	"	"	"	"		"	"	"	"
			67	"	"	"	"	"	"	"		"	"	"	"
			68	"	"	"	"	"	"	"		"	"	"	"
			69	"	"	"	"	"	"	"		"	"	"	"
			70	"	"	"	"	"	"	"		"	"	"	"
	I_{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	GND	5.5 V	5.5 V	GND	5.5 V	GND
	I_{OHZ}	3021	72	GND	GND	GND	GND	GND	GND	GND	5.5 V	GND	"	GND	GND
	I_{OLZ}	3020	73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	"	5.5 V	5.5 V
	I_{OLZ}	3020	74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	"	GND	5.5 V
	I_{CC1}	3005	75	GND	GND	GND	GND	GND	GND	GND		"	"	5.5 V	GND
	I_{CC2}		76	"	"	"	"	"	"	"		"	"	"	"
	I_{CC3}		77	"	"	"	"	"	"	"		"	"	"	"
	I_{CC4}		78	"	"	"	"	"	"	"		"	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.														
4 T_C = +25°C	C_{in}	3012	79	10/	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/
8 T_C = +125°C	Power down		80	11/	11/	11/	11/	11/	11/	11/		11/	"	11/	11/
	Functional tests		81	12/	12/	12/	12/	12/	12/	12/		12/	"	12/	12/

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R / Case Z / Test no.	13 / 15 / A_7	14 / 16 / A_8	15 / 17 / A_9	16 / 20 / A_{10}	17 / 21 / A_{11}	18 / 22 / A_{12}	19 / 23 / A_{13}	20 / 24 / V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{IL}	3010	54	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A_0		-1.0	µA
			55	"	"	"	"	"	"	"	"	A_1		"	"
			56	"	"	"	"	"	"	"	"	A_2		"	"
			57	"	"	"	"	"	"	"	"	A_3		"	"
			58	"	"	"	"	"	"	"	"	A_4		"	"
			59	"	"	"	"	"	"	"	"	A_5		"	"
			60	"	"	"	"	"	"	"	"	A_6		"	"
			61	"	"	"	"	"	"	"	"	$\overline{WE}$		"	"
			62	"	"	"	"	"	"	"	"	$\overline{CE}$		"	"
			63	"	"	"	"	"	"	"	"	D_{IN}		"	"
			64	GND	"	"	"	"	"	"	"	A_7		"	"
			65	5.5 V	GND	"	"	"	"	"	"	A_8		"	"
			66	"	5.5 V	GND	"	"	"	"	"	A_9		"	"
			67	"	"	5.5 V	GND	"	"	"	"	A_{10}		"	"
			68	"	"	"	5.5 V	GND	"	"	"	A_{11}		"	"
			69	"	"	"	"	5.5 V	GND	"	"	A_{12}		"	"
			70	"	"	"	"	5.5 V	5.5 V	GND	"	A_{13}		"	"
	I_{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	"	"	D_Q		10	"
	I_{OHZ}	3021	72	GND	GND	GND	GND	GND	GND	"	"	D_Q		10	"
	I_{OLZ}	3020	73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	D_Q		-10	"
	I_{OLZ}	3020	74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	D_Q		-10	"
	I_{CC1}	3005	75	GND	GND	GND	GND	GND	GND	GND	"	V_{CC} 7/		200	"
	I_{CC2}		76	"	"	"	"	"	"	"	"	V_{CC} 8/		"	"
	I_{CC3}		77	"	"	"	"	"	"	"	"	V_{CC} 9/		"	"
	I_{CC4}		78	"	"	"	"	"	"	"	"	V_{CC} 2/		"	"
2															
3															
4 T_C = +25°C	C_{in}	3012	79	10/	10/	10/	10/	10/	10/	10/	5.5 V	All inputs		8	pF
8 T_C = +125°C	Power down		80	11/	11/	11/	11/	11/	11/	11/	11/	V_{CC}		3.0	V
	Functional tests		81	12/	12/	12/	12/	12/	12/	12/	12/	D_Q	12/	12/	V

TABLE III. Group A inspection for device type 08 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	D_Q	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}
9 T_C = +25°C	t_{AVQV}	See fig. 8	82	13/	13/	13/	13/	13/	13/	13/	13/	13/	GND	13/	13/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.														
12 T_C = +25°C	I_{CCOP}		83	14/	14/	14/	14/	14/	14/	14/	14/	14/	GND	14/	14/

1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are as follows: V_{IC}(pos) tests, the V_{SS} terminals shall be open; V_{IC}(neg) tests, the V_{CC} terminal shall be open; I_{SS} tests, the output terminals shall be open.

2/ V_{IL} = 0.8 V, V_{IH} = 3.0 V.

3/ Contents of addressed cell shall be = data "0", I_{OL} = 5 mA.

4/ V_{IL} = 0.8 V; V_{IH} = 2.3 V.

5/ Contents of addressed cell shall be = data "1", I_{OH} = -5 mA.

6/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at +25°C for each individual input or measure all inputs together.

7/ Random data pattern (data in memory established by power turn-on).

8/ All data are "1's" in memory.

9/ All data are "0's" in memory.

10/ See 4.4.1c.

11/ Power down test (PWRDWN) terminal conditions shall be as follows:

a. Use timing parameters and limits specified on figure 5.

b. $V_{OL} \leq 0.45$ V; $V_{OH} \geq 2.4$ V.

c. Use load specified on figure 6.

d. V_{IL} = 0 V; V_{IH} = 4.5 V.

e. The power down test shall be performed as follows:

(1) Power up RAM to V_{CC} = 4.5 V.

(2) Write topologically true checkerboard pattern into RAM memory array (see figure 4 and appendix).

(3) Reduce V_{CC} to 2.0 V. All device inputs shall be reduced along with V_{CC} exercising special care to avoid latch-up. (See 4.5.)

(4) Maintain RAM at reduced voltage for 500 ms (0.5 second) minimum.

(5) Raise V_{CC} to 4.5 V.

(6) Verify RAM contents to be unchanged from pattern written in (2) above.

(7) Repeat steps (1) through (6), except use the complement of the first checkerboard pattern.

TABLE III. Group A inspection for device type 08 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Z	15	16	17	20	21	22	23	24				
			Test no.	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	V_{CC}		Min	Max	
9 T_C = +25°C	t_{AVQV}	See fig. 8	82	13/	13/	13/	13/	13/	13/	13/	4.5 V	D_Q		175	ns
10															
11															
12 T_C = +25°C	I_{CCOP}		83	14/	14/	14/	14/	14/	14/	14/	5.5 V	V_{CC}		6	mA

12/ ADDCOMP (Functional) test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 5.

b. The output voltages shall be $V_{OL} \leq 0.45$ V; $V_{OH} \geq 2.4$ V.

c. Use ADDCOMP pattern (see appendix).

d. Use load specified on figure 6.

e. $V_{CC} = 4.5$ V; $V_{IL} = 0.8$ V; $V_{IH} = 2.3$ V.

13/ Timing test terminal conditions shall be as follows:

a. Use timing parameter and limits specified on figure 5.

b. $V_{OL} \leq 0.45$ V; $V_{OH} \geq 2.4$ V.

c. Use MARCH pattern (see appendix).

d. Use load specified on figure 6.

e. $V_{CC} = 4.5$ V; $V_{IL} = 0.8$ V; $V_{IH} = 2.3$ V.

14/ Operating current test (I_{CCOP}) terminal conditions shall be as follows:

a. Use timing parameters and limits specified on figure 5.

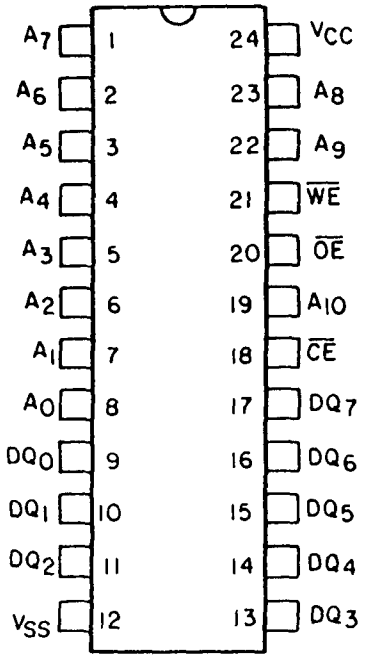
b. Use topologically true checkerboard pattern (see figure 4 and appendix).

c. Use load specified on figure 6.

d. $V_{IL} = 0.8$ V; $V_{IH} = 5.5$ V.

Device types 01, 02, 04, 05, and 10

Case outline J



Case outline X

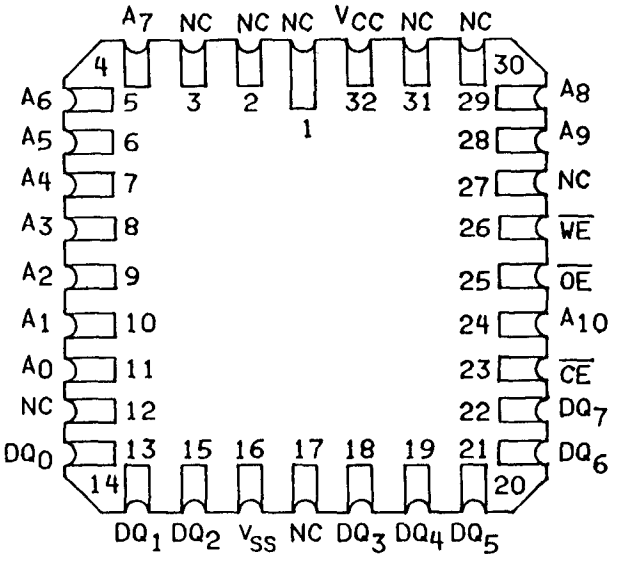
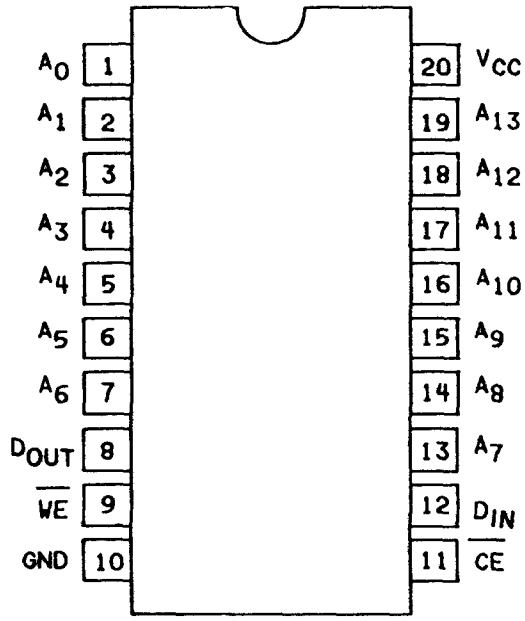


FIGURE 1. Terminal connections.

Device types 03, 06, 07, 08, and 09

Case outline R



Device types 03, 06, and 09

Case outline Y

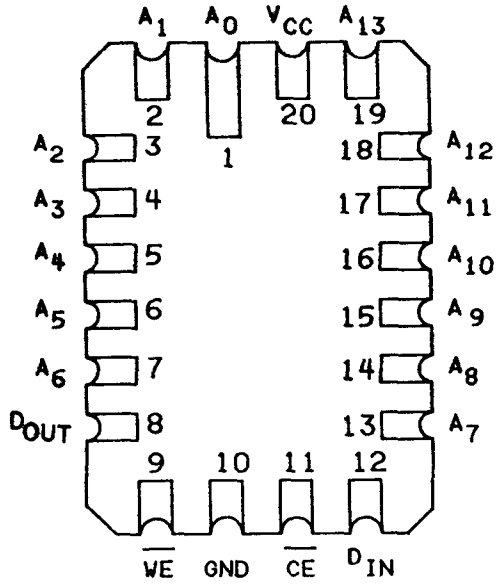


FIGURE 1. Terminal connections - Continued.

Device types 07 and 08

Case outline Z

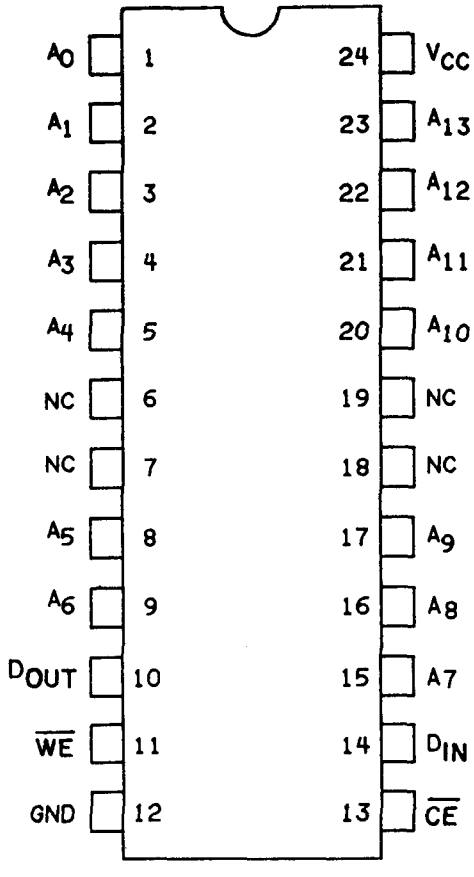


FIGURE 1. Terminal connections - Continued.

Device types 01, 04, 05, and 10

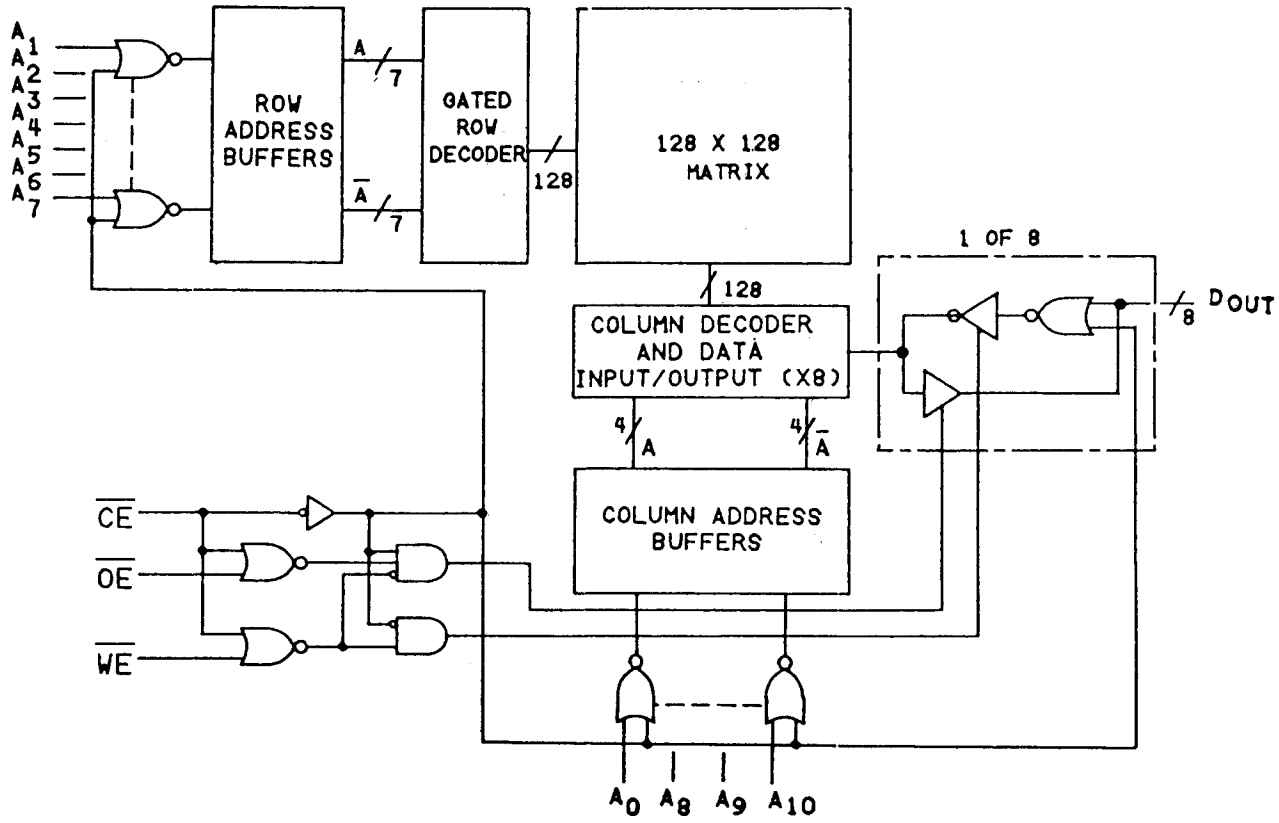


FIGURE 2. Block diagrams.

Device type 02

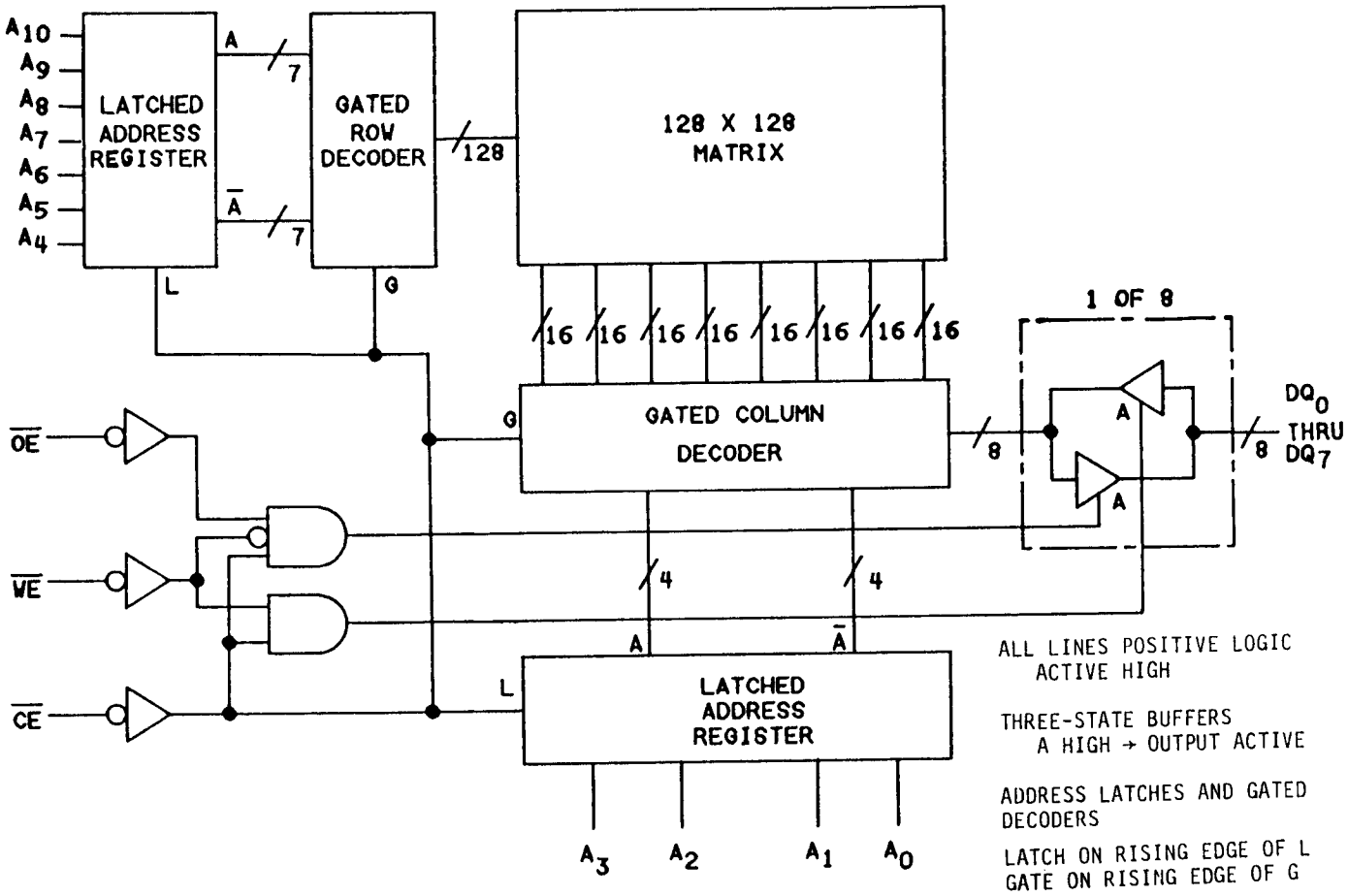


FIGURE 2. Block diagrams - Continued.

Device types 03, 06, and 09

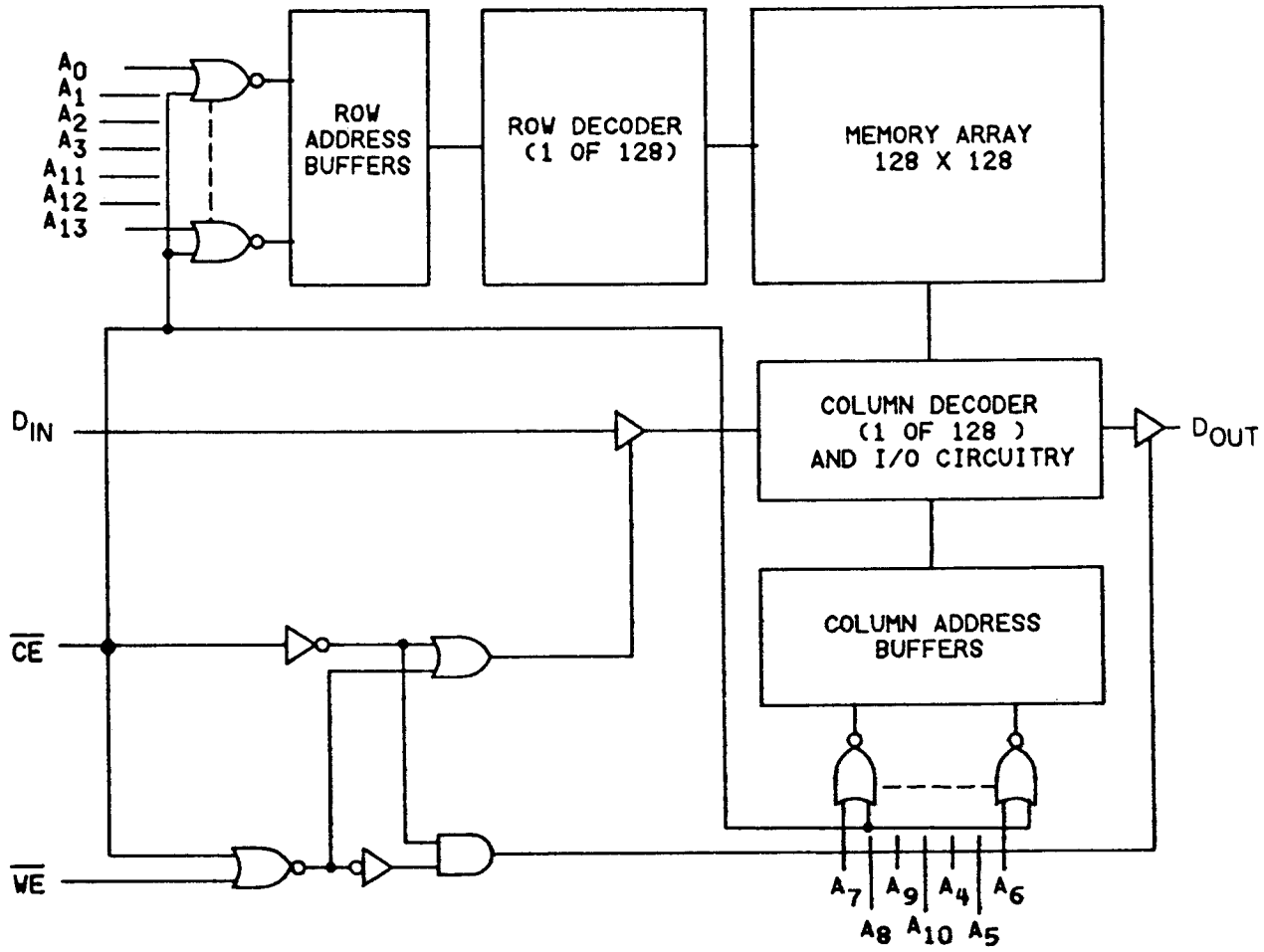


FIGURE 2. Block diagrams - Continued.

Device types 07 and 08

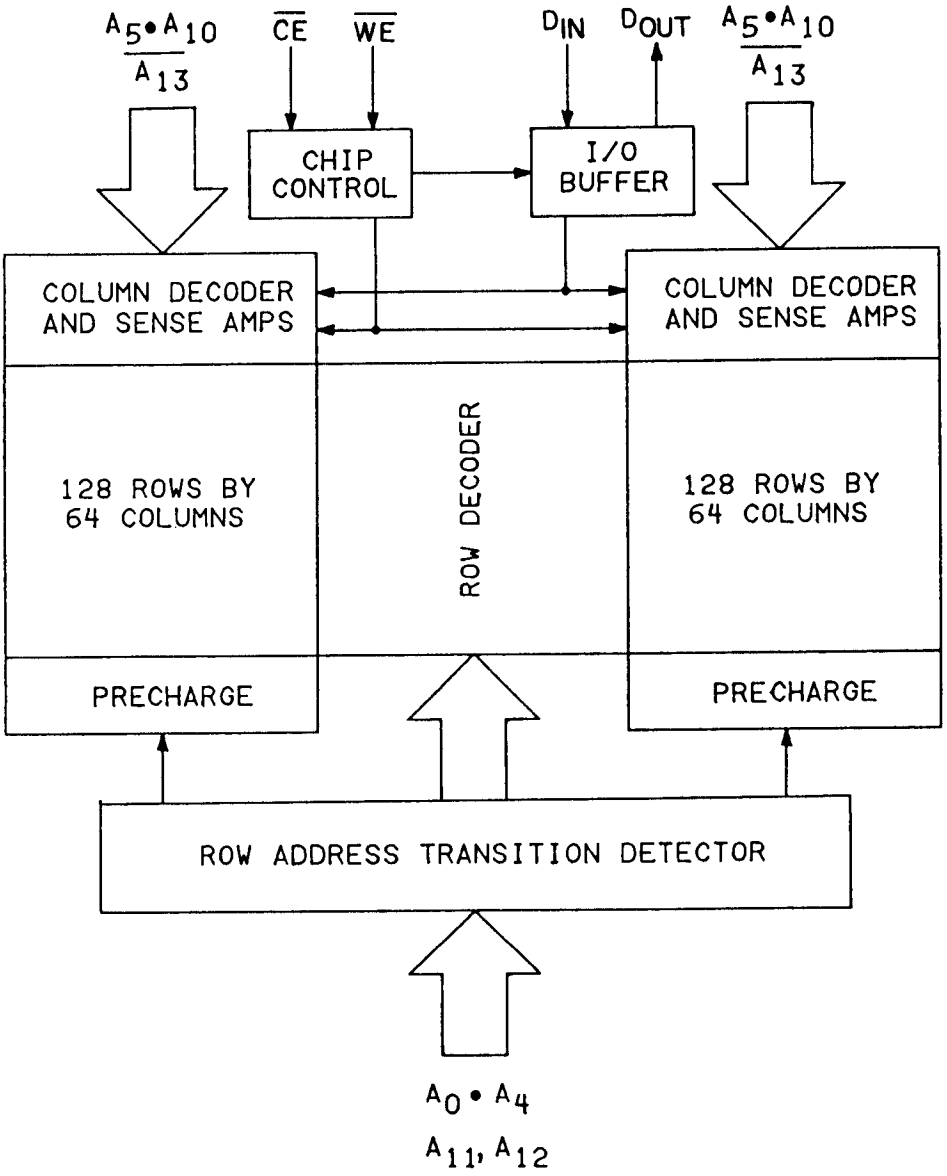


FIGURE 2. Block diagrams - Continued.

Device types 01, 04, 05 and 10

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O operation
Standby	H	X	X	High Z
Read	L	L	H	D_{out}
Read	L	H	H	High Z
Write	L	X	L	D_{in}

Read cycle

Device type 02

Inputs					Function
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	
H	X	X	X	Z	Memory disable
↘	H	X	V	Z	Cycle begins, addresses are latched
L	H	L	X	X	Output enable
L	H	L	X	V	Output valid
↗	H	X	X	V	Read accomplished
H	X	X	X	Z	Prepare for next cycle
↘	H	X	V	Z	Cycle ends, next cycle begins

Write cycle

Device type 02

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	Function
H	X	H	X	X	Memory disable
↘	X	H	V	X	Cycle begins, addresses are latched
L	L	H	X	X	Write period begins
L	↗	H	X	V	Data in is written
↗	H	H	X	X	Write completed
H	X	H	X	X	Prepare for next cycle
↘	X	H	V	X	Cycle ends, next cycle begins

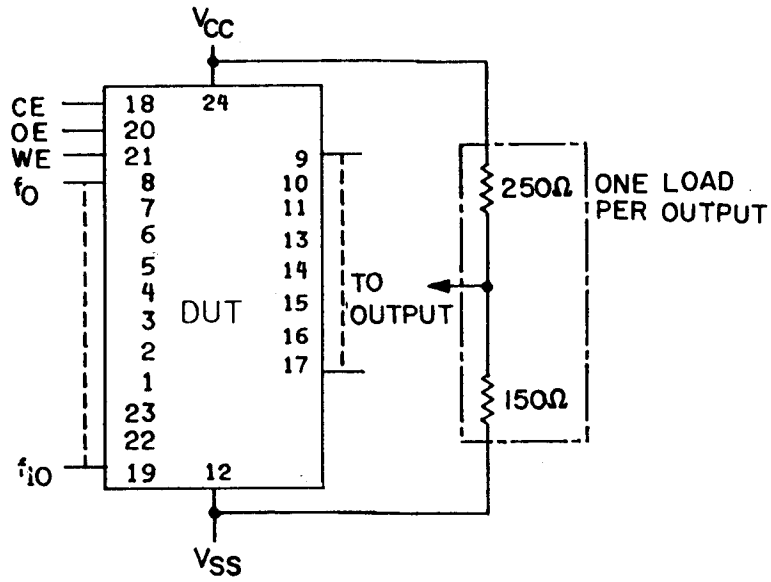
FIGURE 3. Truth table.

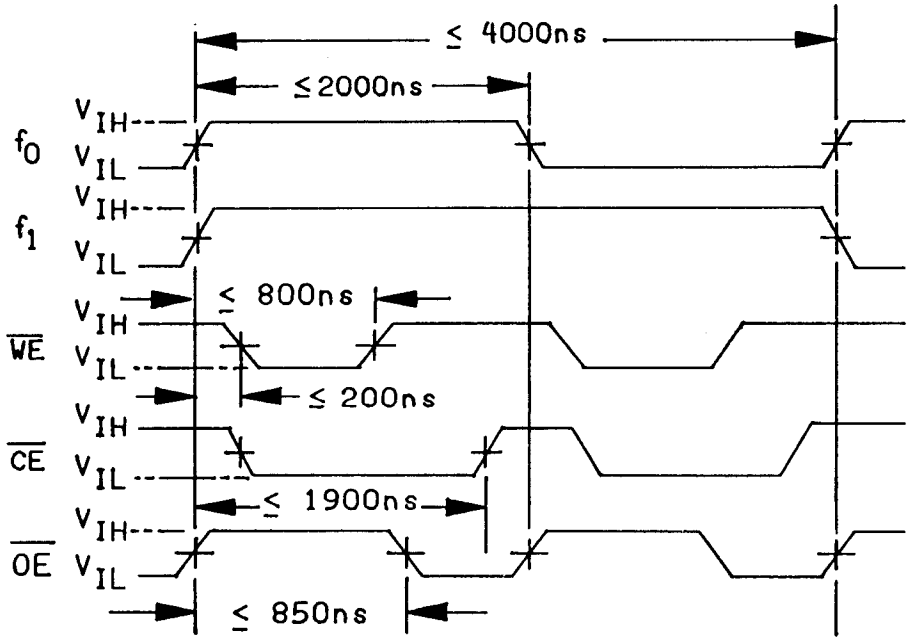
Device types 03, 06, 07, 08, and 09

Mode	$\overline{CE}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{out}	Active
Write	L	L	High Z	Active

FIGURE 3. Truth tables - Continued.

Device types 01 and 05

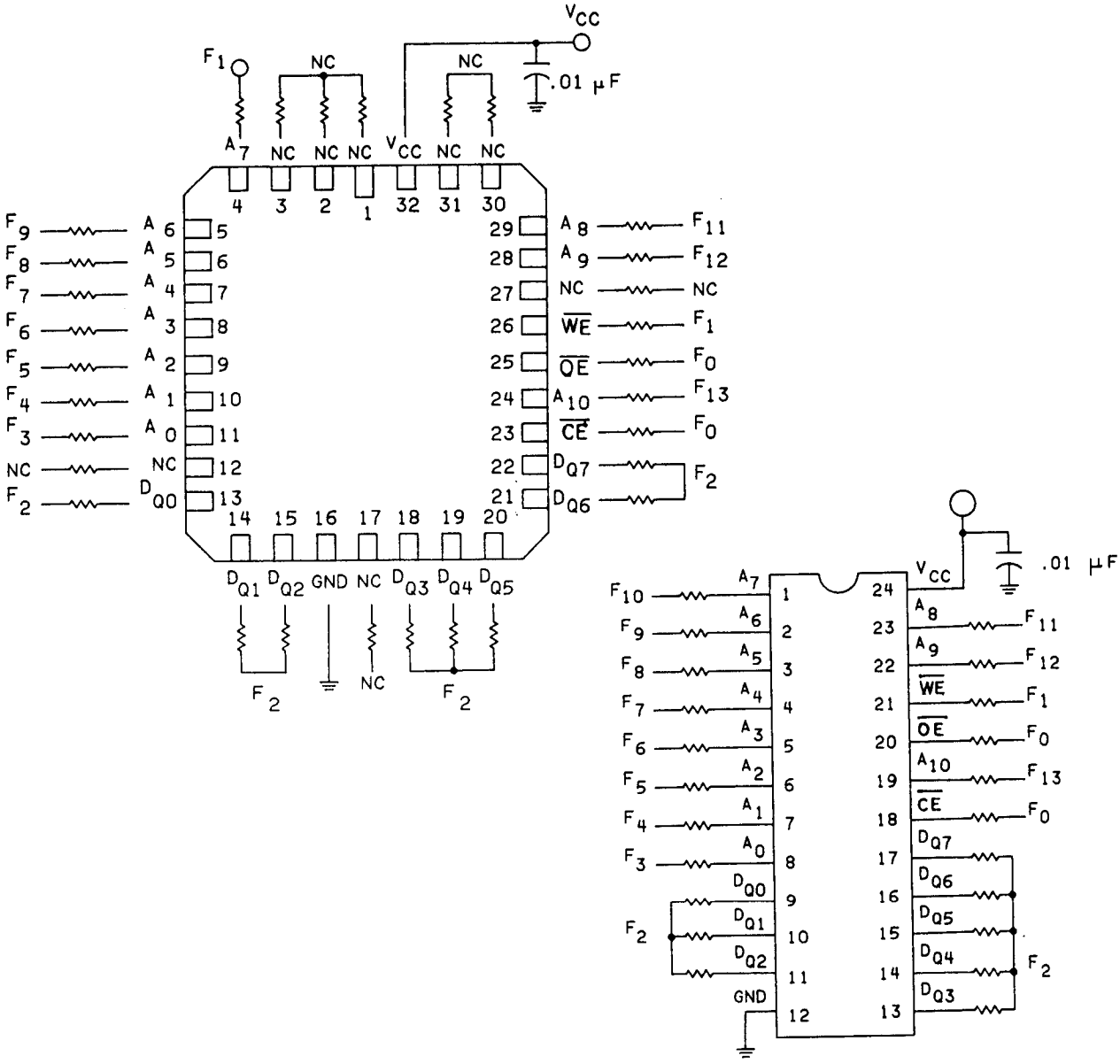




NOTES:
1. V_{CC} = 5.0 V, V_{SS} = 0 V.
2. V_{IH} = 2.0 V to V_{CC}, V_{IL} = 0 V to 0.8 V.
3. f_x = frequency applied to input terminal.
   $f_1 = \frac{f_0}{2}$, $f_2 = \frac{f_1}{2}$, -----, $f_{10} = \frac{f_9}{2}$

FIGURE 4. Burn-in and steady-state life test circuits.

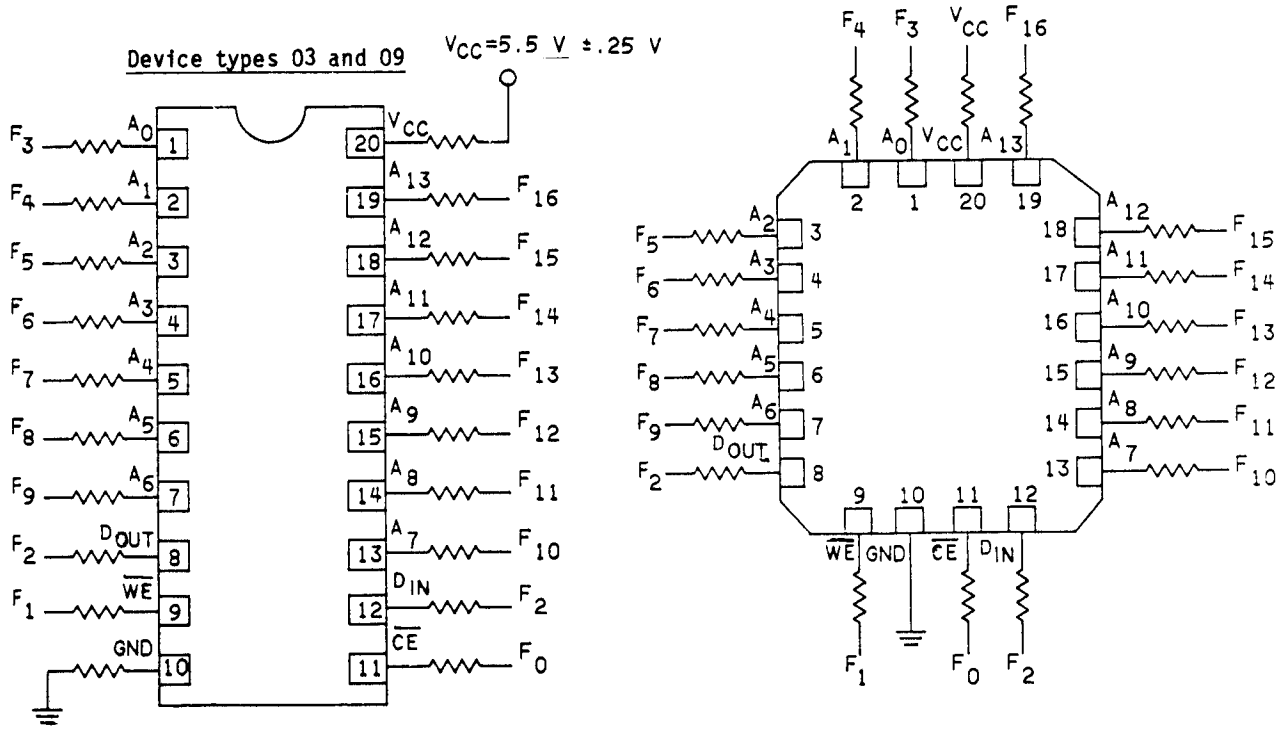
Device types 02, 04, and 10



NOTES:
V_{CC} = 5.0 V minimum at device pin
V_{IL} minimum = 0.0 V
V_{IH} maximum = 4.5 V
R = 47 kΩ ±10%
Caps = 0.01 μF ±10%

F_0 = 100 kHz ± 10%
$F_1 = F_0/2$
$F_2 = F_1/2$
$F_3 = F_2/2$
$F_4 = F_3/2$
$F_5 = F_4/2$
$F_6 = F_5/2$
$F_7 = F_6/2$
$F_8 = F_7/2$
$F_9 = F_8/2$
$F_{10} = F_9/2$
$F_{11} = F_{10}/2$
$F_{12} = F_{11}/2$
$F_{13} = F_{12}/2$

FIGURE 4. Burn-in and steady-state life test circuits - Continued.

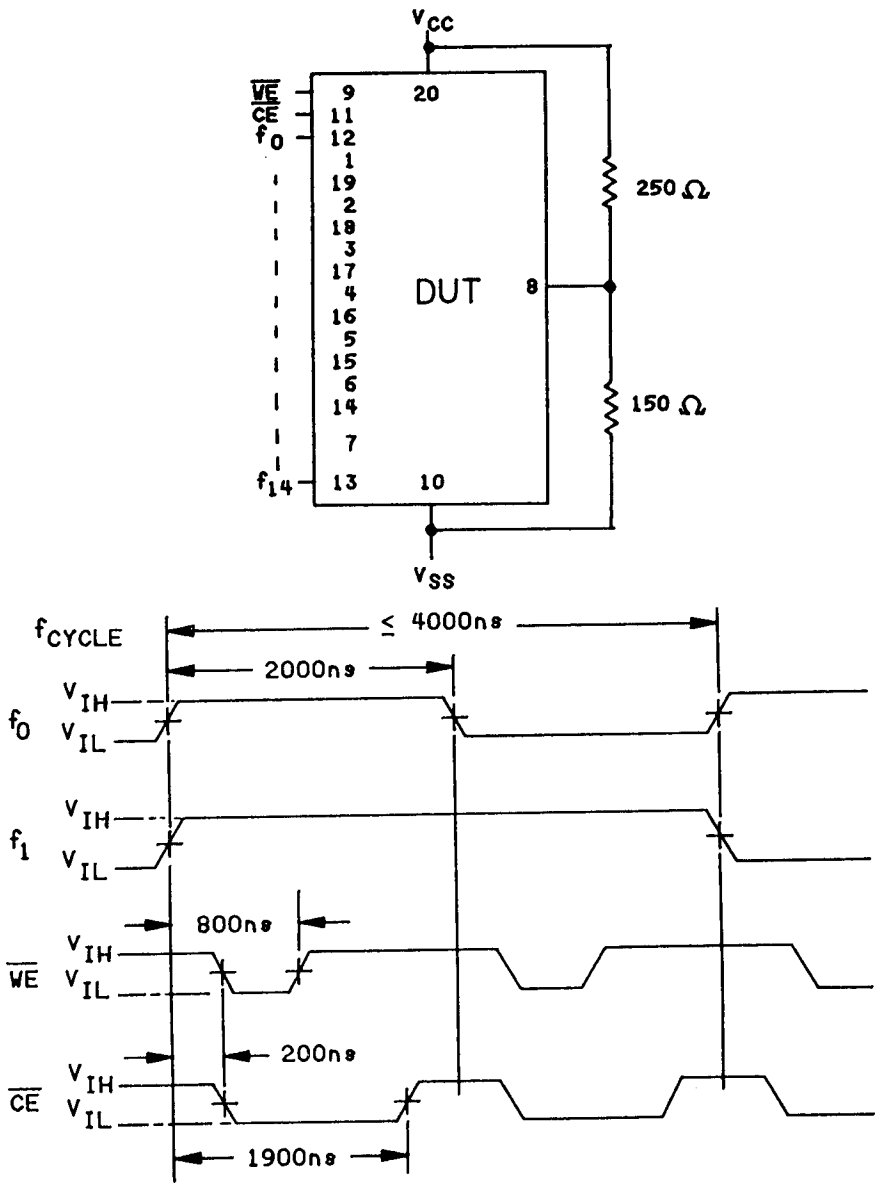


NOTES:
1. All resistor = 47 kΩ ±10%.
   F_0 = 100 kHz ±10%.
   $F_1 = F_{0/2}$, $F_2 = F_{1/2}$.....$F_{16} = F_{15/2}$.
2. Burn-in voltage:
   GND = 0 V.
3. Input voltage levels:
   $4.5\ V \leq V_{IH} \leq V_{CC}$

   $0\ V \leq V_{IL} \leq 0.8\ V$.

FIGURE 4. Burn-in and steady-state life test circuits - Continued.

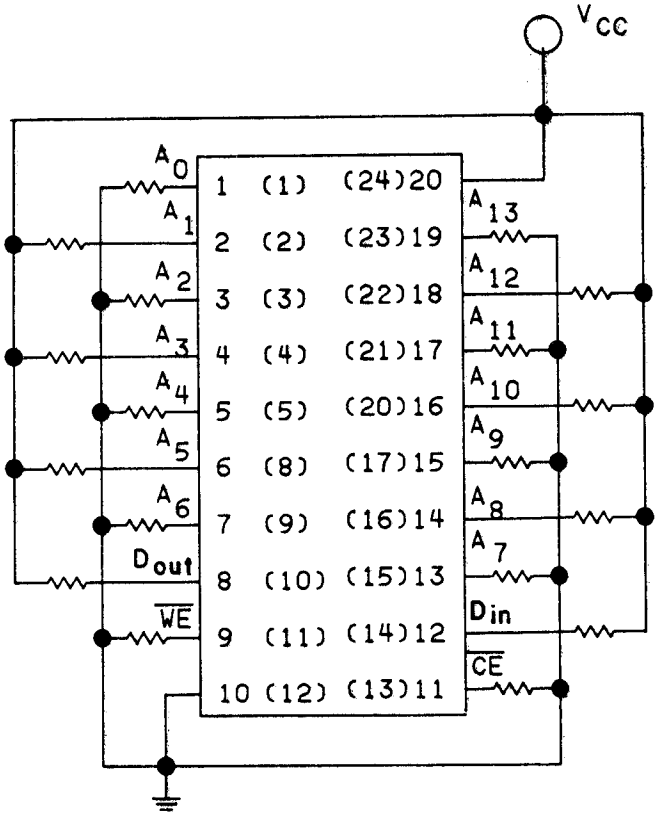
Device type 06



NOTES:
1. V_{CC} = 5.0 V, V_{SS} = 0 V.
2. V_{IH} = 2.0 V to V_{CC}, V_{IL} = 0 V to 0.8 V.
3. f_x = frequency applied to input terminal.
   $f_1 = \frac{f_0}{2}$, $f_2 = \frac{f_1}{2}$, -----, $f_{14} = \frac{f_{13}}{2}$

FIGURE 4. Burn-in and steady-state life test circuits - Continued.

Device types 07 and 08

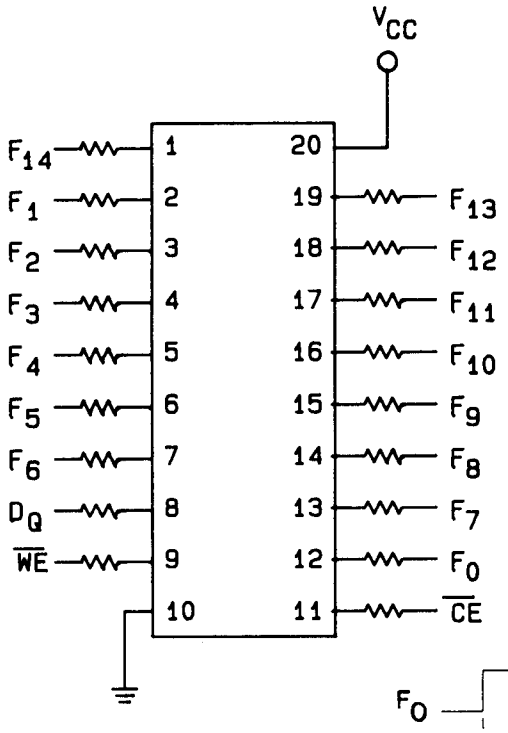


NOTE:
Numbers in parentheses are terminal numbers for the F-6A flat package.
V_{CC} = 6.0 volts ±10%
R = 27 kΩ, 1/4 watt, 10%

T_{Amax} = +135°C
Package: 20-lead DIP and 24-lead flat package

FIGURE 4. Burn-in and steady-state life test circuits - Continued.

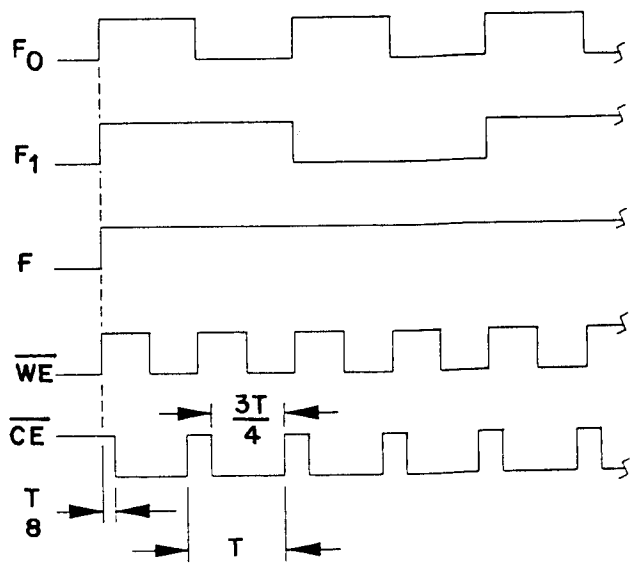
Device types 07 and 08



V_{CC} = 6.0 volts
All R = 27 kΩ, 1/4 watt, ±10%
Packages: 20 pin DIP
V_{CC} must be removed.
Use 0.1 μF decoupling capacitor between V_{CC} and GND each position.
F_0 = 100 kHz = 10%, 50% duty cycle

I_{CC} < 5 mA
V_{IL} = 0.8 volt
V_{IH} = V_{CC} -2.0 volts

$F_1 = F_0/2$	$F_8 = F_7/2$
$F_2 = F_1/2$	$F_9 = F_8/2$
$F_3 = F_2/2$	$F_{10} = F_9/2$
$F_4 = F_3/2$	$F_{11} = F_{10}/2$
$F_5 = F_4/2$	$F_{12} = F_{11}/2$
$F_6 = F_5/2$	$F_{13} = F_{12}/2$
$F_7 = F_6/2$	$F_{14} = F_{13}/2$

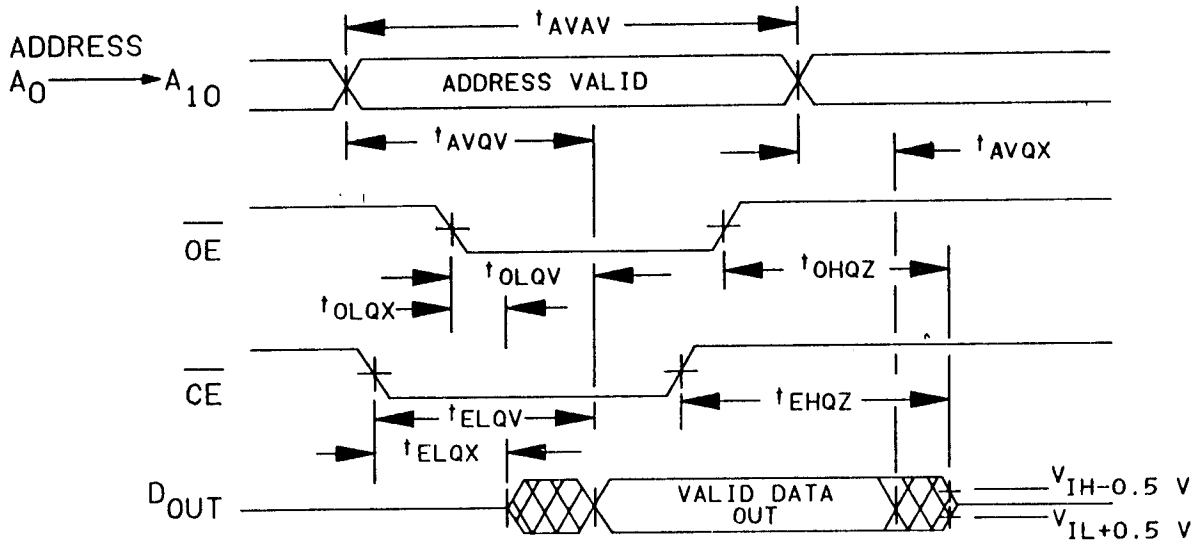


NOTES:
1. All pulse generators have the following characteristics: V_{IL} = 0 V to 0.8 V maximum; V_{IH} = 4.5 V minimum to V_{CC} maximum; 50% ±15% duty cycle and frequencies as specified in note 3.
2. Input frequencies are as follows: F_0 = 100 kHz minimum. $F_1 = F_0/2$, $F_2 = F_1/2$, $F_3 = F_2/2$, $F_4 = F_3/2 \ldots F_{14} = F_{13}/2$.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.

Dynamic burn-in and steady-state life

FIGURE 4. Burn-in and steady-state life test circuits - Continued.

Read cycle for device types 01, 04, 05, and 10



Write cycle timing for device types 01, 04, 05, and 10

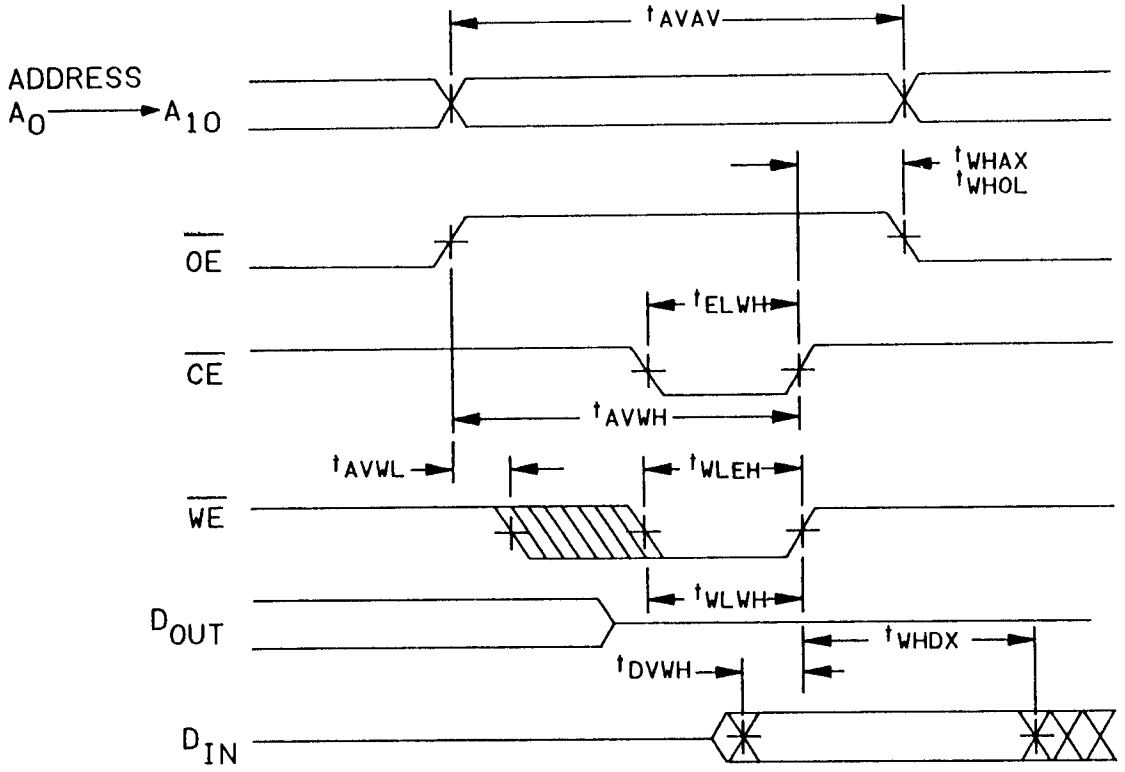
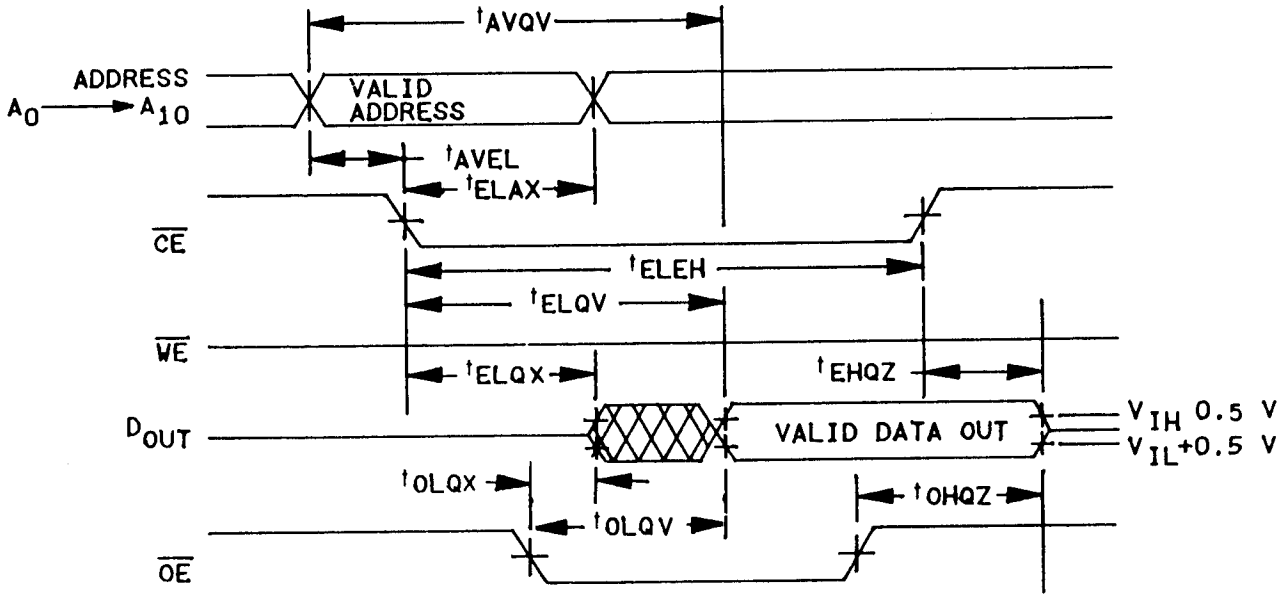


FIGURE 5. Timing diagrams.

Read cycle timing for device type 02



Write cycle timing for device type 02

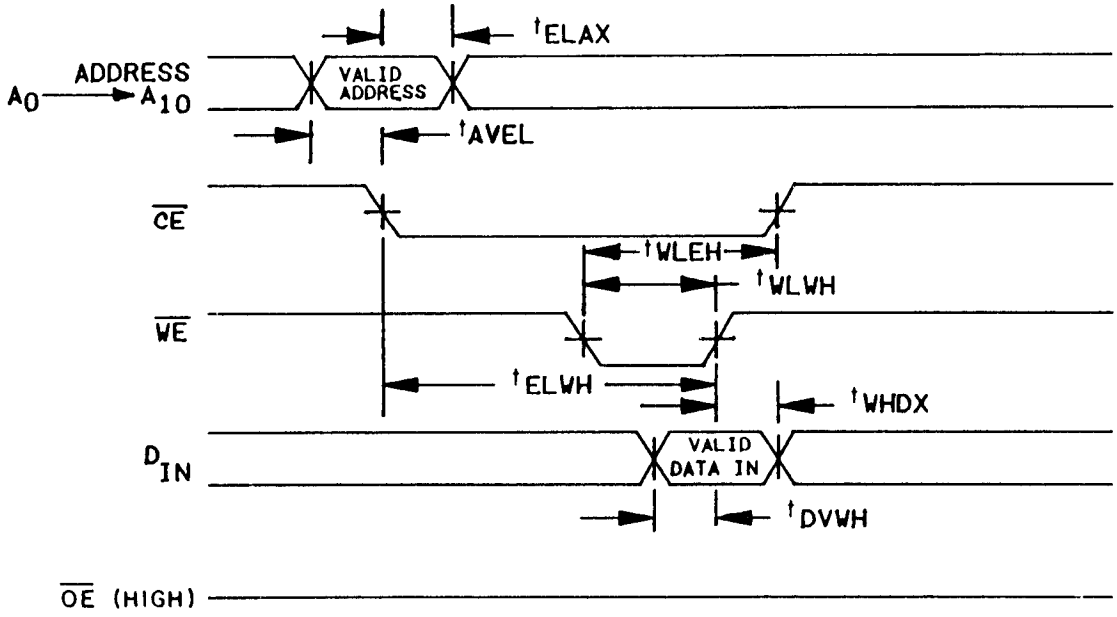
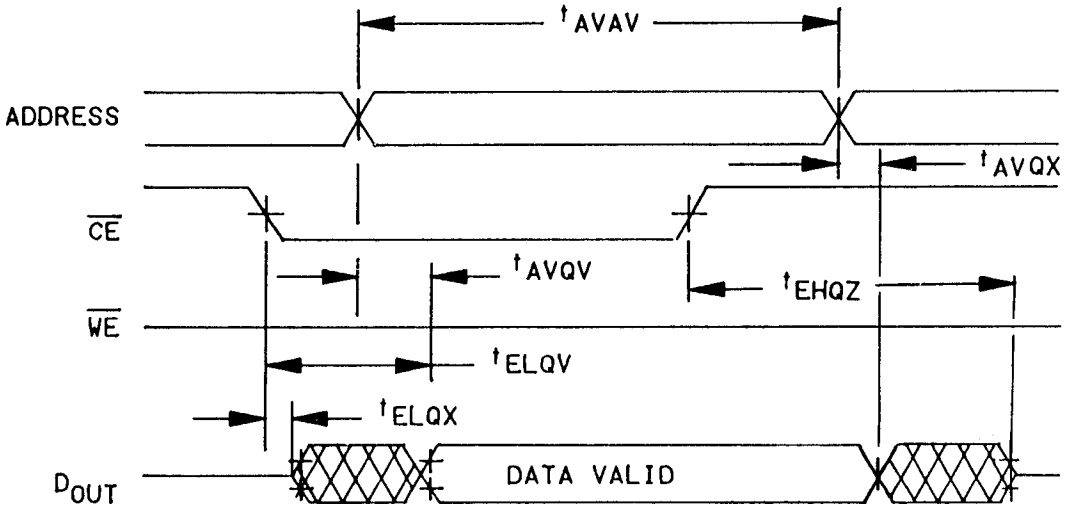


FIGURE 5. Timing diagrams - Continued.

Read cycle timing for device types 03, 06, and 09



Write cycle timing for device types 03, 06, and 09

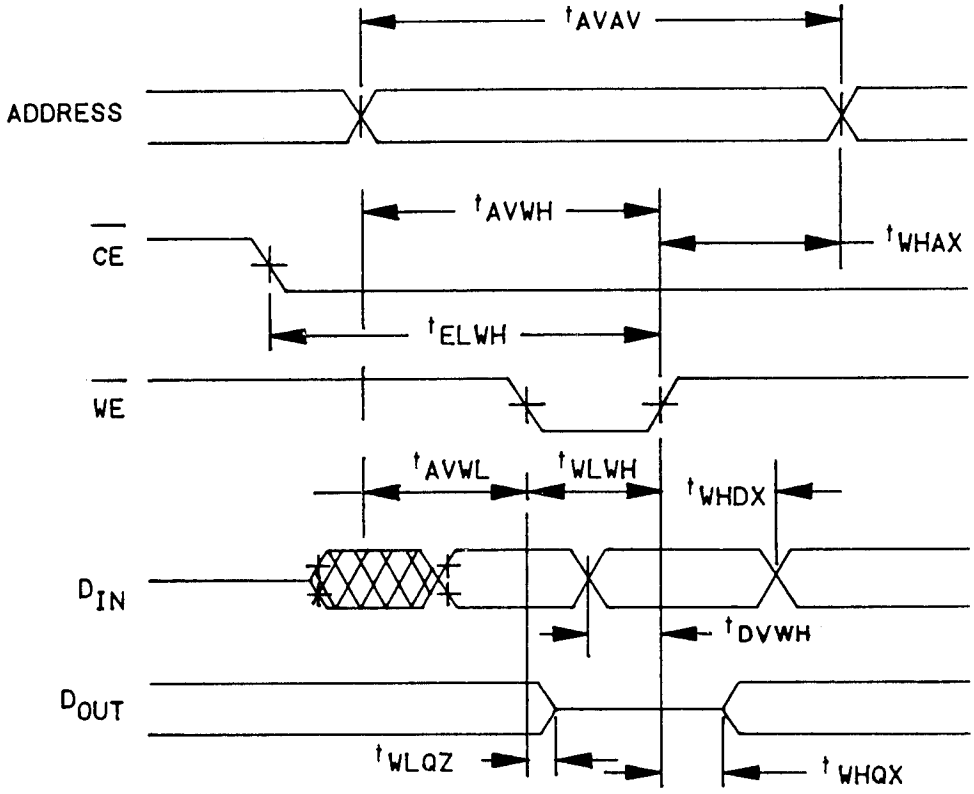
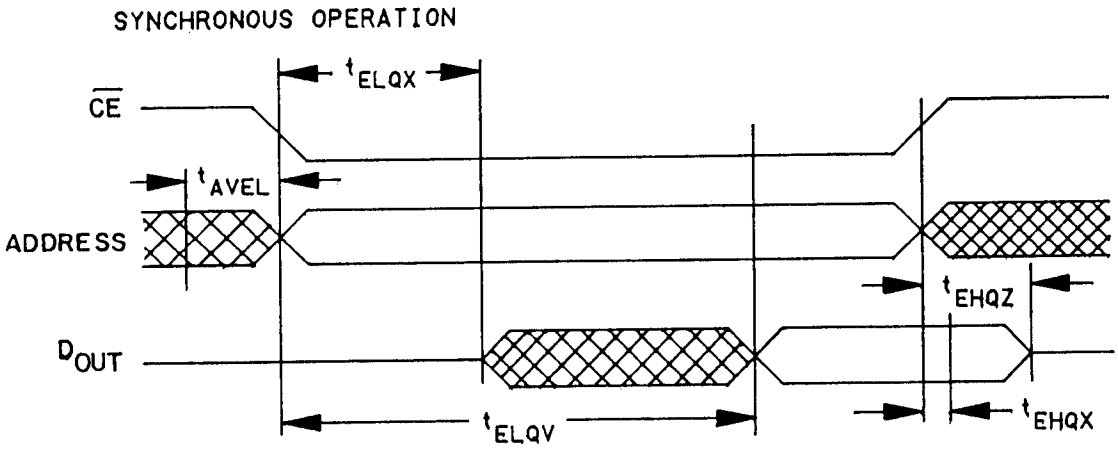


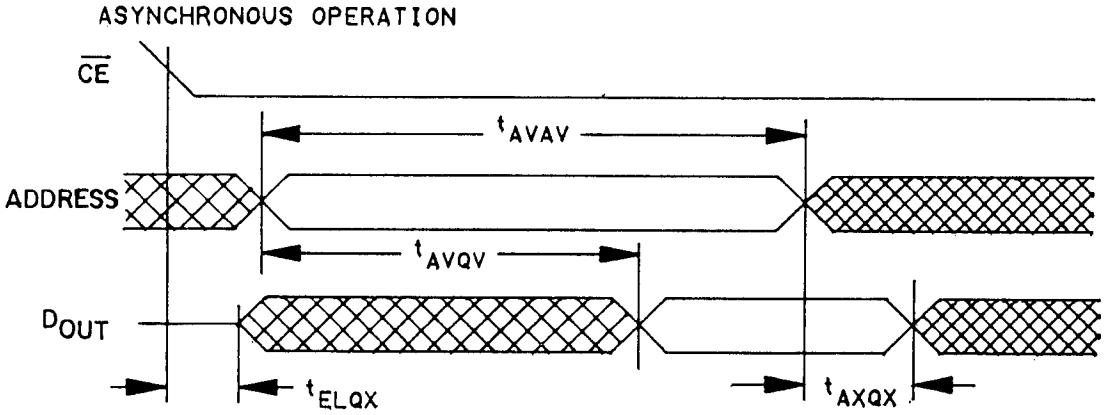
FIGURE 5. Timing diagrams - Continued.

Read cycle timing for device types 07 and 08



NOTES:
1. $\overline{WE}$ is held high for entire cycle and D_{out} is ignored. Address is stable by the time $\overline{CE}$ goes low and remains valid until $\overline{CE}$ goes high.
2. See figure 7 for test conditions.

Read cycle waveforms for device types 07 and 08

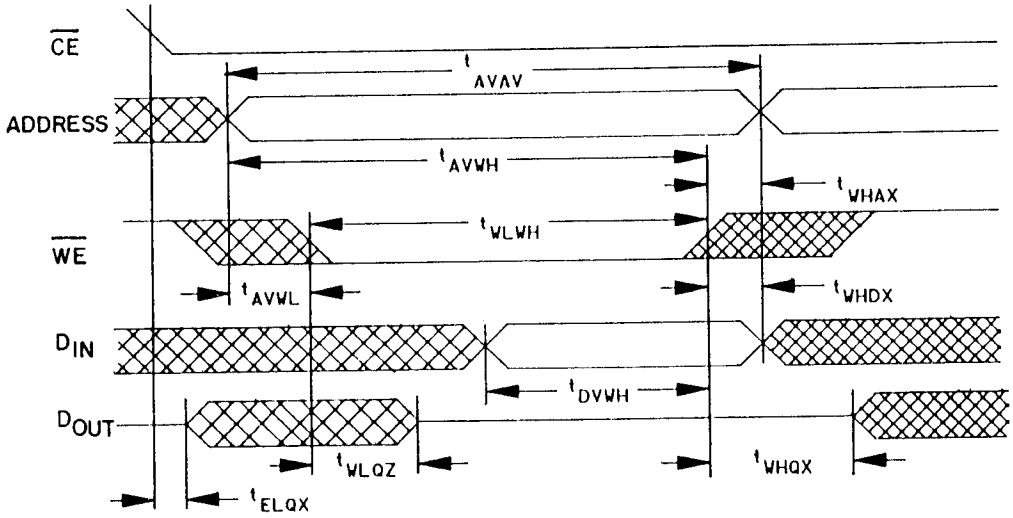


NOTES:
1. $\overline{WE}$ is high for entire cycle and D_{OUT} is ignored. $\overline{CE}$ is stable prior to address becoming valid and after address becomes invalid.
2. See figure 7 for test conditions.

FIGURE 5. Timing diagrams - Continued.

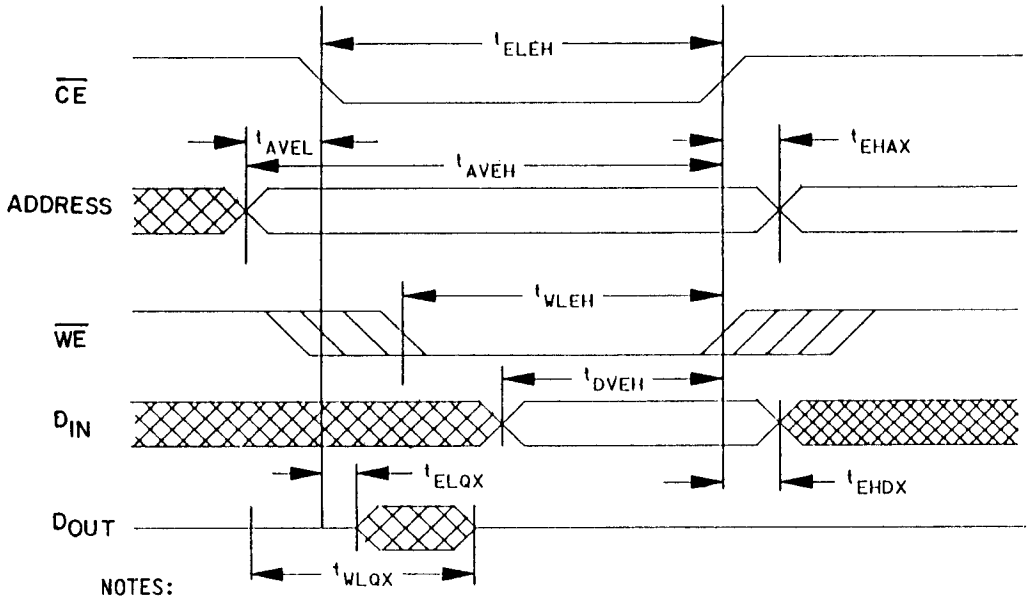
Write cycle timing for device types 07 or 08

ASYNCHRONOUS OPERATION



NOTES:
1. In this mode. $\overline{CE}$ rises after $\overline{WE}$. The address must remain stable whenever both $\overline{CE}$ and $\overline{WE}$ are low.
2. See figure 7 for test conditions.

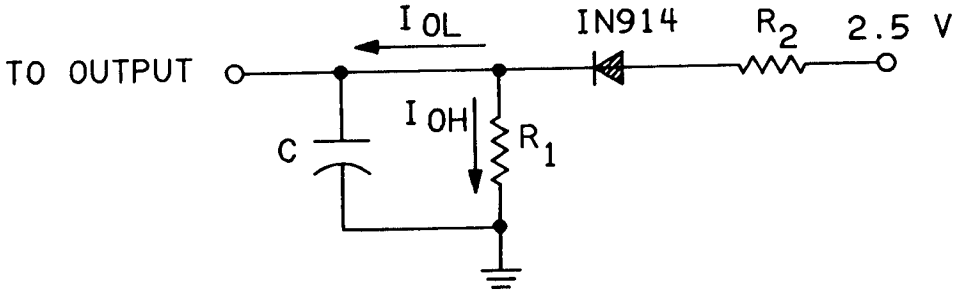
SYNCHRONOUS OPERATION



NOTES:
1. In this mode. $\overline{WE}$ rises after $\overline{CE}$. if t_{WLEL} ±0 ($\overline{WE}$ low before $\overline{CE}$) then D_{out} will remain in the high impedance state throughout the cycle. The address must remain stable whenever $\overline{CE}$ and $\overline{WE}$ are both low.
2. See figure 7 for test conditions.

FIGURE 5. Timing diagrams - Continued.

Device types 01, 05, and 06



Device types 01 and 05

NOTE:
R_1 = 2.4 kΩ ±5%
R_2 = 140Ω ±5%
C = 34 pF including jig and probe capacitance

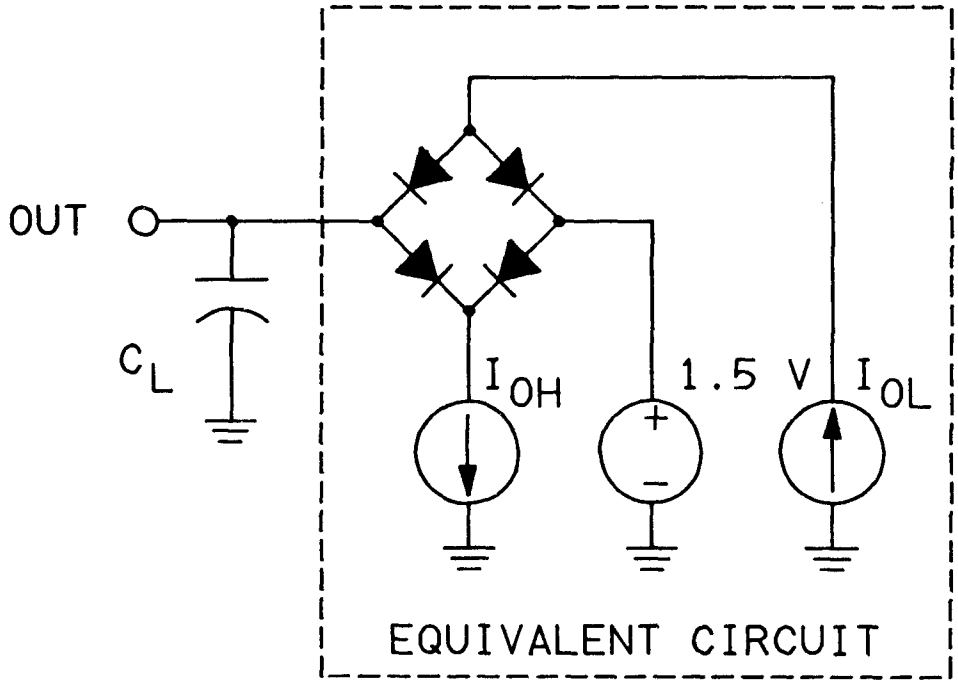
Device type 06

NOTE:
R_1 = 620Ω ±5%
R_2 = 180Ω ±5%
C = 30 pF including jig and probe capacitance

Output load circuit

FIGURE 6. Output load and switching time test circuits.

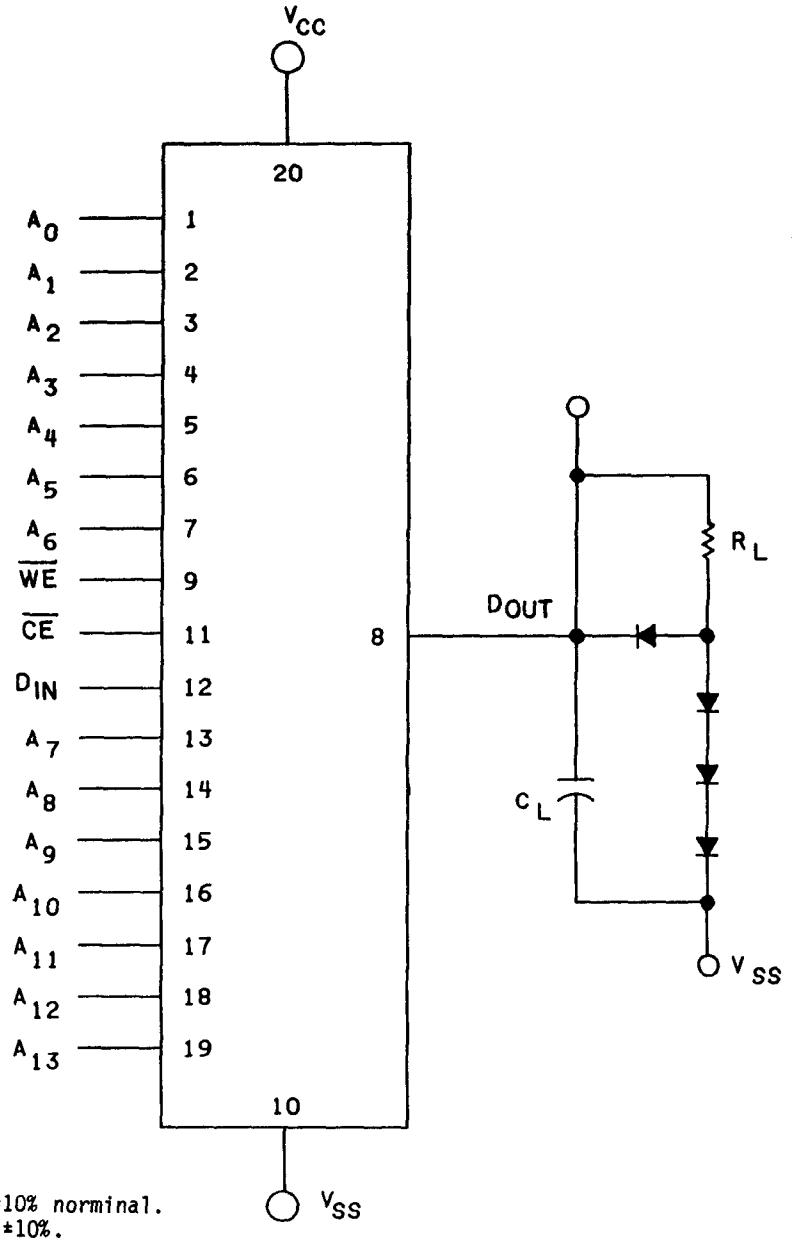
Device types 02, 03, 04, 09, and 10



NOTE: C_L = 50 pF.

FIGURE 6. Output load and switching time test circuits - Continued.

Device types 07 and 08

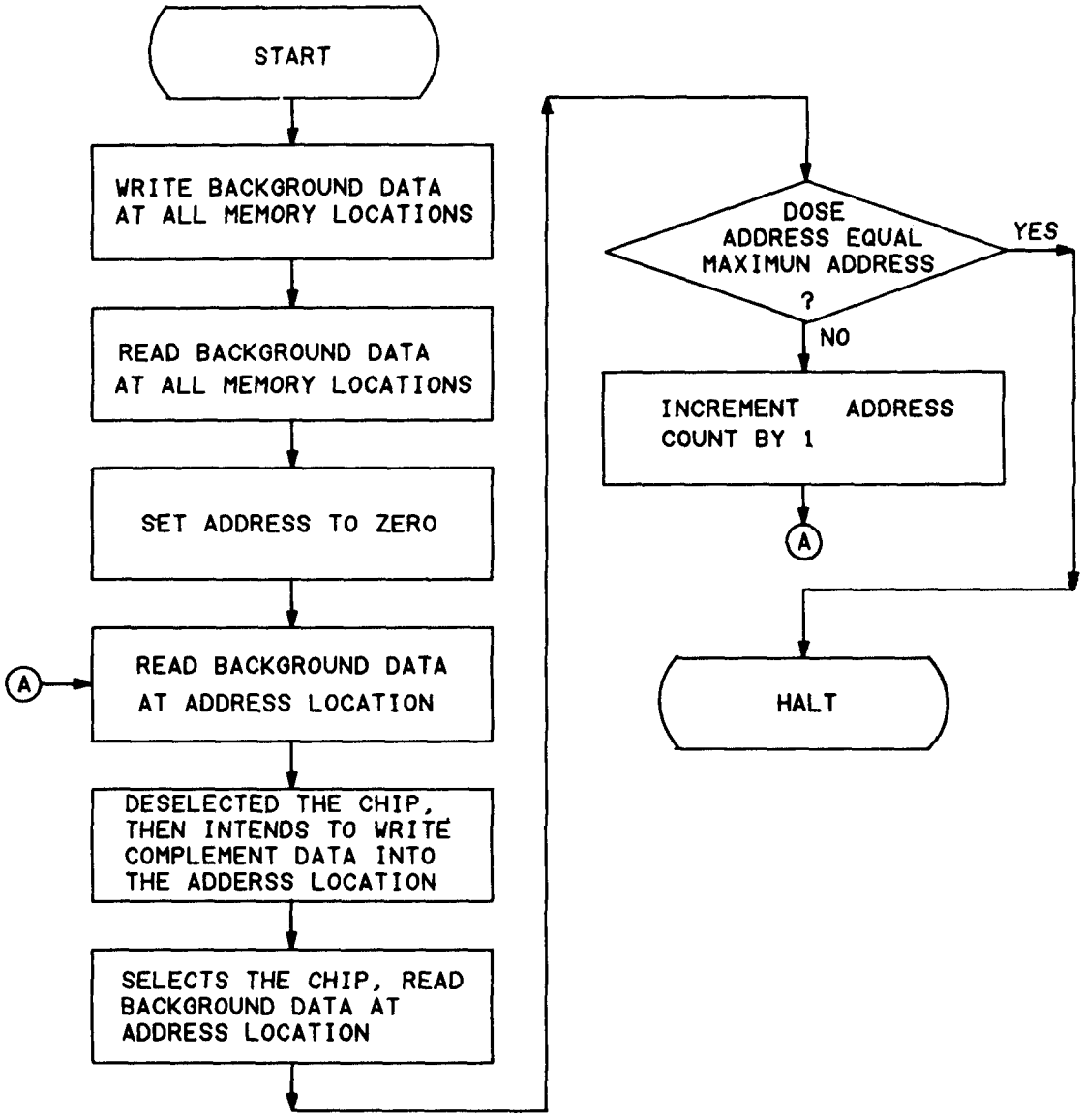


NOTES:
1. C_L = 50 pF ±10% norminal.
2. R_L = 2.2 kΩ ±10%.
3. Diodes are 1N914 or equivalent.
4. All t_{TLH} and $t_{THL} \leq 20$ ns.
5. All generator output impedance = 50 ohms nominal.
6. All voltages measured with respect to V_{SS} terminal.
7. See figure 5 for waveforms and figure 7 for timing conditions.

FIGAURE 6. Output load and switching time test circuits - Continued.

Timing parameter	Description	Device type 07		Device type 08		Unit
		Min	Max	Min	Max	
t_{AVAV}	Read cycle time	150	---	175	---	ns
t_{AVEL}	Address setup time	0	---	0	---	ns
t_{AVQV}	Address access time	---	150	---	175	ns
t_{ELQV}	Chip enable access time	---	150	---	175	ns
t_{ELQX}	Chip enable output enable time	20	---	40	---	ns
t_{EHQX}	Chip disable output hold time	20	---	40	---	ns
t_{AXQX}	Address invalid output hold time	40	---	60	---	ns
t_{EHQZ}	Chip disable output disable time	---	25	---	50	ns
t_{AVAV}	Write cycle time	150	---	175	---	ns
t_{ELWH}	Chip enable to end-of-write	100	---	125	---	ns
t_{WLWH}	Write enable pulse width	75	---	100	---	ns
t_{AVWL}	Address setup time	0	---	0	---	ns
t_{WHAX}	Address hold time	20	---	25	---	ns
t_{DVWH}	Data setup time	75	---	100	---	ns
t_{WHDX}	Data hold time	0	---	0	---	ns
t_{WLQZ}	Write enable output disable time	---	25	---	50	ns
t_{WHQX}	Write disable output enable time	0	---	---	---	ns
t_{AVWH}	Address valid to end-of-write	100	---	125	---	ns
t_{AVEL}	Address setup time	0	---	0	---	ns
t_{EHAX}	Address hold time	0	---	0	---	ns
t_{AVEH}	Address valid to end-of-write	100	---	125	---	ns
t_{ELEH}	Enable pulse width	100	---	125	---	ns
t_{WLEH}	Write to end-of-write	100	---	125	---	ns
t_{DVEH}	Data setup time	75	---	100	---	ns
t_{EHDX}	Data hold time	0	---	0	---	ns

FIGURE 7. Timing test conditions over operating temperature range.



Step 1. Write the array with background data.

Step 2. Read the array for background data.

Step 3. Read address location zero for background data.

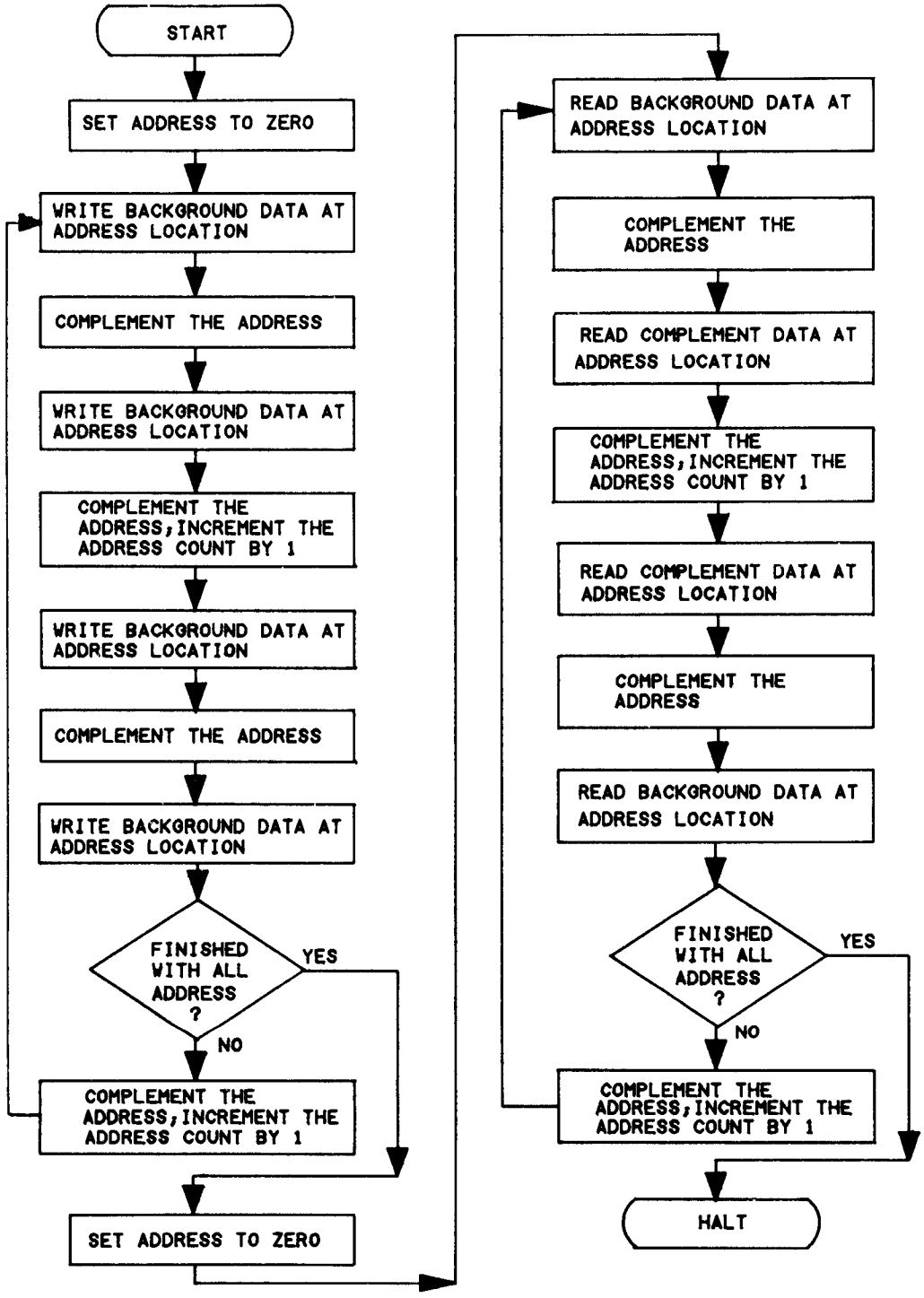
Step 4. Apply a Write cycle while deselecting the device (verifies that a Write operation cannot be performed while the device is disabled).

Step 5. Select the chip, and read address location zero for background data.

Step 6. Repeat steps 3 through 5 for each address location (sequentially).

Step 7. Repeat steps 1 through 6 with complement background data.

FIGURE 8. Not write pattern flow-chart.



DATA = 1 COMPLEMENT DATA = Ø FOR DEVICE TYPE 01
DATA = 10101010 FOR DEVICE TYPE 02

COMPLEMENT DATA = 01010101

FIGURE 9. Write/write address complement flow-chart.

3.6.2 Correctness of indexing and marking. All devices shall be subjected to the final electrical test specified in table II after marking to verify that they are correctly indexed and identified by part number. Optionally, an approved electrical test may be devised especially for this requirement.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Step coverage acceptance criteria. The step coverage acceptance criteria (class S microcircuits) of 3.7.1 of method 2018 should read, "Oxide steps. All four directional edges of every type of oxide step (contact window or other type of oxide step) shall be examined (refer to 3.4.2). A directional edge shall be unacceptable if any defect or combination of defects, excluding thinning, reduces the cross section area on either side of the directional edge. The metal shall not be thinned to less than 4,000 A. For an oxide step (contact window or other type of oxide step) to be acceptable, all four directional edges must be covered with metallization (in accordance with 3.4.2) and be acceptable (in accordance with the preceding sentence) except in the cases described in 3.7.1a and 3.7.1b. Where all contact cuts are completely covered by metal, the metallization viewed from the normal viewing angle (refer to 3.4.1) will show evidence of contoured metal flow into the contact area. Verification of the actual step coverage shall be determined by cross sectioning an additional die from the same wafer or using a test die to show contact step coverage of 4,000 A or more.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.

b. Burn-in (method 1015 of MIL-STD-883).

(1) Static test (test condition A) using the circuit shown on figure 4, or equivalent. Ambient temperature (T_A) shall be +125°C minimum. Test duration for the static test shall be 48 hours minimum for class S. The 48-hour burn-in may, at the manufacturer's option, be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic test (test condition D or E) using the circuit shown on figure 4, or equivalent. Test duration and temperature shall be in accordance with method 5004 of MIL-STD-883.

c. Interim and final electrical parameters shall be as specified in table II herein.

d. Post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.

e. The manufacturers of SOS devices shall use a high temperature stress test prior to the static burn-in. Conditions shall be static II, +125°C, supply voltage at 7 V ±0.5 V, and a duration of 48 hours minimum. A PDA of 15 percent shall be imposed. Devices need not be serialized prior to stress testing.

f. At the manufacturer's option, class S visual inspection is to be performed in accordance with MIL-STD-883, method 2010, condition A, except as follows:

(1) High magnification inspection is performed at 100X to 300X on the high current area of the chip.

(2) Criteria 3.1.1.1 and 3.1.1.2 shall be replaced by criteria 3.2.1.1 and 3.2.1.2, respectively, however, the 75 percent of the original metal width over passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.

(3) Criteria 3.1.1.7 shall apply to three areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and shall consist only of the area in the immediate field of view.

(4) Criteria 3.1.3c shall be replaced by 3.2.3c. Cracks greater than 5 mils are rejected only if they point to or cross the scribe grid line.

(5) Burn-in testing shall be performed at an operating voltage of 7 V ±0.5 V, if this option is chosen.

g. At the manufacturer's option, the class B visual inspection is to be performed in accordance with MIL-STD-883, method 2010, condition B, except as follows:

(1) Criteria 3.2.1.1 and 3.2.1.2 metallization scratches and voids, the 75 percent of the original metal width over passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.

(2) Criteria 3.2.1.7 shall apply to three areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and consist only of the area in the immediate field of view.

(3) Criteria 3.2.3c. Cracks greater than 5 mils are rejected only if they point or cross the scribe grid line.

(4) Burn-in testing shall be performed at an operating voltage of 7 ±0.5 V, if this option is chosen.

4.2.1 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in for all failures, with 3 percent maximum on functional failures for either burn-in. Static burn-in failures for the split sequence (where a split sequence procedure is used) shall be cumulative for determining PDA.

b. If interim electrical parameter measurements are made to remove defective devices from the lot prior to the burn-in sequence, the number of devices that fail these measurements may be excluded from the PDA calculations for class S devices. Following this, pre and post burn-in electrical parameter measurements results shall be used as specified to compute PDA's.

c. Those devices whose measured characteristics after burn-in exceed the specified delta (Δ) limits or specified electrical parameter limits are failures and shall be removed from the lot (see 3.5 and 4.5.3). The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA or one device, whichever is greater.

d. The PDA for class B devices shall be 5 percent for subgroup 1 failures after dynamic burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection. If a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device may be part I qualified without further qualification testing. At the manufacturer's request, the slower device types will be added to the QPL.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be performed in accordance with table II herein.

b. The following subgroups of table I of method 5005 of MIL-STD-883 shall be omitted:

(1) Class S devices: Subgroups 5, 6, and 7.

(2) Class B devices: Subgroups 5, 6, and 8.

c. Subgroup 4 (C_i, C_o measurements) shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz and a signal amplitude not to exceed 50 mV rms. This test shall be performed using a fixed sample size of 25 devices and an acceptance number of zero.

d. Subgroup 12 shall be added to the group A inspection requirements using an LTPD of 15 and shall consist of the procedures, test conditions, and limits specified in table III herein.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Class S steady-state life test circuit of figure 4, or equivalent shall be used.

b. Class S electrical test requirements shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection and shall consist of tests specified in table IV herein.

c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4, or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883, and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Life test (method 1005 of MIL-STD-883) conditions, or equivalent.

(1) Test condition D or F as specified in 4.5.2 and figure 4, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for the RHA devices and shall be performed in accordance with table V of method 5005 of MIL-STD-883, 4.5.6, and table VI herein.

4.4.6 Inspection of packaging. The inspection of packaging shall be as specified in MIL-M-38510.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown and electrical test procedures. When devices are measured at +25°C following application of the life or burn-in test condition, all devices shall be cooled to +35°C prior to removal of bias voltages. Any electrical tests required shall first be performed at -55°C or +25°C prior to any +125°C tests that are required.

4.5.3 Delta measurements. Delta measurements, as specified in table II, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IV herein.

TABLE IV. Delta limits at +25°C.

Parameters 1/	Limits		
	02, 03, 04, 09, 10	07, 08	01, 05, 06
I_{CC}	+30 μA	±30 μA	
V_{OL}	+60 mV	±40 mV	+60 mV
V_{OH}	-400 mV	±340 mV	-200 mV
I_{IL}	-500 nA	±100 nA	-50 nA
I_{IH}	+500 nA	±100 nA	+50 nA

1/ Conditions and mechanization of measurements shall be as specified in table III, subgroup 1.

4.5.4 Electrostatic discharge sensitivity (ESD) classification. Electrostatic discharge sensitivity (ESD) shall be performed in accordance with method 3015 of MIL-STD-883. ESD testing shall be measured for initial qualification and after process or design changes which may affect ESD classification. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass (ESD) testing in accordance with method 3015 of MIL-STD-883 shall be considered as conforming to the requirements of this specification.

4.5.5 Quiescent supply current tests. When performing quiescent supply current measurements, the meter shall be placed so that all currents flow through the meter.

4.5.6 RHA testing. The RHA testing shall be performed in accordance with procedures and sampling specified in table V of method 5005 of MIL-STD-883 and herein:

a. Before irradiation, selected samples shall be assembled in qualified packages and pass the governing electrical parameters (group A, subgroup 1 at +25°C).

b. Radiation exposure shall be performed according to method 1019 of MIL-STD-883 with the devices biased in accordance with table V, and meet the group E end-point electrical parameters as defined in table I at +25°C ±5°C after exposure. The ionizing radiation exposure shall be 200 KRads (Si).

4.6 Data reporting. When specified in the contract or purchase order, a copy of the following data, as applicable, shall be supplied:

a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and steady-state life tests.

b. A copy of each radiograph.

c. The quality conformance inspection data (see 4.4).

d. Parameter distribution data on parameters evaluated during burn-in.

e. Final electrical parameters data.

TABLE V. Bias during exposure to radiation.

Device type	Pin connections	V_{SS} = GND	V_{CC} = 5 V dc
	V_{CC} (through a 1 kΩ to 60 kΩ resistor)		
07	1, 2, 3, 4, 5, 6, 7, 8*, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	10	20
08	1, 2, 3, 4, 5, 6, 7, 8*, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	10	20

* Output pins connected to voltage divider.

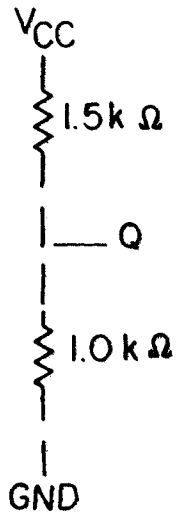


TABLE VI. Group E end-point electrical parameter limits for devices 07 and 08.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, V_{CC} = 5.5 V -55°C < T_C < +125°C unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 5.0 mA	07 08		0.4 0.4	V V
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -5 mA	07 08	4.0 4.0		V V
Input leakage current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	07 08		1.0 1.0	µA µA
Input leakage current	I_{IL}	V_{CC} = 5.5 V V_{IN} = GND	07 08		-1.0 -1.0	µA µA
High impedance output leakage	I_{OHZ}	V_{CC} = 5.5 V	07 08		10.0 10.0	µA µA
High impedance	I_{OLZ}	V_{CC} = 5.5 V	07 08		-10.0 -10.0	µA µA
Standby supply	I_{CC}	V_{CC} = 5.5 V	07 08		200 5	µA mA
Data retention supply voltage	V_{CCDR}	V_{CC} = 3.0 V minimum (see power down test in table III)	07 08	3.0 3.0		V V
Operating current	I_{CCOP}	T_C = +25°C, V_{CC} = 5.5 V f = 1 MHz	07 08		6 6	mA mA
Data retention quiescent supply current	I_{CCDR}	V_{CC} = 3.0 V, I_O = 0 V_I = V_{CC} or GND	07 08		100 100	µA µA
Input capacitance	C_I	V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND f = 1 MHz	07 08		8 8	pF pF

See footnote at end of table.

TABLE VI. Group E end-point electrical parameter limits for devices 07 and 08 - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, V_{CC} = 5.5 V -55°C < T_C < +125°C unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Address access time	t_{AVQV}	See table III	07 08	150 175		ns ns
Chip enable access	t_{ELQV}		07 08	150 175		ns ns
Read cycle time	t_{AVAV}		07 08	150 175		ns ns
Chip enable output time	t_{ELQX}		07 08	20 40		ns ns
Chip enable output disable	t_{EHQZ} 1/		07 08		25 50	ns ns
Chip enable pulse negative width	t_{ELEH}		07 08	100 125		ns ns
Chip disable output hold time	t_{EHQX}		07 08	20 40		ns ns
Address setup time	t_{AVEL}		07 08	0 0		ns ns
Address invalid output hold time	t_{AXQX}		07 08	40 60		ns ns
Write enable pulse width	t_{WLWH}		07 08	75 100		ns ns
Write enable pulse setup time	t_{WLEH}		07 08	100 125		ns ns
Address setup time	t_{AVWL}		07 08	0 0		ns ns
Chip enable to end-of-write	t_{ELWH}	See table III I_O = 0, V_I = V_{CC} or GND	07 08	100 125		ns ns

See footnote at end of table.

TABLE VI. Group E end-point electrical parameter limits for devices 07 and 08 - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, V_{CC} = 5.5 V -55°C < T_C < +125°C unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Write disable output enable time	t_{WHQX}	See table III	07 08	0 0		ns ns
Address valid to end-of-write	t_{AVWH}		07 08	100 125		ns ns
Address hold time	t_{WHAX}		07 08	15 25		ns ns
Address hold time	t_{EHAX}		07 08	0 0		ns ns
Address valid to end-of-write	t_{AVEH}		07 08	100 125		ns ns
Write enable output disable time	t_{WLQZ}		07 08		25 50	ns ns
Data setup time	t_{DVWH}		07 08	75 100		ns ns
Data hold time	t_{WHDX}		07 08	0 0		ns ns
Data setup time	t_{DVEH}		07 08	75 100		ns ns
Data hold time	t_{EHDX}		07 08	0 0		ns ns

1/ This parameter is guaranteed, but not tested.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure anaylsis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

h. Requirements for JAN marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

V_{SS}	Common or reference voltage mode.
V_{CC}	Supply voltage.
A_0-A_{13}	Address inputs, used to address 1 of 16,384/1 bit locations in static storage array.
$\overline{CE}$	Chip enable, used along with the write enable ($\overline{WE}$) signal to control the states of the data in (D_{IN}) and data out (D_{OUT})/(D_Q) buses.
D_{OUT}/D_Q	Data output.
D_{IN}	Data input through which data is stored.
$\overline{WE}$	Write enable, used to select the Read or Write mode.
I_{CC}	Supply current.

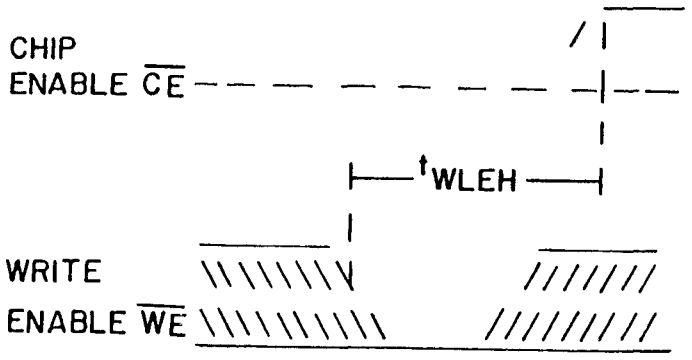
I_{IH}, I_{IL}	Input leakage current.
I_{OHZ}, I_{OLZ}	High impedance output leakage current.
V_{IL}	Logical low input voltage.
V_{IH}	Logical high input voltage.
V_{OL}	Logical low output voltage.
V_{OH}	Logical high output voltage.
C_i	Input capacitance.
C_o	Output capacitance.
t_{ELQV}	Chip enable access time.
t_{AVQV}	Address access time.
t_{EHQZ}	Chip enable to output disable.
t_{AVAV}	Read cycle time.
t_{AVQX}	Output hold after address change.
t_{ELQX}	Chip enable to output active.
t_{WLWH}	Write pulse width.
t_{ELWH}	Chip enable to end-of-write.
t_{DVWH}	Data setup to end-of-write.
t_{WHDX}	Data hold after end-of-write.
t_{AVWL}	Address setup before write enable low.
t_{AVWH}	Address setup to end-of-write.
t_{WHAV}	Write recovery time.
t_{OLQV}	Output enable access time.
t_{OLQX}	Output enable to output active.
t_{OHQX}	Output enable to output disable time.
t_{AVEL}	Address to chip enable setup time.
t_{ELAX}	Address to chip enable hold time.
t_{ELEH}	Chip enable pulse negative width.
t_{EHEL}	Chip enable pulse positive width.
t_{WLEH}	Write enable pulse setup time.
t_{ELEL}	Read or Write cycle time.

6.3.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus, the format is:

Initial character	t	X	X	X	X
Signal name from which interval is defined					
Transition direction for first signal					
Signal name to which interval is defined					
Transition direction for second signal					

Signal definitions:
A = Address
D_{IN} = Data in
D_{OUT}/D_Q = Data out
$\overline{WE}$ = Write enable
$\overline{CE}$ = Chip enable
O = Output enable

Transition definitions:
H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)



The example shows Write pulse setup time defined as t_{WLEH}-time from Write enable low to Chip enable high.

Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of views. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Waveforms

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKOWN
		HIGH IMPEDANCE

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01,04,05	6116
02	6516
03, 09	65262
04, 10	65162
06	61C16
07	65C262RH
08	65T262RH

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment, tools, and operator.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive foam or carriers.

e. The use of plastic, rubber, or silk in MOS areas should be avoided.

f. Relative humidity should be maintained above 50 percent, if practical.

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS.

30.1 Algorithm A (pattern 1).

30.1.1 Address complement, data background = all "0's".

This pattern produces maximum address line noise. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Read minimum address location.
Step 3. Load minimum address location with "1".
Step 4. Read maximum address location.
Step 5. Load maximum address location with "1".
Step 6. Read minimum address location +1.
Step 7. Load minimum address location +1 with "1".
Step 8. Read maximum address location -1.
Step 9. Load maximum address location -1 with "1".
Step 10. Repeat steps 2 through 9 until all address locations have been read and loaded with "1's".
Step 11. Repeat steps 2 through 10 reading "1's" and loading "0's".
Step 12. Read memory, all "0's".

30.2 Algorithm B (pattern 2).

30.2.1 GALPAT (ping pong) data background = "0".

This pattern tests for performance sensitivities by testing all possible combinations of address and data out transitions. It is performed in the following manner:

Step 1. Load memory with data background.
Step 2. Write data complement in location 0 (test bit).
Step 3. Alternately read test bit and each location in the array.
Step 4. Write the test bit back to background data.
Step 5. Repeat steps 2 through 4 with each location in the array.
Step 6. Repeat steps 1 through 5 with complemented background data.

30.3 Algorithm C (pattern 3).

30.3.1 March data, data background = all "0's".

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Read location 0.
Step 3. Write data complement in location 0.
Step 4. Read data complement in location 0.
Step 5. Repeat steps 2 through 4 for all other locations in memory (sequentially).
Step 6. Read data complement at location 0.
Step 7. Write data at location 0.
Step 8. Read data at location 0.
Step 9. Repeat steps 6 through 8 for all other locations in the memory (sequentially).
Step 10. Repeat steps 1 through 9 with data background of all "1's".

30.4 Algorithm D (pattern 4).

30.4.1 Data retention, data background = checkerboard.

This algorithm tests for data retention mode functionality. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Set chip enable = V_{CC}.
Step 3. Reduce V_{CC} and chip enable to minimum V_{DR}.
Step 4. Pause for 200 ms.
Step 5. Bring V_{CC} and chip enable back up and test for background data.
Step 6. Repeat steps 1 through 5 with complemented background data.

30.5 Algorithm E (pattern 5).

30.5.1 Checkerboard, $\overline{\text{checkerboard}}$.

Step 1. Load memory with a checkerboard pattern.
Step 2. Read the memory, verifying the checkerboard pattern.
Step 3. Load the memory with a $\overline{\text{checkerboard pattern}}$.
Step 4. Read the memory, verifying the $\overline{\text{checkerboard}}$ pattern.

30.6 Algorithm F (pattern 6).

30.6.1 Butterfly.

Step 1. Write a background pattern of "0's" throughout the memory.
Step 2. Write a "1" (test bit) at the first location.
Step 3. Read the test cell and the next sequential cell in the same row, then the test cell and the next sequential cell in the same column, until all cells have been tested in the same row and column as the test cell.
Step 4. Rewrite the test cell to "0", write a "1" into the next cell which will become the test cell, then repeat the ping-pong row-column march.
Step 5. After all cells have been used as test cells, repeat the test with complement data.

30.7 Algorithm G (pattern 7).

30.7.1 Spiral complement.

Step 1. Write a background pattern of "0's" in all cells.
Step 2. Beginning at cell "0", write and read a diagonal of "1's" on the field of "0's".
Step 3. Shift the diagonal one increment in the x-direction until each row has been used as a starting point of the diagonal and all cells within the diagonal have been tested.
Step 4. Repeat the test with complement data.

CONCLUDING MATERIAL

Custodians:
Air Force - 17
Army - ER
Navy - EC

Review activities:
Air Force - 11, 19, 85, 99
Army - AR, MI
Navy - OS, SH, TD
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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