

QUALIFICATION
REQUIREMENTS
REMOVED

MIL-M-38510/42C
3 May 1982
SUPERSEDING
MIL-M-0038510/42B
16 April 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, LOW POWER,
MONOSTABLE MULTIVIBRATORS, MONOLITHIC SILICON

INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, low power, monostable multivibrator microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device types shall be as follows:

Device type	Circuit
01	Single monostable multivibrator
02	Single retriggerable monostable multivibrator with clear

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline, (see MIL-M-38510, appendix C)
A	F-1 (14-lead, 1/4" x 1/4", flat package)
B	F-3 (14-lead, 1/4" x 1/8", flat package)
C	D-1 (14-lead, 1/4" x 3/4", dual-in-line package)
D	F-2 (14-lead, 1/4" x 3/8", flat package)

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	0 V to 8.0 V
Input voltage range - - - - -	0 V to 5.5 V
Storage temperature range - - - - -	-65° to 150°C
Maximum power dissipation per multivibrator, (P _D), <u>1/</u> :	
Device type 01 - - - - -	110 mWdc
Device type 02 - - - - -	77 mWdc
Lead temperature (soldering, 10 seconds) - -	300°C
Thermal resistance, junction to case (θ _{JC}):	
Cases A, B, D - - - - -	0.09°C/W for flat-package
Case C - - - - -	0.08°C/W for dual-in-line package
Junction temperature (T _J) - - - - -	175°C

1/ Must withstand the added P_D due to short circuit tests (e.g., I_{OS}).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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1.4 Recommended operating conditions.

Supply voltage-	4.5 V minimum to 5.5 V maximum
Minimum high level input voltage-	2.0 V
Maximum low level input voltage -	0.8 V
Normalized fanout (each output) <u>2/</u> :	
Device type 01-	10 maximum
Device type 02:	
Low level logic -	10 maximum
High level logic-	20 maximum
Case operating temperature range-	-55° to 125°C
Input pulse rise/fall time,	
Device type 01:	
Schmitt input (B) -	1 v/s maximum
Logic inputs (A1, A2) -	1 v/μs maximum
Input data setup time, t _{SETUP}	
Device type 01-	100 ns minimum
Device type 02-	50 ns minimum
Input data hold time, t _{HOLD}	
Device type 01-	0
Device type 02-	50 ns minimum
External timing resistance	
Device type 01-	1.4 kΩ minimum to 30 kΩ maximum
Device type 02-	5 kΩ minimum to 25 kΩ maximum

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and 1.2.3 herein.

3.2.1 Logic diagram and terminal connections. The logic diagram and terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

2/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}, I_{OH} = -.2 \text{ mA}$	01	2.4	---	V
		$V_{CC} = 4.5 \text{ V}, I_{OH} = -.4 \text{ mA}$ <u>1/</u>	02	2.4	---	V
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}$ <u>1/</u>	01, 02	---	0.4	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}, I_{IN} = -12 \text{ mA}$ $T_C = 25^\circ\text{C}$	01, 02	---	-1.5	V
Low level input current at A ₁ or A ₂	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	01	-0.35	-0.8	mA
Low level input current at B	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	01	-0.7	-1.6	mA
Low level input current at data inputs	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	02	-0.35	-0.8	mA
Low level input current at clear input	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	02	-0.7	-1.6	mA
High level input current at A ₁ or A ₂	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	01		20	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	01		100	μA
High level input current at B	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	01		40	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	01		200	μA
High level input current at data input	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	02		20	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	02		100	μA
High level input current at clear input	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	02		40	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	02		200	μA
Short circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0 \text{ V}$ <u>1/</u> <u>2/</u>	01	-10	-27	mA
			02	-5	-20	mA
Supply current (Quiescent)	I_{CC1}	$V_{CC} = 5.5 \text{ V},$ <u>3/</u>	01		12	mA
			02		14	mA
Supply current (Triggered)	I_{CC2}	$V_{CC} = 5.5 \text{ V},$ <u>4/</u>	01		20	mA
			02		14	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Positive-going threshold voltage at A input	$V_{T+(A)}$	$V_{CC} = 4.5 \text{ V}$	01		2.0	V
Negative-going threshold voltage at A input	$V_{T-(A)}$	$V_{CC} = 4.5 \text{ V}$	01	0.8		V
Positive-going threshold voltage at B input	$V_{T+(B)}$	$V_{CC} = 4.5 \text{ V}$	01		2.0	V
Negative-going threshold voltage at B input	$V_{T-(B)}$	$V_{CC} = 4.5 \text{ V}$	01	0.8		V
Propagation delay time to high level (B input to Q output)	t_{PLH1}	$V_{CC} = 5 \text{ V}$ $C_L = 50 \text{ pF}$ minimum $C_X = 80 \text{ pF}$ minimum $\pm 10\%$ $R_L = 800 \Omega \pm 5\%$	01	15	132	ns
Propagation delay time to low level (B input to \bar{Q} output)	t_{PHL1}	Figure 4		20	156	ns
Propagation delay time to high level (A_1 or A_2 inputs to Q output)	t_{PLH2}			25	168	ns
Propagation delay time to low level (A_1 or A_2 inputs to \bar{Q} output)	t_{PHL2}			30	192	ns
Propagation delay time to high level (A_1 or A_2 inputs to Q output)	t_{PLH1}	$V_{CC} = 5 \text{ V}$ $C_X = 0$ $C_L = 50 \text{ pF}$ minimum $R_X = 5 \text{ k}\Omega \pm 5\%$ $R_L = 800 \Omega \pm 5\%$	02	7	82	ns
Propagation delay time to high level (B_1 or B_2 inputs to Q output)	t_{PLH2}	Figure 6		7	70	ns
Propagation delay time to low level (A_1 or A_2 inputs to \bar{Q} output)	t_{PHL1}			7	100	ns
Propagation delay time to low level (B_1 or B_2 inputs to \bar{Q} output)	t_{PHL2}			7	90	ns
Propagation delay time to low level (clear input to \bar{Q} output)	t_{PHL3}			7	69	ns
Propagation delay time to high level (clear input to \bar{Q} output)	t_{PLH3}			7	100	ns
Minimum pulse width of Q output pulse	$t_{W(MIN)}$			---	130	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Width of Q output pulse	t_W	$R_L = 800\Omega \pm 5\%$; $V_{CC} = 5\text{ V}$. $C_L = 15\text{ pF}$ minimum $C_X = 400\text{ pF} \pm 10\%$ $R_X = 10\text{ k}\Omega \pm 5\%$ Figure 6	02	1.7	2.1	μs
Pulse width obtained with internal timing resistor	$t_P(\text{OUT})_1$	$R_L = 800\Omega \pm 5\%$; $V_{CC} = 5\text{ V}$. $C_L = 50\text{ pF}$ minimum $R_X = \text{open}$ (Figure 5) $C_X = 80\text{ pF} \pm 10\%$ pin 9 connected to V_{CC}	01	70	260	ns
Pulse width obtained with zero timing capacitance	$t_P(\text{OUT})_2$	$R_L = 800\Omega \pm 5\%$; $V_{CC} = 5\text{ V}$. $C_L = 50\text{ pF}$ minimum $R_X = \text{open}$ $C_X = 0$ pin 9 connected to V_{CC} Figure 5	01	20	70	ns
Pulse width obtained with external timing resistor	$t_P(\text{OUT})_3$	$V_{CC} = 5\text{ V}$ $C_X = 100\text{ pF} \pm 10\%$ $C_L = 50\text{ pF}$ min.	01	600	850	ns
	$t_P(\text{OUT})_4$	$R_X = 10\text{ k}\Omega \pm 5\%$ $C_X = 1\text{ }\mu\text{F} \pm 10\%$ pin 9 open Figure 5	01	6	8	ms
Minimum duration of trigger pulse	t_{SETUP}	$R_L = 800\Omega \pm 5\%$; $V_{CC} = 5\text{ V}$ $C_L = 50\text{ pF}$ minimum $C_X = 80\text{ pF} \pm 10\%$ pin 9 connected to V_{CC} Figure 5	01		100	ns

1/ Ground C_X to measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q. C_X is open to measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at \bar{Q} (type 02).

2/ Not more than one output should be shorted at a time.

3/ For type 02: I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_X = 0.02\text{ }\mu\text{F}$ and $R_X = 25\text{ k}\Omega$. R_{INT} is open.

4/ For type 02: I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_X = 0.02\text{ }\mu\text{F}$ and $R_X = 25\text{ k}\Omega$. R_{INT} is open.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements shall be as specified in table III. The subgroups of table III which constitute the minimum electrical test requirements for screening and quality conformance inspection by device class are specified in table II.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class B devices	Class C devices
Interim electrical test parameters (pre burn-in) (method 5004)	1	None
Final electrical test parameters (method 5004)	1*2,3,9	1
Group A test requirements (method 5005)	1,2,3,9	1,2,3,9
Group C end-point electrical test parameters (method 5005)	1,2,3	1
Group D end-point electrical test parameters (method 5005)	1,2,3	1
Additional electrical test parameters for group C inspection	10,11	10,11

*PDA applies to subgroup 1 (see 4.2c).

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 17 (see MIL-M-38510, appendix E).

3.8 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have manufacturer certification in accordance with MIL-M-38510 for the applicable technology group and shall follow the applicable provisions of the product assurance plan in manufacturing and testing these devices.

3.9 Listing on qualified products list (QPL). Devices supplied to this specification shall be listed on QPL-38510, part I. To obtain part I, QPL-38510 listing, a manufacturer shall submit to the qualifying activity a request for listing on the QPL plus the material required by MIL-M-38510, appendix D, paragraphs 20.2.1 h, i, j, k, l, m, n, and q. Additionally, variables electrical test data for 10 devices for each device type tested in accordance with table III shall be submitted to the qualifying activity. The listing shall be revoked by the qualifying activity when this specification is no longer needed for logistic purposes or for cause.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E, using the circuit shown on figure 7 or equivalent.

(2) $T_A = 125^\circ\text{C}$ minimum.

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- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameter tests prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroup 1 tests after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped. The retention of qualification requirement of MIL-M-38510 shall apply.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical test parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B and C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A inspection.
- c. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 7, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

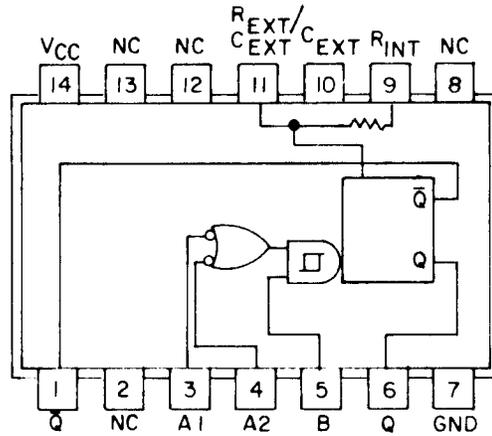
4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical test parameters shall be as specified in table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be as specified in MIL-M-38510.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

Device type 01
Cases A, B, C and D

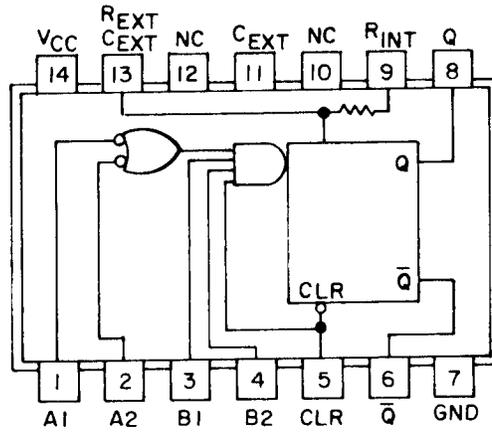


NOTES:

1. To use internal timing resistor ($4\text{ k}\Omega$), connect R_{INT} to VCC .
2. An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
3. For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and VCC , with R_{INT} open-circuited.
4. To obtain variable pulse width connect variable resistance between R_{INT} or R_{EXT}/C_{EXT} and VCC .

FIGURE 1. Logic diagrams and terminal connections.

Device type 02
Cases A, B, C and D



NOTES:

1. To use internal timing resistor ($20\text{ k}\Omega$), connect R_{INT} to V_{CC} .
2. An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} . (positive).

FIGURE 1. Logic diagrams and terminal connections - Continued.

Device type 01

t_n INPUT			t_{n+1} INPUT			OUTPUT
A ₁	A ₂	B	A ₁	A ₂	B	
H	H	L	H	H	H	INHIBIT
L	X	H	L	X	L	INHIBIT
X	L	H	X	L	L	INHIBIT
L	X	L	L	X	H	ONE SHOT
X	L	L	X	L	H	ONE SHOT
H	H	H	X	L	H	ONE SHOT
H	H	H	L	X	H	ONE SHOT
X	L	L	X	H	L	INHIBIT
L	X	L	H	X	L	INHIBIT
X	L	H	H	H	H	INHIBIT
L	X	H	H	H	H	INHIBIT
H	H	L	X	L	L	INHIBIT
H	H	L	L	X	L	INHIBIT

NOTES:

1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a low or high level may be present.
4. A₁ and A₂ are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to low level with B at high level.
5. B is a positive Schmitt-Trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical H with either A₁ or A₂ at low level.

Device type 02

INPUTS				OUTPUTS	
A ₁	B ₂	B ₁	B ₂	Q	\bar{Q}
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⌈	⌋
L	X	H	↑	⌈	⌋
X	L	H	H	L	H
X	L	↑	H	⌈	⌋
X	L	H	↑	⌈	⌋
H	↓	H	H	⌈	⌋
↓	↓	H	H	⌈	⌋
↓	H	H	H	⌈	⌋

NOTES:

H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⌈ = one high-level pulse, ⌋ = one low-level pulse, X = irrelevant (any input, including transitions).

FIGURE 2. Truth tables.

Description of device type 01

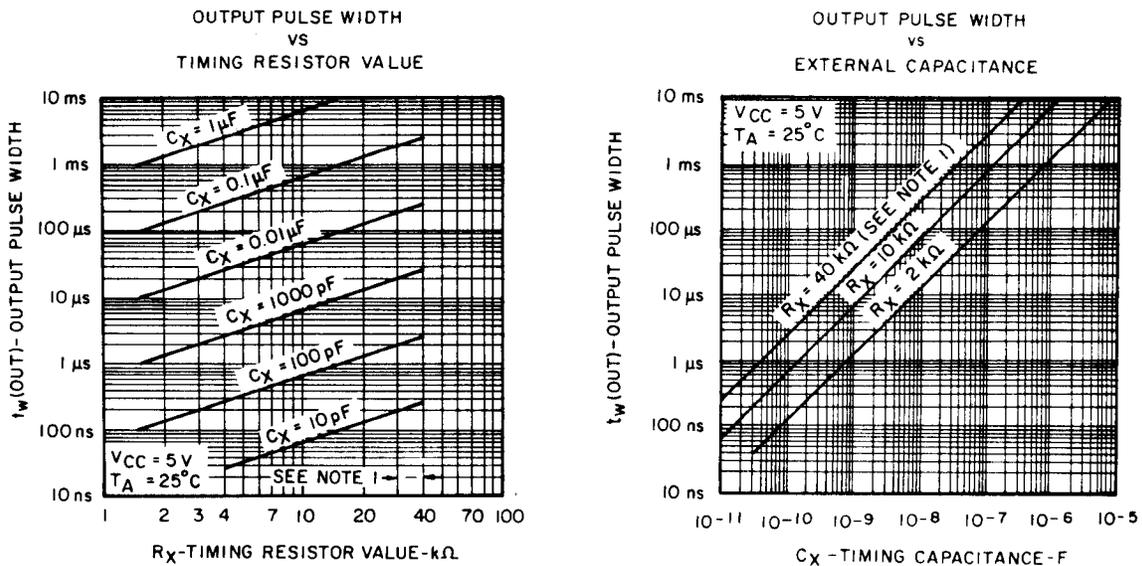
These multivibrators feature dual negative-transition-triggered inputs and a single positive transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i. e., R_{INT} connected to V_{CC} , C_{EXT} and R_{EXT}/C_{EXT} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_T R_T \ln 2 \approx 0.7 C_T R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1,000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

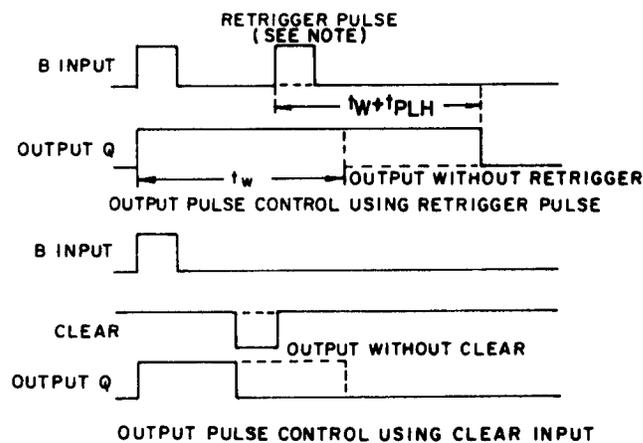


NOTE: These values of resistance exceed the maximum recommended for use over the full temperature range.

FIGURE 3. Device descriptions.

Description of device type 02

These multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. The figure below illustrates triggering the one-shot with the high-level-active (B) inputs.



NOTE: Retrigger pulse must not start before 0.22 C_{EXT} (in picofarads) nanoseconds after previous trigger pulse.

TYPICAL INPUT/OUTPUT PULSES

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. It has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with device type 01.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{EXT} > 1,000$ pF, the output pulse width (t_w) is defined as:

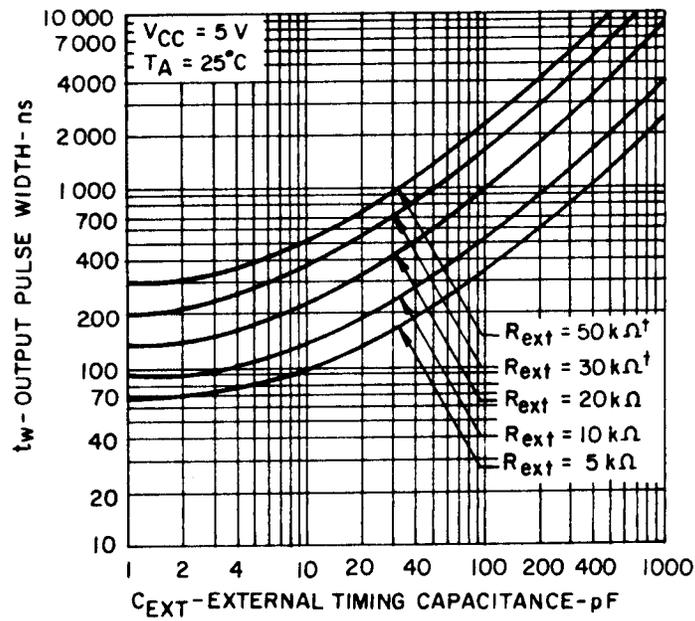
$$t_w = 0.37 R_X C_X \left(1 + \frac{0.7}{R_X} \right)$$

where R_X is in $k\Omega$ (either internal or external timing resistor),
 C_X is in pF,
 t_w is in ns.

FIGURE 3. Device descriptions - Continued.

Description of device type 02 - continued

OUTPUT PULSE WIDTH
VS
EXTERNAL TIMING CAPACITANCE

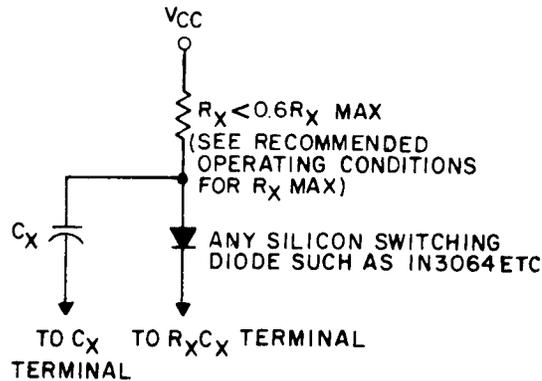


[†]These values of resistance exceed the maximums recommended for use over the full temperature range.

FIGURE 3. Device descriptions - Continued

Description of device type 02 - continued

To prevent reverse voltage across C_X it is recommended that the following circuit be employed when using electrolytic capacitors and also in applications utilizing the clear functions and $C_X > 1,000$ pF.



In all applications using the diode, the pulse width is:

$$t_w = 0.33 R_X C_X \left(1 + \frac{0.7}{R_X} \right)$$

where R_X is in $k\Omega$
 C_X is in pF
 t_w is in ns

For pulse widths when $C_X \leq 1,000$ pF, the following circuit for timing component connections is recommended.

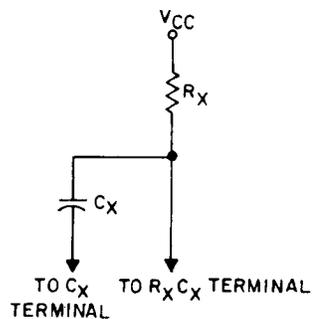
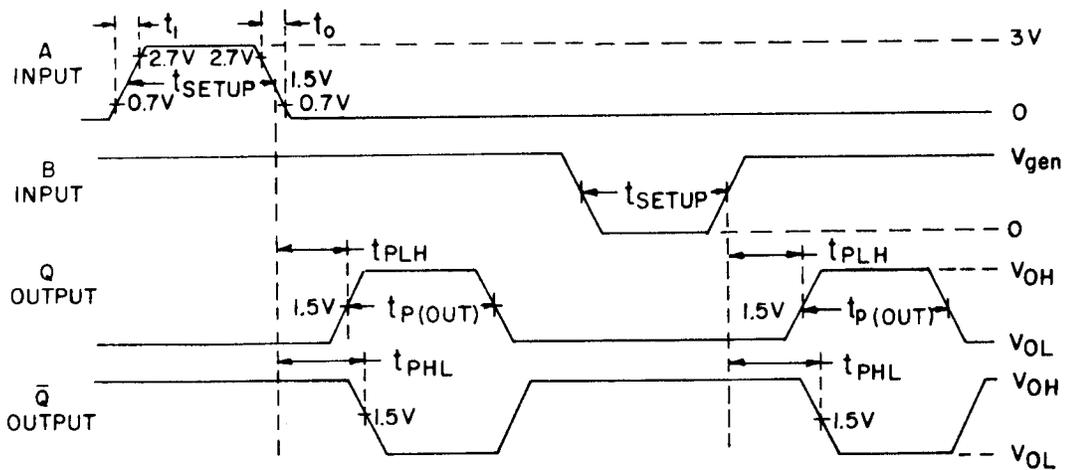
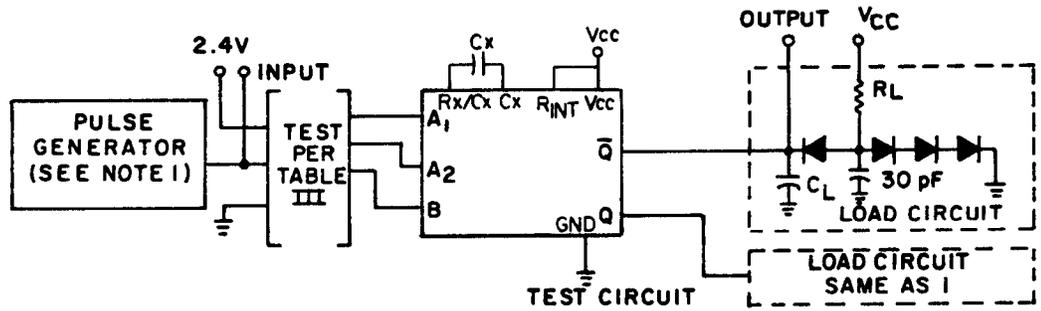


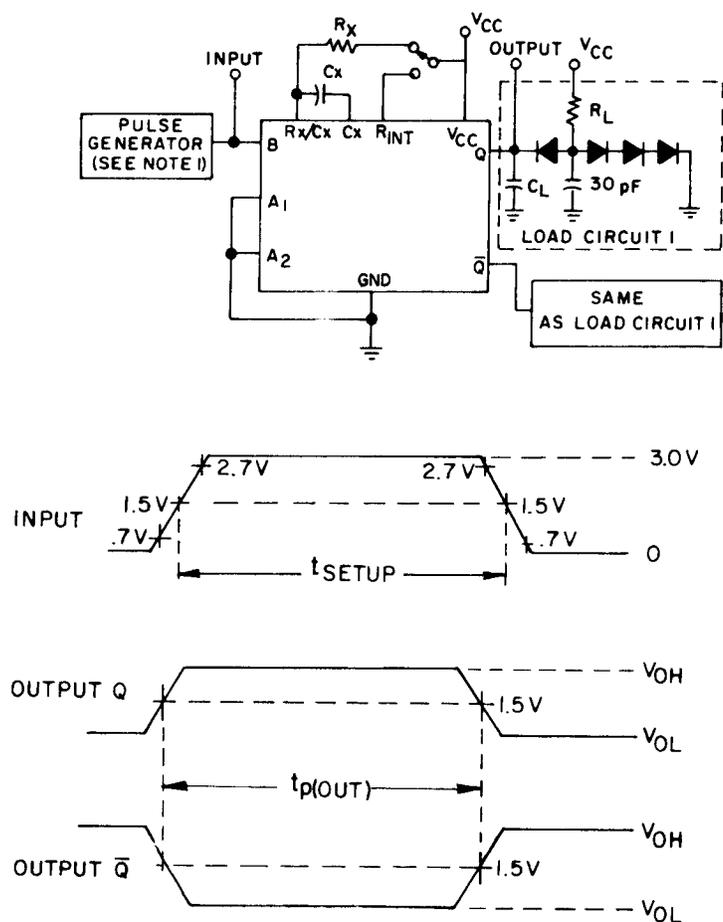
FIGURE 3. Device descriptions - Continued.



NOTES:

1. The pulse generator has the following characteristics: $V_{gen} = 3.0 \text{ V}$, $t_0 \leq 10 \text{ ns}$, $t_1 \leq 10 \text{ ns}$, $t_p(\text{in}) \geq 100 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, and $Z_{out} \approx 50 \Omega$.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50 \text{ pF}$ minimum including probe and jig capacitance.
4. $R_L = 800 \Omega \pm 5\%$.
5. $V_{CC} = 5.0 \text{ V}$ minimum.
6. See table III for R_X and C_X values.

FIGURE 4. Switching test circuit for t_{PHL} and t_{PLH} of device type 01.



NOTES:

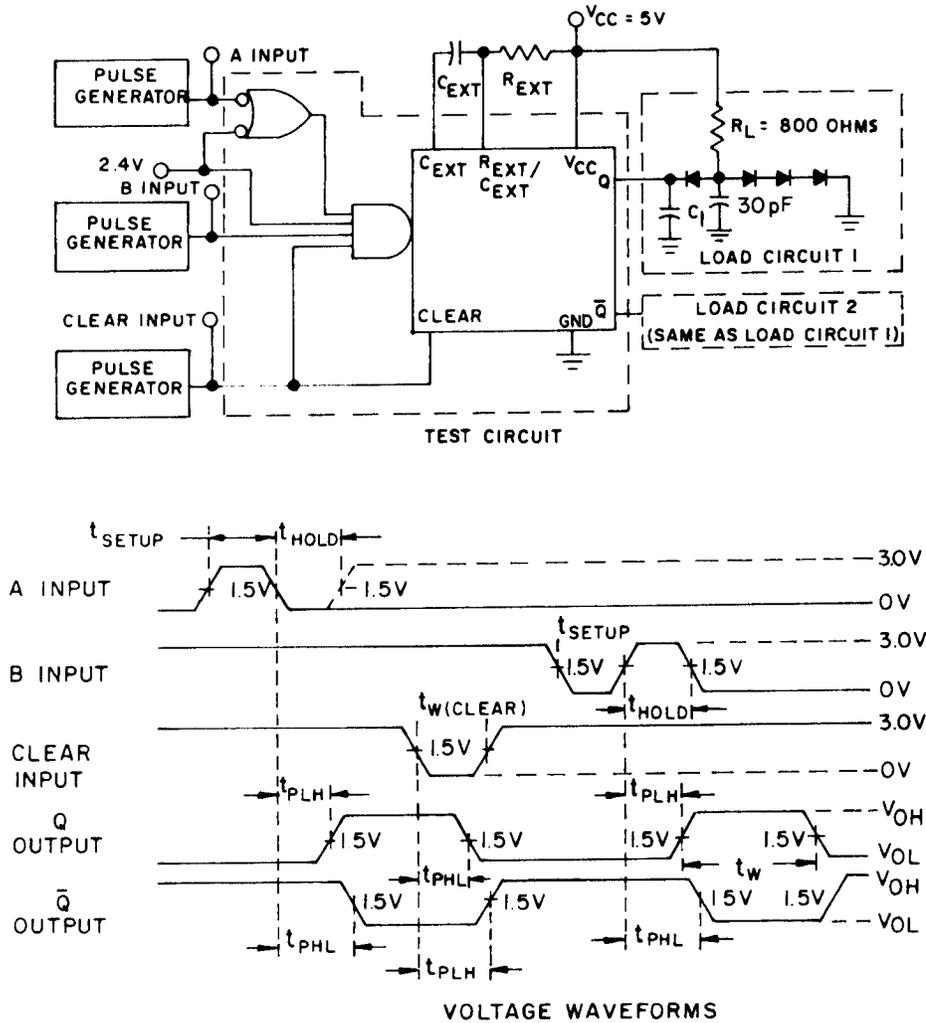
1. The pulse generator has the following characteristics: $V_{gen} = 3.0 V$, $t_0 \leq 10 ns$, $t_1 \leq 10 ns$, $t_{setup} = 100 ns$, $Z_{out} \approx 50 \Omega$ and PRR is as follows:

TEST	PRR
$t_{p(out)1}$ and $t_{p(out)2}$	1 MHz
$t_{p(out)3}$	500 kHz
$t_{p(out)4}$	50 Hz

2. $V_{CC} = 5.0 V$ minimum; $R_L = 800 \Omega \pm 5\%$, $C_L = 50 pF$ minimum including jig and probe capacitance.
3. See table III for R_X and C_X values.
4. All diodes are 1N3064, or equivalent.

FIGURE 5. Test circuit for t_{setup} and $t_{p(out)}$ of device type 01.

Device type 02



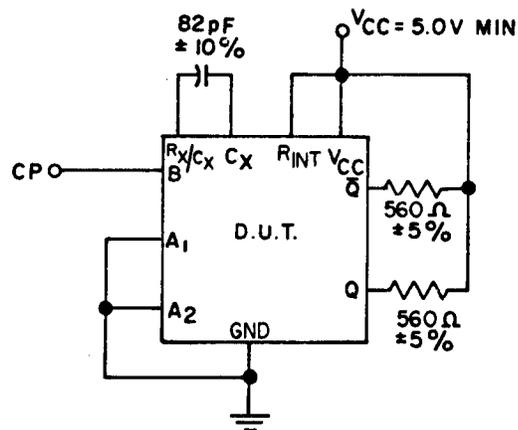
NOTES:

1. The pulse generators have the following characteristics: $t_r \leq 10$ ns (10 percent to 90 percent level), $t_f \leq 10$ ns, $PRR \leq 1$ MHz, duty cycle ≤ 50 percent. $Z_{out} \approx 50$ ohms.
2. See test conditions, switching characteristics table II, for values of R_{EXT} and C_{EXT} .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50$ pF minimum including scope probe, wiring, and stray capacitance, without package in test fixture.

FIGURE 6. Switching time tests for device type 02.

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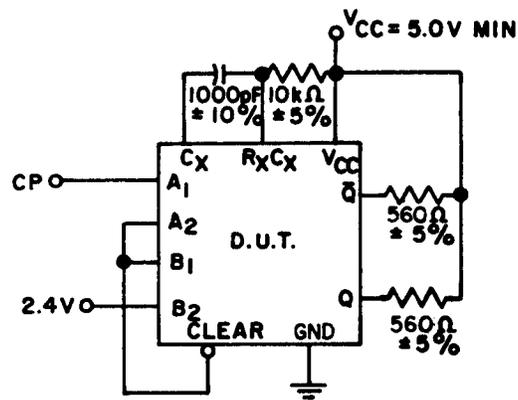
Device type 01



NOTE: The clock pulse (CP) has the following characteristics:
 $V_{gen} = 3.0 \text{ V minimum}$, $PRR \leq 1 \text{ MHz}$, duty cycle = 50%.

FIGURE 7. Burn-in and steady state life test circuits.

Device type 02



NOTES:

1. The clock pulse (CP) has the following characteristics:
 $V_{gen} = 3.0 \text{ V minimum}$, $PRR \leq 1 \text{ MHz}$, duty cycle = 50%.
2. Both halves connected as shown.

FIGURE 7. Burn-in and steady state life test circuits - Continued.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D														Test limits				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit	
9 T _C = 25 °C	t _{PLH1}	3003 (Fig 4)	Q	NC	A1	A2	B	Q	GND	NC	R _{INT}	C _X	R _X C _X	NC	NC	V _{CC}	B to Q	15	110	ns	
	t _{PHL1}		OUT		IN	IN	IN	OUT									B to Q	20	130		
	t _{PLH2}		OUT		IN	5.0 V	5.0 V	OUT									A2 to Q	25	140		
	t _{PHL2}		OUT		IN	5.0 V	5.0 V	OUT									A2 to Q	30	160		
	t _{P(OUT)1}	(Fig 5)			GND	GND	IN	OUT	OUT									Q	70	260	
	t _{P(OUT)2}																	Q	20	70	
10 T _C = 125 °C	t _{PLH1}	3003 (Fig 4)	OUT		GND	IN	IN	OUT									B to Q	15	132	ns	
	t _{PHL1}		OUT		GND	IN	IN	OUT									B to Q	20	156		
	t _{PLH2}		OUT		5.0 V	5.0 V	5.0 V	OUT									A2 to Q	25	168		
	t _{PHL2}		OUT		5.0 V	5.0 V	5.0 V	OUT									A2 to Q	30	192		
	t _{P(OUT)1}	(Fig 5)			GND	GND	IN	OUT	OUT									Q	70	260	
	t _{P(OUT)2}																	Q	20	70	
11	t _{P(OUT)3}																Q	600	850	ms	
	t _{P(OUT)4}																Q	6	8	ms	
	t _{SETUP}																Q	---	100	ns	
																		B to Q	15	132	ns

Same tests, terminal conditions and limits as subgroup 10, except T_C = -55 °C.

NOTES:

- (1) C_X connected to R_X C_X through a 0.1 μF capacitor.
- (2) R_X C_X connected to V_{CC} through a 10 kΩ resistor.
- (3) R_{INT} connected to V_{CC}.
- (4) C_X connected to R_X C_X through an 80 pF capacitor.
- (5) C_X connected to R_X C_X through a 100 pF capacitor.
- (6) C_X connected to R_X C_X through a 1 μF capacitor.
- (7) R_X C_X and C_X are open.
- (8) In transition from high level to low level.
- (9) In transition from low level to high level.
- (10) Input may be high level, low level or open.
- (11) Output voltages for subgroups 7 and 8 shall be either:
 - a. H = 2.4 volts minimum and L = 0.4 volts maximum when using a high speed checker double comparator, or
 - b. H > 1.5 volts and L < 1.5 volts when using a high speed checker single comparator.
- (12) One high level logic pulse.
- (13) One low level logic pulse.
- (14) 5.0 V, then 0.8 V.
- (15) GND, then 2.0 V.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D				Case C				Case A, B, D				Case C				Test limits						
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	13	14	Meas. terminal	Min	Max	Unit			
1 T _C = 25°C	VOL	3007	A1	A2	B1	B2	Clear	Q	R _{INT}	NC	C _X	NC	R _X	C _X	V _{CC}	14	14	Q	0.4	0.4	V				
	VOL	3007	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V	8 mA	4.5 V										Q						
	VOH	3006	0.8 V	2.0 V	2.0 V	0.8 V	2.0 V	-4 mA	GND										Q	2.4	2.4				
	VOH	3006	0.8 V	2.0 V	2.0 V	0.8 V	2.0 V	-4 mA	GND										Q	2.4	2.4				
	V _{IC}		-12 mA	-12 mA															A1	-1.5					
				-12 mA	-12 mA														A2						
																			B1						
																			B2						
																			Clear						
		I _{IL1}	3009	0.4 V	5.5 V	0.4 V	5.5 V	5.5 V	-12 mA										A1	-0.35	-0.8	mA			
				5.5 V	0.4 V	5.5 V	5.5 V	5.5 V											A2						
																			B1						
																			B2						
																			Clear						
		I _{IH1}	3010	2.4 V	GND	2.4 V	GND	5.5 V	5.5 V										A1	0	20	μA			
				GND	2.4 V	GND	2.4 V	GND											A2						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B1						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B2						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											A1						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											A2						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B1						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B2						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear						
				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear						
		I _{IH3}		GND	5.5 V	5.5 V	GND	5.5 V											A1						
		I _{IH4}		GND	5.5 V	5.5 V	GND	5.5 V											A2						
		I _{OS}	3011	GND	5.5 V	5.5 V	GND	5.5 V											B1						
			GND	5.5 V	5.5 V	GND	5.5 V											B2							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear							
	I _{OS}	3011	GND	5.5 V	5.5 V	GND	5.5 V											A1							
			GND	5.5 V	5.5 V	GND	5.5 V											A2							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B1							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											B2							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											Clear							
	I _{CC1}	3005	5.5 V	GND	5.5 V	GND	5.5 V											Q	-5	-20	mA				
	I _{CC2}	3005	GND	5.5 V	5.5 V	5.5 V	5.5 V											Q	-5	-20	mA				
			GND	5.5 V	5.5 V	5.5 V	5.5 V											V _{CC}							
			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											V _{CC}							
2	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																								
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																								
7 T _C = 25°C	Truth table test		29	5.0 V	5.0 V	5.0 V	5.0 V	L	L										(2) (3)						
			30	GND	GND	5.0 V	5.0 V	H	H											(2) (4)	5.0 V				
			31	GND	GND	5.0 V	5.0 V																		
			32	GND	GND	5.0 V	5.0 V																		
			33	GND	GND	5.0 V	5.0 V																		
			34	GND	GND	5.0 V	5.0 V																		
			35	GND	GND	5.0 V	5.0 V																		
			36	GND	GND	5.0 V	5.0 V																		
			37	GND	GND	5.0 V	5.0 V																		
			38	5.0 V	5.0 V	5.0 V	5.0 V																		
			39	5.0 V	5.0 V	5.0 V	5.0 V																		
			40	5.0 V	5.0 V	5.0 V	5.0 V																		
			41	5.0 V	5.0 V	5.0 V	5.0 V																		
			42	5.0 V	5.0 V	5.0 V	5.0 V																		
43	5.0 V	5.0 V	5.0 V	5.0 V																					
8	Repeat subgroup 7 at T _C = 125°C and T _C = -55°C.																								

See notes at end of device type 02

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be as specified in MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for packaging and packing.
- f. Requirements for failure analysis (including required test condition of method 5003), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirement for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - -	Electrical ground (common terminal)
V _{IN} - - - - -	Voltage level at an input terminal
V _{IC} - - - - -	Input clamp voltage
I _{IN} - - - - -	Current flowing into an input terminal
T _C - - - - -	Case temperature

6.5 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54L121
02	54L122

6.7 Ordering guidance. Since the qualification requirements have been removed from the specification, orders may be placed immediately. However for the convenience of contractors and logistic support, eligible device manufacturers will be listed on the qualified products list.

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17
NASA - NA

Preparing activity:
Air Force - 17

(Project 5962-0418)

Review activities:

Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Agent:

DLA - ES