

MILITARY SPECIFICATION

MICROCIRCUITS DIGITAL, INTEGRATED INJECTION LOGIC (I<sup>2</sup>L),  
PARALLEL 16-BIT MICROPROCESSOR, MONOLITHIC SILICON

This specification is approved for use by all Departments  
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic silicon, integrated injection logic (I<sup>2</sup>L), parallel 16-bit microprocessor. One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, with the exception that the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Clock frequency</u>	<u>Circuit</u>
01	Static to 4.4 MHz	16-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level B as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
Y	See figure 1 (64-lead, 0.9" x 3.2"), dual-in-line package
Z	C-7 (68-terminal, .950" x .950"), square chip carrier package

1.3 Absolute maximum ratings.

Supply current, (I <sub>INJ</sub> )	750 mA
Input voltage:	
V <sub>IN</sub> (all except INJ input)	+5.5 V dc
V <sub>INJ</sub>	+2.0 V dc
Power dissipation	750 mW
Junction temperature (T <sub>J</sub> )	+175°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> )	13°C/W
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C

I Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.
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1.4 Recommended operating conditions (unless otherwise noted,  $I_{INJ} = 400$  mA).

Supply current:	
$I_{INJ}$ - - - - -	380 mA minimum to 420 mA maximum
$V_{INJ}$ - - - - -	1.25 V dc
High-level input voltage ( $V_{IH}$ )- - - - -	2.0 V dc minimum
Low-level input voltage ( $V_{IL}$ ) - - - - -	0.7 V dc maximum
Frequency of operation- - - - -	0 to 4.4 MHz maximum
High-level output voltage ( $V_{OH}$ ) - - - - -	5.5 V dc maximum
Low-level output voltage ( $V_{OL}$ )- - - - -	16 mA maximum
Width of clock pulse ( $t_w$ ) - - - - -	114 ns minimum
Case of operating temperature range ( $T_C$ )- -	-55°C to +125°C
Clock rise time ( $t_r$ )- - - - -	20 ns maximum
Clock fall time ( $t_f$ )- - - - -	20 ns maximum

## 2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, forms a part of this specification to the extent specified herein.

## SPECIFICATION

## MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

## STANDARD

## MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall superseded applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and pin assignments. The terminal connections (pin assignments) shall be as specified on figure 3.

3.2.2 Block diagram. The block diagram (architecture) shall be as specified on figure 4; the microprocessor flow chart is shown on figure 5.

3.2.3 Memory map. The memory map shall be as specified on figure 6.

3.2.4 General features, functional description, and instruction set. The general features, functional description, and instruction set (with terms and symbols) shall be as specified.

3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance requirements. The electrical performance characteristics are as specified in table I and figure 7 and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II. (Table III (case outline Z) for chip carrier.)

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C	Limits		Unit
			Min	Max	
Input clamp voltage	V <sub>IK</sub>	I <sub>IH</sub> = -12 mA		-1.5	V
High-level output current	I <sub>OH</sub>	I <sub>INJ</sub> = NOM, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V, V <sub>OH</sub> = 5.5 V		1000 250	μA
Low-level output voltage	V <sub>OL</sub>	I <sub>INJ</sub> = NOM, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V, I <sub>OL</sub> = 16 mA		0.4	V
Input current	I <sub>IH1</sub>	V <sub>IN</sub> = 2.4 V		600 300	μA
	I <sub>IH2</sub>	V <sub>IN</sub> = 5.5 V		2000 750	
Output breakdown voltage	V <sub>OB</sub>	I <sub>INJ</sub> = NOM, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V, I <sub>OL</sub> = 1 mA		5.5	V
Clock frequency	f <sub>clock</sub>			4.4	MHz

Parameter	From	To	Test conditions	Min	Max	Unit
t <sub>pd1</sub>	CLK ↑	Address bus (A0-A14)	C <sub>L</sub> = 100 pF I <sub>INJ</sub> = 400 mA R <sub>L</sub> = 300Ω See figure 2		140	ns
t <sub>pd2</sub>	CLK ↑	Memory map enable (MPEN)			140	
t <sub>pd3</sub>	CLK ↑	Data bus (D0-D15)			180	
t <sub>pd4</sub>	CLK ↑	Write enable (WE)			175	
t <sub>pd5</sub>	CLK ↑	Cycle end (CYCEND)			155	
t <sub>pd6</sub>	CLK ↑	Data bus in (DBIN)			140	
t <sub>pd7</sub>	CLK ↑	Memory enable (MEMEN)			195	
t <sub>plh8</sub>	CLK ↑	+CRU clock (CRUCLK)			185	
t <sub>ph9</sub>	CLK ↓	+CRU clock (CRUCLK)			175	
t <sub>pd10</sub>	CLK ↑	CRU data out (CRUOUT)			150	
t <sub>pd11</sub>	CLK ↑	Hold acknowledge (HOLDA)			140	
t <sub>pd12</sub>	CLK ↑	Wait			140	
t <sub>pd13</sub>	CLK ↑	Instruction acquisition (IAQ)			145	
t <sub>pd14</sub>	CLK ↑	Multiprocessor interlock (MPILCK)			150	
t <sub>pd15</sub>	CLK ↑	Interrupt acknowledge (INTACK)				
t <sub>pd1</sub>	CLK ↑	Address bus (A0-A14)	When leaving a hold state, C <sub>L</sub> = 100 pF		200	ns
t <sub>pd2</sub>	CLK ↑	Memory map enable (MPEN)		200		
t <sub>pd3</sub>	CLK ↑	Data bus (D0-D15)		200		
t <sub>pd7</sub>	CLK ↑	Memory enable (MEMEN)		200		
t <sub>pd6</sub>	CLK ↑	Data bus in (DBIN)		200		
t <sub>pd13</sub>	CLK ↑	Instruction acquisition (IAQ)		200		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	From	To	Test conditions	Min	Max	Unit
Setup time, $t_{su}$	$t_{su1}$	HOLD		0		ns
	$t_{su2}$	READY		25		
	$t_{su3}$	DO-D15		45		
	$t_{su4}$	CRUI		70		
	$t_{su5}$	INTREQ		55		
	$t_{su6}$	ICO - IC3		55		
	$t_{su7}$	XIPP		50		
	$t_{su8}$	LOAD		20		
	$t_{su9}$	RESET		0		
Hold time, $t_{sh}$	$t_{sh1}$	HOLD		25		ns
	$t_{sh2}$	READY		30		
	$t_{sh3}$	DO-D15		35		
	$t_{sh4}$	CRUI		25		
	$t_{sh5}$	INTREQ		30		
	$t_{sh6}$	ICO - IC3		30		
	$t_{sh7}$	XIPP		5		
	$t_{sh8}$	LOAD		25		
	$t_{sh9}$	RESET		45		

1/ For test conditions shown as NOM, see the appropriate value under Recommended Operating Conditions.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see (see table III)
	Class B devices
Interim electrical parameters (method 5004)	1,7,9
Final electrical test parameters (method 5004) 1/	1,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,7,9

1/ PDA applies to subgroup 1, 7, and 9 (see 4.3f).

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. The "JAN" or "J" certification mark shall not be used.

3.7 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line (not necessarily the line producing the device type described herein).

3.8 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 108.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection is not required.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and as modified herein, shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The alternate screening option of MIL-STD-883, method 5004, is applicable.
- b. Constant acceleration shall be 5,000 G maximum.
- c. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition D, using the circuits shown on figures 8 and 9,
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- d. Reverse bias burn-in and interim electrical test in accordance with method 5004 of MIL-STD-883 may be omitted.
- e. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- f. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, and 4.4.3).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table II of method 5005 of MIL-STD-883 shall be omitted.
- c. Variables data shall be taken for subgroups 9, 10, and 11 only during initial qualification and after process or design changes.
- d. LTPD'S for subgroups shall be combined as follows:

<u>Subgroups</u>	<u>Combined LTPD</u>
1, 7, 9	7
2, 8, 10	10
3, 8, 11	10

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Groups C and D inspections. Groups C and D inspections shall be in accordance with tables III and IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Constant acceleration, shall be condition A (5,000 G).

## c. Operating life test (method 1005 of MIL-STD-883) conditions:

- (1) Test condition D, using the circuit shown on figures 8 and 9.
- (2)  $T_A = +125^\circ\text{C}$ , minimum.
- (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Functional and switching tests. Functional and switching tests (see 6.4) shall be performed using the pattern sets of table IV. The pattern definition and matrix key shall be as shown on figures 10 and 11. The timing for the pins under test (i.e., ABUS, DBUS, WE, etc.) is given on figure 7. Worst case set-up and hold times are specified in 1.4, and worst case propagation delays are listed in table I. The following conditions shall apply:

	<u>Functional test</u>		<u>AC test</u>	<u>f<sub>MAX</sub> test</u>
Injector current	380 mA	420 mA	400 mA	400 mA
Input level	$V_{IH}$	2.0 V	2.0 V	3.0 V
	$V_{IL}$	0.7 V	0.7 V	0.0 V
Output levels	$V_{OH}$	2.0 V	2.0 V	---
	$V_{OL}$	0.7 V	0.7 V	---
	Trip level	---	---	1.5 V
Frequency	0.5 MHz	0.5 MHz	0.5 MHz	4.4 MHz

## 5. PACKAGING

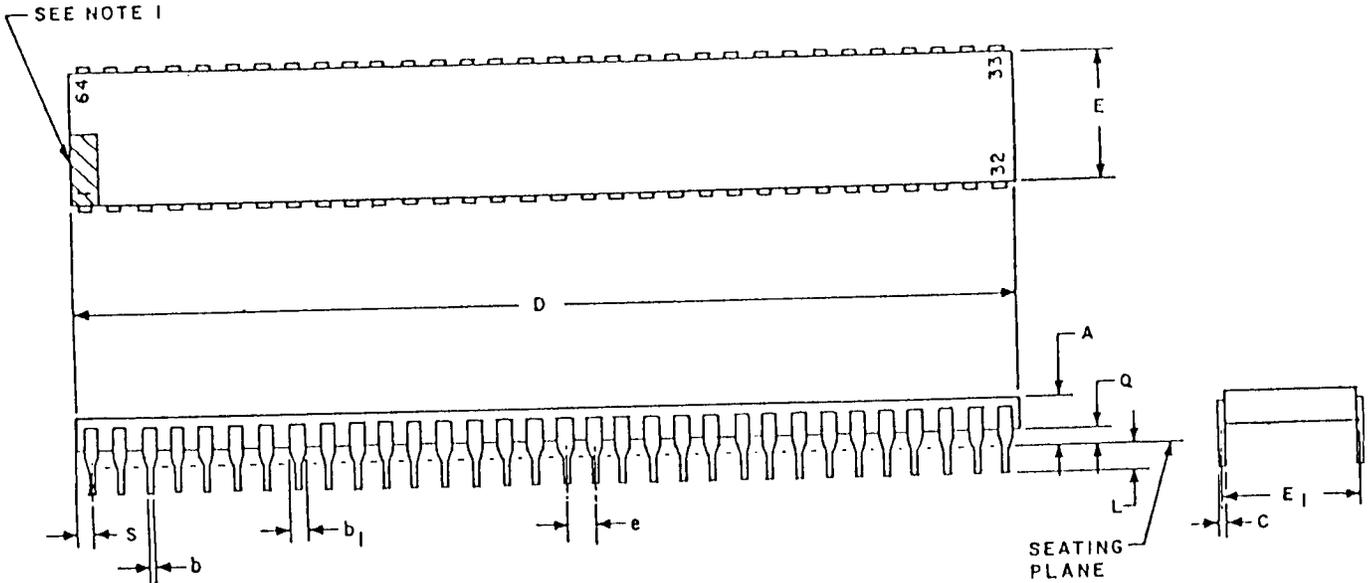
5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.



DIM	Inches		mm		NOTES
	Min	Max	Min	Max	
A		.225		5.72	
b	0.015	0.020	0.38	0.51	8
b <sub>1</sub>		0.070		1.77	2,8
c	.008	.013	0.20	0.33	8
D	3.168	3.232	80.47	82.10	4
E	.880	.900	22.35	22.86	4
E <sub>1</sub>	.890	.910	22.61	23.11	7
e	0.100	BSC	2.54	BSC	5,9
L	0.100	0.165	2.54	4.19	
Q	0.020	0.060	0.51	1.52	3
S	.020	.065	0.51	1.65	6
α	0°	15°			

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b<sub>1</sub> may be .020 (0.51 mm) for leads number 1, 32, 33 and 64 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to pin 1 and 64.
6. Applies to all four corners (leads number 1, 32, 33 and 64).
7. E<sub>1</sub> shall be measured at the centerline of the leads.
8. All leads - increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Sixty two spaces.

FIGURE 1. Case outline Y (64-lead, 0.8 "X 3.2").

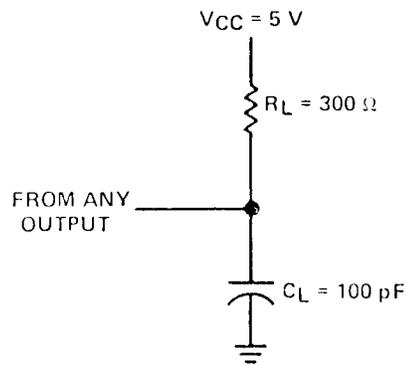
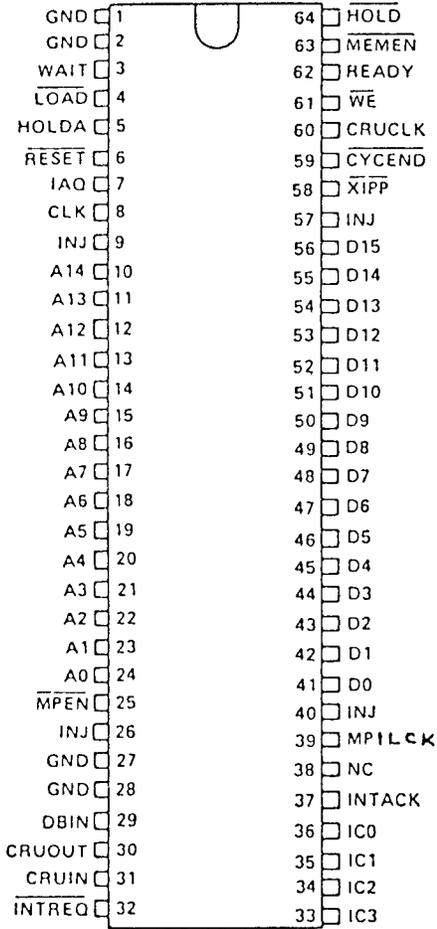


FIGURE 2. Switching time load circuit.

Case Y  
64-Pin ceramic dual-in-line package  
(Top view)



Case Z  
68-Terminal ceramic chip carrier  
(Top view)

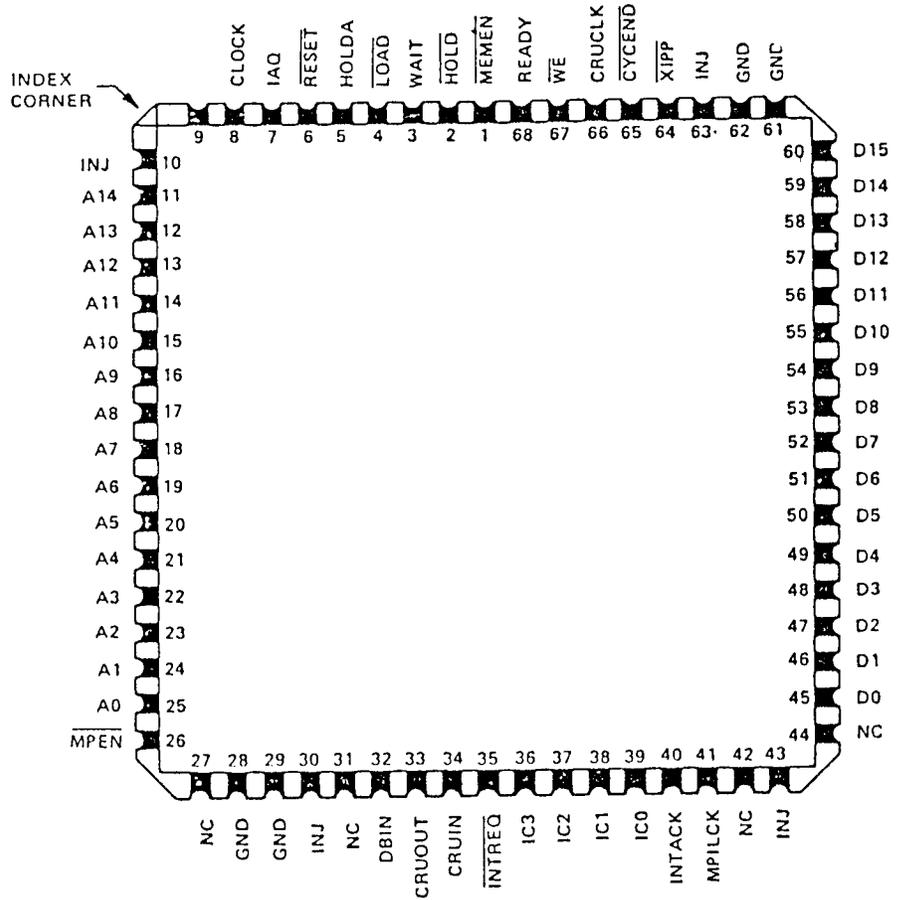


FIGURE 3. Terminal connections (pin assignments).

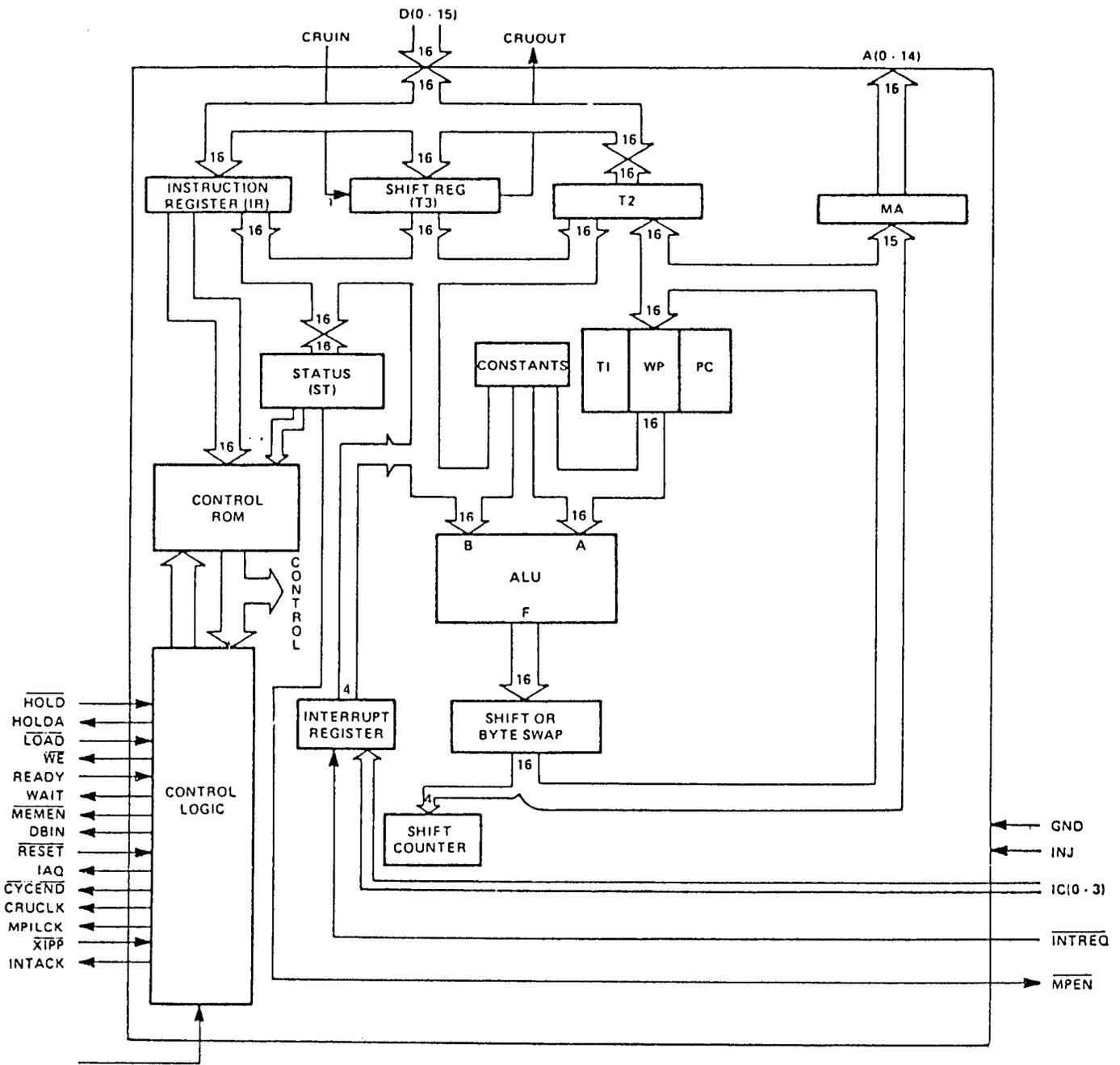


FIGURE 4. Block diagram (architecture).

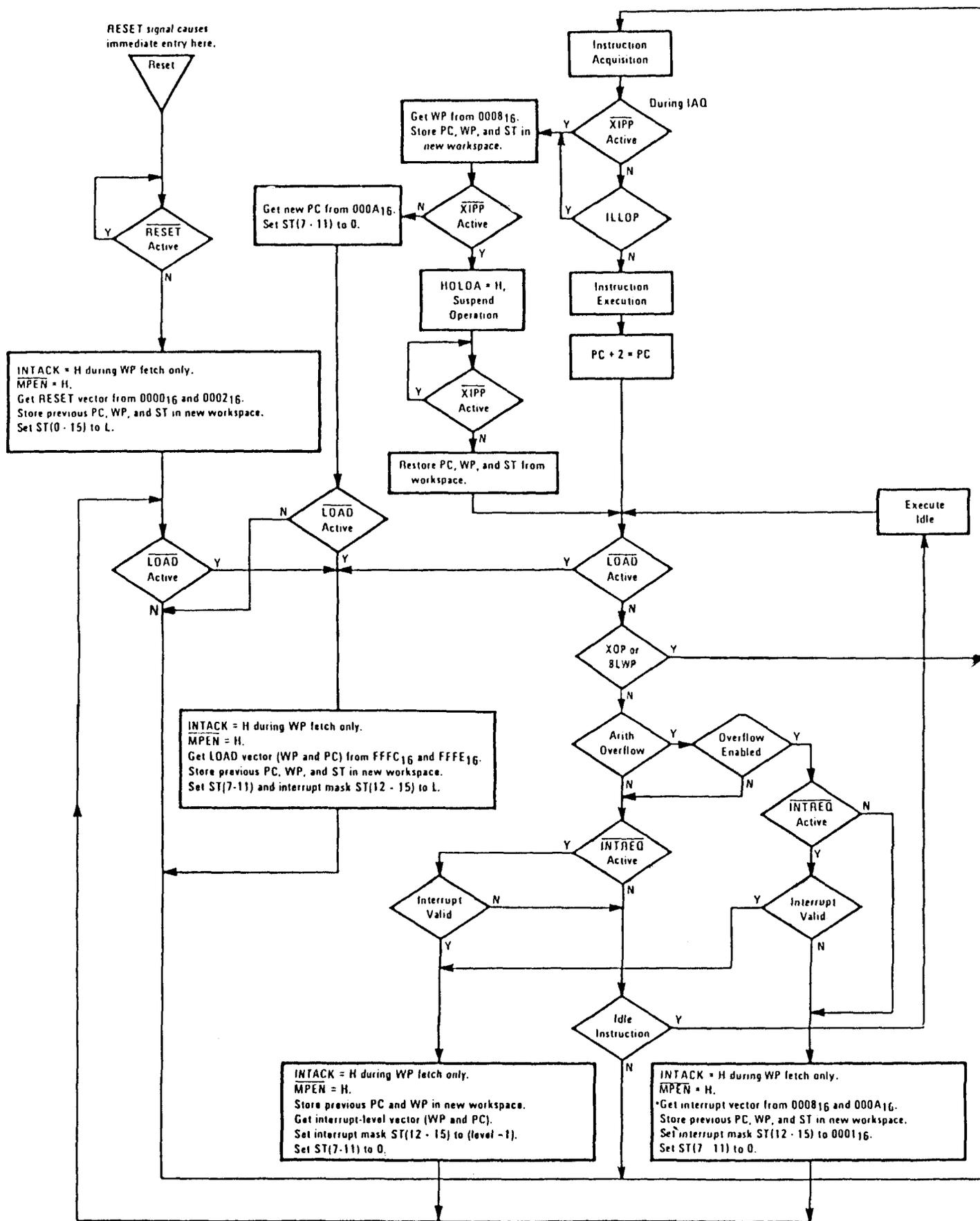


FIGURE 5. Flow chart.

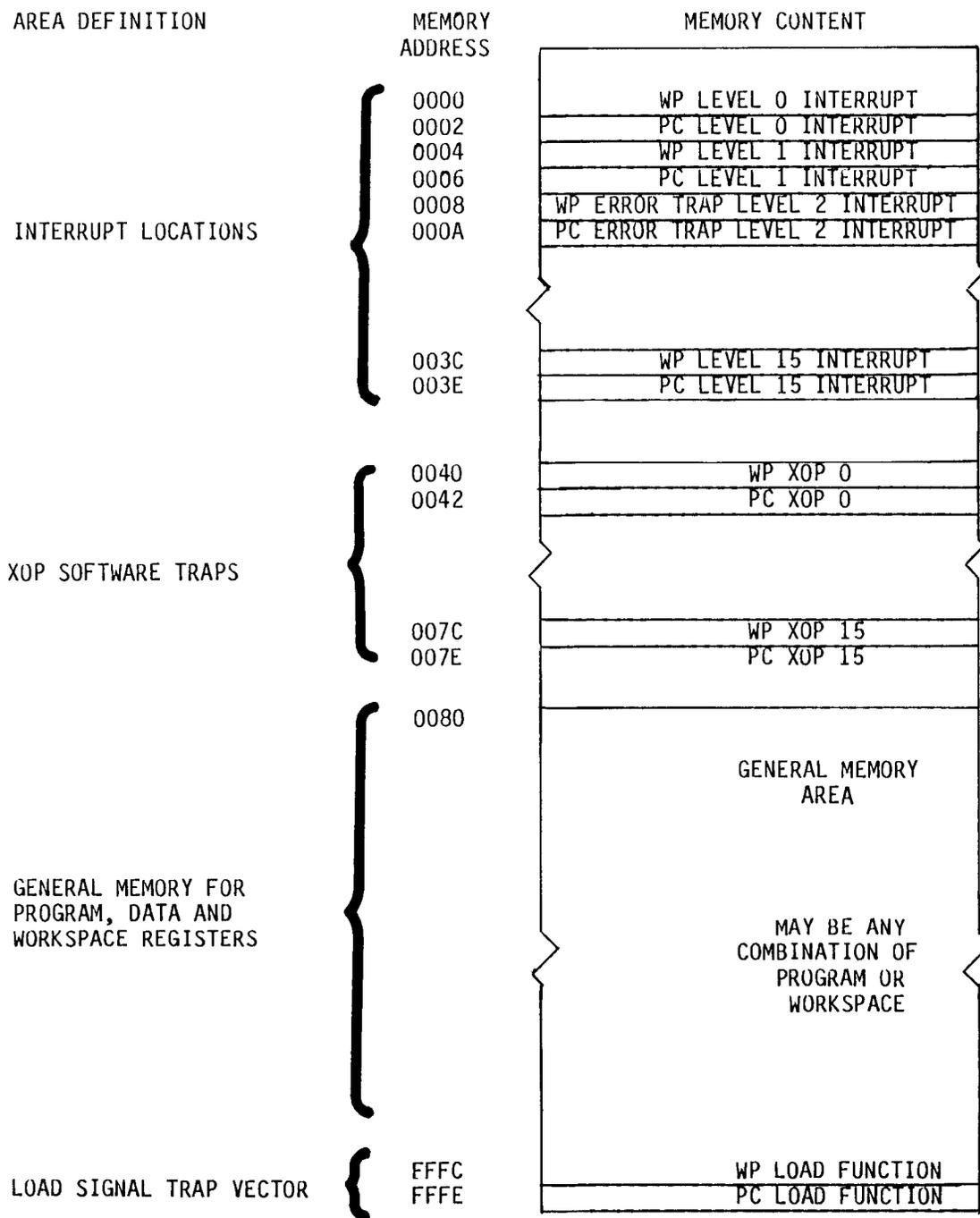


FIGURE 6. Memory map.

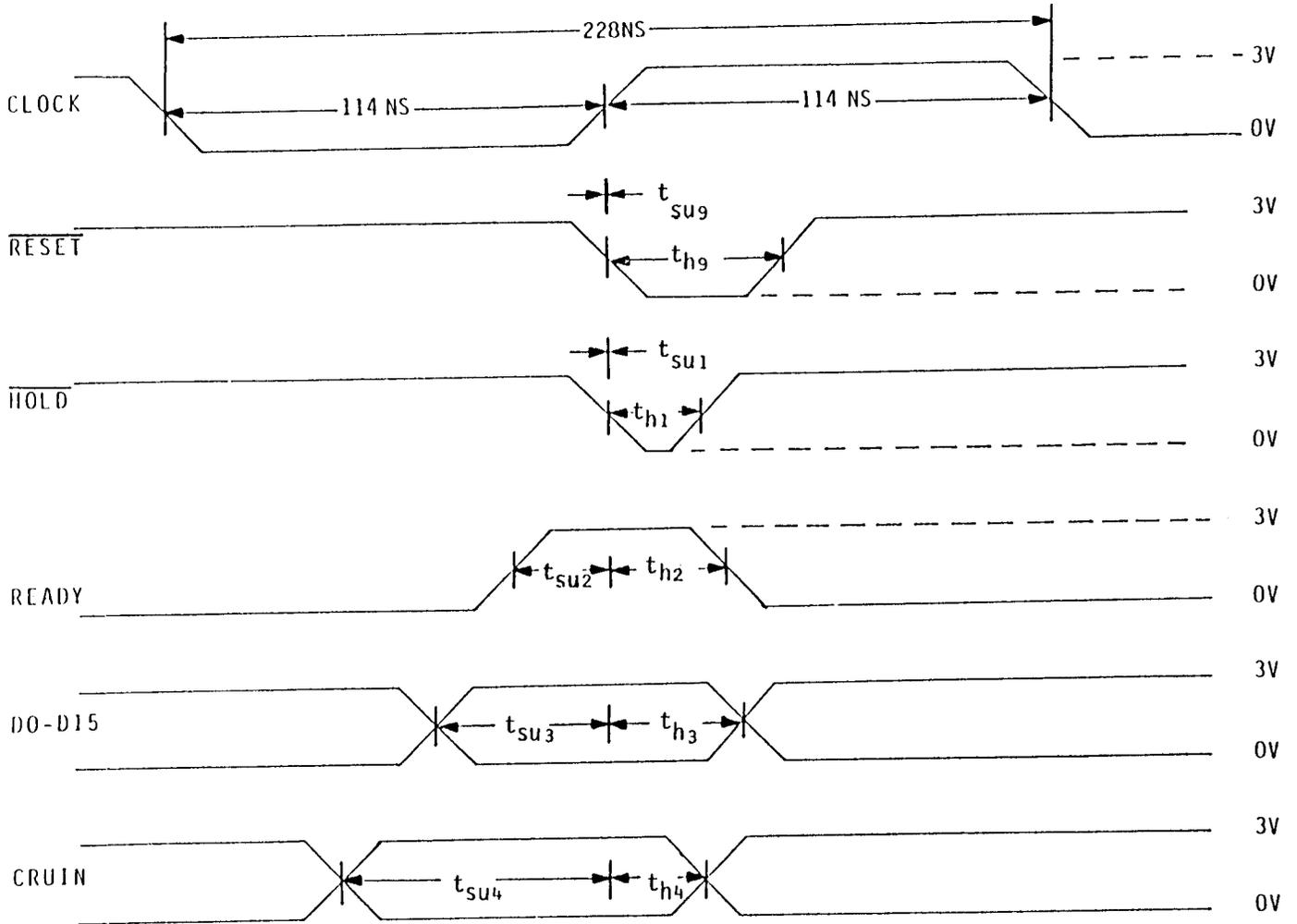


FIGURE 7. AC parametric waveforms.

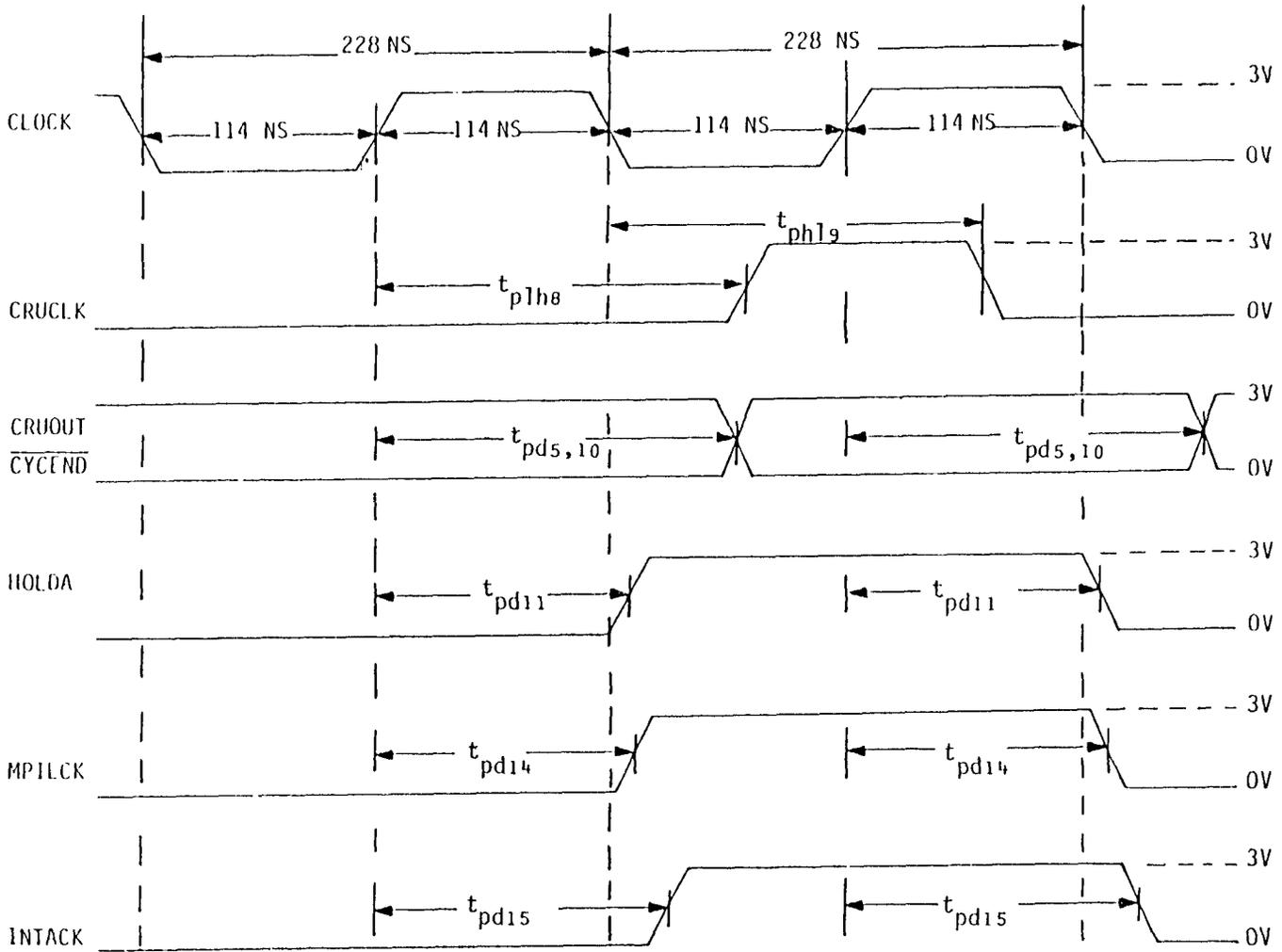


FIGURE 7. AC parametric waveforms - Continued.

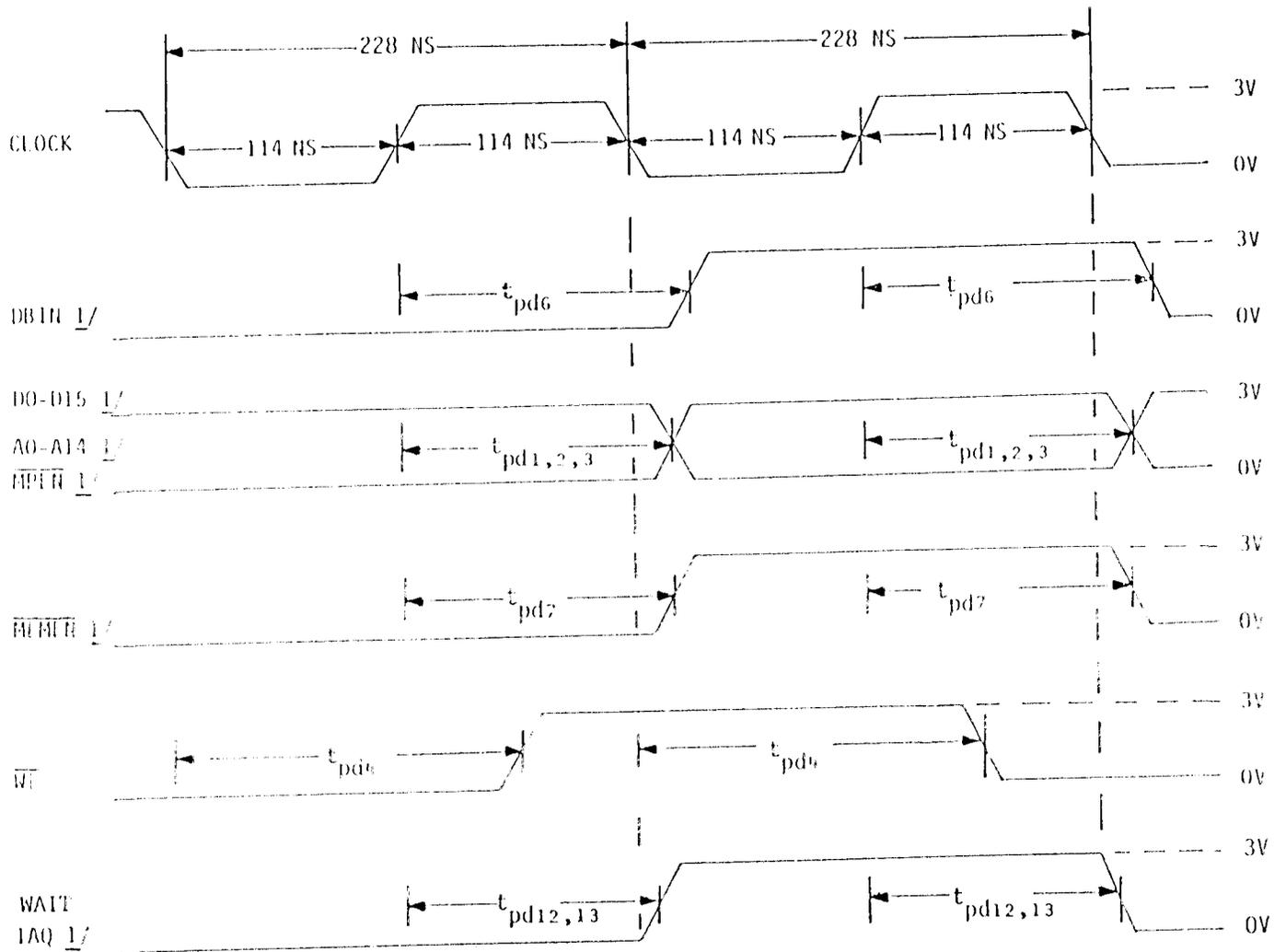
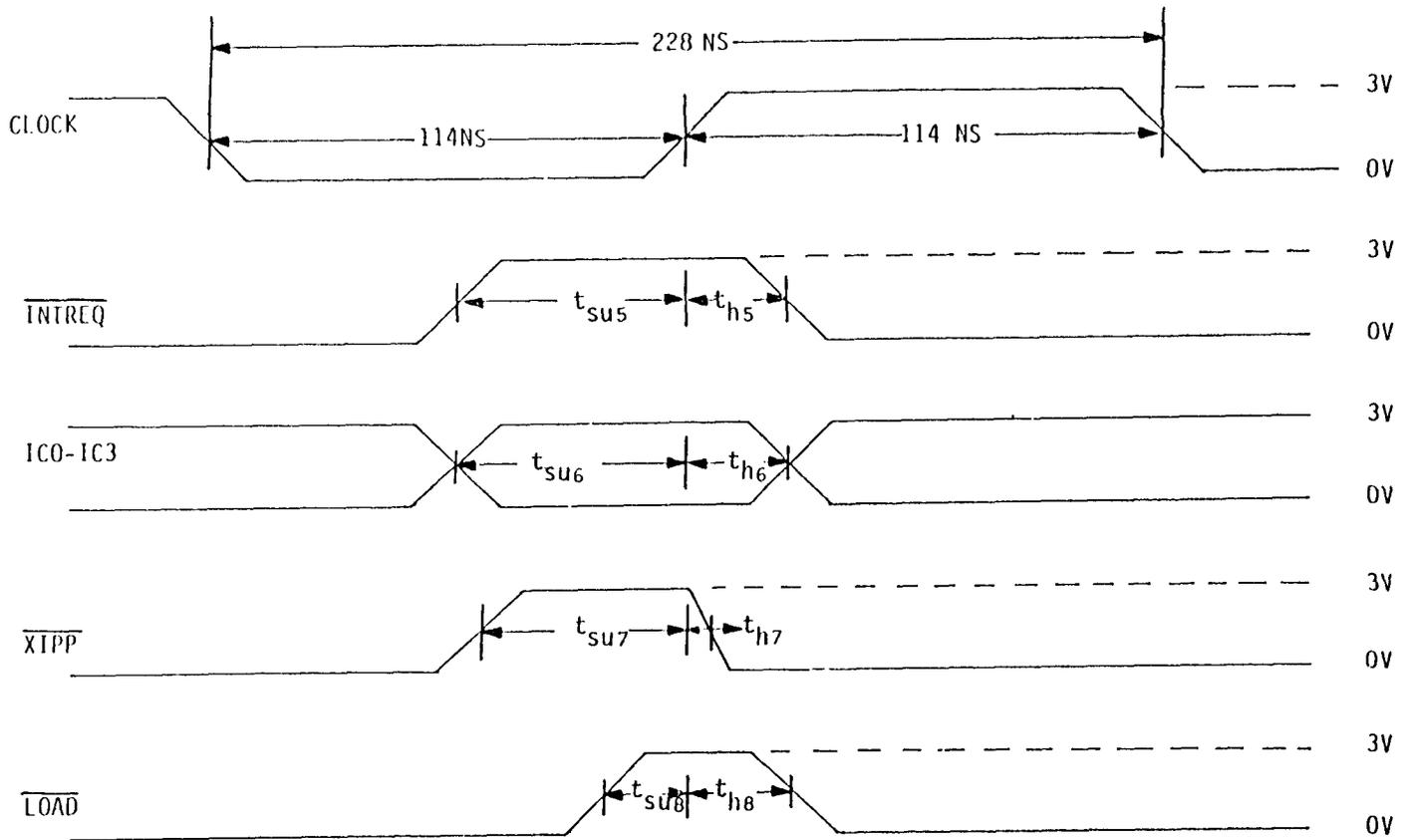


FIGURE 7. AC parametric waveforms - Continued.

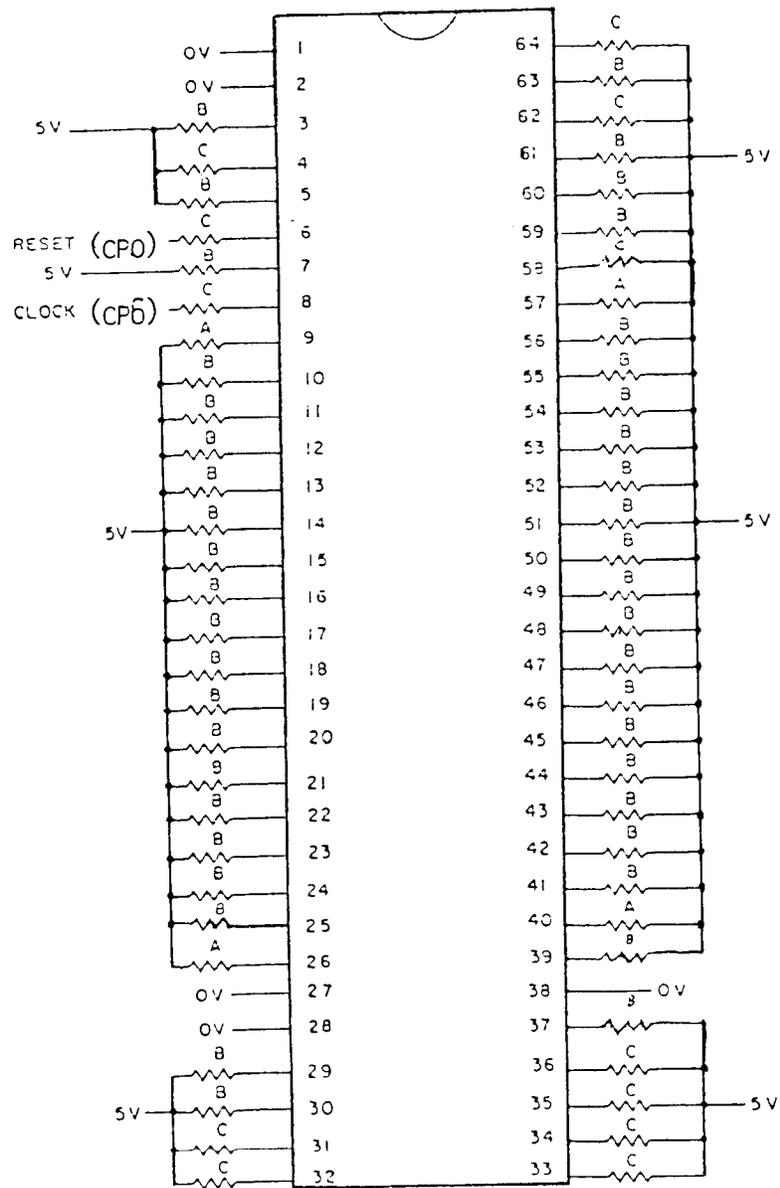
$\frac{1}{2}$   $t_{pd}$  shown must be increased to a maximum of 200 ns when leaving a hold state.



NOTE: In addition to the switching characteristics pictured above, the following signal relationships exist:

1. During write operations:
  - a. ADDR lines are valid prior to  $\overline{WE}$  active.
  - b.  $\overline{WE}$  goes inactive prior to ADDR lines going invalid.
  - c. Data lines are valid prior to  $\overline{WE}$  active.
  - d.  $\overline{WE}$  goes inactive prior to Data lines going invalid.
  - e.  $\overline{WE}$  does not go active before  $\overline{MEMEN}$  goes active.
  - f.  $\overline{WE}$  goes inactive before  $\overline{MEMEN}$  goes inactive.
2. During read operations:
  - a.  $\overline{DBIN}$  does not go inactive before the maximum data hold time ( $t_{h3}$ ) runs out.
  - b.  $\overline{MEMEN}$  does not go inactive before the maximum data hold time ( $t_{h3}$ ) runs out.
3. During CRU output operations:
  - a. CRUCLK goes inactive prior to ADDR lines going invalid.
  - b. CRUCLK goes inactive prior to CRUOUT going invalid.

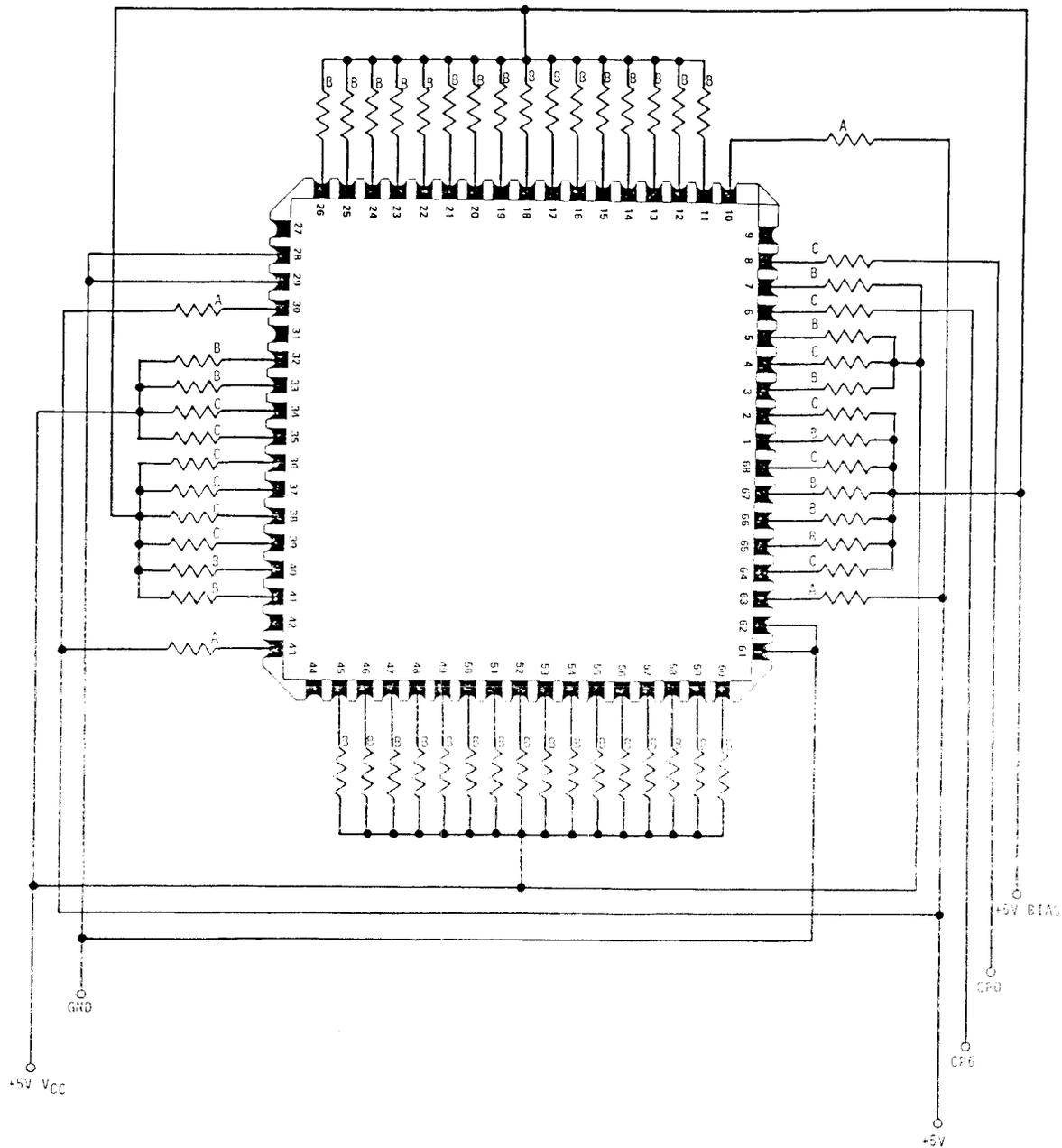
FIGURE 7. AC parametric waveforms - Continued.



## NOTES:

- All resistor values are in ohms.  
A = 33 $\Omega$ , B = 330 $\Omega$ , C = 1 k $\Omega$ .
- Pins 9, 26, 40 and 57 are injector sources.
- The four 33-ohm resistors are metal film 1 watt  $\pm 1\%$  tolerance, and all other resistors are > 1/4 watt  $\pm 5\%$ .
- CP0 = 3.125 kHz; CP6 = 200 kHz.

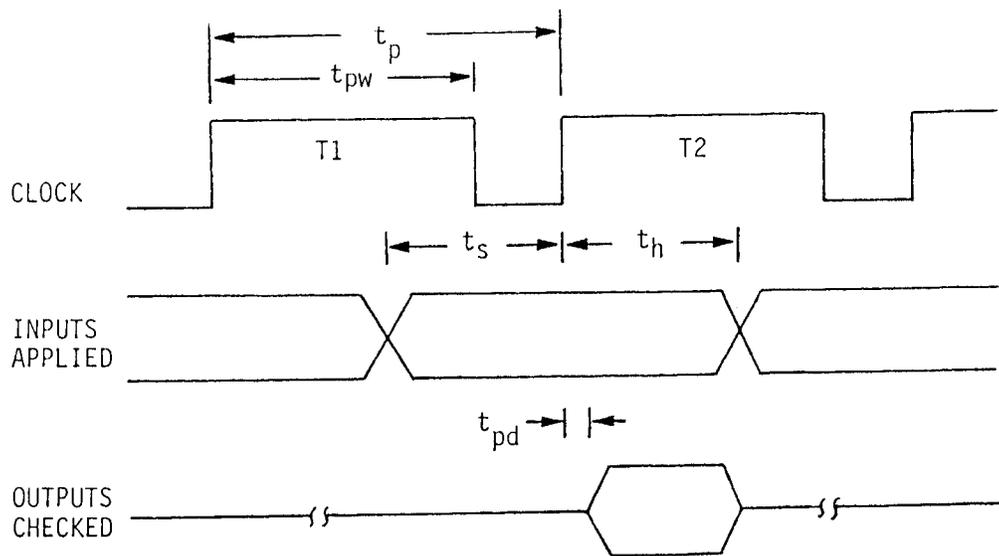
FIGURE 8. Burn-in and operating life test circuit (64-pin DIP).



NOTES:

1. All resistor values are in ohms.  
A = 33Ω, B = 330Ω, C = 1 kΩ.
2. Pins 10, 30, 43 and 63 are injector sources.
3. The "A" resistors are metal film 1 watt ±1%,  
all other resistors are 1/4 watt, ±5%.
4. CP0 = 3.125 kHz; CP6 = 200 kHz.

FIGURE 9. Burn-in and operating life test circuit (68-pad chip carrier).



## NOTES:

- Actual pattern of input data is defined and described in figure 11. Patterns will be executed in series until the specific exit pattern number listed in table III is reached.
- Definition of t terms:
  - $t_{pw}$  = clock pulse width = 1.5  $\mu$ s
  - $t_p$  = clock period = 2.0  $\mu$ s
  - $t_s$  = data setup time = 1.0 ms
  - $t_{pd}$  = prop. delay time = 600  $\mu$ s
  - $t_h$  = data hold time = 800  $\mu$ s

FIGURE 10. DC parametric waveforms.

Functional patterns are defined in fields separated by commas. The fields are defined in hexadecimal with each bit corresponding to a device pin. The fields are filled from left to right with unused trailing bits set to zero. Field names are assigned as follows:

PTT	X'	FFF,	0000000,	FFFFFFF,	8,	0000,	FFFF;	0
PATTERN		INPUTS	OUTPUTS	OUTPUT MASK	CLOCK	I/O'S	I/O MASK	DRIVE

These fields correspond to the following pins:

INPUTS - LOAD, RESET, CRUIN, INTREQ,  
IC3-ICO, XIPP, READY, HOLD

OUTPUTS - WAIT, HOLDA, IAQ, A14-A0,  
MPEN, DBIN, CRUOUT, INTACK,  
CYCEND, CRUCLK, WE, MEMEN

OUTPUT MASK - MASK FOR OUTPUTS

CLOCK - CLOCK PIN

I/O'S - D0 - D15

I/O MASK - MASK FOR I/O'S

DRIVE - INDICATES DIRECTION FOR I/O PINS "1" INDICATES  
DATA BEING DRIVEN INTO PART

PATTERN - PATTERN (PTT) OR REPEAT (RPT) AND COUNT

FIGURE 11. Functional patterns definition.

The actual functional patterns used are described below:

	Pattern set		Pattern number
RPT	2,X'90E,0000004,FFFFFFE,8,0000,FFFF;0	*.	1
PTT	X'DOE,0000016,1FFFE80,8,0000,FFFF;0	*.	3
PTT	X'DOE,0000006,1FFFE80,8,0000,FFFF;0	*.	4
PTT	X'DOE,0000016,1FFFE80,8,0000,FFFF;0	*.	5
PTT	X'DOE,0000006,1FFFE80,8,0000,FFFF;0	*.	6
PTT	X'DOE,0000354,0000080,8,0000,FFFF;8	*.	7
PTT	X'DOA,8000354,0000080,8,0000,FFFF;8,PM	*.	8
PTT	X'DOE,0000344,0000080,8,AA8C,FFFF;8	*.	9
PTT	X'DOE,0000216,0000080,8,AA8C,FFFF;8	*.	10
PTT	X'DOE,0000206,0000080,8,AA8C,FFFF;0	*.	11
PTT	X'DOE,1555614,0000080,8,AA8C,FFFF;0	*.	12
PTT	X'DOE,1555600,0000080,8,AA8C,FFFF;0,PM	*.	13
PTT	X'DOE,1555616,0000080,8,AA8C,FFFF;0	*.	14
PTT	X'DOE,1555606,0000080,8,AA8C,FFFF;0	*.	15
PTT	X'DOE,0555614,0000080,8,AA8C,FFFF;0	*.	16
PTT	X'DOC,0555600,0000080,8,AA8C,FFFF;0	*.	17
PTT	X'DOC,7FFFF16,0000080,8,FFFF,0000;0,PM	*.	18
PTT	X'DOE,0555616,0000080,8,FFFF,FFFF;0	*.	19
PTT	X'DOE,0555606,0000080,8,FFFF,FFFF;0	*.	20
PTT	X'DOE,1955614,0000080,8,FFFF,FFFF;0	*.	21
PTT	X'DOE,1955600,0000080,8,FFFF,FFFF;0	*.	22
PTT	X'DOE,1000314,0000080,8,FFFF,FFFF;0	*.	23
PTT	X'DOE,1000304,0000080,8,5554,0000;8	*.	24
PTT	X'DOE,1000216,0000080,8,5554,0000;8	*.	25
PTT	X'DOE,1000206,0000080,8,5554,0000;0,PM	*.	26
PTT	X'DOE,2AAAB14,0000080,8,5554,0000;0	*.	27
PTT	X'DOE,2AAAB04,0000080,8,0740,0000;8,PM	*.	28
PTT	X'DOE,0AAAA16,0000000,8,0740,0000;8	*.	29
PTT	X'DOE,0AAAA06,0000000,8,5554,0000;0	*.	30
PTT	X'DOE,0C55734,0000000,8,5554,0000;0	*.	31
PTT	X'DOE,0C55724,0000000,8,D555,0000;8,PM	*.	32
PTT	X'DOE,0C556B6,0000000,8,D555,0000;8	*.	33
PTT	X'DOE,0C556A6,0000000,8,5554,0000;0	*.	34
PTT	X'DOE,0C556B6,0000000,8,5554,0000;0	*.	35
PTT	X'DOE,0C556A6,0000000,8,5554,0000;0	*.	36
PTT	X'DOE,0C556B6,0000000,8,2AAA,0000;0	*.	37
PTT	X'DOE,0C556A6,0000000,8,2AAA,0000;0	*.	38
PTT	X'DOE,0C556B4,0000000,8,2AAB,0000;0	*.	39
PTT	X'DOE,2C556A4,0000000,8,2AAB,0000;0,PM	*.	40
PTT	X'DOE,3AAAA90,0000000,8,2AAB,0000;0	*.	41
PTT	X'DOE,1AAAAA4,0000000,8,0080,0000;8	*.	42
PTT	X'DOE,1AAAA96,0000000,8,0080,0000;8	*.	43
PTT	X'DOE,1AAAA86,0000000,8,2AAB,0000;0	*.	44
PTT	X'DOE,0C55794,0000000,8,2AAB,0000;0	*.	45
PTT	X'DOE,0C55784,0000000,8,8080,0000;8	*.	46
PTT	X'DOE,0C55696,0000000,8,8080,0000;8	*.	47
PTT	X'DOE,0C55486,0000000,8,8080,0000;0	*.	48
PTT	X'DOE,0C55496,0000000,8,8080,0000;0	*.	49
PTT	X'DOE,0C55486,0000000,8,8080,0000;0,PM	*.	50
PTT	X'DOE,26AA994,0000000,8,8080,0000;0	*.	51
PTT	X'DOE,26AA984,0000000,8,1E00,0000;8	*.	52
PTT	X'DOE,06AA816,0000000,8,1E00,0000;8	*.	53
PTT	X'DOE,06AA806,0000000,8,8080,0000;0	*.	54
PTT	X'DOE,06AA816,0000000,8,8080,0000;0	*.	55
PTT	X'DOE,06AA806,0000000,8,8080,0000;0	*.	56
PTT	X'DOE,0955534,0000000,8,8080,0000;0	*.	57
PTT	X'DOE,0955524,0000000,8,0080,0000;8	*.	58
PTT	X'DOE,0955436,0000000,8,0080,0000;8	*.	59
PTT	X'DOE,0955426,0000000,8,8080,0000;0	*.	60
PTT	X'DOE,0000136,0000000,8,FFFF,0000;0	*.	61
PTT	X'DOE,000012E,0000000,8,FFFF,0000;0,PM	*.	62
PTX	X'DOE,000012E,0000000,0,FFFF,0000;0,EX	*.	

FIGURE 11. Functional patterns definition - Continued.







- 1/ Inputs and/or outputs which are tested with the same conditions (i.e., A0-A15, IC3-IC0, and D0-D15) are shown together in this table for simplification. Only in the actual test, the test conditions are applied to each pin, one at a time.
- 2/ For this test  $V_{IH} = 2 \text{ V}$  and  $V_{IL} = 7 \text{ V}$  to obtain the correct pattern number.
- 3/ All "INJ" inputs must be wired together to a common source of 400 mA.
- 4/ For information on subgroups 7, 8, 9, 10, and 11, see 4.5.2 and 6.4.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Ground zero voltage potential.
V <sub>IN</sub>	- - - - -	Voltage level at an input terminal.
V <sub>IC</sub>	- - - - -	Input clamp voltage.
I <sub>IN</sub>	- - - - -	Current flowing into an input terminal.

6.4 Functional pattern sets. The table for the functional and switching test is not printed herein because of its extreme length and pattern complexity. The test program output should be obtained in a form compatible with test system architecture. The device manufacturer may be consulted for information on obtaining such output.

TABLE IV. Functional pattern sets for group A inspection (subgroups 7, 8, 9, 10, and 11).

Number	Name	No. patterns	Subgroups
99890000	RSET (PS01)	28	7,8
99890001	998901 (T1B1) (PS02)	329	7,8
99890002	998902 (T2B1) (PS03)	4133	7,8
99890003	998903 (M0RC) (PS04)	2349	7,8
99890100	T1B1AC (PS07)	829	7,8,9,10,11
99890200	T2B1AC (PS08)	598	7,8,9,10,11
99890300	T2B2AC (PS09)	572	7,8,9,10,11
99890400	T2B3AC (PS10)	671	7,8,9,10,11
99890500	T2B5AC (PS11)	299	7,8,9,10,11
99890600	X1PAC (PS12)	337	7,8,9,10,11
99890101	T1B1IC (PS13)	829	7,8,9,10,11
99890201	T2B1IC (PS14)	598	7,8,9,10,11
99890301	T2B2IC (PS15)	572	7,8,9,10,11
99890407	T2B3IC (PS16)	671	7,8,9,10,11
99890501	T2B5IC (PS17)	299	7,8,9,10,11
99890601	X1P0IC (PS18)	337	7,8,9,10,11
99891000	MAXFRQ (PS19)	829	9,10,11

6.5 Pin definitions. The following describes the function of each pin. (See figure 3 for their assigned location.)

Signature	Case Y	Case Z	I/O	Description
ADDRESS BUS				
A0 (MSB) ↓ A14 (LSB)	24 ↓ 10	25 ↓ 11	OUT*	A0-A14 comprise the address bus. This open-collector bus provides the memory address to the memory system when MEMEN is active and CRU I/O bit address to the I/O system when MEMEN is inactive and DBIN is active.
MPEN	25	26	OUT*	MEMORY MAP ENABLE. MPEN represents the inverted value of Status Register Bit 8 (ST8). MPEN can be changed by any instruction (i.e., LST, etc.) affecting ST8 and will be set to 1 during trap addressing; namely interrupts, LOAD, RESET, XOP and ILL0P, MPEN may be used to allow memory expansion to 64 kilowords.
DATA BUS				
D0 (MSB) ↓ D15 (LSB)	41 ↓ 55	45 ↓ 60	I/O*	D0-D15 comprise the bidirectional, open-collector data bus. This bus transfers memory data to (when writing) and from (when reading) the external memory system when MEMEN is active.

\* When HOLDA is active, these terminals are high.

Signature	Case Y	Case Z	I/O	Description
POWER SUPPLY				
INJ	9	10		Injector-supply current
INJ	26	30		Injector-supply current
INJ	40	43		Injector-supply current
INJ	57	63		Injector-supply current
GND	1	61		Ground
GND	2	62		Ground
GND	27	28		Ground
GND	28	29		Ground
CLOCK				
CLK	8	8	IN	Single-phase clock input
BUS CONTROL				
$\overline{\text{MEMEN}}$	63	1	OUT*	MEMORY ENABLE. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a valid memory address.
DBIN	29	32	OUT*	DATA BUS IN. When activated (high) by the device during $\overline{\text{MEMEN}}$ , DBIN indicates that the device has disabled its output buffers to allow the memory system to place memory read data on the bus. The device will also activate DBIN during all CRU operations and during the execution of the five external instructions. In all other cases except when HOLDA is active, the device will maintain DBIN at a low logic level.
$\overline{\text{WE}}$	61	67	OUT*	WRITE ENABLE. When active (low), $\overline{\text{WE}}$ indicates that the data bus is outputting data to be written into memory.
COMMUNICATION REGISTER UNIT (CRU)				
CRUCLK	60	66	OUT	CRU CLOCK. When active (high), CRUCLK indicates to the external logic the presence of output data on CRUOUT or the presence of an encoded external instruction on A0-A2.
CRUIN	31	34	IN	CRU DATA IN. CRUIN receives input data from the external interface logic. When the device executes a STCR or TB instruction, it samples CRUIN for the level of the CRU bit specified by the address bus (A3-A14).
CRUOUT	30	33	IN	CRU DATA OUT. CRUOUT outputs serial data when the device executes a LDCR, SBZ, or SBO instruction. The data on CRUOUT should be sampled by the external interface logic when CRUCLK goes active.

\* When HOLDA is active, these terminals are high.

Signature	Case Y	Case Z	I/O	Description
INTERRUPT CONTROL				
$\overline{\text{INTREQ}}$	32	35	IN	INTERRUPT REQUEST. When active (low), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requesting service. If $\overline{\text{INTREQ}}$ is active the device loads the data on the interrupt code input lines IC0-IC3 into the internal interrupt-code storage register. The code is then compared to the interrupt mask bits of the status register. If the interrupt code is equal to or less than Status Register Bits 12-15 (equal or higher priority than the previous enabled interrupt level), the device initiates the interrupt sequence. If the comparison fails, the device ignores the interrupt request. In the case, $\overline{\text{INTREQ}}$ should be held active. The device will continue to sample IC0-IC3 until the program enables a sufficiently low interrupt level to accept the requesting interrupt.
IC0 (MSB) ↓ IC3 (LSB)	36 ↓ 33	39 ↓ 36	IN	INTERRUPT CODES IC0 (MSB)-IC3 (LSB), indicates an interrupt identity code, are sampled by the device when $\overline{\text{INTREQ}}$ is active (low). When IC0-IC3 are LLLL, the highest-priority external interrupt is requesting service; when HHHH, the lowest-priority external interrupt is requesting service.
INTACK	37	40	OUT	INTERRUPT ACKNOWLEDGE. When active (high) during nonhold states, INTACK indicates the device has initiated a trap sequence caused by the receipt of a valid interrupt, $\overline{\text{LOAD}}$ or $\overline{\text{RESET}}$ . INTACK shall be activated in the trap sequence while the device is obtaining the new WP value from memory. An external device may determine which function or interrupt level is being serviced by monitoring the address bus during the INTACK time. When the device is in a hold state (caused by activation of $\overline{\text{XIPP}}$ or $\overline{\text{HOLD}}$ ) INTACK indicates that the device has received a valid interrupt (level is less than value of interrupt mask), a $\overline{\text{LOAD}}$ or $\overline{\text{RESET}}$ . INTACK will remain valid (high) until the device leaves a hold state ( $\overline{\text{HOLD}}$ or $\overline{\text{XIPP}}$ released) or until the signal requesting interrupt is released.
MEMORY CONTROL				
$\overline{\text{HOLD}}$	64	2	IN	HOLD. When active (low), $\overline{\text{HOLD}}$ indicates to the device that an external controller (e.g., DMA device) desires to use the memory bus for direct memory data transfers. In response, the device enters the hold state after completion of its present cycle (memory or nonmemory). The device then asserts $\overline{\text{HOLDA}}$ and allows its address bus, $\overline{\text{MPEN}}$ , data bus, $\overline{\text{MEMEN}}$ , $\overline{\text{WE}}$ , $\overline{\text{DBIN}}$ , $\overline{\text{IAQ}}$ and $\overline{\text{CYCEND}}$ to be pulled to the high logic state. When $\overline{\text{HOLD}}$ is deactivated, the device reassumes bus control and continues operation by resuming execution of the suspended instruction.
$\overline{\text{HOLDA}}$	5	5	OUT	HOLD ACKNOWLEDGE. When active (high) $\overline{\text{HOLDA}}$ indicates that the device is in a hold state and that its address bus, $\overline{\text{MPEN}}$ , data bus, $\overline{\text{MEMEN}}$ , $\overline{\text{WE}}$ , $\overline{\text{DBIN}}$ , $\overline{\text{IAQ}}$ , and $\overline{\text{CYCEND}}$ are pulled to the high state. The device will enter a hold state in response to the activation of $\overline{\text{HOLD}}$ or $\overline{\text{XIPP}}$ (during the execution of an ILL0P or X0P instruction).

Signature	Case Y	Case Z	I/O	Description
READY	62	68	IN	READY. When active (high) READY indicates that the memory (for memory operations) or CRU device (for CRU operations) will be ready to read or write during the next clock cycle. The READY is not active (low), the device enters a wait state and suspends internal operations until the memory system or CRU device activates READY.
WAIT	3	3	OUT	WAIT. When active (high), WAIT indicates the device has entered a wait state in response to a not READY condition from a memory system or a CRU device.
TIMING AND CONTROL				
IAQ	7	7	OUT*	INSTRUCTION ACQUISITION. IAQ is activated (high) by the device during any indicated instruction acquisition memory cycle. Consequently, IAQ may be used by an external device as an indication of when to sample the memory data bus to obtain instruction operations code data.
$\overline{\text{CYCEND}}$	59	65	OUT*	END OF CYCLE. When active (low), $\overline{\text{CYCEND}}$ indicates that the device will initiate a new microinstruction cycle on the next low-to-high transition of the clock.
MPILCK	39	41	OUT	MULTIPROCESSOR INTERLOCK. When active (high) MPILCK indicates the device is performing the operations associated with operand transfer and manipulation for the ABS instruction. MPILCK shall be activated by the device during any ABS instruction upon initiation of the operand read operation and remain active until the completion of the instruction (i.e. MPILCK remain active for the duration of the ready-modify-write operation cycle for the ABS instruction). Consequently, MPILCK may be used in the implementation of a nonseperable test and set capability. HOLD is sampled during MPILCK activation, so MPILCK can be used to control assertion of HOLD.
XIPP	58	64	IN	EXTENDED INSTRUCTION PROCESSOR PRESENT. When activated (low) by an external device (an extended instruction processor, XIP) upon detection of the acquisition of an undefined op code. $\overline{\text{XIPP}}$ indicates the XIP will execute the undefined instructions. Recognition of XIPP will cause the device to allow its memory bus signals to be pulled high, activate HOLDA and enter a hold state (i.e., suspend internal operation) after it has stored its WP, PC and ST in the workspace defined by the interrupt-level-2 trap vector. Upon receipt of HOLDA, the XIP may then proceed to execute the undefined instruction. During the instruction execution, the XIP may utilize the WP, PC and ST previously stored in memory by the device. Upon completion of its instruction execution, the XIP releases $\overline{\text{XIPP}}$ and allows the device to resume bus control and restart instruction execution. The device will resume operation by reloading (from memory) its WP, PC and ST. $\overline{\text{XIPP}}$ may also be used to initiate a trap to interrupt-level-2 by going active during IAQ for any instruction. This is useful for implementing break points or maintenance panels.

\* When HOLDA is active, these terminals are high.

Signature	Case Y	Case Z	I/O	Description
$\overline{\text{LOAD}}$	4	4	IN	<p><math>\overline{\text{LOAD}}</math>. When active (low), <math>\overline{\text{LOAD}}</math> causes the device to set <math>\overline{\text{MPEN}}</math> high, issue <math>\text{INTACK}</math>, store old PC, WP, and ST, set Status Register Bits 7-15 low, and execute a nonmaskable interrupt with unmapped memory addresses <math>\text{FFFC}_{16}</math> and <math>\text{FFFE}_{16}</math> containing the associated trap vectors (WP and PC). The load sequence is initiated after the instruction being executed is completed. <math>\overline{\text{LOAD}}</math> will also terminate an idle state. If <math>\overline{\text{LOAD}}</math> is active at the end of a reset function, the <math>\overline{\text{LOAD}}</math> trap will occur after the reset function is completed. If <math>\overline{\text{LOAD}}</math> is activated during a hold state (caused by <math>\overline{\text{XIPP}}</math> or <math>\overline{\text{HOLD}}</math>), the device will activate <math>\text{INTACK}</math> to indicate a pending <math>\overline{\text{LOAD}}</math> needs to be serviced. During hold states, <math>\overline{\text{LOAD}}</math> will remain active until the device leaves the hold state and the above conditions are met. <math>\overline{\text{LOAD}}</math> may be used to implement bootstrap loaders. Additionally, front-panel routines may be implemented using CRU bits as front panel interface signals, and software control routines to direct the panel operations.</p>
$\overline{\text{RESET}}$	6	6	IN	<p><math>\overline{\text{RESET}}</math>. When active (low logic level), <math>\overline{\text{RESET}}</math> causes the device to reset itself, and inhibit <math>\overline{\text{WE}}</math> and <math>\overline{\text{CRUCLK}}</math>. When <math>\overline{\text{RESET}}</math> is released, the device goes through a level-zero interrupt sequence by causing <math>\overline{\text{MPEN}}</math> to go to high, issuing <math>\text{INTACK}</math>, storing old PC, WP, and ST, setting all status register bits low, acquiring the WP and PC trap vectors from memory locations <math>\text{0000}_{16}</math> and <math>\text{0002}_{16}</math>, and then fetching the first instruction of the reset programs environment if <math>\overline{\text{LOAD}}</math> is not active. The device continuously samples <math>\overline{\text{RESET}}</math> on low-to-high clock transitions <math>\overline{\text{RESET}}</math> must be active for one low-to-high transition of the clock and satisfy the hold time requirements of this signal.</p>

5.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	SBP9989

6.7 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:  
Air Force - 17  
Navy - EC  
Army - ER

Review activities:  
Army - AR, MI  
Navy - OS, SH, TD  
Air Force - 11, 19, 85, 99  
DLA - ES

User activities:  
Army - SM  
Navy - AS, CG, MC

Preparing activity:  
Air Force - 17

Agent:  
DLA - ES

(Project 5962-0955-2)