MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS, SILICON GATE, MONOLITHIC, 8-BIT MICROPROCESSOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic CMOS, silicon gate microprocessor. One product assurance class (B) and a choice of case outline and lead finish are provided for each type, and are reflected in the Part or Identifying Number (PIN) (see 6.7).

1.2 Classification.

1.2.1 Device type. The device type shall be as follows:

Device type	Clock frequency	Circuit
01	6.0 MHz	8-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline, (see MIL-M-38510, appendix C)
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Voltage on V_{CC} with respect to V_{SS} - - - -	-0.3 V to +7 V
Voltage on any pin (referenced to V_{SS}) - - -	-0.3 V to V_{CC} +3.0 V
Storage temperature range- - - - - - - - - - -	-65°C to +150°C
Maximum power dissipation- - - - - - - - - - -	1.0 W
Lead temperature (soldering, 5 seconds)- - -	270°C
Maximum junction temperature (T_J)- - - - - -	170°C 1/
Thermal resistance, junction to case (θ_{JC}) -	See MIL-M-38510, appendix C

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening condition in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.4 Recommended operating conditions.

Supply voltage - - - - - - - - - - - - - - - - -	4.5 V minimum to 5.5 V maximum
Minimum high-level input voltage:	
Logic inputs (V_{IH}) - - - - - - - - - - - - - -	2.2 V
Clock input (V_{IHC}) - - - - - - - - - - - - - -	V_{CC} -0.6 V
Maximum low-level input voltage:	
Logic inputs (V_{IL}) - - - - - - - - - - - - - -	+0.8 V
Clock input (V_{ILC}) - - - - - - - - - - - - - -	+.45 V
Frequency of operation - - - - - - - - - - - - - -	0.5 MHz to 6.0 MHz
Case operating temperature range - - - - - - -	-55°C to +125°C
Clock rise time (t_r) - - - - - - - - - - - - -	20 ns maximum
Clock fall time (t_f) - - - - - - - - - - - - -	20 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections and pin assignments. The terminal connections and pin assignments shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Terms and definitions. Terms and definitions shall be as specified in 6.4.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits		Unit
					Min	Max	
Clock input low voltage	V_{ILC}				-0.3	0.45	V
Clock input high voltage	V_{IHC}				V_{CC}-0.6	V_{CC}+0.3	V
Input low voltage	V_{IL}				-0.3	0.8	V
Input high voltage	V_{IH}				2.2	V_{CC}	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA				0.4	V
Output high voltage	V_{OH1}	I_{OH} = -250 μA			V_{CC}-0.8		V
Output high voltage	V_{OH2}	I_{OH} = -1.6 mA			2.4		V
Power supply current	I_{CC}	V_{CC} = 5.5 V				250	mA
Input leakage current, low	I_{IL1}	V_{IN} = 0.4 V			-10	+10	μA
Input leakage current, high	I_{IH1}	V_{IN} = 2.4 V			-10	+10	μA
Three-state output leakage, current, low	I_{ZL}	V_{OUT} = 0.4 V			-10	+10	μA
Three-state output leakage, current, high	I_{ZH}	V_{OUT} = 2.4 V			-10	+10	μA
Input leakage current, low-data bus	I_{IL2}	V_{IN} = 0.4 V			-10	+10	μA
Input leakage current, high-data bus	I_{IH2}	V_{IN} = 2.4 V			-10	+10	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits Min	Limits Max	Unit
Clock capacitance	C_C	f = 1 MHz, T_C = 25°C, from input or output pin to ground; all other pins at ground				10	pF
Input capacitance, all other inputs	C_I					10	pF
Output capacitance, all outputs and data bus	C_O					20	pF
Maximum clock frequency	f_{MAX}	V_{CC} = 4.5 V, C_L = 50 pF ±10%			6.0		MHz
Maximum clock frequency	f_{MAX}	V_{CC} = 5.5 V, C_L = 50 pF ±10%			6.0		MHz
Clock cycle time	t_{cyc}	T_C = -55°C to +125°C, V_{CC} = 5.0 V ±10%, unless otherwise specified, C_L = 140 pF ±10%	6	1	165	3/	ns
Clock time Rise	t_r		6	5		20	ns
Fall	t_f		6	4		20	ns
Clock pulse width High	t_{PWH1}		6	2	65	2,000	ns
Low	t_{PWL1}		6	3	65	2,000	ns
$\overline{MREQ}$ pulse width High	t_{PWH2}		6	10	4/		ns
Low	t_{PWL2}		6	11	5/		ns
$\overline{WR}$ pulse width low	t_{PWL3}		6	31	6/		ns
$\overline{NMI}$ pulse width low	t_{PWL4}		6		70		ns
Data setup to clock ↑ (D_0 - D_7)	t_{SZH1}		6	15	30		ns
	t_{SZL1}		6	15	30		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits Min	Limits Max	Unit
$\overline{WAIT}$ setup to clock ↓	t_{SLH1}	T_C = -55°C to +125°C, V_{CC} = 5.0 V ±10%, unless otherwise specified; C_L = 140 pF ±10%	6	17	60		ns
	t_{SHL1}			17	60		
Data setup to clock ↓ (D_0 - D_7)	t_{SZH2}			25	40		
	t_{SZL2}			25	40		
$\overline{BUSRQ}$ setup to clock ↑	t_{SLH2}			38	50		
	t_{SHL2}			38	50		
$\overline{Reset}$ setup to clock ↑	t_{SLH3}				60		
	t_{SHL3}				60		
$\overline{INT}$ setup to clock ↑	t_{SLH4}				70		
	t_{SHL4}				70		
Data valid after RD ↑ (D_0 - D_7)	t_{HLZ1}			16	0		
	t_{HHZ1}			16	0		
$\overline{WAIT}$ valid after clock ↓	t_{HLH1}			18	0		
	t_{HHL1}			18	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits Min	Limits Max	Unit
$\overline{BURSQ}$ valid after clock ↑	t_{HLH2}	T_C = -55°C to +125°C, V_{CC} = 5.0 V ±10%, unless otherwise specified, C_L = 140 pF ±10%	6	39	0		ns
	t_{HHL2}			39	0		
$\overline{Reset}$ valid after clock ↑	t_{HLH3}				0		
	t_{HHL3}				0		
$\overline{INT}$ valid after clock ↑	t_{HLH4}				0		
	t_{HHL4}				0		
Clock ↑ to address valid delay (A_0 - A_{15})	t_{PLH1}			6		90	
	t_{PHL1}			6		90	
Address valid to $\overline{MREQ}$ ↓ delay	t_{PLH2}			7	7/		
	t_{PHL2}			7	7/		
Address stable before $\overline{IORQ}$ ↓	t_{PLH3}			26	8/		
	t_{PHL3}			26	8/		
Clock ↑ to address float delay	t_{PLZ1}			44		80	
	t_{PHZ1}			44		80	
Address stable from $\overline{MREQ}$ ↑, $\overline{RD}$ ↑, $\overline{WR}$ ↑, or $\overline{IORQ}$ ↑	t_{PLH4}			45	9/		
	t_{PHL4}			45	9/		
Data stable before $\overline{WR}$ ↓ (memory write)	t_{PZL1}			29	10/		
	t_{PZH1}			29	10/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits Min	Limits Max	Unit
Data stable before $\overline{WR}$ ↓ (I/O write)	t_{PZL2}	T_C = -55°C to +125°C, V_{CC} = 5.0 V ±10%, unless otherwise specified, C_L = 140 pF ±10%	6	33	11/		ns
	t_{PZH2}			33	11/		
Data stable from $\overline{WR}$ ↑	t_{PLZ2}			35	12/		
	t_{PHZ2}			35	12/		
Clock ↑ to data float delay	t_{PLZ3}			42		80	
	t_{PHZ3}			42		80	
Clock ↓ to data valid delay	t_{PZL3}			53		130	
	t_{PZH3}			53		130	
Clock ↓ to $\overline{MREQ}$ ↓ delay	t_{PHL5}			8		70	
Clock ↓ to $\overline{MREQ}$ ↑ delay	t_{PLH5}			12		70	
Clock ↑ to $\overline{MREQ}$ ↑ delay	t_{PLH6}			9		70	
Clock ↑ to $\overline{IORQ}$ ↓ delay	t_{PHL7}			27		65	
Clock ↑ to $\overline{IORQ}$ ↑ delay	t_{PLH7}			52		70	
Clock ↓ to $\overline{IORQ}$ ↑ delay	t_{PLH8}			28		70	
Clock ↓ to $\overline{IORQ}$ ↓ delay	t_{PHL8}			51		70	
Clock ↓ to $\overline{RD}$ ↓ delay	t_{PHL9}			13		80	
Clock ↓ to $\overline{RD}$ ↑ delay	t_{PLH9}			23		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = 55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Fig. no. 1/	Ref. no. 2/	Limits Min	Limits Max	Unit
Clock ↑ to $\overline{RD}$ ↑ delay	t_{PLH10}	T_C = -55°C to +125°C, V_{CC} = 5.0 V ±10%, unless otherwise specified, C_L = 140 pF ±10%	6	14		70	ns
Clock ↑ to $\overline{RD}$ ↓ delay	t_{PHL10}			24		70	
Clock ↓ to $\overline{WR}$ ↓ delay	t_{PHL11}			30		70	
Clock ↓ to $\overline{WR}$ ↑ delay	t_{PLH11}			32		70	
Clock ↑ to $\overline{WR}$ ↓ delay (I/O to write)	t_{PHL12}			34		70	
Clock ↑ to $\overline{MI}$ ↓ delay	t_{PHL13}			19		80	
Clock ↑ to $\overline{MI}$ ↑ delay	t_{PLH13}			20		80	
$\overline{MI}$ ↓ before $\overline{IORQ}$ ↓	t_{PHL14}			50	13/		
Clock ↑ to $\overline{RFSH}$ ↓ delay	t_{PHL15}			21		110	
Clock ↑ to $\overline{RFSH}$ ↑ delay	t_{PLH15}			22		100	
Clock ↓ to $\overline{HALT}$ valid delay	t_{PLH16}			36		260	
	t_{PHL16}			36		260	
Clock ↑ to $\overline{BUSAK}$ ↓ delay	t_{PHL17}			40		90	
Clock ↓ to $\overline{BUSAK}$ ↑ delay	t_{PLH18}			41		90	
Clock ↑ to $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, float delay	t_{PHZ4}			43		70	

See footnotes at end of table.

1/ Figure 6 represents the electrical performance characteristics associated with the ac limits shown in table I.

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ $t_{cyc} = t_{PWH1} + t_{PWL1} + t_r + t_f$

4/ $t_{PWH2} = t_{PWH1} + t_f - h$

5/ $t_{PWL2} = t_{cyc} - g$

6/ $t_{PWL3} = t_{cyc} - j$

7/ t_{PLH2} or $t_{PHL2} = t_{PWH1} + t_f - a$

8/ t_{PLH3} or $t_{PHL3} = t_{cyc} - b$

9/ t_{PLH4} or $t_{PHL4} = t_{PWL1} + t_r - c$

10/ t_{PZL1} or $t_{PZH1} = t_{cyc} - d$

11/ t_{PZL2} or $t_{PZH2} = t_{PWL1} + t_r - e$

12/ t_{PLZ2} or $t_{PHZ2} = t_{PWL1} + t_r - f$

13/ $t_{PHL13} = 2\ (t_{cyc}) + t_{PWH1} + t_r - k$

14/ The ac parameters represented by notes 1 through 11 are CLK dependant, the equations are used to calculate limits for any given set of CLK parameters (clock high, clock low, clock cycle time) within the frequency of operation.

Constant	Device 01	Unit
a	50	ns
b	55	
c	50	
d	140	
e	140	
f	55	
g	30	
h	40	
j	30	
k	50	

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3, herein.

3.2.5 Register configuration. Register configuration shall be as specified in figure 7.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and on figure 6 and, unless otherwise specified, apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III, table IV and figure 6.

3.6 Microprocessor instructions. The microprocessor instructions shall be as specified in table VIII.

3.7 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in a microcircuit group number 105 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirement	Subgroups (see table III) Class B devices
1	Interim electrical parameters (method 5004)	1,7
2	Dynamic burn-in (method 1015)	Required
3	Final electrical test parameters (method 5004)	*1,2,3,*7,8,9, 10,11 1/
4	Group A test requirements (method 5005)	1,2,3,4,7,8,9, 10,11,12 2/
5	Group C end-point electrical parameters (method 5005)	1,2,3,7,8 (Δ) 3/
6	Group D end-point electrical parameters (method 5005)	1,2,3,7,8

1/ (*) PDA applies to subgroups 1 and 7 (see 4.2d).
2/ Capacitance testing (see 4.4.1b).
3/ (Δ) indicates a delta limit shall be required for initial qualification and any design change only on table III, subgroup 1 and the delta values shall be computed with reference to the previous interim electrical parameters (see tabke IV).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 ~~and 5007~~ of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 6 of table II herein.

b. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D using the circuit shown on figure 3, or equivalent.

(2) $T_A = +125°C$.

c. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

d. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits specified in table VI herein, or electrical parameter limits specified in table III, subgroup 1, are defective and shall be removed from the lot. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

e. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.3.1 Qualification extension. For qualification inspection, if a manufacturer qualifies to a higher frequency device type which is designed and manufactured identically to a lower frequency device type on this specification, then the lower frequency device type may be part I qualified by conducting only group A electrical tests and electricals specified as additional group C subgroups in table II (when authorized by the qualifying activity) and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and acceptance values shown in table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II, herein.

b. Subgroup 4 (C_I, C_O, C_C measurement) shall be performed only for initial qualification and after process or package or design changes which may affect design capacitance. Tests 167 through 204 of table III herein shall be performed on 5 devices. Test 10 additional devices with the exception that one test be chosen from each of the following two test groups and performed as representative of the test group. The representative tests that are chosen will be the worst case high measured values taken on the previous units. The two test groups from table III herein are tests 173 through 180 (data bus outputs) and 134 through 171, 194 through 204 (address outputs).

c. Subgroup 12 shall be added to group A inspection requirements for class B devices using an accept on zero reject number of 22 and consist of the procedures, test conditions, and limits specified in table III. This subgroup shall be used for initial qualification only and variables data shall be submitted.

d. Subgroups 5 and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and acceptance values shown in table II of method 5005 of MIL-STD-883 as follows:

a. A special subgroup shall be added to the group B inspection requirements, using an accept on zero reject number of 15 for class B.

b. This test is required only for initial qualification or after redesign. This subgroup shall consist of a high voltage test of the input protection circuits, V_{ZAP} (see 4.5.2).

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups shown in tables III and IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II, herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table VI herein. These tests shall be required for initial qualification or after redesign only.

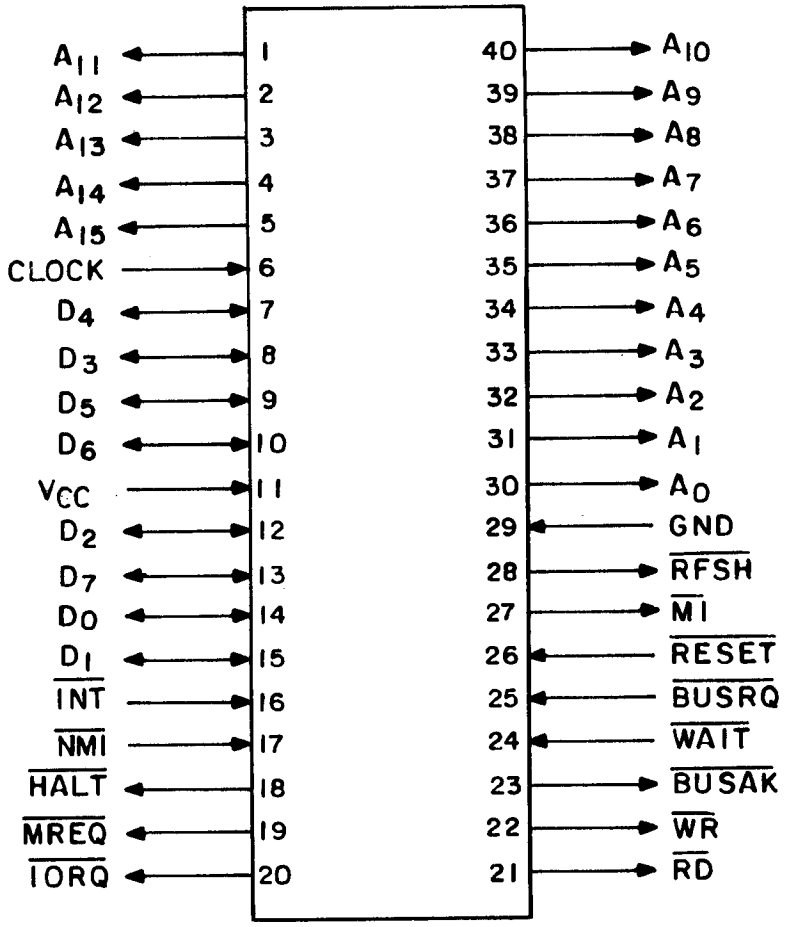
b. Steady state life test (method 1005 of MIL-STD-883).

(1) Test condition D using the circuit shown on figure 3.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.



Case Q

FIGURE 1. Terminal connections (pin assignments).

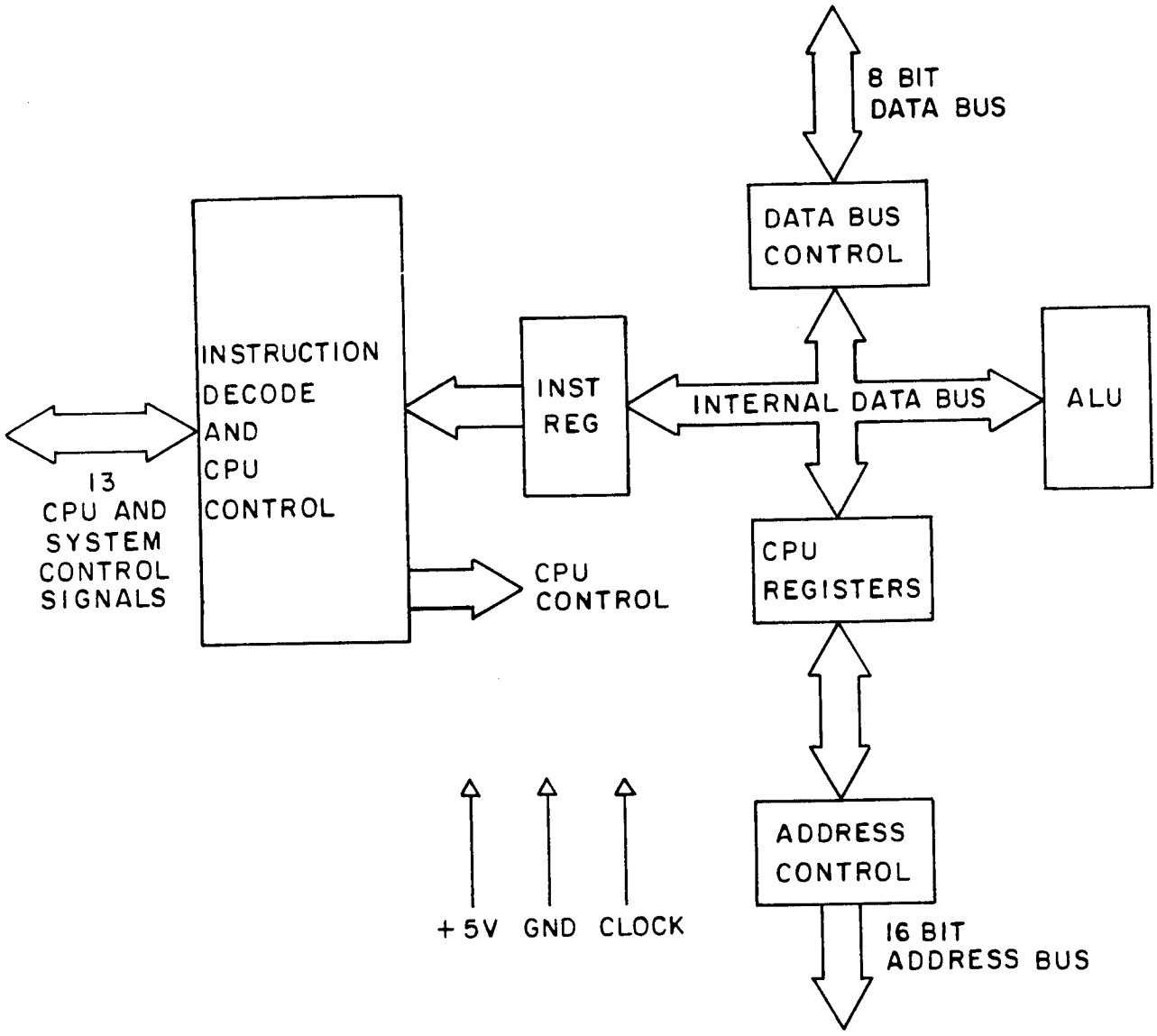
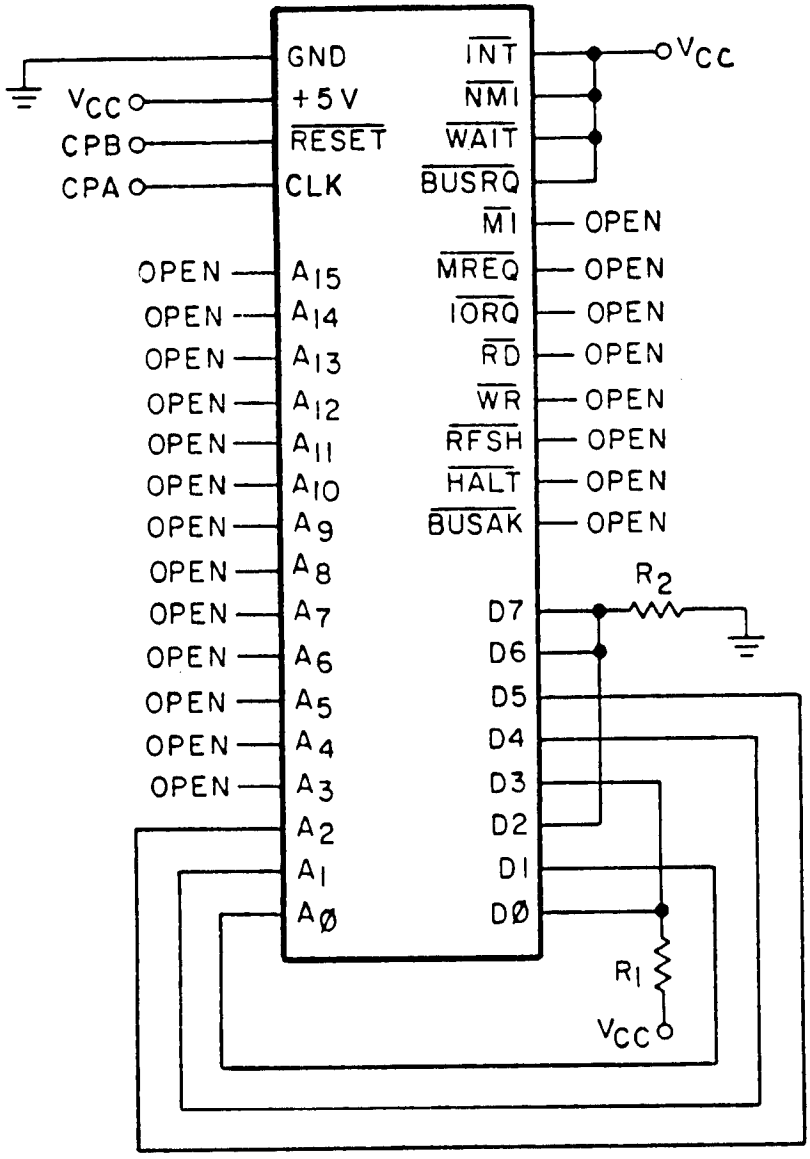


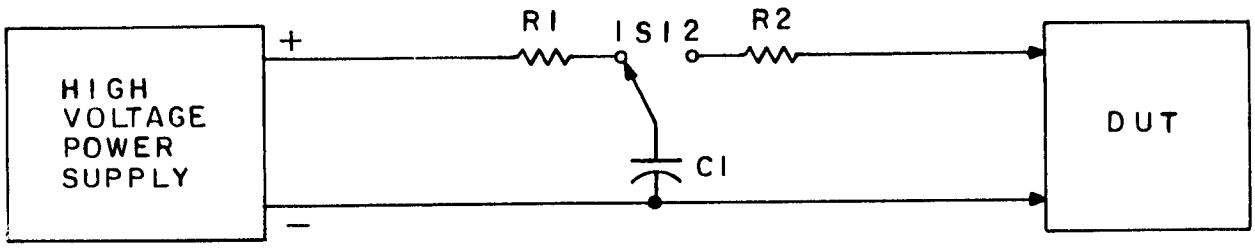
FIGURE 2. Functional block diagram.



NOTES:

1. CPA = 100 kHz ±50% square wave; duty cycle = 50 ±15%. Low level pulse shall be no greater than .45 V and high level pulse shall be no less than 3.9 V.
2. R1, R2 = 1 kΩ ±10%.
3. V_{CC} shall be no less than 4.5 V and no greater than 5.5 V.
4. CPB is a reset signal generator and is low for 16 clks, high for (4096-16) clks.

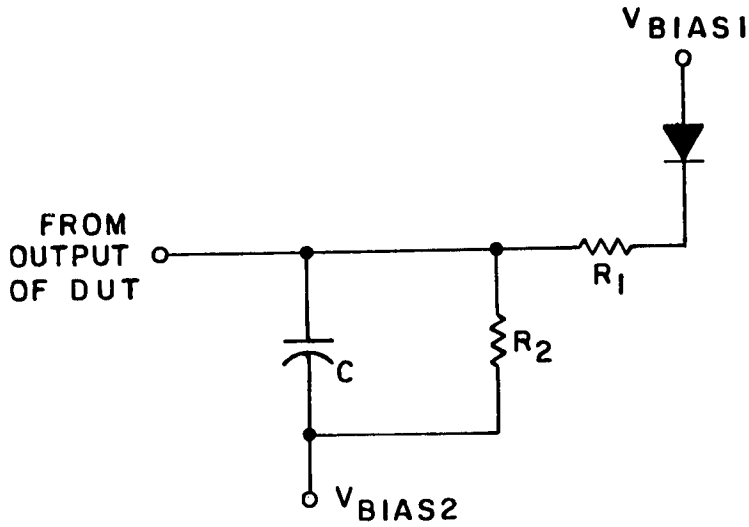
FIGURE 3. Dynamic burn-in and life test.



V_{ZAP} = 400 V minimum charge on C1.
1 MΩ < R1 < 5 MΩ.
R2 = 1.5 kilohms ±5%.
C1 = 100 pF ±10%.
S1 = Hg-wetted "bounceless" relay.

NOTE: All pins grounded except DUT pin under test.

FIGURE 4. High voltage (V_{ZAP}) test circuit.



NOTES:

1. C = 140 pF ±20% for pins 1-5, 7-10, 12-15, 18-23, 27, 28, 30-40.
2. R_1 = 550Ω ±5%, R_2 = 9.6 kΩ ±5%.
3. All diodes are 1N3064 or equivalent.
4. For ac testing:
   V_{Bias1} = 2.1 V ±5%, V_{Bias2} = 0 V.

FIGURE 5. Output load circuit for functional and ac testing, all device types.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)).

Subgroup	Symbol	MIL-STD-883	Case Q Test no.	1 A_{11}	2 A_{12}	3 A_{13}	4 A_{14}	5 A_{15}	6 C	7 D_4	8 D_3	9 D_5	10 D_6	11 V_{CC}	12 D_2	13 D_7	14 D_0	15 D_1	16 $\overline{INT}$	17 $\overline{NMI}$	18 $\overline{HALT}$	19 $\overline{MREQ}$	20 $\overline{IORQ}$
1 $T_C=+25°C$	I_{CC1}	3005	1						4.9 V	0.8 V	0.8 V	0.8 V	0.8 V	5.5 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V			
	I_{CC2}	3005	2						0.0 V	0.8 V	0.8 V	0.8 V	0.8 V	5.0 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V			
	I_{ZL}		3						4.9 V	"	"	"	"	5.5 V	"	"	"	"	"	"			
			4						"	"	"	"	"	"	"	"	"	"	"	"			
			5						"	"	"	"	"	"	"	"	"	"	"	"			
			6						"	"	"	"	"	"	"	"	"	"	"	"			
			7						"	"	"	"	"	"	"	"	"	"	"	"			
			8						"	"	"	"	"	"	"	"	"	"	"	"			
			9						"	"	"	"	"	"	"	"	"	"	"	"			
			10						"	"	"	"	"	"	"	"	"	"	"	"			
			11						"	"	"	"	"	"	"	"	"	"	"	"			
			12						"	"	"	"	"	"	"	"	"	"	"	"			
			13						"	"	"	"	"	"	"	"	"	"	"	"			
			14	0.4 V					"	"	"	"	"	"	"	"	"	"	"	"			
			15		0.4 V				"	"	"	"	"	"	"	"	"	"	"	"			
			16			0.4 V			"	"	"	"	"	"	"	"	"	"	"	"			
			17				0.4 V		"	"	"	"	"	"	"	"	"	"	"	"			
			18					0.4 V	"	"	"	"	"	"	"	"	"	"	"	"			
	I_{IL2}		19						"	0.4 V	"	"	"	"	"	"	"	"	"	"			
			20						"	0.8 V	0.4 V	"	"	"	"	"	"	"	"	"			
			21						"	"	0.8 V	0.4 V	"	"	"	"	"	"	"	"			
			22						"	"	"	0.8 V	0.4 V	"	"	"	"	"	"	"			
			23						"	"	"	"	0.8 V	"	0.4 V	"	"	"	"	"			
			24						"	"	"	"	"	"	0.8 V	0.4 V	"	"	"	"			
			25						"	"	"	"	"	"	"	0.8 V	0.4 V	"	"	"			
			26						"	"	"	"	"	"	"	"	0.8 V	0.4 V	"	"			
	I_{ZL}		27						"	"	"	"	"	"	"	"	"	0.8 V	"	"		0.4 V	
			28						"	"	"	"	"	"	"	"	"	"	"	"			0.4 V
			29						"	"	"	"	"	"	"	"	"	"	"	"			
			30						"	"	"	"	"	"	"	"	"	"	"	"			
	I_{IL1}		31						"	"	"	"	"	"	"	"	"	"	0.4 V	"			
			32						"	"	"	"	"	"	"	"	"	"	0.8 V	0.4 V			
			33						"	"	"	"	"	"	"	"	"	"	"	0.8 V			
			34						"	"	"	"	"	"	"	"	"	"	"	"			
			35						"	"	"	"	"	"	"	"	"	"	"	"			
			36						0.4 V	"	"	"	"	"	"	"	"	"	"	"			
	I_{ZH}		37						4.9 V	"	"	"	"	"	"	"	"	"	"	"			
			38						"	"	"	"	"	"	"	"	"	"	"	"			
			39						"	"	"	"	"	"	"	"	"	"	"	"			
			40						"	"	"	"	"	"	"	"	"	"	"	"			
			41						"	"	"	"	"	"	"	"	"	"	"	"			
			42						"	"	"	"	"	"	"	"	"	"	"	"			
			43						"	"	"	"	"	"	"	"	"	"	"	"			
			44						"	"	"	"	"	"	"	"	"	"	"	"			
			45						"	"	"	"	"	"	"	"	"	"	"	"			
			46						"	"	"	"	"	"	"	"	"	"	"	"			
			47						"	"	"	"	"	"	"	"	"	"	"	"			
			48	2.4 V					"	"	"	"	"	"	"	"	"	"	"	"			
			49		2.4 V				"	"	"	"	"	"	"	"	"	"	"	"			
			50			2.4 V			"	"	"	"	"	"	"	"	"	"	"	"			
			51				2.4 V		"	"	"	"	"	"	"	"	"	"	"	"			
			52					2.4 V	"	"	"	"	"	"	"	"	"	"	"	"			

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	$\overline{RD}$	$\overline{WR}$	$\overline{BUSAK}$	$\overline{WAIT}$	$\overline{BUSRQ}$	$\overline{RESET}$	$\overline{MI}$	$\overline{RFSH}$	GND	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}				
1				0.8 V	0.8 V	0.8 V			GND												V_{CC}		35	mA
2				0.8 V	0.8 V	0.8 V			GND												V_{CC}		100	µA
3				"	"	"			"	0.4 V											A_0	-10	10	µA
4				"	"	"			"		0.4 V										A_1	"	"	"
5				"	"	"			"			0.4 V									A_2	"	"	"
6				"	"	"			"				0.4 V								A_3	"	"	"
7				"	"	"			"					0.4 V							A_4	"	"	"
8				"	"	"			"						0.4 V						A_5	"	"	"
9				"	"	"			"							0.4 V					A_6	"	"	"
10				"	"	"			"								0.4 V				A_7	"	"	"
11				"	"	"			"									0.4 V			A_8	"	"	"
12				"	"	"			"										0.4 V		A_9	"	"	"
13				"	"	"			"											0.4 V	A_{10}	"	"	"
14				"	"	"			"												A_{11}	"	"	"
15				"	"	"			"												A_{12}	"	"	"
16				"	"	"			"												A_{13}	"	"	"
17				"	"	"			"												A_{14}	"	"	"
18				"	"	"			"												A_{15}	"	"	"
19				"	"	"			"												D_4	"	"	"
20				"	"	"			"												D_3	"	"	"
21				"	"	"			"												D_5	"	"	"
22				"	"	"			"												D_6	"	"	"
23				"	"	"			"												D_2	"	"	"
24				"	"	"			"												D_7	"	"	"
25				"	"	"			"												D_0	"	"	"
26				"	"	"			"												D_1	"	"	"
27				"	"	"			"												$\overline{MREQ}$	"	"	"
28				"	"	"			"												$\overline{IORQ}$	"	"	"
29	0.4 V			"	"	"			"												$\overline{RD}$	"	"	"
30		0.4 V		"	"	"			"												$\overline{WR}$	"	"	"
31				"	"	"			"												$\overline{INT}$	"	"	"
32				"	"	"			"												$\overline{NMI}$	"	"	"
33				"	0.4 V	"			"												$\overline{BUSRQ}$	"	"	"
34				"	0.8 V	0.4 V			"												$\overline{RESET}$	"	"	"
35				0.4 V	"	0.8 V			"												$\overline{WAIT}$	"	"	"
36				0.8 V	"	"			"												C	"	"	"
37				"	"	"			"	2.4 V											A_0	"	"	"
38				"	"	"			"		2.4 V										A_1	"	"	"
39				"	"	"			"			2.4 V									A_2	"	"	"
40				"	"	"			"				2.4 V								A_3	"	"	"
41				"	"	"			"					2.4 V							A_4	"	"	"
42				"	"	"			"						2.4 V						A_5	"	"	"
43				"	"	"			"							2.4 V					A_6	"	"	"
44				"	"	"			"								2.4 V				A_7	"	"	"
45				"	"	"			"									2.4 V			A_8	"	"	"
46				"	"	"			"										2.4 V		A_9	"	"	"
47				"	"	"			"											2.4 V	A_{10}	"	"	"
48				"	"	"			"												A_{11}	"	"	"
49				"	"	"			"												A_{12}	"	"	"
50				"	"	"			"												A_{13}	"	"	"
51				"	"	"			"												A_{14}	"	"	"
52				"	"	"			"												A_{15}	"	"	"

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Subgroup	Symbol	MIL-STD-883	Case Q Test no.	1 A_{11}	2 A_{12}	3 A_{13}	4 A_{14}	5 A_{15}	6 C	7 D_4	8 D_3	9 D_5	10 D_6	11 V_{CC}	12 D_2	13 D_7	14 D_0	15 D_1	16 $\overline{INT}$	17 $\overline{NMI}$	18 $\overline{HALT}$	19 $\overline{MREQ}$	20 $\overline{IORQ}$
1 T_C=+25°C	I_{IH2}		53						4.9 V	2.4 V	0.8 V	0.8 V	0.8 V	5.5 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V			
			54						"	0.8 V	2.4 V	"	"	"	"	"	"	"	"	"			
			55						"	"	0.8 V	2.4 V	"	"	"	"	"	"	"	"			
			56						"	"	"	0.8 V	2.4 V	"	"	"	"	"	"	"			
			57						"	"	"	"	0.8 V	"	2.4 V	"	"	"	"	"			
			58						"	"	"	"	"	"	0.8 V	2.4 V	"	"	"	"			
			59						"	"	"	"	"	"	"	0.8 V	2.4 V	"	"	"			
			60						"	"	"	"	"	"	"	0.8 V	0.8 V	2.4 V	"	"			
	I_{ZH}		61						4.9 V	0.8 V	0.8 V	0.8 V	0.8 V	5.5 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V		2.4 V	
			62						"	"	"	"	"	"	"	"	"	"	"	"			2.4 V
			63						"	"	"	"	"	"	"	"	"	"	"	"			
			64						"	"	"	"	"	"	"	"	"	"	"	"			
	I_{IH1}		65						"	"	"	"	"	"	"	"	"	"	2.4 V	"			
			66						"	"	"	"	"	"	"	"	"	"	0.8 V	2.4 V			
			67						"	"	"	"	"	"	"	"	"	"	"	0.8 V			
			68						"	"	"	"	"	"	"	"	"	"	"	"			
			69						"	"	"	"	"	"	"	"	"	"	"	"			
			70						2.4 V	"	"	"	"	"	"	"	"	"	"	"			
	V_{OH1}	3006	71						3.9 V					4.5 V					2.2 V	2.2 V			
			72						"					"					"	"			
			73						"					"					"	"			
			74						"					"					"	"			
			75						"					"					"	"			
			76						"					"					"	"			
			77						"					"					"	"			
			78						"					"					"	"			
			79						"					"					"	"			
			80						"					"					"	"			
			81						"					"					"	"			
			82	1.6 mA					"					"					"	"			
			83		1.6 mA				"					"					"	"			
			84			1.6 mA			"					"					"	"			
			85				1.6 mA		"					"					"	"			
			86					1.6 mA	"					"					"	"			
			87						"	1.6 mA				"					"	"			
			88						"		-250 μA			"					"	"			
			89						"					"					"	"			
			90						"				1.6 mA	"					"	"			
			91						"					"	1.6 mA				"	"			
			92						"					"					"	"			
			93						"					"		1.6 mA			"	"			
			94						"					"				1.6 mA	"	"			
			95						"					"					"	"		1.6 mA	
			96						"					"					"	"			1.6 mA
			97						"					"					"	"			
			98						"					"					"	"			
			99						"					"					"	"			
			100						"					"					"	"	1.6 mA		
			101						"					"					"	"			
			102						"					"					"	"			

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	$\overline{RD}$	$\overline{WR}$	$\overline{BUSAK}$	$\overline{WAIT}$	$\overline{BUSRQ}$	$\overline{RESET}$	$\overline{MI}$	$\overline{RFSH}$	GND	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}				
53				0.8 V	0.8 V	0.8 V			GND												D_4	-10	10	μA
54				"	"	"			"												D_3	"	"	"
55				"	"	"			"												D_5	"	"	"
56				"	"	"			"												D_6	"	"	"
57				"	"	"			"												D_2	"	"	"
58				"	"	"			"												D_7	"	"	"
59				"	"	"			"												D_0	"	"	"
60				"	"	"			"												D_1	"	"	"
61				0.8 V	0.8 V	0.8 V			GND												$\overline{MREQ}$	-10	10	μA
62				"	"	"			"												$\overline{IORQ}$	"	"	"
63	2.4 V			"	"	"			"												$\overline{RD}$	"	"	"
64		2.4 V		"	"	"			"												$\overline{WR}$	"	"	"
65				"	"	"			"												$\overline{INT}$	"	"	"
66				"	"	"			"												$\overline{NMI}$	"	"	"
67				"	2.4 V	"			"												$\overline{BUSRQ}$	"	"	"
68				"	0.8 V	2.4 V			"												$\overline{RESET}$	"	"	"
69				2.4 V	"	0.8 V			"												$\overline{WAIT}$	"	"	"
70				0.8 V	"	0.8 V			"												C	"	"	"
71				2.2 V	2.2 V	2.2 V			"	1.6 mA											A_0	2.4		V
72				"	"	"			"		1.6 mA										A_1	"		"
73				"	"	"			"			1.6 mA									A_2	"		"
74				"	"	"			"				1.6 mA								A_3	"		"
75				"	"	"			"					1.6 mA							A_4	"		"
76				"	"	"			"						1.6 mA						A_5	"		"
77				"	"	"			"							1.6 mA					A_6	"		"
78				"	"	"			"								1.6 mA				A_7	"		"
79				"	"	"			"									1.6 mA			A_8	"		"
80				"	"	"			"										1.6 mA		A_9	"		"
81				"	"	"			"											1.6 mA	A_{10}	"		"
82				"	"	"			"												A_{11}	"		"
83				"	"	"			"												A_{12}	"		"
84				"	"	"			"												A_{13}	"		"
85				"	"	"			"												A_{14}	"		"
86				"	"	"			"												A_{15}	"		"
87				"	"	"			"												D_4	"		"
88				"	"	"			"												D_3	"		"
89				"	"	"			"												D_5	"		"
90				"	"	"			"												D_6	"		"
91				"	"	"			"												D_2	"		"
92				"	"	"			"												D_7	"		"
93				"	"	"			"												D_0	"		"
94				"	"	"			"												D_1	"		"
95				"	"	"			"												$\overline{MREQ}$	"		"
96				"	"	"			"												$\overline{IORQ}$	"		"
97	1.6 mA			"	"	"			"												$\overline{RD}$	"		"
98		1.6 mA		"	"	"			"												$\overline{WR}$	"		"
99				"	"	"	1.6 mA		"												$\overline{MI}$	"		"
100				"	"	"		1.6 mA	"												$\overline{RFSH}$	"		"
101				"	"	"			"												$\overline{HALT}$	"		"
102			1.6 mA	"	"	"			"												$\overline{BUSAK}$	"		"

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case Q Test no.	1 A_{11}	2 A_{12}	3 A_{13}	4 A_{14}	5 A_{15}	6 C	7 D_4	8 D_3	9 D_5	10 D_6	11 V_{CC}	12 D_2	13 D_7	14 D_0	15 D_1	16 $\overline{INT}$	17 $\overline{NMI}$	18 $\overline{HALT}$	19 $\overline{MREQ}$	20 $\overline{IORQ}$
1 $T_C=+25°C$	V_{OH2}	3006	103						3.9 V					4.5 V					2.2 V	2.2 V			
			104						"					"					"	"			
			105						"					"					"	"			
			106						"					"					"	"			
			107						"					"					"	"			
			108						"					"					"	"			
			109						"					"					"	"			
			110						"					"					"	"			
			111						"					"					"	"			
			112						"					"					"	"			
			113						"					"					"	"			
			114	-250 μA					"					"					"	"			
			115		-250 μA				"					"					"	"			
			116			-250 μA			"					"					"	"			
			117				-250 μA		"					"					"	"			
			118					-250 μA	"					"					"	"			
			119						"	-250 μA				"					"	"			
			120						"		-250μA			"					"	"			
			121						"					"					"	"			
			122						"				-250 μA	"					"	"			
			123						"					"	-250 μA				"	"			
			124						"					"		-250 μA			"	"			
			125						"					"			-250 μA		"	"			
			126						"					"				-250 μA	"	"			
			127						"					"					"	"		-250 μA	
			128						"					"					"	"			-250 μA
			129						"					"					"	"			
			130						"					"					"	"			
			131						"					"					"	"			
			132						"					"					"	"			
			133						"					"					"	"	-250 μA		
			134						"					"					"	"			
	V_{OL}	3007	135						"					"					"	"			
			136						"					"					"	"			
			137						"					"					"	"			
			138						"					"					"	"			
			139						"					"					"	"			
			140						"					"					"	"			
			141						"					"					"	"			
			142						"					"					"	"			
			143						"					"					"	"			
			144						"					"					"	"			
			145						"					"					"	"			
			146	1.8 mA					"					"					"	"			
			147		1.8 mA				"					"					"	"			
			148			1.8 mA			"					"					"	"			
			149				1.8 mA		"					"					"	"			
			150					1.8 mA	"					"					"	"			
			151						"	1.8 mA				"					"	"			
			152						"		1.8 mA			"					"	"			
			153						"			1.8 mA		"					"	"			

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
	$\overline{RD}$	$\overline{WR}$	$\overline{BUSAK}$	$\overline{WAIT}$	$\overline{BUSRQ}$	$\overline{RESET}$	$\overline{MI}$	$\overline{RFSH}$	GND	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}		Min	Max	
103				2.2 V	2.2 V	2.2 V			"	-250 μA											A_0	V_{CC} -0.8		V
104				"	"	"			"		-250 μA										A_1	"		"
105				"	"	"			"			250 μA									A_2	"		"
106				"	"	"			"				-250 μA								A_3	"		"
107				"	"	"			"					-250 μA							A_4	"		"
108				"	"	"			"						-250 μA						A_5	"		"
109				"	"	"			"							-250 μA					A_6	"		"
110				"	"	"			"								-250 μA				A_7	"		"
111				"	"	"			"									-250 μA			A_8	"		"
112				"	"	"			"										-250 μA		A_9	"		"
113				"	"	"			"											-250 μA	A_{10}	"		"
114				"	"	"			"												A_{11}	"		"
115				"	"	"			"												A_{12}	"		"
116				"	"	"			"												A_{13}	"		"
117				"	"	"			"												A_{14}	"		"
118				"	"	"			"												A_{15}	"		"
119				"	"	"			"												D_4	"		"
120				"	"	"			"												D_3	"		"
121				"	"	"			"												D_5	"		"
122				"	"	"			"												D_6	"		"
123				"	"	"			"												D_2	"		"
124				"	"	"			"												D_7	"		"
125				"	"	"			"												D_0	"		"
126				"	"	"			"												D_1	"		"
127				"	"	"			"												$\overline{MREQ}$	"		"
128				"	"	"			"												$\overline{IORQ}$	"		"
129	-250 μA			"	"	"			"												$\overline{RD}$	"		"
130		-250 μA		"	"	"			"												$\overline{WR}$	"		"
131				"	"	"	-250 μA		"												$\overline{MI}$	"		"
132				"	"	"		-250μA	"												$\overline{RFSH}$	"		"
133				"	"	"			"												$\overline{HALT}$	"		"
134			-250 μA	"	"	"			"												$\overline{BUSAK}$	"		"
135				"	"	"			"	1.8 mA											A_0		0.4	"
136				"	"	"			"		1.8 mA										A_1		"	"
137				"	"	"			"			1.8 mA									A_2		"	"
138				"	"	"			"				1.8 mA								A_3		"	"
139				"	"	"			"					1.8 mA							A_4		"	"
140				"	"	"			"						1.8 mA						A_5		"	"
141				"	"	"			"							1.8 mA					A_6		"	"
142				"	"	"			"								1.8 mA				A_7		"	"
143				"	"	"			"									1.8 mA			A_8		"	"
144				"	"	"			"										1.8 mA		A_9		"	"
145				"	"	"			"											1.8 mA	A_{10}		"	"
146				"	"	"			"												A_{11}		"	"
147				"	"	"			"												A_{12}		"	"
148				"	"	"			"												A_{13}		"	"
149				"	"	"			"												A_{14}		"	"
150				"	"	"			"												A_{15}		"	"
151				"	"	"			"												D_4		"	"
152				"	"	"			"												D_3		"	"
153																					D_5			

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case Q Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	C	D_4	D_3	D_5	D_6	V_{CC}	D_2	D_7	D_0	D_1	$\overline{INT}$	$\overline{NMI}$	$\overline{HALT}$	$\overline{MREQ}$	$\overline{IORQ}$
1 T_C=+25°C	V_{OL}	3007	154						3.9 V				1.8 mA	4.5 V					2.2 V	2.2 V			
			155						"					"	1.8 mA				"	"			
			156						"					"		1.8 mA			"	"			
			157						"					"			1.8 mA		"	"			
			158						"					"				1.8 mA	"	"		1.8 mA	
			159						"					"					"	"			
			160						"					"					"	"			
			161						"					"					"	"			
			162						"					"					"	"			1.8 mA
			163						"					"					"	"			
			164						"					"					"	"			
			165						"					"					"	"	1.8 mA		
			166						"					"					"	"			
2				Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C																			
3				Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C																			
4	C_O	3012	167	1/	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
			168	GND	1/	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			169	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			170	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			171	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_C		172	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_O		173	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"
			174	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"
			175	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"
			176	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"
			177	"	"	"	"	"	"	"	"	"	GND	"	1/	"	"	"	"	"	"	"	"
			178	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"
			179	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"
			180	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"
	C_I		181	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"
			182	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"
	C_O		183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"
			184	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"
			185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/
			186	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND
			187	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			188	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_I		189	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			190	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			191	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_O		192	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			193	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			194	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			195	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			196	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			197	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			198	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			199	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			200	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			201	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			202	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			203	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			204	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	$\overline{RD}$	$\overline{WR}$	$\overline{BUSAK}$	$\overline{WAIT}$	$\overline{BUSRQ}$	$\overline{RESET}$	$\overline{MI}$	$\overline{RFSH}$	GND	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}				
154				2.2 V	2.2 V	2.2 V			GND												D_6		0.4	V
155				"	"	"			"												D_2		"	"
156				"	"	"			"												D_7		"	"
157				"	"	"			"												D_0		"	"
158				"	"	"			"												D_1		"	"
159				"	"	"			"												$\overline{MREQ}$		"	"
160	1.8 mA			"	"	"			"												$\overline{RD}$		"	"
161				"	"	"	1.8 mA		"												$\overline{MI}$		"	"
162				"	"	"		1.8 mA	"												$\overline{RFSH}$		"	"
163				"	"	"			"												$\overline{IORQ}$		"	"
164		1.8 mA		"	"	"			"												$\overline{WR}$		"	"
165			1.8 mA	"	"	"			"												$\overline{BUSAK}$		"	"
166				"	"	"			"												$\overline{HALT}$		"	"
167	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	A_{11}		20	pF
168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_{12}		"	"
169	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_{13}		"	"
170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_{14}		"	"
171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A_{15}		"	"
172	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	C		10	"
173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_4		20	"
174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_3		"	"
175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_5		"	"
176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_6		"	"
177	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_2		"	"
178	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_7		"	"
179	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_6		"	"
180	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D_1		"	"
181	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{INT}$		10	"
182	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{NMI}$		10	"
183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{HALT}$		20	"
184	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MREQ}$		"	"
185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{IORQ}$		"	"
186	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{RD}$		"	"
187	"	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{WR}$		"	"
188	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{BUSRQ}$		"	"
189	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{WAIT}$		10	"
190	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{BUSRQ}$		"	"
191	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{RESET}$		"	"
192	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MI}$		20	"
193	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{RFSH}$		"	"
194	"	"	"	"	"	"	"	GND	"	1/	"	"	"	"	"	"	"	"	"	"	A_0		"	"
195	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	"	A_1		"	"
196	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	"	A_2		"	"
197	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	"	A_3		"	"
198	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	"	A_4		"	"
199	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	"	A_5		"	"
200	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	"	A_6		"	"
201	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	"	A_7		"	"
202	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	"	A_8		"	"
203	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	"	A_9		"	"
204	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	1/	A_{10}		"	"

See footnotes at end of table III.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case Q Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	C	D_4	D_3	D_5	D_6	V_{CC}	D_2	D_7	D_0	D_1	$\overline{INT}$	$\overline{NMI}$	$\overline{HALT}$	$\overline{MREQ}$	$\overline{IORQ}$
7 T_C=+25°C	2/,3/, 4/,5/	3014		See 6.3 (Table VI)																			
8	2/,3/, 4/,5/	3014		Same tests, terminal conditions, and limits as for subgroup 7 except T_C = +125°C and -55°C.																			
9 T_C=25°C	2/,3/, 4/	Fig. 4																					
10 T_C=125°C	2/,3/, 4/	Fig. 4		Same tests, terminal conditions, and limits as for subgroup 9																			
11 T_C=-55°C	2/,3/, 4/	Fig. 4		Same tests, terminal conditions, and limits as for subgroup 9																			

See footnotes at end of table.

TABLE III. Group A inspection (terminal conditions (pins not designated are open)) - Continued.

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
	$\overline{RD}$	$\overline{WR}$	$\overline{BUSAK}$	$\overline{WAIT}$	$\overline{BUSRQ}$	$\overline{RESET}$	$\overline{MI}$	$\overline{RFSH}$	GND	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}		Min	Max	

See footnotes at end of table III.

TABLE III. Group A inspection.

Symbol	Test no.	Terminals	Figure number 3/	Reference number 6/	Subgroup 12 limits +25°C, +125°C 7/ 8/		
					Device type 01		Unit
					Minimum	Maximum	
t_{PLH1} t_{PHL1} 9/	205	ADDRESS	6	6 6		90 90	ns
t_{PLZ1} t_{PHZ1} 9/	206	ADDRESS		44 44		80 80	
t_{PLZ3} t_{PHZ3} 9/	207	DATA OUT		42 42		80 80	
t_{PZL3} t_{PZH3} 9/	208	DATA OUT		53 53		130 130	
t_{PHL5}	209	$\overline{MREQ}$		8		70	
t_{PLH5}	210	$\overline{MREQ}$		12		70	
t_{PLH6}	211	$\overline{MREQ}$		9		70	
t_{PHL7}	212	$\overline{IORQ}$		27		65	
t_{PLH8}	213	$\overline{IORQ}$		28		70	
t_{PHL8}	214	$\overline{IORQ}$		51		70	
t_{PLH7}	215	$\overline{IORQ}$		52		70	
t_{PHL9}	216	$\overline{RD}$		13		80	
t_{PLH10}	217	$\overline{RD}$		14		70	
t_{PLH9}	218	$\overline{RD}$		23		70	

See footnotes at end of table.

TABLE III. Group A inspection - Continued.

Symbol	Test no.	Terminals	Figure number 3/	Reference number 6/	Subgroup 12 limits +25°C, +125°C 7/ 8/		
					Device type 01		Unit
					Minimum	Maximum	
t_{PHL10}	219	$\overline{RD}$	6	24		70	ns
t_{PHL11}	220	$\overline{RD}$		30		70	
t_{PLH11}	221	$\overline{WR}$		32		70	
t_{PHL12}	222	$\overline{WR}$		34		60	
t_{PHL13}	223	$\overline{MI}$		19		80	
t_{PLH13}	224	$\overline{MI}$		20		80	
t_{PHL15}	225	$\overline{RFSH}$		21		110	
t_{PLH15}	226	$\overline{RFSH}$		22		100	
t_{PLH16} t_{PHL16}	227	$\overline{HALT}$		36 36		260 260	
t_{PHL17}	228	$\overline{BUSAK}$		40		90	
t_{PLH18}	229	$\overline{BUSAK}$		41		90	
t_{PHZ4}	230	$\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$		41		90	

See footnotes at end of table.

1/ The capacitance measurement shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measurement instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

2/ Input and output conditions:
   a. For subgroups 7, 8, 9, 10, 11, and 12 tests input conditions A, B, C, and D for all device types appear in table IV.
   b. For subgroups 7, 8, 9, 10, and 11 tests output conditions for all device types appear in table V.

3/ Figure 6 represents the timing diagrams associated with subgroups 7, 8, 9, 10, 11, and 12.

4/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.

5/ The table V functional tests shall be repeated for each input test condition (A-D) of table IV.

6/ The reference number refers to the position where the parameter being measured appears on figure 6.

7/ Subgroup 12 tests are the only test for which an ac data value is actually recorded. Subgroups 7, 8, 9, 10, and 11 are pass/fail tests and shall be checked by an automated tester controlled by the test software represented in table VI using input and output conditions in tables IV and V.

8/ Limits shown for subgroup 12 are from F_{MAX} input conditions A and B of table IV. Limits for F_{MIN} from input conditions C and D of table IV are not shown.

9/ Where propagation delay tests for subgroup 12 indicates a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst delay requires recording. In some cases this will be a minimum reading while for others it will be a maximum reading as indicated in the table.

TABLE IV. Input conditions for device type 01 functional tests.

Symbol 1/	Reference 2/	Input conditions					
		Terminal	A 3/	B 3/	C 3/	D 3/	Unit
V_{CC}		V_{CC}	5.5	4.5	4.5	4.5	V
V_{IH}		Logic inputs	2.2	2.2	2.2	2.2	V
V_{IL}		Logic inputs	0.8	0.8	0.8	0.8	V
V_{IH}(CLK)		CLK	4.9	3.9	4.9	3.9	V
V_{IL}(CLK)		CLK	0.45	0.45	0.45	0.45	V
t_{cyc}	1	CLK	165	165	2000	2000	ns
t_{PWL4}	37	$\overline{NMI}$	70	70	70	70	ns
t_{SZH1} t_{SZL1}	15	DATA (IN)	30	30	30	30	ns
t_{SLH1} t_{SHL1}	17	$\overline{WAIT}$	60	60	60	60	ns
t_{SZH2} t_{SZL2}	25	DATA (IN)	40	40	40	40	ns
t_{SLH2} t_{SHL2}	38	$\overline{BUSRQ}$	50	50	50	50	ns
t_{SLH3} t_{SHL3}	46	$\overline{RESET}$	60	60	60	60	ns
t_{SLH4} t_{SHL4}	48	$\overline{INT}$	70	70	70	70	ns
t_{HLZ1} t_{HHZ1}	16	DATA (IN)	0	0	0	0	ns

See footnotes at end of table.

TABLE IV. Input conditions for device type 01 functional tests - Continued.

Symbol 1/	Reference 2/	Input conditions					
		Terminal	A 3/	B 3/	C 3/	D 3/	Unit
t_{HLH1} t_{HHL1}	18	$\overline{WAIT}$	0	0	0	0	ns
t_{HLH2} t_{HHL2}	39	$\overline{BUSRQ}$	0	0	0	0	ns
t_{HLH3} t_{HHL3}	47	$\overline{RESET}$	0	0	0	0	ns
t_{HLH4} t_{HHL4}	49	$\overline{INT}$	0	0	0	0	ns

1/ Clock input rise and fall times shall be as 20 ns maximum.

2/ The reference number refers to the position where the parameter being measured appears on figure 8.

3/ Input conditions A and B are at F_{MAX}, input conditions C and D are at F_{MIN}.

TABLE V. Output conditions for device type 01 functional tests.

Symbol 1/	Reference 2/	Terminal(s)	Test limits 3/		Unit
			Min	Max	
V_{OL}		All outputs		0.8	V
V_{OH}		All outputs	2.4		V
t_{PLH1} t_{PHL1}	6	ADDRESS		90	ns
t_{PHL5}	8	MREQ		70	ns
t_{PLH5}	12	MREQ		70	ns
t_{PLH6}	9	MREQ		70	ns
t_{PHL7}	27	IORQ		65	ns
t_{PLH7}	52	IORQ		70	ns
t_{PLH8}	28	IORQ		70	ns
t_{PHL8}	51	IORQ		70	ns
t_{PLH9}	23	RD		70	ns
t_{PHL9}	13	RD		80	ns
t_{PLH10}	14	RD		70	ns
t_{PHL10}	24	RD		70	ns
t_{PLH11}	32	WR		70	ns
t_{PHL11}	30	WR		70	ns
t_{PHL12}	34	WR		60	ns

See footnotes at end of table.

TABLE V. Output conditions for device type 01 functional tests - Continued.

Symbol 1/	Reference 2/	Terminal(s)	Test limits 3/		Unit
			Min	Max	
t_{PLH13}	20	M1		80	ns
t_{PHL13}	19	M1		80	ns
t_{PHL15}	21	RFSH		110	ns
t_{PLH15}	22	RFSH		100	ns
t_{PLH16} t_{PHL16}	36	HALT		260	ns
t_{PHL17}	40	BUSAX		90	ns
t_{PLH18}	41	BUSAX		90	ns

1/ Clock input rise and fall times shall be as 20 ns maximum.

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ Output conditions for all device types are constant for both F_{MAX} and F_{MIN}.

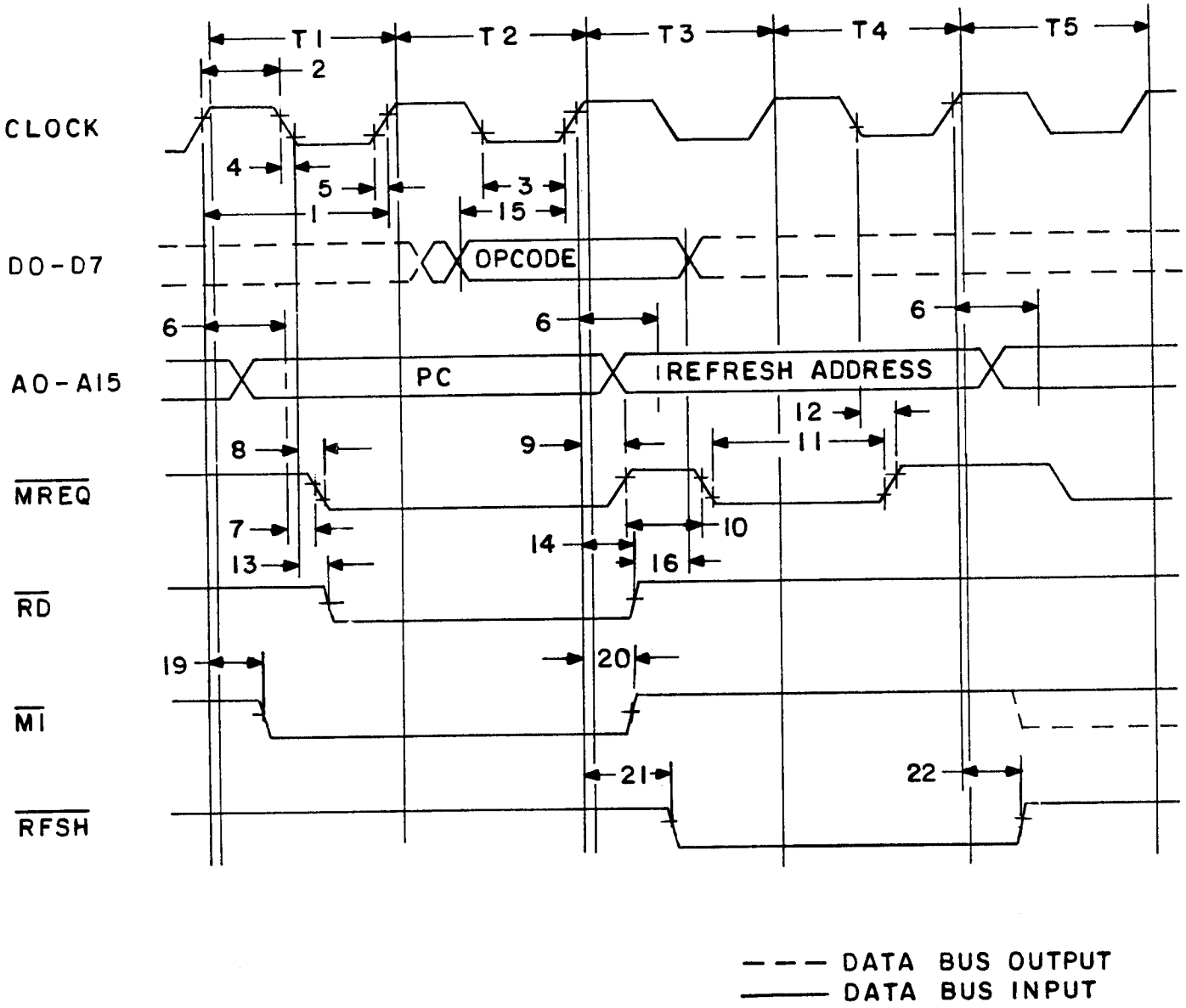


FIGURE 6. Timing diagram (instruction opcode fetch (M1 cycle)).

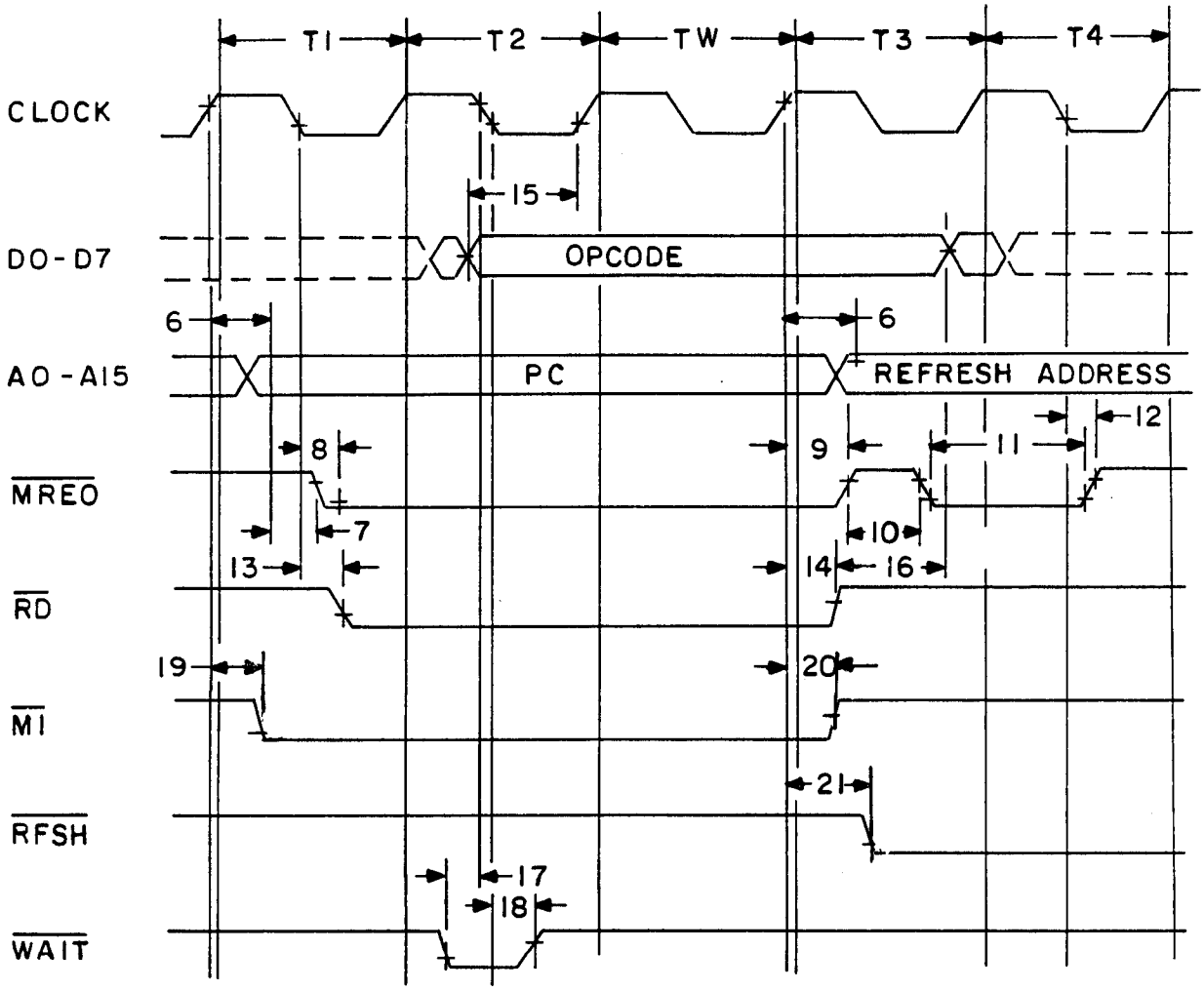


FIGURE 6. Timing diagram (instruction opcode fetch w/wait (s)) - Continued.

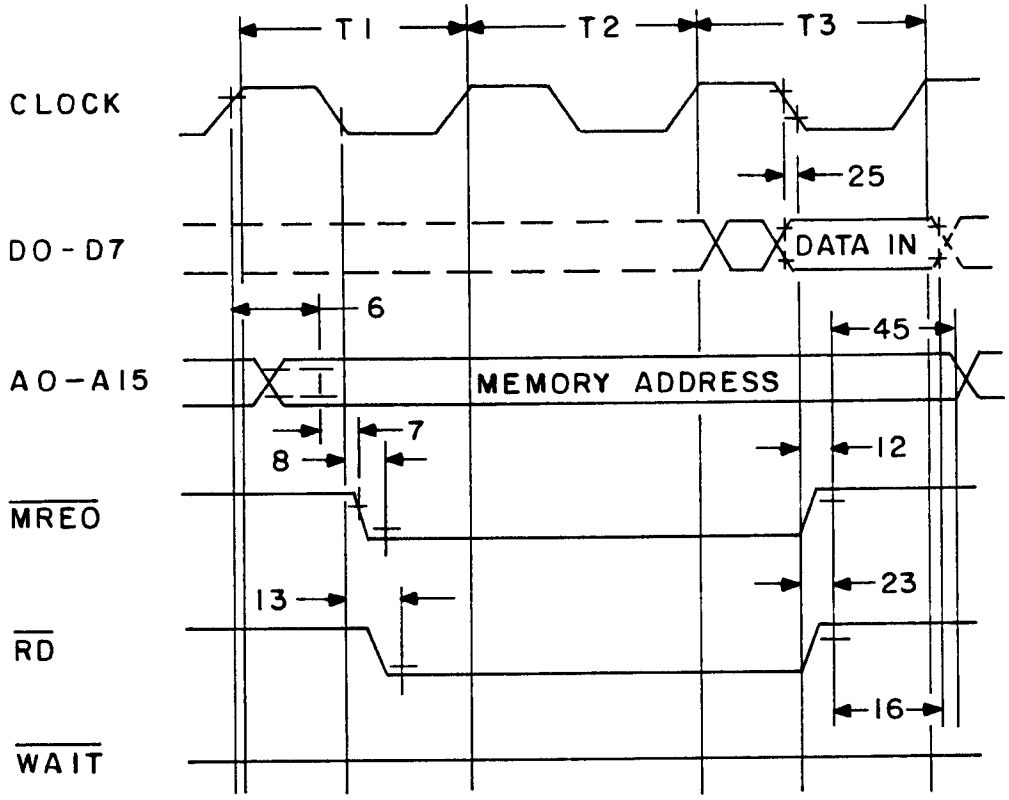


FIGURE 6. Timing diagram (memory read cycle) - Continued.

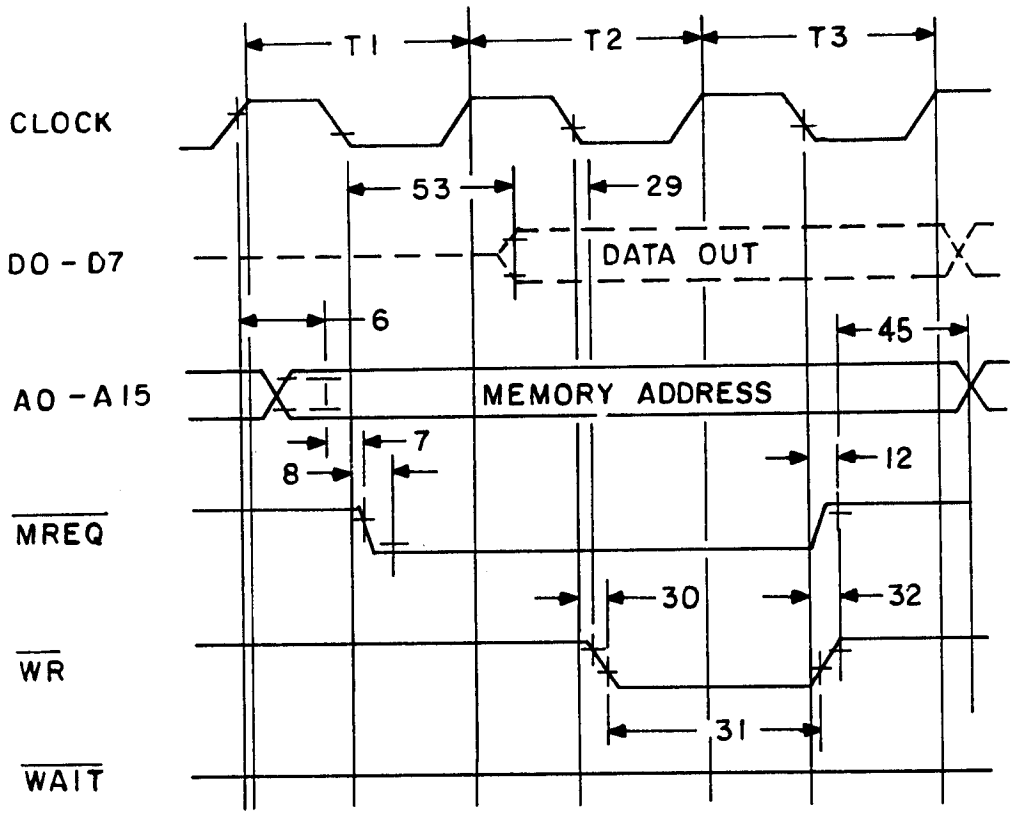


FIGURE 6. Timing diagram (memory write cycle) - Continued.

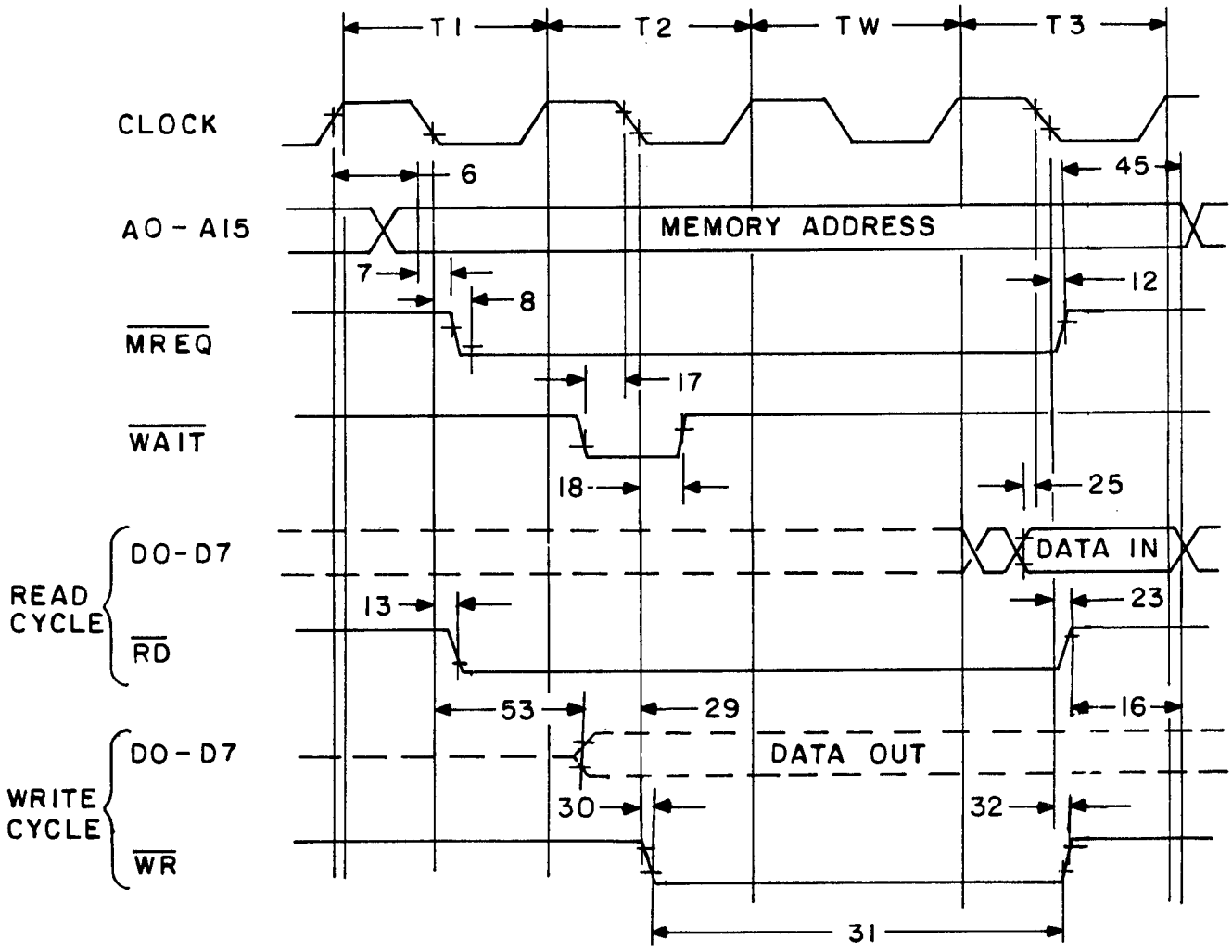
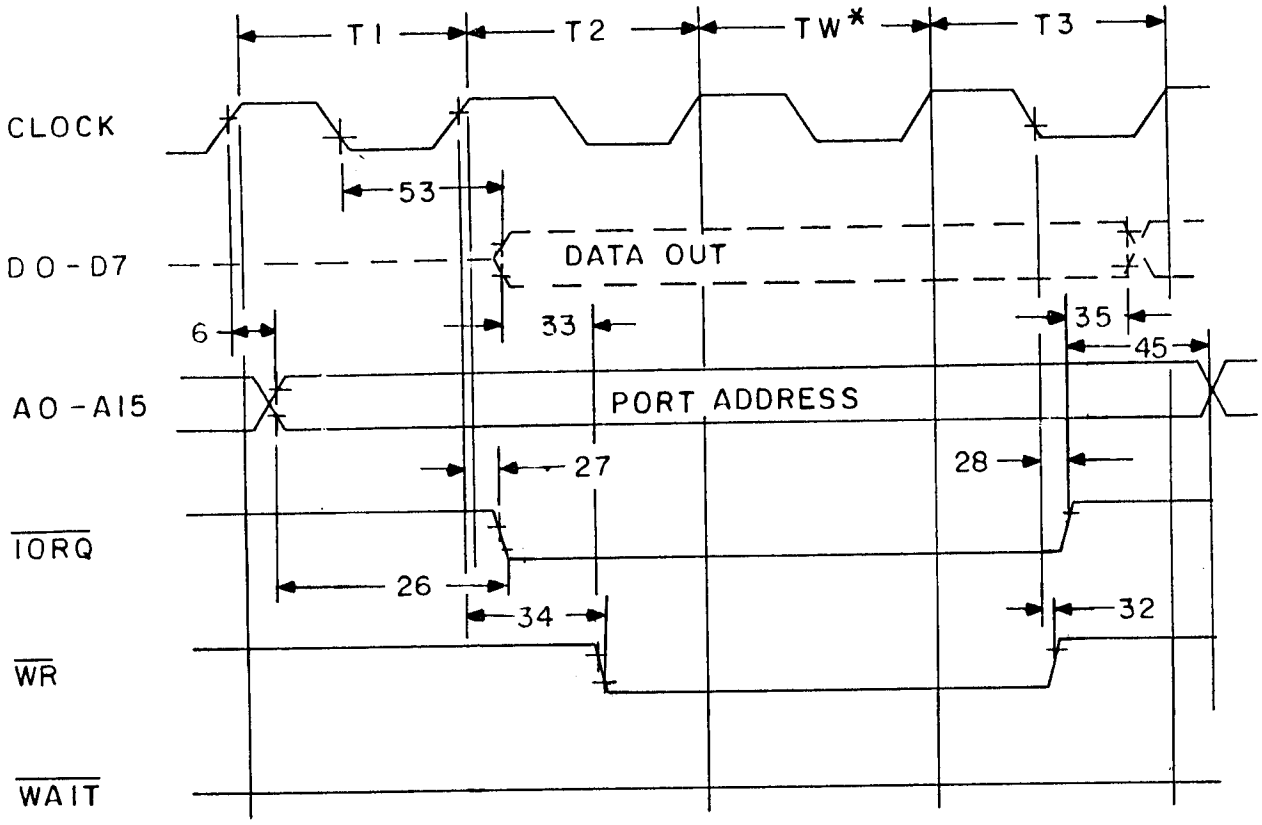
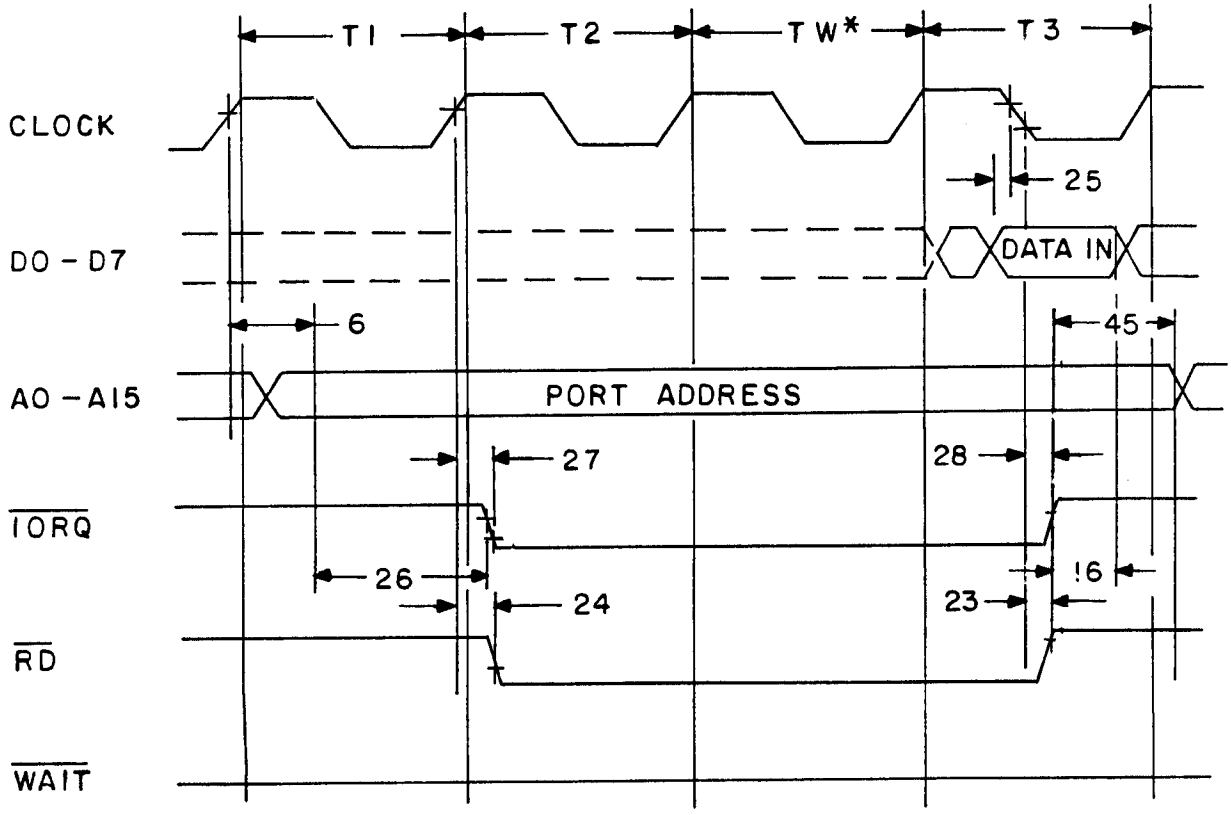


FIGURE 6. Timing diagram (memory read/write cycles w/wait (s)) - Continued.



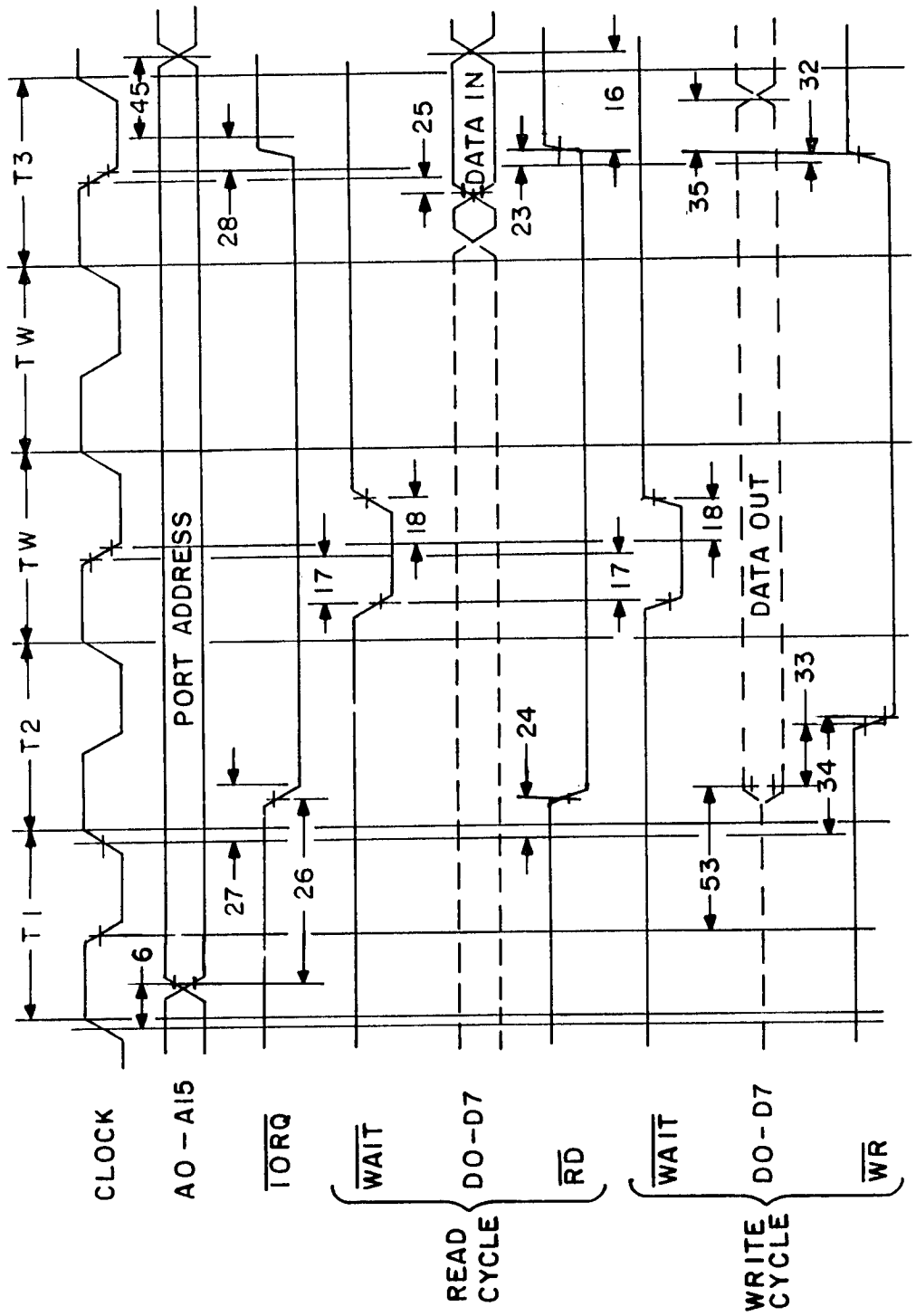
*TW AUTOMATICALLY INSERTED WAIT STATE BY CPU

FIGURE 6. Timing diagram (I/O write cycle) - Continued.



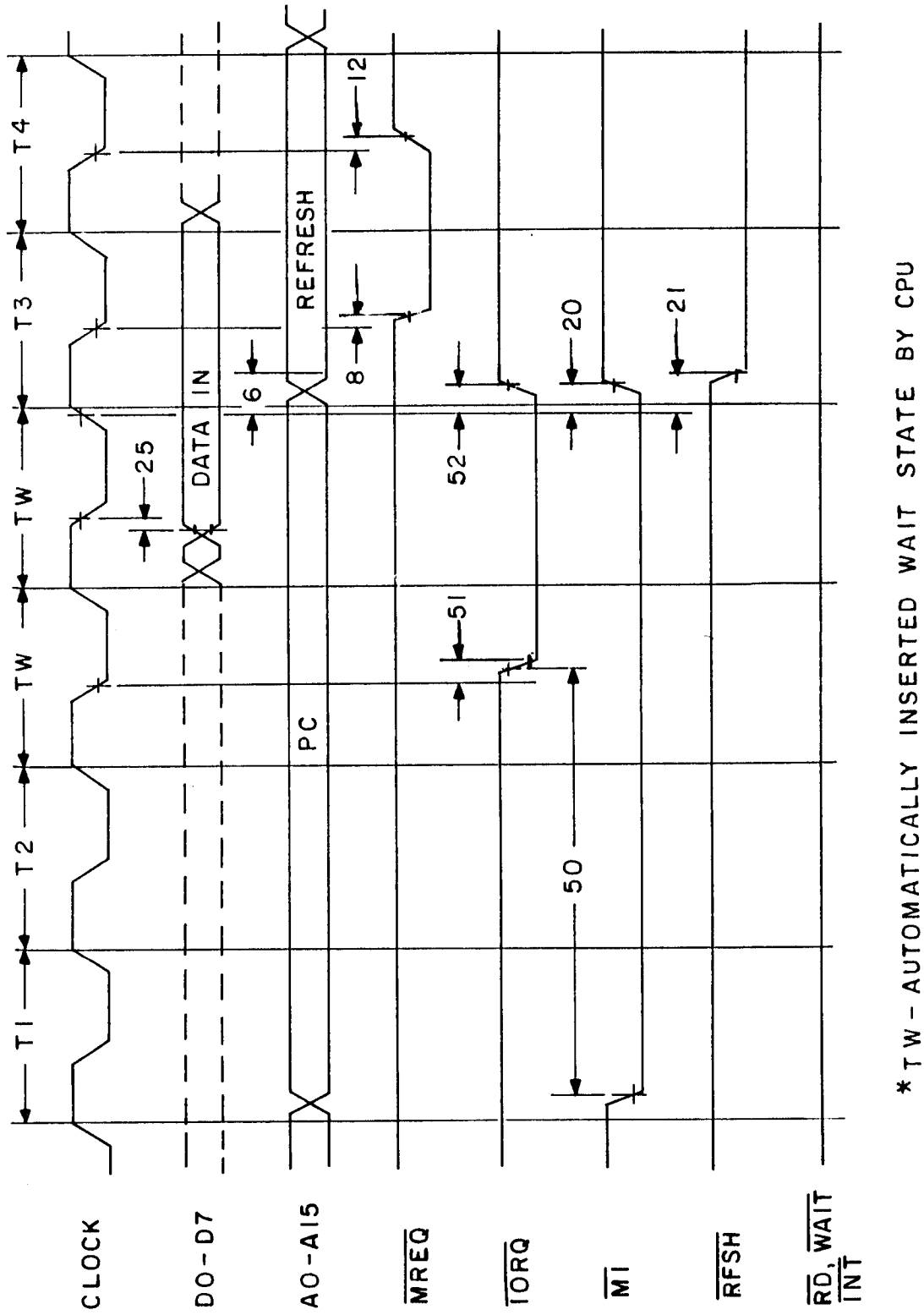
*TW - AUTOMATICALLY INSERTED WAIT STATE BY CPU

FIGURE 6. Timing diagram (I/O read cycle) - Continued.



* TW - AUTOMATICALLY INSERTED WAIT STATE BY CPU

FIGURE 6. Timing diagram (I/O read/write/ w/wait (s)) - Continued.



1. Basic timing cycles with wait states expand in multiples of T_{C3}.

FIGURE 6. Timing diagram (interrupt acknowledge cycle) - Continued.

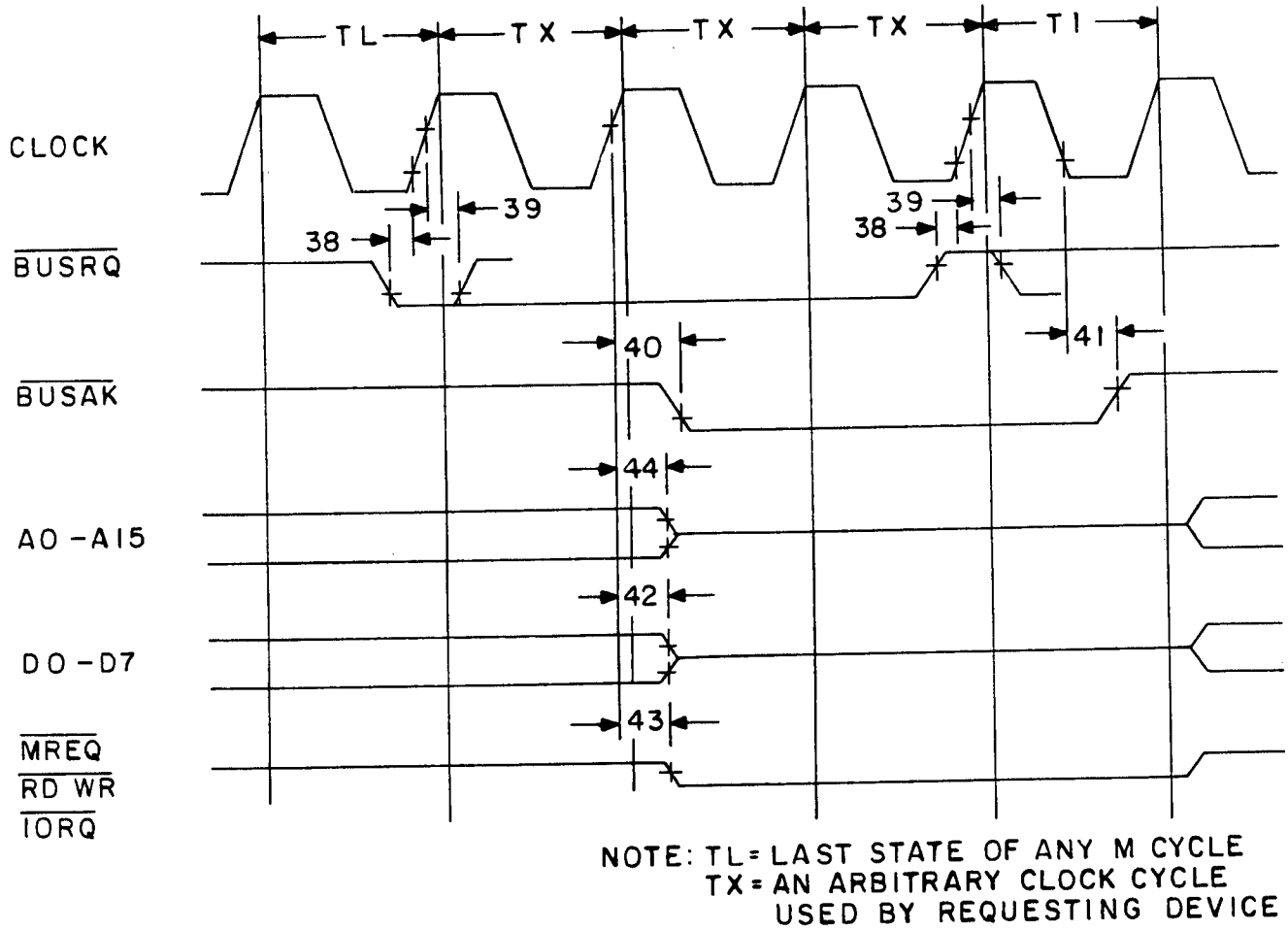


FIGURE 6. Output timing diagram (BUS REQUEST/ACKNOWLEDGE) cycle - Continued.

TABLE VI. Test vectors.

Table VI, not printed herein, is a computer listing for use with table III. Each vector identifies activity states by pin function. See 6.3 for information on obtaining the complete table in a compatible output format.

TABLE VII. Delta limits at 25°C.

Parameter 1/	Device types
	All
I_{DD}	25 mA
I_{IL1}	1 μA
I_{IH1}	1 μA
I_{ZL}	1 μA
I_{ZH}	1 μA
I_{IL2}	1 μA
I_{IH2}	1 μA

1/ The above parameters shall be recorded before and after the required life tests to determine delta (Δ) limits.

TABLE VIII. CPU instruction set for all device types.

OBJ CODE	SOURCE STATEMENT		OPERATION
8E	ADC	A,(HL)	Add with Carry Oper. and to Acc.
DD8E05	ADC	A,(1X+d)	
FD8E05	ADC	A,(1Y+d)	
8F	ADC	A,A	
88	ADC	A,B	
89	ADC	A,C	
8A	ADC	A,D	
8B	ADC	A,E	
8C	ADC	A,H	
8D	ADC	A,L	
CE20	ADC	A,n	
ED4A	ADC	HL,BC	Add with Carry Reg. Pair to HL
ED5A	ADC	HL,DE	
ED6A	ADC	HL,HL	
ED7A	ADC	HL,SP	
86	ADD	A,(HL)	Add Operand to Acc.
DD8605	ADD	A,(1X+d)	
FD8605	ADD	A,(1Y+d)	
87	ADD	A,A	
80	ADD	A,B	
81	ADD	A,C	
82	ADD	A,D	
83	ADD	A,E	
84	ADD	A,H	
85	ADD	A,L	
CE20	ADD	A,n	
09	ADD	HL,BC	Add Reg. Pair to HL
19	ADD	HL,DE	
29	ADD	HL,HL	
39	ADD	HL,SP	
DD09	ADD	1X,BC	Add Reg. Pair to IX
DD19	ADD	1X,DE	
DD29	ADD	1X,1X	
DD39	ADD	1X,SP	
FD09	ADD	1Y,BC	Add Reg. Pair to IY
FD19	ADD	1Y,DE	
FD29	ADD	1Y,1Y	
FD39	ADD	1Y,SP	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
A6	AND	(HL)	Logical "AND" of Operand and Acc.
DDA605	AND	(1X+d)	
FDA605	AND	(1Y+d)	
A7	AND	A	
A0	AND	B	
A1	AND	C	
A2	AND	D	
A3	AND	E	
A4	AND	H	
A5	AND	L	
E620	AND	n	
CB46	BIT	0,(HL)	Test Bit b of Location or Reg.
DDCB0546	BIT	0,(1X+d)	
FDCB0546	BIT	0,(1Y+d)	
CB47	BIT	0,A	
CB40	BIT	0,B	
CB41	BIT	0,C	
CB42	BIT	0,D	
CB43	BIT	0,E	
CB44	BIT	0,H	
CB45	BIT	0,L	Test Bit b of Location or Reg.
CB4E	BIT	1,(HL)	
DDCB054E	BIT	1,(1X+d)	
FDCB054E	BIT	1,(1Y+d)	
CB4F	BIT	1,A	
CB48	BIT	1,B	
CB49	BIT	1,C	
CB4A	BIT	1,D	
CB4B	BIT	1,E	
CB4C	BIT	1,H	
CB4D	BIT	1,L	
CB56	BIT	2,(HL)	
DDCB0556	BIT	2,(1X+d)	
FDCB0556	BIT	2,(1Y+d)	
CB57	BIT	2,A	
CB50	BIT	2,B	
CB51	BIT	2,C	
CB52	BIT	2,D	
CB53	BIT	2,E	
CB54	BIT	2,H	
CB55	BIT	2,L	
CB5E	BIT	3,(HL)	
DDCB055E	BIT	3,(1X+d)	
FDCB055E	BIT	3,(1Y+d)	
CB5F	BIT	3,A	
CB58	BIT	3,B	
CB59	BIT	3,C	
CB5A	BIT	3,D	
CB5B	BIT	3,E	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
CB5C	BIT	3,H	Test Bit b of Location or Reg.
CB5D	BIT	3,L	
CB66	BIT	4,(HL)	
DDCB0566	BIT	4,(1X+d)	
FDCB0566	BIT	4,(1Y+d)	
CB67	BIT	4,A	
CB60	BIT	4,B	
CB61	BIT	4,C	
CB62	BIT	4,D	
CB63	BIT	4,E	
CB64	BIT	4,H	
CB65	BIT	4,L	
CB6E	BIT	5,(HL)	
DDCB056E	BIT	5,(1X+d)	
FDCB056E	BIT	5,(1Y+d)	
CB6F	BIT	5,A	
CB68	BIT	5,B	
CB69	BIT	5,C	
CB6A	BIT	5,D	
CB6B	BIT	5,E	
CB6C	BIT	5,H	
CB6D	BIT	5,L	
CB76	BIT	6,(HL)	
DDCB0576	BIT	6,(1X+d)	
FDCB0576	BIT	6,(1Y+d)	
CB77	BIT	6,A	
CB70	BIT	6,B	
CB71	BIT	6,C	
CB72	BIT	6,D	
CB73	BIT	6,E	
CB74	BIT	6,H	
CB75	BIT	6,L	
CB7E	BIT	7,(HL)	
DDCB057E	BIT	7,(1X+d)	
FDCB057E	BIT	7,(1Y+d)	
CB7F	BIT	7,A	
CB78	BIT	7,B	
CB79	BIT	7,C	
CB7A	BIT	7,D	
CB7B	BIT	7,E	
CB7C	BIT	7,H	
CB7D	BIT	7,L	
DC8405	CALL	C,nn	Call Subroutine at Location nn if Condition True
FC8405	CALL	M,nn	
D48405	CALL	NC,nn	
C48405	CALL	NZ,nn	
F48405	CALL	P,nn	
EC8405	CALL	PE,nn	
E48405	CALL	PO,nn	
CC8405	CALL	Z,nn	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
CD8405	CALL	nn	Unconditional Call to Subroutine at nn
3F	CCF		Complement Carry Flag
BE	CP	(HL)	Compare Operand with Acc.
DDBE05	CP	(1X+d)	
FDBE05	CP	(1Y+d)	
BF	CP	A	
B8	CP	B	
B9	CP	C	
BA	CP	D	
BB	CP	E	
BC	CP	H	
BD	CP	L	
FE20	CP	n	
EDA9	CPD		Compare Location (HL) and ACC. Decrement HL and BC
EDB9	CPDR		Compare Location (HL) and ACC. Decrement HL and BC. Repeat until BC = 0
EDA1	CP1		Compare Location (HL) and ACC. Increment HL and Decrement BC
EDB1	CP1R		Compare Location (HL) and ACC Increment HL. Decrement BC. Repeat until BC = 0
2F	CPL		Complement Acc (1's Comp)
27	DAA		Decimal Adjust Acc

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
35	DEC	(HL)	Decrement Operand
DD3505	DEC	(1X+d)	
FD3505	DEC	(1Y+d)	
3D	DEC	A	
05	DEC	B	
0B	DEC	BC	
0D	DEC	C	
15	DEC	D	
1B	DEC	DE	
1D	DEC	E	
25	DEC	H	
2B	DEC	HL	
DD2B	DEC	1X	
FD2B	DEC	1Y	
2D	DEC	L	
3B	DEC	SP	
F3	D1		Disable Interrupts
102E	DJNZ	e	Decrement B and Jump Relative if B = 0
FB	E1		Enable Interrupts
E3	EX	(SP),HL	Exchange Location and (SP)
DDE3	EX	(SP),1X	
FDE3	EX	(SP),1Y	
08	EX	AF,AF	Exchange the Contents of AF and AF
EB	EX	DE,HL	Exchange the Contents of DE and HL
D9	EXX		Exchange the Contents of BC, DE, HL with Contents of BC, DE, HL Respectively
76	HALT		HALT (Wait for Interrupt or Reset)
ED46	1M	0	Set Interrupt Mode
ED56	1M	1	
ED5E	1M	2	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE		SOURCE STATEMENT	OPERATION
ED78	1N	A,(C)	Load Reg with Input from Device (C)
ED40	1N	B,(C)	
ED48	1N	C,(C)	
ED50	1N	D,(C)	
ED58	1N	E,(C)	
ED60	1N	H,(C)	
ED68	1N	L,(C)	
34	1NC	(HL)	Increment Operand
DD3405	1NC	(1X+d)	
FD3405	1NC	(1Y+d)	
3C	1NC	A	
04	1NC	B	
03	1NC	BC	
0C	1NC	C	
14	1NC	D	
13	1NC	DE	
1C	1NC	E	
24	1NC	H	
23	1NC	HL	
DD23	1NC	1X	
FD23	1NC	1Y	
2C	1NC	L	
33	1NC	SP	
DB20	1N	A,(n)	Load Acc with Input from Device n
EDAA	1ND		Load location (HL) with Input from Port (C), Decrement HL and B
EDBA	1NDR		Load location (HL) with Input from Port (C), Decrement HL and Decrement B Repeat until B = 0
EDA2	1ND1		Load location (HL) with Input from Port (C), Increment HL and Decrement B
EDB2	1ND1R		Load location (HL) with Input from Port (C), Increment HL and Decrement B Repeat until B = 0

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
C38405	JP	nn	Unconditional Jump to Location
E9	JP	(HL)	
DDE9	JP	(1X)	
FDE9	JP	(1Y)	
DA8405	JP	C,nn	Jump to Location if Condition True
FA8405	JP	M,nn	
D28405	JP	NC,nn	
C28405	JP	NZ,nn	
F28405	JP	P,nn	
EA8405	JP	PE,nn	
E28405	JP	PO,nn	
CA8405	JP	Z,nn	
382E	JR	C,e	Jump Relative to PC+e if Condition True
302E	JR	NC,e	
202E	JR	NZ,e	
282E	JR	Z,e	
182E	JR	e	Unconditional Jump Relative to PC+e
02	LD	(BC),A	Load Source to Destination
12	LD	(DE),A	
77	LD	(HL),A	
70	LD	(HL),B	
71	LD	(HL),C	
72	LD	(HL),D	
73	LD	(HL),E	
74	LD	(HL),H	
75	LD	(HL),L	
3620	LD	(HL),n	
DD7705	LD	(1X+d),A	
DD7005	LD	(1X+d),B	
DD7105	LD	(1X+d),C	
DD7205	LD	(1X+d),D	
DD7305	LD	(1X+d),E	
DD7405	LD	(1X+d),H	
DD7505	LD	(1X+d),L	
DD360520	LD	(1X+d),n	
FD7705	LD	(1Y+d),A	
FD7005	LD	(1Y+d),B	
FD7105	LD	(1Y+d),C	
FD7205	LD	(1Y+d),D	
FD7305	LD	(1Y+d),E	
FD7405	LD	(1Y+d),H	
FD7505	LD	(1Y+d),L	
FD360520	LD	(1Y+d),n	
38405	LD	(nn),A	
ED438405	LD	(nn),BC	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
ED538405	LD	(nn),DE	Load Source to Destination
228405	LD	(nn),HL	
DD228405	LD	(nn),1X	
FD228405	LD	(nn),1Y	
ED738405	LD	(nn),SP	
0A	LD	A,(BC)	
1A	LD	A,(DE)	
7E	LD	A,(HL)	
DD7E05	LD	A,(1X+d)	
FD7E05	LD	A,(1Y+d)	
3A8405	LD	A,(nn)	
7F	LD	A,A	
78	LD	A,B	
79	LD	A,C	
7A	LD	A,D	
7B	LD	A,E	
7C	LD	A,H	
ED57	LD	A,1	
7D	LD	A,L	
3E20	LD	A,n	
ED5F	LD	A,R	
46	LD	B,(HL)	
DD4605	LD	B,(1X+d)	
FD4605	LD	B,(1Y+d)	
47	LD	B,A	
40	LD	B,B	
41	LD	B,C	
42	LD	B,D	
43	LD	B,E	
44	LD	B,H	
45	LD	B,L	
0620	LD	B,n	
ED4B8405	LD	BC,(nn)	
018405	LD	BC,nn	
4E	LD	C,(HL)	
DD4E05	LD	C,(1X+d)	
FD4E05	LD	C,(1Y+d)	
4F	LD	C,A	
48	LD	C,B	
49	LD	C,C	
4A	LD	C,D	
4B	LD	C,E	
4C	LD	C,H	
4D	LD	C,L	
0E20	LD	C,n	
56	LD	D,(HL)	
DD5605	LD	D,(1X+d)	
FD4E05	LD	D,(1Y+d)	
57	LD	D,A	
50	LD	D,B	
51	LD	D,C	
52	LD	D,D	
53	LD	D,E	
54	LD	D,H	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
55	LD	D,L	Load Source to Destination
1620	LD	D,n	
ED5B8405	LD	DE,(nn)	
118405	LD	D,nn	
5E	LD	E,(HL)	
DD5E05	LD	E,(1X+d)	
FD5E05	LD	E,(1Y+d)	
5F	LD	E,A	
58	LD	E,B	
59	LD	E,C	
5A	LD	E,D	
5B	LD	E,E	
5C	LD	E,H	
5D	LD	E,L	
1E20	LD	E,n	
66	LD	H,(HL)	
DD6605	LD	H,(1X+d)	
FD6605	LD	H,(1Y+d)	
67	LD	H,A	
60	LD	H,B	
61	LD	H,C	
62	LD	H,D	
63	LD	H,E	
64	LD	H,H	
65	LD	H,L	
2620	LD	H,n	
66	LD	H,(HL)	
2A8405	LD	HL,(nn0	
218405	LD	HL,nn	
ED47	LD	1,A	
DD2A8405	LD	1X,(nn)	
DD218405	LD	1X,nn	
FD2A8405	LD	1Y,(nn)	
FD218405	LD	1Y,nn	
6E	LD	L,(HL)	
DD6E05	LD	L,(1X+d)	
FD6E05	LD	L,(1Y+d)	
6F	LD	L,A	
68	LD	L,B	
69	LD	L,C	
6A	LD	L,D	
6B	LD	L,E	
6C	LD	L,H	
6D	LD	L,L	
2E20	LD	L,n	
ED4F	LD	R,A	
ED7B8405	LD	SP,(nn)	
F9	LD	SP,HL	
DDF9	LD	SP,1X	
FDF9	LD	SP,1Y	
318405	LD	SP,nn	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
EDA8	LDD		Load Location, (DE) with Location (HL) Decrement DE, HL and BC
EDBB	LDDR		Load Location (DE) with Location (HL) Repeat until BC = 0
EDA0	LD1		Load Location (DE) with Location (HL) Increment DE, HL, Decrement BC
EDB0	LD1R		Load Location, DE, with Location (HL) Increment DE, HL Decrement BC and Repeat until BC = 0
ED44	NEG		Negate Acc 2's Complement
00	NOP		No Operation
B6	OR	(HL)	Logical "OR" of Operand and Acc
DDB605	OR	(1X+d)	
FDB605	OR	(1Y+d)	Logical "OR" o' Operand and Acc
B7	OR	A	
B0	OR	B	
B1	OR	C	
B2	OR	D	
B3	OR	E	
B4	OR	H	
B5	OR	L	
F620	OR	n	
ED8B	OTDR		Load Output Port (C) with Location (HL) Decrement HL and B, Repeat until B = 0
EDB3	OT1R		Load Output Port (C) with Location (HL) Increment HL, Decrement B, Repeat until B = 0

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
ED79	OUT	(C),A	Load Output Port (C) with Reg.
ED41	OUT	(C),B	
ED49	OUT	(C),C	
ED51	OUT	(C),D	
ED59	OUT	(C),E	
ED61	OUT	(C),H	
ED69	OUT	(C),L	
D320	OUT	(n),A	Load Output Port (n) with Acc.
EDAB	OUTD		Load Output Port (C) with Location (HL), Decrement HL and B
EDA3	OUT1		Load Output Port (C) with Location (HL), Increment HL and Decrement B
F1	POP	AF	Load Destination with Top of Stack
C1	POP	BC	
D1	POP	DE	
E1	POP	HL	
DDE1	POP	IX	
FDE1	POP	IY	
F5	PUSH	AF	Load Source to Stack
C5	PUSH	BC	
D5	PUSH	DE	
E5	PUSH	HL	
DDE5	PUSH	IX	
FDE5	PUSH	IY	
CB86	RES	0,(HL)	Reset Bit b of Operand
DDCB0586	RES	0,(1X+d)	
FDCB0586	RES	0,(1Y+d)	
CB87	RES	0,A	
CB80	RES	0,B	
CB81	RES	0,C	
CB82	RES	0,D	
CB83	RES	0,E	
CB84	RES	0,H	
CB85	RES	0,L	
CB8E	RES	1,(HL)	
DDCB058E	RES	1,(1X+1)	
FDCB058E	RES	1,(1Y+d)	
CB8F	RES	1,A	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
CB88	RES	1,B	Reset Bit b of Operand
CB89	RES	1,C	
CB8A	RES	1,D	
CB8B	RES	1,E	
CB8C	RES	1,H	
CB8D	RES	1,L	
CB96	RES	2,(HL)	
DDCB0596	RES	2,(1X+d)	
FDCB0596	RES	2,(1Y+d)	
CB97	RES	2,A	
CB90	RES	2,B	
CB91	RES	2,C	
CB92	RES	2,D	
CB93	RES	2,E	
CB94	RES	2,H	
CB95	RES	2,L	
CB9E	RES	3,(HL)	
DDCB059E	RES	3,(1X+d)	
FDCB059E	RES	3,(1Y+d)	
CB9F	RES	3,A	
CB98	RES	3,B	
CB99	RES	3,C	
CB9A	RES	3,D	
CB9B	RES	3,E	
CB9C	RES	3,H	
CB9D	RES	3,L	
CBA6	RES	4,(HL)	
DDCB05A6	RES	4,(1X+d)	
FDCB05A6	RES	4,(1Y+d)	
CBA7	RES	4,A	
CBA0	RES	4,B	
CBA1	RES	4,C	
CBA2	RES	4,D	
CBA3	RES	4,E	
CBA4	RES	4,H	
CBA5	RES	4,L	
CBAE	RES	5,(HL)	
DDCB05AE	RES	5,(1X+d)	
FDCB05AE	RES	5,(1Y+d)	
CBAF	RES	5,A	
CBA8	RES	5,B	
CBA9	RES	5,C	
CBAA	RES	5,D	
CBAB	RES	5,E	
CBAC	RES	5,H	
CBAD	RES	5,L	
CBB6	RES	6,(HL)	
DDCB05B6	RES	6,(1X+d)	
FDCB05B6	RES	6,(1Y+d)	
CBB7	RES	6,A	
CBB0	RES	6,B	
CBB1	RES	6,C	
CBB2	RES	6,D	
CBB3	RES	6,E	
CBB4	RES	6,H	
CBB5	RES	6,L	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
CBBE	RES	7,(HL)	Reset Bit b of Operand
DDCB05BE	RES	7,(1X+d)	
FDCB05BE	RES	7,(1Y+d)	
CBBF	RES	7,A	
CBB8	RES	7,B	
CBB9	RES	7,C	
CBBA	RES	7,D	
CBBB	RES	7,E	
CBBC	RES	7,H	
CBBD	RES	7,L	
C9	RET		Return from Subroutine
D8	RET	C	Return from Subroutine if Condition True
F8	RET	M	
D0	RET	NC	
C0	RET	NZ	
F0	RET	P	
E8	RET	PE	
E0	RET	PO	
C8	RET	Z	
ED4D	RET1		Return from Interrupt
ED45	RETN		Return from Non-Maskable Interrupt
CB16	RL	(HL)	Rotate Left Through Carry
DDCB0516	RL	(1X+d)	
FDCB0516	RL	(1Y+d)	
CB17	RL	A	
CB10	RL	B	
CB11	RL	C	
CB12	RL	D	
CB13	RL	E	
CB14	RL	H	
CB15	RL	L	
17	RLA		Rotate Left Acc. Through Carry
CB06	RLC	(HL)	Rotate Left Circular
DDCB0506	RLC	(1X+d)	
FDCB0506	RLC	(1Y+d)	
CB07	RLC	A	
CB00	RLC	B	
CB01	RLC	C	
CB02	RLC	D	
CB03	RLC	E	
CB04	RLC	H	
CB05	RLC	L	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
07	RLCA		Rotate Left Circular Acc.
ED6F	RLD		Rotate Digit Left and Right between Acc. and Location (HL)
CB1E	RR	(HL)	Rotate Left Through Carry
DDCB051E	RR	(1X+d)	
FDCB051E	RR	(1Y+d)	
CB1F	RR	A	
CB18	RR	B	
CB19	RR	C	
CB1A	RR	D	
CB1B	RR	E	
CB1C	RR	H	
CB1D	RR	L	
1F	RRA		Rotate Right Acc. Through Carry
CB0E	RRC	(HL)	Rotate Right Circular
DDCB050E	RRC	(1X+d)	
FDCB050E	RRC	(1Y+d)	
CB0F	RRC	A	
CB08	RRC	B	
CB09	RRC	C	
CB0A	RRC	D	
CB0B	RRC	E	
CB0C	RRC	H	
CB0D	RRC	L	
0F	RRCA		Rotate Right Circular Acc.
ED67	RRD		Rotate Digit Right and Left Between Acc. and Location (HL)
C7	RST	00H	Restart to Location
CF	RST	08H	
D7	RST	10H	
DF	RST	18H	
E7	RST	20H	
EF	RST	28H	
F7	RST	30H	
FF	RST	38H	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
DE20	SBC	A,n	Subtract Operand from Acc. with Carry
9E	SBC	A,(HL)	
DD9E05	SBC	A,(1X+d)	
FD9E05	SBC	A,(1Y+d)	
9F	SBC	A,A	
98	SBC	A,B	
99	SBC	A,C	
9A	SBC	A,D	
9B	SBC	A,E	
9C	SBC	A,H	
9D	SBC	A,L	
ED42	SBC	HL,BC	
ED52	SBC	HL,DE	
ED62	SBC	HL,HL	
ED72	SBC	HL,SP	
37	SCF		Set Carry Flag (C - 1)
CBC6	SET	0,(HL)	Set Bit b of Location
DDCB05C6	SET	0,(1X+d)	
FDCB05C6	SET	0,(1Y+d)	
CBC7	SET	0,A	
CBC0	SET	0,B	
CBC1	SET	0,C	
CBC2	SET	0,D	
CBC3	SET	0,E	
CBC4	SET	0,H	
CBC5	SET	0,L	
CBCE	SET	1,(HL)	
DDCB05CE	SET	1,(1X+d)	
FDCB05CE	SET	1,(1Y+d)	
CBCF	SET	1,A	
CBC8	SET	1,B	
CBC9	SET	1,C	
CBCA	SET	1,D	
CBCB	SET	1,E	
CBCC	SET	1,H	
CBCD	SET	1,L	
CBD6	SET	2,(HL)	
DDCB05D6	SET	2,(1X+d)	
FDCB05D6	SET	2,(1Y+d)	
CBD7	SET	2,A	
CBD0	SET	2,B	
CBD2	SET	2,C	
CBD2	SET	2,D	
CBD3	SET	2,E	
CBD4	SET	2,H	
CBD5	SET	2,L	

TABLE VIII. CPU instruction set for all device types - Continued.

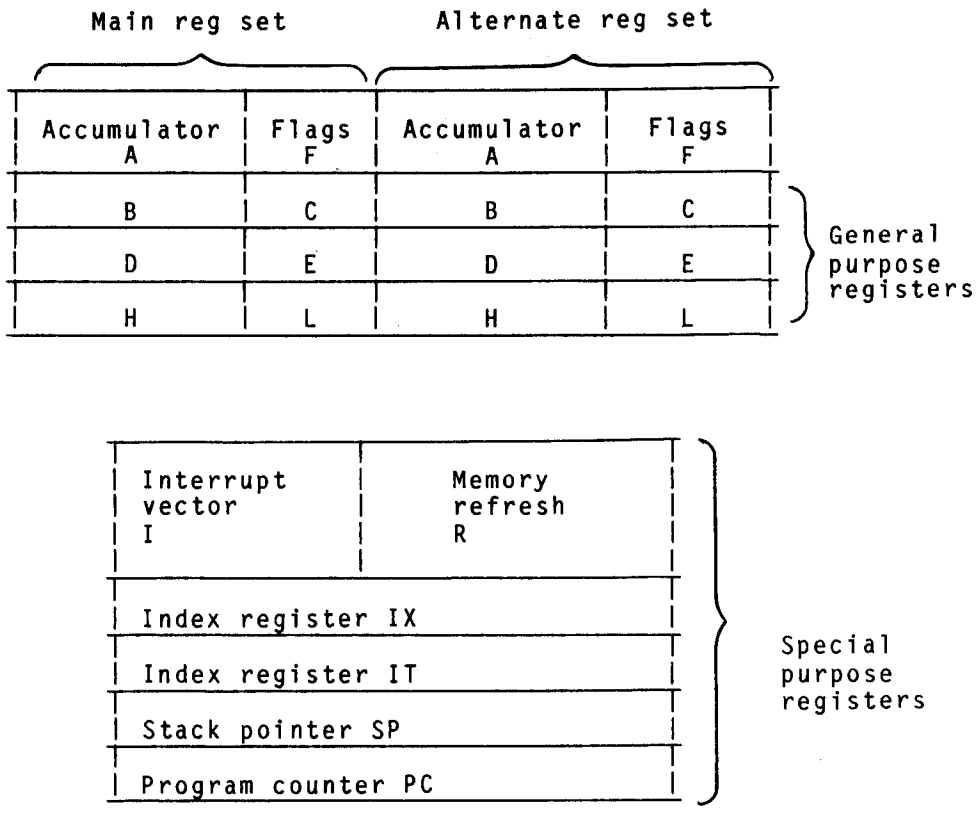
OBJ CODE	SOURCE STATEMENT		OPERATION
CBD8	SET	3,B	Set Bit b of Location
CBDE	SET	3,(HL)	
DDCB05DE	SET	3,(1X+d)	
FDCB05DE	SET	3,(1Y+d)	
CBDF	SET	3,A	
CBD9	SET	3,B	
CBDA	SET	3,C	
CBDB	SET	3,D	
CBDC	SET	3,E	
CBDD	SET	3,H	
CBE6	SET	3,L	
CBE6	SET	4,(HL)	
DDCB05E6	SET	4,(1X+d)	
FDCB05E6	SET	4,(1Y+d)	
CBE7	SET	4,A	
CBE0	SET	4,B	
CBE1	SET	4,C	
CBE2	SET	4,D	
CBE3	SET	4,E	
CBE4	SET	4,H	
CBE5	SET	4,L	
CBEE	SET	5,(HL)	
DDCB05EE	SET	5,(1X+d)	
FDCB05EE	SET	5,(1Y+d)	
CBEF	SET	5,A	
CBEB	SET	5,B	
CBE9	SET	5,C	
CBEA	SET	5,D	
CBEB	SET	5,E	
CBEC	SET	5,H	
CBED	SET	5,L	
CBF6	SET	6,(HL)	
DDCB05F6	SET	6,(1X+d)	
FDCB05F6	SET	6,(1Y+d)	
CBF7	SET	6,A	
CBF0	SET	6,B	
CBF1	SET	6,C	
CBF2	SET	6,D	
CBF3	SET	6,E	
CBF4	SET	6,H	
CBF5	SET	6,L	
CBFE	SET	7,(HL)	
DDCB05FE	SET	7,(1X+d)	
FDCB05FE	SET	7,(1Y+d)	
CBFF	SET	7,A	
CBF8	SET	7,B	
CBF9	SET	7,C	
CBFA	SET	7,D	
CBFB	SET	7,E	
CBFC	SET	7,H	
CBFD	SET	7,L	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
CB26	SLA	(HL)	Shift Operand Left Arithmetic
DDCB0526	SLA	(1X+d)	
FDCB0526	SLA	(1Y+d)	
CB27	SLA	A	
CB20	SLA	B	
CB21	SLA	C	
CB22	SLA	D	
CB23	SLA	E	
CB24	SLA	H	
CB25	SLA	L	
CB2E	SRA	(HL)	Shift Operand Left Arithmetic
DDCB052E	SRA	(1X+d)	
FDCB052E	SRA	(1Y+d)	
CB2F	SRA	A	
CB28	SRA	B	
CB29	SRA	C	
CB2A	SRA	D	
CB2B	SRA	E	
CB2C	SRA	H	
CB2D	SRA	L	
CB3E	SRL	(HL)	Shift Operand Right Logical
DDCB053E	SRL	(1X+d)	
FDCB053E	SRL	(1Y+d)	
CB3F	SRL	A	
CB38	SRL	B	
CB39	SRL	C	
CB3A	SRL	D	
CB3B	SRL	E	
CB3C	SRL	H	
CB3D	SRL	L	
96	SUB	(HL)	Subtract Operand from Acc.
DD9605	SUB	(1X+d)	
FD9605	SUB	(1Y+d)	
97	SUB	A	
90	SUB	B	
91	SUB	C	
92	SUB	D	
93	SUB	E	
94	SUB	H	
95	SUB	L	
D620	SUB	n	

TABLE VIII. CPU instruction set for all device types - Continued.

OBJ CODE	SOURCE STATEMENT		OPERATION
AE	XOR	(HL)	Exclusive "OR"
DDAE05	XOR	(1X+d)	Operand and Acc.
FDAE05	XOR	(1Y+d)	
AF	XOR	A	
A8	XOR	B	
A9	XOR	C	
AA	XOR	D	
AB	XOR	E	
AC	XOR	H	
AD	XOR	L	
EE20	XOR	n	



NOTES:

1. CPU registers. The CPU contains 208 bits of R/W memory that are accessible to the programmer and is configured into eighteen 8-bit registers and four 16-bit registers. All registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulator and flag registers.

2. Special purpose registers.

   a. Program counter (PC). The program counter holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transferred to the address lines. When a program jump occurs, the new value is automatically placed in the PC, overriding the incrementer.

   b. Stack pointer (SP). The stack pointer holds the 16-bit address of the current top of a stack located anywhere in external system RAM memory. The external stack memory is organized as a last-in first-out (LIFO) file. Data can be pushed onto the stack from specific CPU registers or popped off of the stack into specific CPU registers through the execution of PUSH and POP instructions. The data popped from the stack is always the last data pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting, and simplification of many types of data manipulation.

FIGURE 7. CPU register configuration.

c. Two index registers (IX and IY). The two independent index registers hold a 16-bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer. This mode of addressing greatly simplifies many types of program, especially where tables of data are used.

d. Interrupt page address register (I). The CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I register is used for this purpose to store the high order 8-bits of the indirect address while the interrupting device provides the lower 8-bits of the address. This feature allows interrupt routines to be dynamically located anywhere in memory with absolute minimal access time to the routine.

e. Memory refresh register (R). The CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. Seven bits of this 8-bit register are automatically incremented after each instruction fetch. The eighth bit will remain as programmed as the result of an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the I register are placed on the upper 8 bits of the address bus.

3. Accumulator and flag registers. The CPU includes two independent 8-bit accumulators and associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16-bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair that they wish to work with, with a single exchange instruction so that they may easily work with either pair.

4. General purpose registers. There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE, and HL while the complementary set is called BC , DE , and HL . At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange commands need to be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

FIGURE 7. CPU register configuration - Continued.

5. Arithmetic and logic unit (ALU). The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset bit
Compare	Test bit

6. Instruction register and CPU control. As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

FIGURE 7. CPU register configuration - Continued.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{ZAP}) test of input protection circuits. The following terminals, NMI, MREQ, A_3 and BUSRQ of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V. This destructive test shall be conducted as follows using the test circuit on figure 4.

a. Measure I_{IH} and I_{IL} at the inputs selected as stated above at 25°C. These measurements shall be made in accordance with table III herein. The test limits for each single terminal measurement of I_{IH} and I_{IL} shall be as specified in table III.

b. Apply the test voltage (V_{ZAP} = 400 V) to the same terminals selected for leakage current measurements. Apply V_{ZAP} in a 2 mode sequence as shown below and by charging C_1 to V_{ZAP} with S_1 in position 1 and then switching to position 2.

(1) Terminal (-) to GND.

(2) Terminal (+) to GND.

c. Within 24 hours repeat the I_{IH} and I_{IL} measurements on the same terminals as performed above. After the V_{ZAP} test, any DUT exhibiting leakage currents in excess of the specified limits is defective.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. Complete Part or Identifying Number (PIN) (see 6.7).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirement for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to qualifying activity, if applicable.

g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

h. Requirements for product assurance options.

i. Requirements for special carriers, lead lengths, or lead forming, if applicable. These special requirements shall not affect the part number.

j. Requirements for "JAN" marking.

6.3 Test vector table. Table VI, which forms a part of this detail specification, is not printed herein because of its extreme length and complexity; and, even when presented as hard copy, it requires conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of an inspection, a test program output should be obtained in a form compatible with test system architecture. The preparing activity, may be consulted for information on obtaining such output.

6.4 Terms and definitions. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

A_0-A_{15} (Address Bus)	3-state output, active high. A_0-A_{15} constitutes a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.
D_0-D_7 (Data Bus)	3-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus used for data exchanges with memory and I/O devices.
$\overline{MI}$ (Machine Cycle One)	Output, active low. $\overline{MI}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-code, $\overline{MI}$ is generated as each op code byte is fetched. These two byte op-codes always begin with DBH, DDH, EDH, or FDH. $\overline{MI}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.
$\overline{MREQ}$ (Memory Request)	3-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$ (Input/Output Request)	3-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds valid I/O address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an M1 signal when an interrupt response vector can be placed on the data bus. Interrupt acknowledge operations occur during M1 time while I/O operations never occur during M1 time.

$\overline{RD}$
(Memory Read)

3-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$
(Memory Write)

3-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$
(Refresh)

Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$
(Halt State)

Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh activity.

$\overline{WAIT}$

Input, active low. $\overline{WAIT}$ indicates to the CPU that (Wait) the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{INT}$
(Interrupt Request)

Input, active low. The interrupt request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M1 time) is sent out at the beginning of the next instruction cycle.

$\overline{NMI}$
(Non-maskable Interrupt)

Input, negative edge triggered. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override a $\overline{NMI}$.

$\overline{RESET}$

Input, active low. $\overline{RESET}$ forces the program counter to zero and initializes the CPU. The CPU initialization includes:

1. Disable the interrupt enable flip-flop.
2. Set Register I = 00H.
3. Set Register R = 00H.
4. Set Interrupt Mode 0.

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. $\overline{RESET}$ must be active for a minimum of three clock cycles.

$\overline{\text{BUSRQ}}$ (Bus Request)	Input, active low. The bus request signal is used to request the CPU address bus, data bus, and 3-state output control signals to go to a high-impedance state so that other devices can control these buses. When $\overline{\text{BUSRQ}}$ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.
$\overline{\text{BUSAK}}$ (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and 3-state control bus signals have been set to their high impedance state and the external device can now control these signals.
CLOCK	Input. Single phase + 5 V clock.

6.5 Logistic support. Lead material and finishes (see 3.3), are interchangeable.
Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Handling. MOS microprocessors should be handled with certain precautions to avoid damage due to the discharge of accumulated static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended.

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive carriers.

e. Avoid uses of plastic, rubber, or silk in MOS areas.

6.7 Part or Identifying Number (PIN). The PIN shall be in accordance with MIL-M-38510.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military-device type	Generic-industry type
01	Z-80B CMOS CPU

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1159)