

I INCH-POUND I

MIL-M-38510/486

16 AUGUST 1989

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS,  
SERIAL COMMUNICATIONS CONTROLLER,  
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS serial communications controller (SCC). One product assurance class (B), one lead finish, and a choice of case outlines are provided and are reflected in the Part or Identifying Number (PIN) (see 6.7).

1.2 Classification.

1.2.1 Device types. The device types should identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Frequency</u>	<u>Circuit function</u>
01	Z85C3006	6.0 MHz	Serial communications controller
02	Z85C3008	8.5 MHz	Serial communications controller

1.2.2 Device class. The device class should be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines should be designated as follows:

<u>Letter</u>	<u>Case outline, (see MIL-M-38510, appendix C)</u>
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square leadless chip carrier

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.3 Absolute maximum ratings. (Referenced to ground).

V <sub>CC</sub> supply voltage range - - - - -	-0.3 V to +7.0 V dc
Voltage on any pin - - - - -	-0.3 V to V <sub>CC</sub> +3.0 V dc
Storage temperature range- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds) - -	+270°C
Maximum operating junction temperature (T <sub>J</sub> )	
T <sub>A</sub> = +125°C- - - - -	+145°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ):	
Cases Q and X- - - - -	See MIL-M-38510, appendix C
Maximum power dissipation - - - - -	500 mW

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V <sub>IH</sub> ) - - -	2.2 V dc
Maximum low level input voltage (V <sub>IL</sub> )- - -	0.8 V dc
Frequency of operation:	
Device 01 - - - - -	0.5 MHz to 6.0 MHz
Device 02 - - - - -	0.5 MHz to 8.5 MHz
Case operating temperature range (T <sub>C</sub> )- - -	-55°C to +125°C
Clock rise and fall times:	
Device 01 - - - - -	10 ns maximum
Device 02 - - - - -	10 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 Associated detail specification. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be as specified in 1.2.3, herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II herein. The electrical tests for each subgroup shall be as specified in tables I and III herein.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table I) Class B devices
Interim electrical test parameters (method 5004)	1,7
Final electrical test parameters (method 5004 and 5010)	*1,2,3,7,8,9,10,11
Group A test requirements (method 5005)	1,2,3,**4,7,8,9,10,11,12
Group C end-point electrical parameters (method 5005)	1,7,8
Group D end-point electrical parameters (method 5005)	1,7,8

\* PDA applies to subgroup 1 only (see 4.2b).

\*\* See 4.4.1b.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in a microcircuit group number 105 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
High input voltage	$V_{IH}$		1,2,3, 12		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
Low input voltage	$V_{IL}$		1,2,3, 12		-0.3	0.8	-0.3 1/	0.8	V
Logic low output voltage	$V_{OL}$	$I_{OL} = 2.0\text{ mA}$	1,2,3, 12			0.5		0.5	V
Logic high output voltage	$V_{OH1}$	$I_{OH} = -1.6\text{ mA}$	1,2,3, 12		2.4		2.4		V
	$V_{OH2}$	$I_{OH} = -250\text{ }\mu\text{A}$	1,2,3, 12		$V_{CC} - 0.8$		$V_{CC} - 0.8$		V
Power supply current	$I_{CC}$	$V_{IH} = 4.8\text{ V}$ $V_{IL} = 0.2\text{ V}$ $V_{CC} = 5.0\text{ V}$ Oscillator off	1,2,3, 12			30		30	mA
Output leakage current low	$I_{LOL}$	$V_{OUT} = 0.2\text{ V}$	1,2,3, 12		-10	+10	-10	+10	$\mu\text{A}$
Output leakage current high	$I_{LOH}$	$V_{OUT} = V_{CC} - 0.2\text{ V}$	1,2,3, 12		-10	+10	-10	+10	$\mu\text{A}$
Input low current	$I_{IL}$	$V_{IN} = 0.2\text{ V}$	1,2,3, 12		-10	+10	-10	+10	$\mu\text{A}$
Input high current	$I_{IH}$	$V_{IN} = V_{CC} - 0.2\text{ V}$	1,2,3, 12		-10	+10	-10	+10	$\mu\text{A}$
Maximum frequency	$f_{MAX}$		9,10,11			6.0		8.5	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
Input capacitance	C <sub>IN</sub>	f = 1 MHz Unmeasured pins returned to ground, T <sub>C</sub> = +25°C	4		10		10	pF	
Output capacitance	C <sub>OUT</sub>		4		15		15	pF	
Bidirectional capacitance	C <sub>I/O</sub>		4		20		20	pF	
PCLK low width	t <sub>wPCl</sub>	See figure 4, read and write, interrupt, reset, and cycling timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11, 12	1	70	1000	50	1000	ns
PCLK high width	t <sub>wPCh</sub>		9,10,11, 12	2	70	1000	50	1000	ns
PCLK fall time 2/	t <sub>fPC</sub>		9,10,11	3		10		10	ns
PCLK rise time 2/	t <sub>rPC</sub>		9,10,11	4		10		10	ns
PCLK cycle time	t <sub>cPC</sub>		9,10,11, 12	5	165	2000	116	2000	ns
Address to WR +setup time	t <sub>sA(WR)</sub>		9,10,11, 12	6	80		66		ns
Address to WR +hold time	t <sub>hA(WR)</sub>		9,10,11	7	0		0		ns
Address to RD+ setup time	t <sub>sA(RD)</sub>		9,10,11, 12	8	80		66		ns
Address to RD+ hold time	t <sub>hA(RD)</sub>		9,10,11	9	0		0		ns
INTACK to PCLK + setup time	t <sub>sIA(PC)</sub>		9,10,11	10	20		20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0 V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
INTACK to WR +setup time <u>4/</u>	t <sub>sIAi(WR)</sub>	See figure 4, read and write, interrupt, reset, and cycle timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	11	160		140		ns
INTACK to WR +hold time	t <sub>hIA(WR)</sub>		9,10,11	12	0		0		ns
INTACK to RD +setup time	t <sub>sIAi(RD)</sub>		9,10,11	13	160		140		ns
INTACK to RD +hold time <u>3/</u>	t <sub>hIA(RD)</sub>		9,10,11	14	0		0		ns
INTACK to PCLK +hold time	t <sub>hIA(PC)</sub>		9,10,11	15	100		38		ns
CE low to WR +setup time	t <sub>sCEl(WR)</sub>		9,10,11	16	0		0		ns
CE to WR + hold time	t <sub>hCE(WR)</sub>		9,10,11	17	0		0		ns
CE high to WR +setup time	t <sub>sCEh(WR)</sub>		9,10,11	18	70		58		ns
CE low to RD +setup time <u>4/</u>	t <sub>sCEl(RD)</sub>		9,10,11	19	0		0		ns
CE to RD + hold time <u>4/</u>	t <sub>hCE(RD)</sub>		9,10,11	20	0		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
CE high to RD+ setup time 4/	t <sub>sCEh(RD)</sub>	See figure 4, read and write, interrupt, reset, and cycle timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	21	70		58		ns
RD low width 4/	t <sub>wRD1</sub>		9,10,11	22	200		145		ns
RD+ to read data active delay 2/	t <sub>dRD(DRA)</sub>		9,10,11	23	0		0		ns
RD+ to read data not valid time 2/	t <sub>dRDv(DR)</sub>		9,10,11	24	0		0		ns
RD+ to read data valid delay	t <sub>dRDF(DR)</sub>		9,10,11,12	25		180		135	ns
RD+ to read data float delay 2/ 5/	t <sub>dRD(DRz)</sub>		9,10,11	26		45		38	ns
Address required valid to read data valid delay	t <sub>dA(DR)</sub>		9,10,11	27		280		210	ns
WR low width	t <sub>wWR1</sub>		9,10,11	28	200		145		ns
Write data WR+ setup time	t <sub>sDW(WR)</sub>		9,10,11,12	29	0		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0 V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
Write data WR↑ hold time	t <sub>hDW</sub> (WR)	See figure 4, read and write, interrupt, reset, and cycle timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	30	0		0		ns
WR↑ to wait valid delay 6/	t <sub>hWR</sub> (W)		9,10,11, 12	31		200		168	ns
RD↑ to wait valid delay 6/	t <sub>dRD</sub> (W)		9,10,11, 12	32		200		168	ns
WR↑ to W/REQ not valid delay	t <sub>dWRf</sub> (REQ)		9,10,11,	33		200		168	ns
RD↑ to W/REQ not valid delay	t <sub>dWRf</sub> (REQ)		9,10,11, 12	34		200		168	ns
WR↑ to DTR/REQ not valid delay	t <sub>dWRr</sub> (REQ)		9,10,11	35		4 t <sub>cPC</sub>		4 t <sub>cPC</sub>	ns
RD↑ to DTR/REQ not valid delay	t <sub>dRD<sub>r</sub></sub> (REQ)		9,10,11	36		4 t <sub>cPC</sub>		4 t <sub>cPC</sub>	ns
PCLK↑ to INT valid delay 6/	t <sub>dPC</sub> (INT)		9,10,11, 12	37		500		500	ns
INTACK to RD↑ (ac- knowledge) delay 7/	t <sub>dIAi</sub> (RD)		9,10,11, 12	38	200		145		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
$\overline{RD}$ (acknowl- edge) width	t <sub>dA</sub> (DD)	See figure 4, read and write, interrupt, reset, and cycle timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	39	200		145		ns
$\overline{RD}$ + (acknowl- edge) to read data valid delay	t <sub>dRDA</sub> (DR)		9,10,11, 12	40		180		135	ns
IEI to $\overline{RD}$ + (acknowl- edge) set- up time	t <sub>sIEI</sub> (RDA)		9,10,11	41	100		95		ns
IEI to $\overline{RD}$ + (acknowl- edge) hold time	t <sub>hIEI</sub> (RDA)		9,10,11	42	0		0		ns
IEI to IEO delay time	t <sub>dIEI</sub> (IEO)		9,10,11	43		100		95	ns
PCLK + to IEO delay	t <sub>dPC</sub> (IEO)		9,10,11	44		250		195	ns
$\overline{RD}$ + to INT inactive time 6/	t <sub>dRDA</sub> (INT)		9,10,11	45		500		480	ns
$\overline{RD}$ + to $\overline{WR}$ + delay for no reset 2/	t <sub>dRD</sub> (WRQ)		9,10,11	46	15		15		ns
$\overline{WR}$ + to $\overline{RD}$ + delay for no reset 2/	t <sub>dWRQ</sub> (RD)		9,10,11	47	30		15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
WR and RD coincident low for reset 2/	t <sub>wRES</sub>	See figure 4, read and write, interrupt, reset, and cycling timings. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	48	200		145		ns
Valid access recovery time 2/ 8/	t <sub>rc</sub>		9,10,11	49	4 t <sub>cPC</sub>		4 t <sub>cPC</sub>		ns
PCLK+ to W/REQ valid delay	t <sub>dPC</sub> (REQ)	See figure 4, general timing. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	1		250		250	ns
PCLK+ to wait inactive delay	t <sub>dPC</sub> (W)		9,10,11	2		350		350	ns
RxC+ to PCLK+ setup time (PCLK+ 4 case only) 9/ 10/ 15/	t <sub>sRXC</sub> (PC)		9,10,11	3	70	t <sub>wPCL</sub>	55	t <sub>wPCL</sub>	ns
RxD to RxC+ setup time (X1 mode) 9/	t <sub>sRXD</sub> (RXC <sub>r</sub> )		9,10,11	4	0		0		ns
RxD to RxC+ hold time (X1 mode) 9/	t <sub>sRXD</sub> (RXC <sub>r</sub> )		9,10,11	5	150		150		ns
RxD to RxC+ setup time (X1 mode) 9/ 11/	t <sub>sRXD</sub> (RXC <sub>f</sub> )		9,10,11	6	0		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
RxD to $\overline{\text{RxC}}$ + hold time (X1 mode) 9/ 11/	t <sub>hRXD</sub> (RXCf)	See figure 4, general timing. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	7	150		150		ns
$\overline{\text{SYNC}}$ to $\overline{\text{RxC}}$ setup time 9/	t <sub>sSY(RXC)</sub>		9,10,11	8	-200		-200		ns
$\overline{\text{SYNC}}$ to $\overline{\text{RxC}}$ + hold time 9/	t <sub>hSY(RXC)</sub>		9,10,11	9	5 t <sub>cPC</sub>		5 t <sub>cPC</sub>		ns
$\overline{\text{TxC}}$ + to PCLK + setup time 10/ 12/	t <sub>sTXC(PC)</sub>		9,10,11	10	0		0		ns
$\overline{\text{TxC}}$ + to TxD delay (X1 mode) 12/	t <sub>dTXCf</sub> (TXD)		9,10,11, 12	11		230		190	ns
$\overline{\text{TxC}}$ + to TxD delay (X1 mode) 11/ 12/	t <sub>dTxCr</sub> (TXD)		9,10,11	12		230		190	ns
TxD to $\overline{\text{TRxC}}$ delay (send clock echo)	t <sub>dTXD(TRX)</sub>		9,10,11	13		200		200	ns
$\overline{\text{RTxC}}$ high width 13/	t <sub>wRTXh</sub>		9,10,11	14	180		130		ns

See footnotes at end of table.

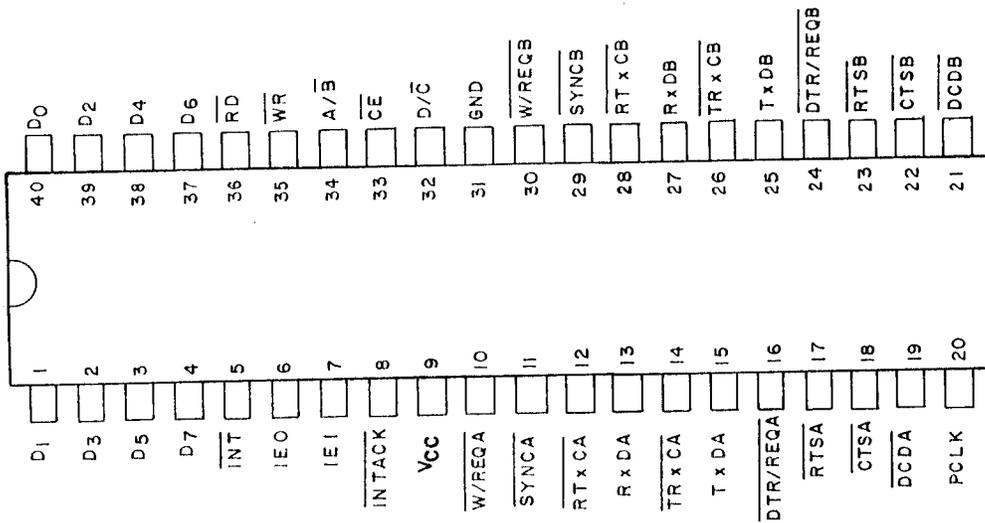
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>CC</sub> = 5.0V ±10% unless otherwise specified	Group A sub- groups	Ref no.	Device types				Unit
					-01		-02		
					Min	Max	Min	Max	
RTxC low width 13/	t <sub>wRTX</sub>	See figure 4, general timing. C <sub>L</sub> = 50 pF ±10% unless otherwise specified.	9,10,11	15	180		130		ns
RTxC cycle time (RxD, TxD) 13/ 16/	t <sub>cRTX</sub>		9,10,11	16	640		472		ns
Crystal oscillator period 2/ 14/	t <sub>cRTXX</sub>		9,10,11	17	165	1000	118	1000	ns
TRxC high width 13/	t <sub>wTRXh</sub>		9,10,11	18	180		120		ns
TRxC low width 13/	t <sub>wTRXl</sub>		9,10,11	19	180		120		ns
TRxC cycle time 13/ 16/	t <sub>cTRX</sub>		9,10,11	20	640		472		ns
D <sub>CD</sub> or C <sub>TS</sub> pulse width	t <sub>wEXT</sub>		9,10,11	21	200		200		ns
SYNC pulse width	t <sub>wSY</sub>		9,10,11	22	200		200		ns

See footnotes on next page.

- 1/ Guaranteed to the limits specified herein by characterization/design if not tested.
- 2/ Guaranteed to the limit specified herein if not tested.
- 3/ Tested in interrupt acknowledge cycle only.
- 4/ Parameter does not apply to interrupt acknowledge transactions.
- 5/ Float delay is defined as the time required for a  $\pm 0.5$  V change in the output with a maximum dc load and minimum ac load.
- 6/ Open-drain output, measured with open-drain test load.
- 7/ Parameter is system dependent. For any SCC in the daisy chain,  $t_{dIA1(RD)}$  must be greater than the sum of  $t_{dPC(IEO)}$  for the highest priority device in the daisy chain,  $t_{sIEI(RDA)}$  for the SCC, and  $t_{dIEIf(IEO)}$ , for each device separating them in the daisy chain.
- 8/ Parameter applies only between transactions involving the SCC.
- 9/  $\overline{RxC}$  is  $\overline{RTxC}$  or  $\overline{TRxC}$ , whichever is supplying the receive clock.
- 10/ Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between  $\overline{RxC}$  and PCLK or  $\overline{TxC}$  and PCLK is required.
- 11/ Parameter applies only to FM encoding/decoding.
- 12/  $\overline{TxC}$  is  $\overline{TRxC}$  or  $\overline{RTxC}$ , whichever is supplying the transmit clock.
- 13/ Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
- 14/ Both  $\overline{RTxC}$  and  $\overline{SYNC}$  have 30 pF capacitors to ground connected to them.
- 15/ This parameter does not apply to this device. Information provided to be consistent with previous devices.
- 16/ The maximum receive or transmit data is one-fourth the PCLK rate.

Device types 01 and 02. Case outline 0.



Device types 01 and 02. Case outline X.

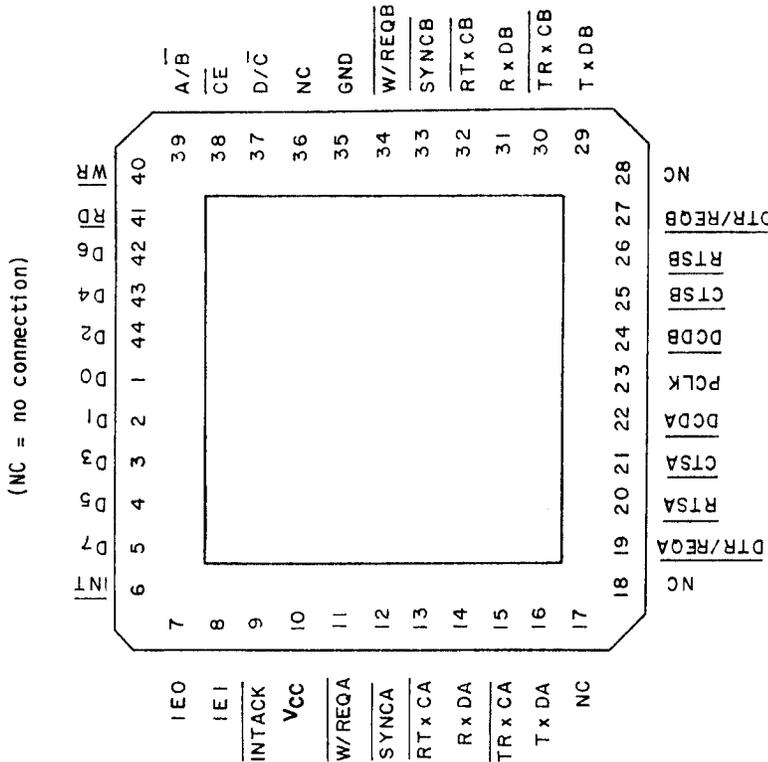


FIGURE 1. Terminal connections.

Device types 01 and 02

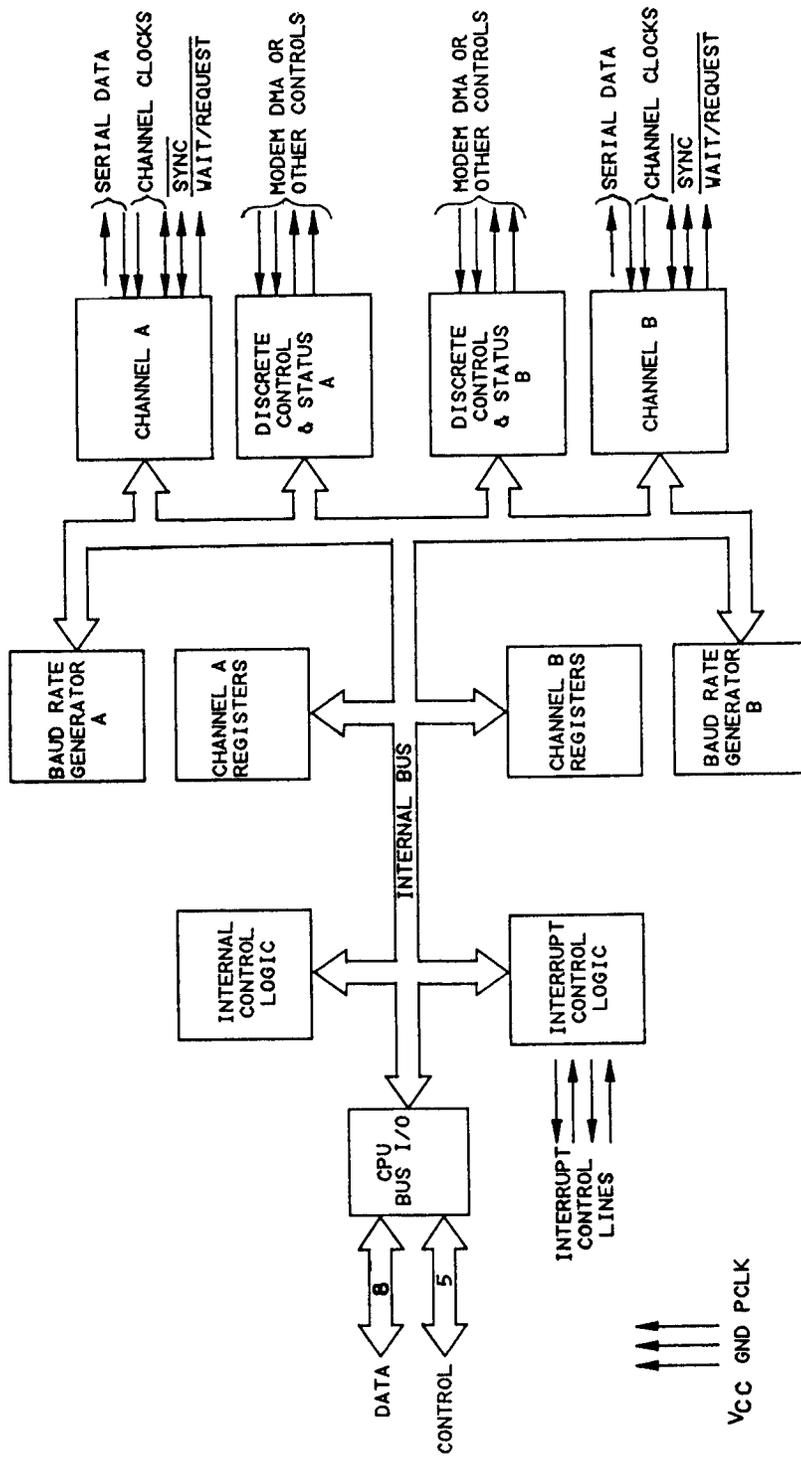
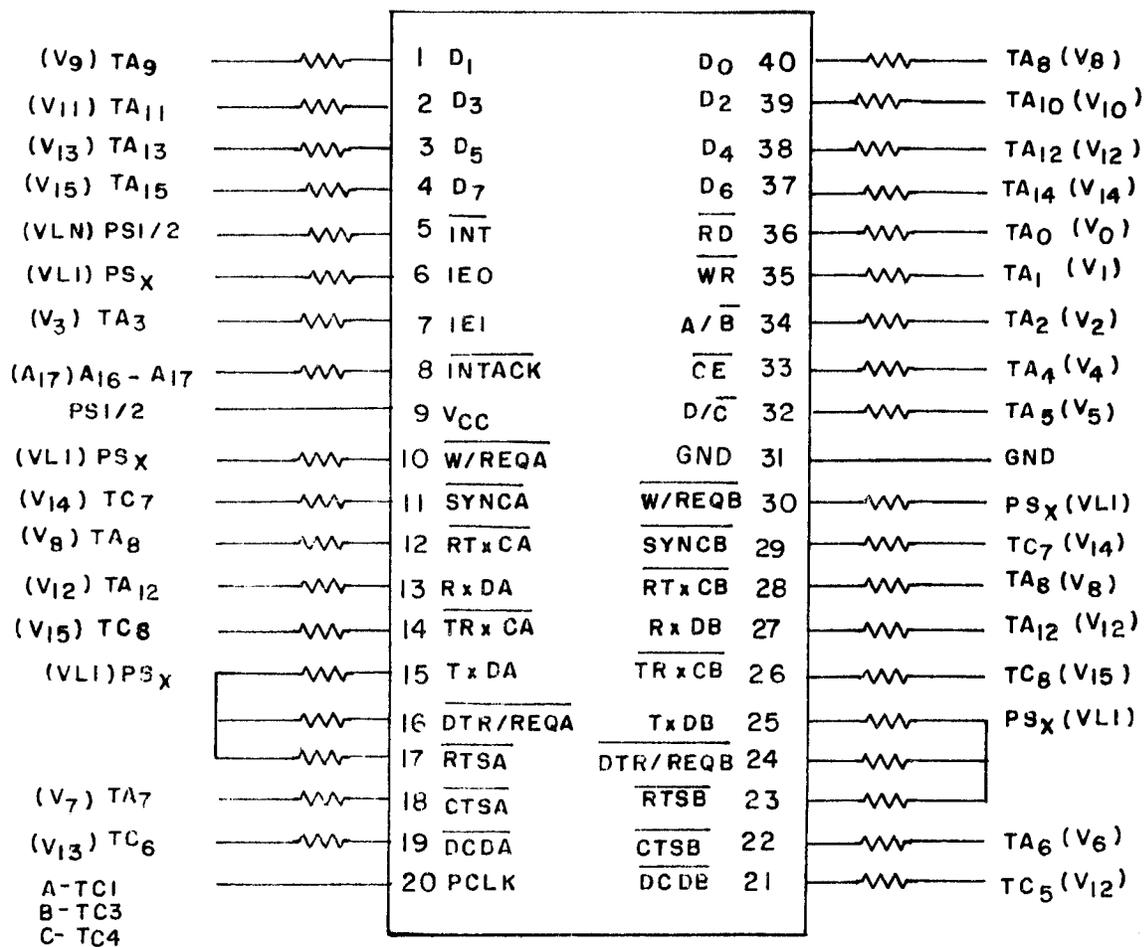


FIGURE 2. Functional block diagram.

## Device types 01 and 02



## NOTES:

1. All resistors 2 k $\Omega$   $\pm$ 1% unless noted otherwise.
2. All signals have 600 $\Omega$  source impedance or less.
3. All power supplies have 100 milliohms impedance or less at device.
4. Vectors (address drivers) levels are GND and  $>$  2.4 volts;  $<$  5.0 volts.
5. Clocks (clock drivers) levels are GND and  $>$  3.6 volts;  $<$  5.0 volts.
6. A<sub>17</sub> (special drive) levels are GND and  $\geq$  5.0 volts;  $\leq$  7.0 volts.
7. PS<sub>1/2</sub> = 5.0 V  $\pm$ 100 mV.
8. PS<sub>X</sub> = +3.5 V  $\pm$ 5%.
9. Clock frequency = 1 MHz  $\pm$ 1%.
10. I<sub>CC</sub> = 250 mA maximum.

FIGURE 3. Dynamic burn-in and life test.

Device types 01 and 02

**READ AND WRITE TIMING**

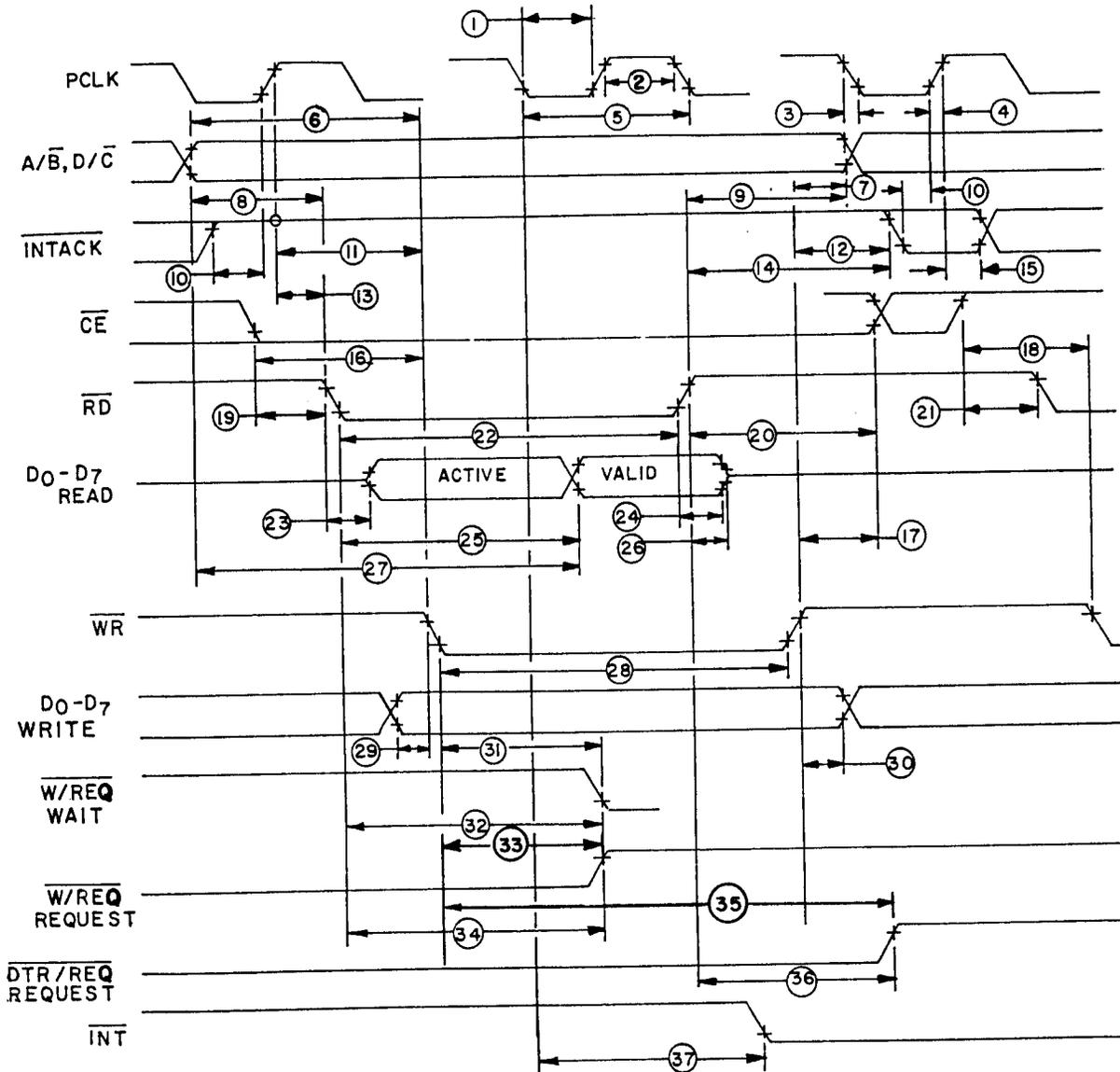
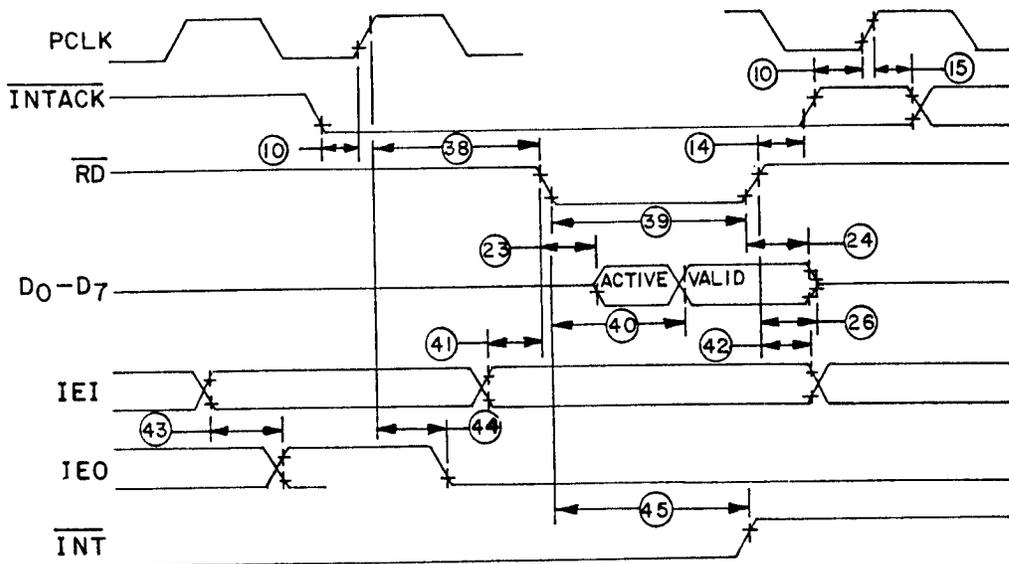


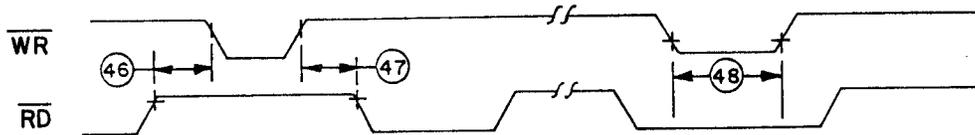
FIGURE 4. Timing diagram.

Device types 01 and 02

INTERRUPT ACKNOWLEDGE TIMING



RESET TIMING



CYCLE TIMING

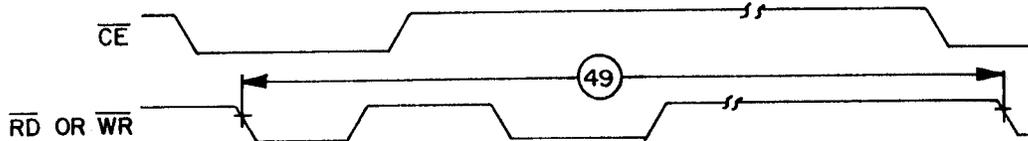


FIGURE 4. Timing diagram - Continued.

Device types 01 and 02

GENERAL TIMING

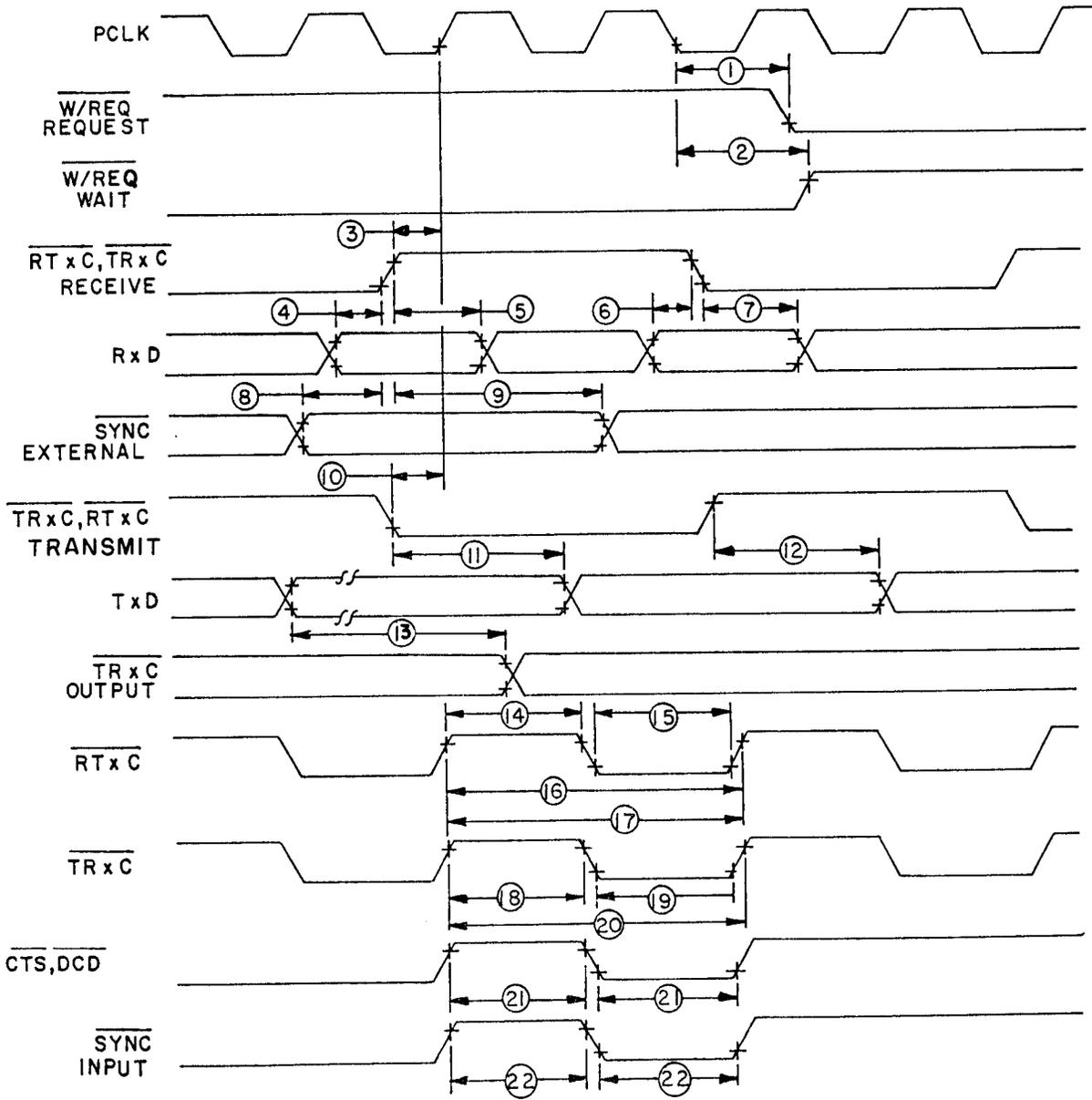
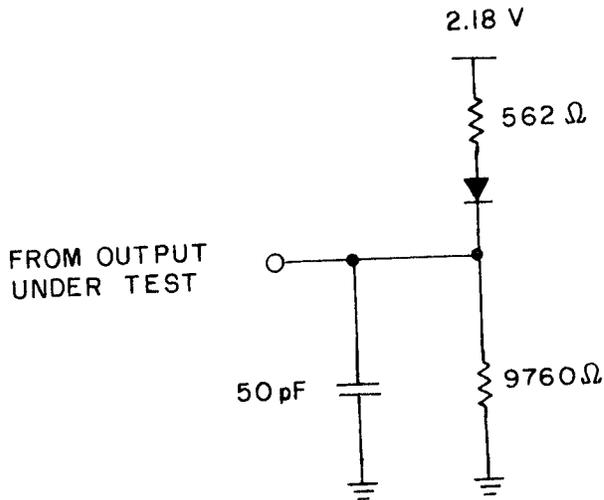


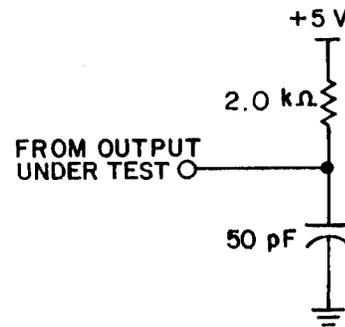
FIGURE 4. Timing diagram - Continued.

Switching test circuits

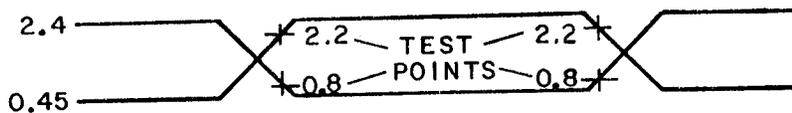
Standard test load



Open drain test load



Switching test input/output waveform



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.2 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 4. Timing diagram - Continued.

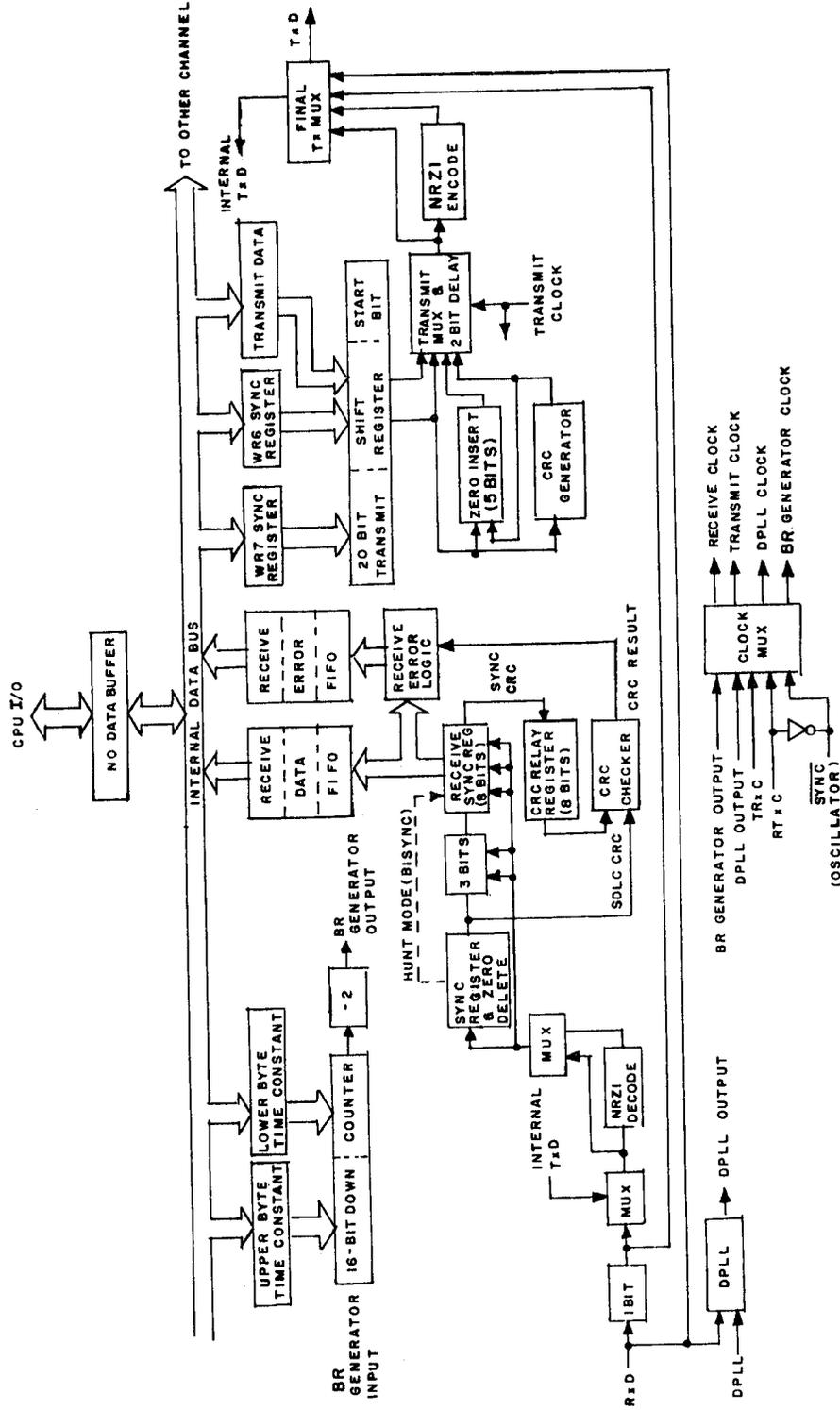


FIGURE 5. Data path.

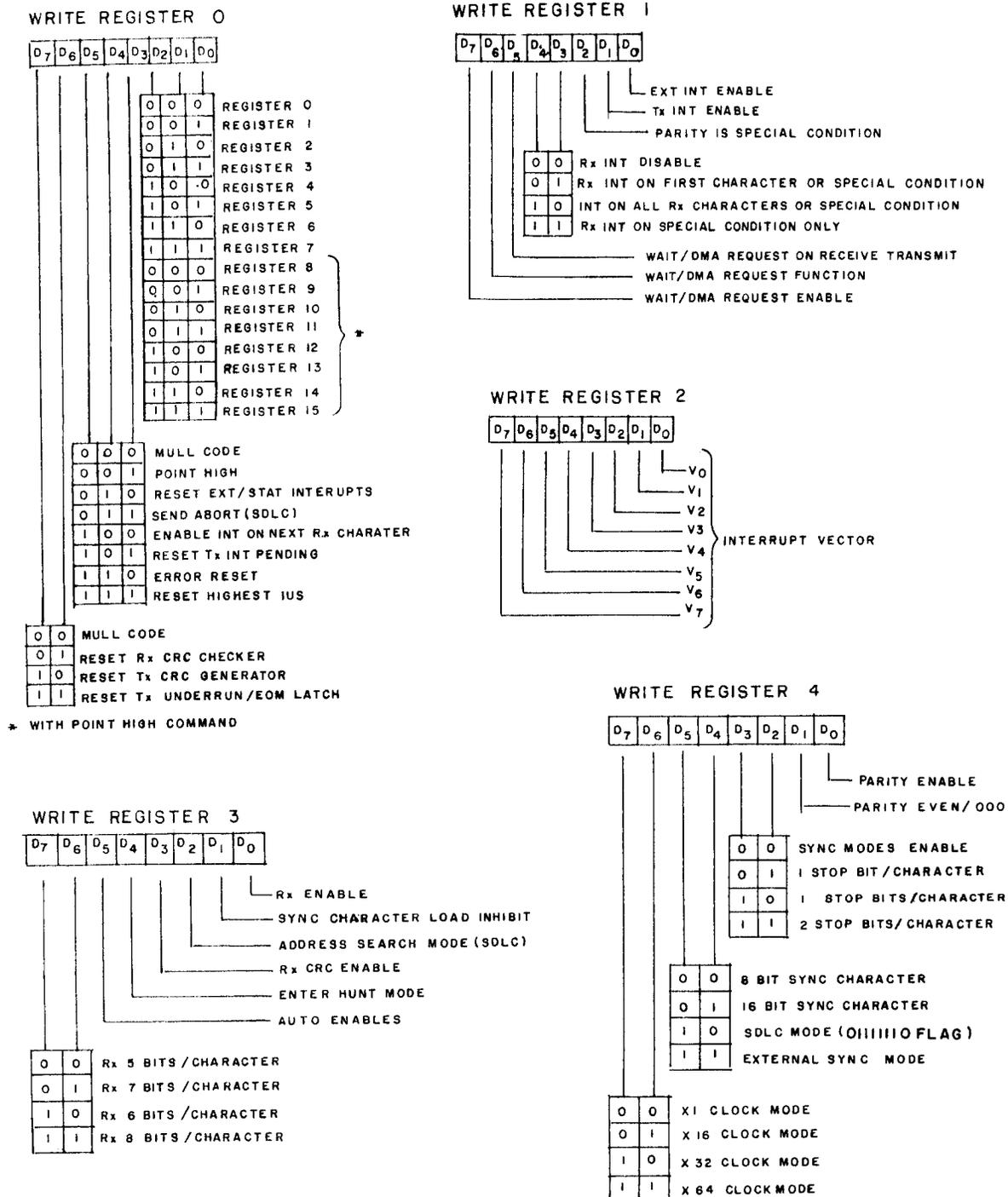
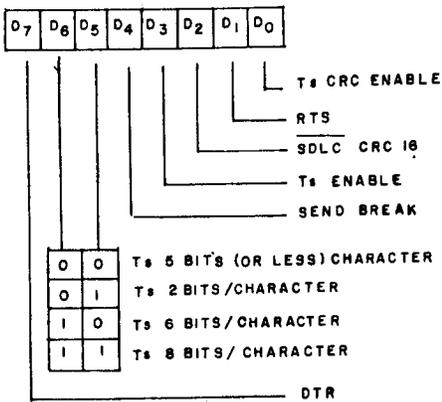
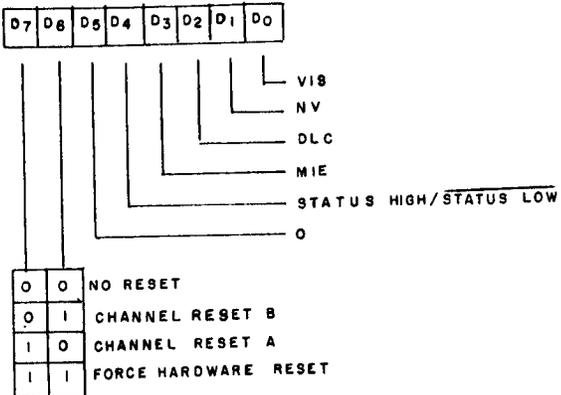


FIGURE 6. Write register bit functions.

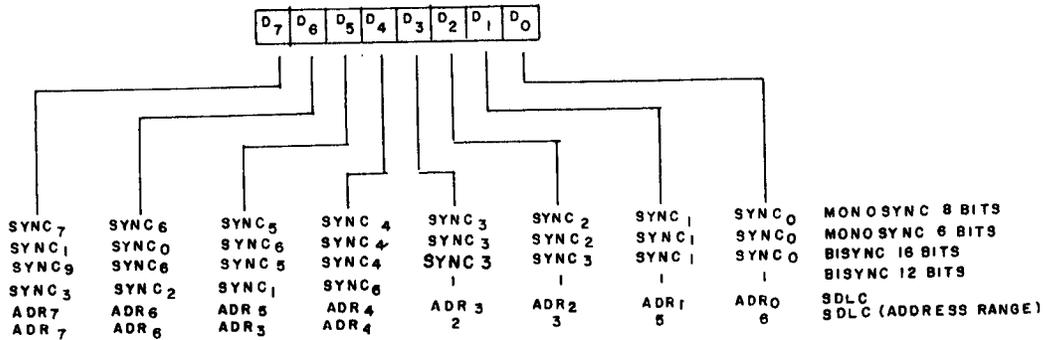
WRITE REGISTER 5



WRITE REGISTER 9



WRITE REGISTER 6



WRITE REGISTER 7

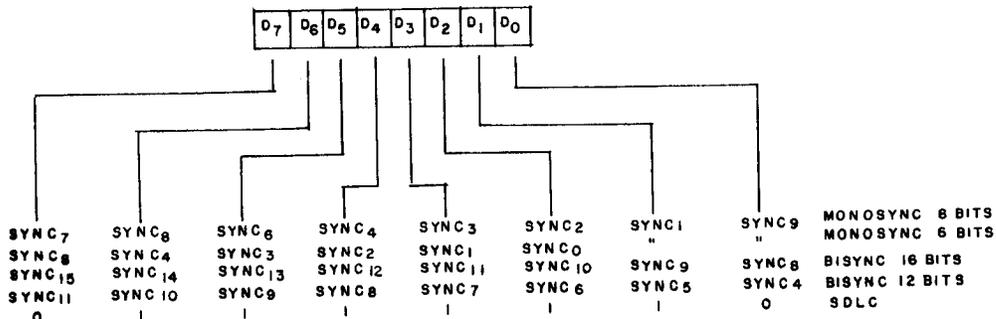


FIGURE 6. Write register bit functions - Continued.

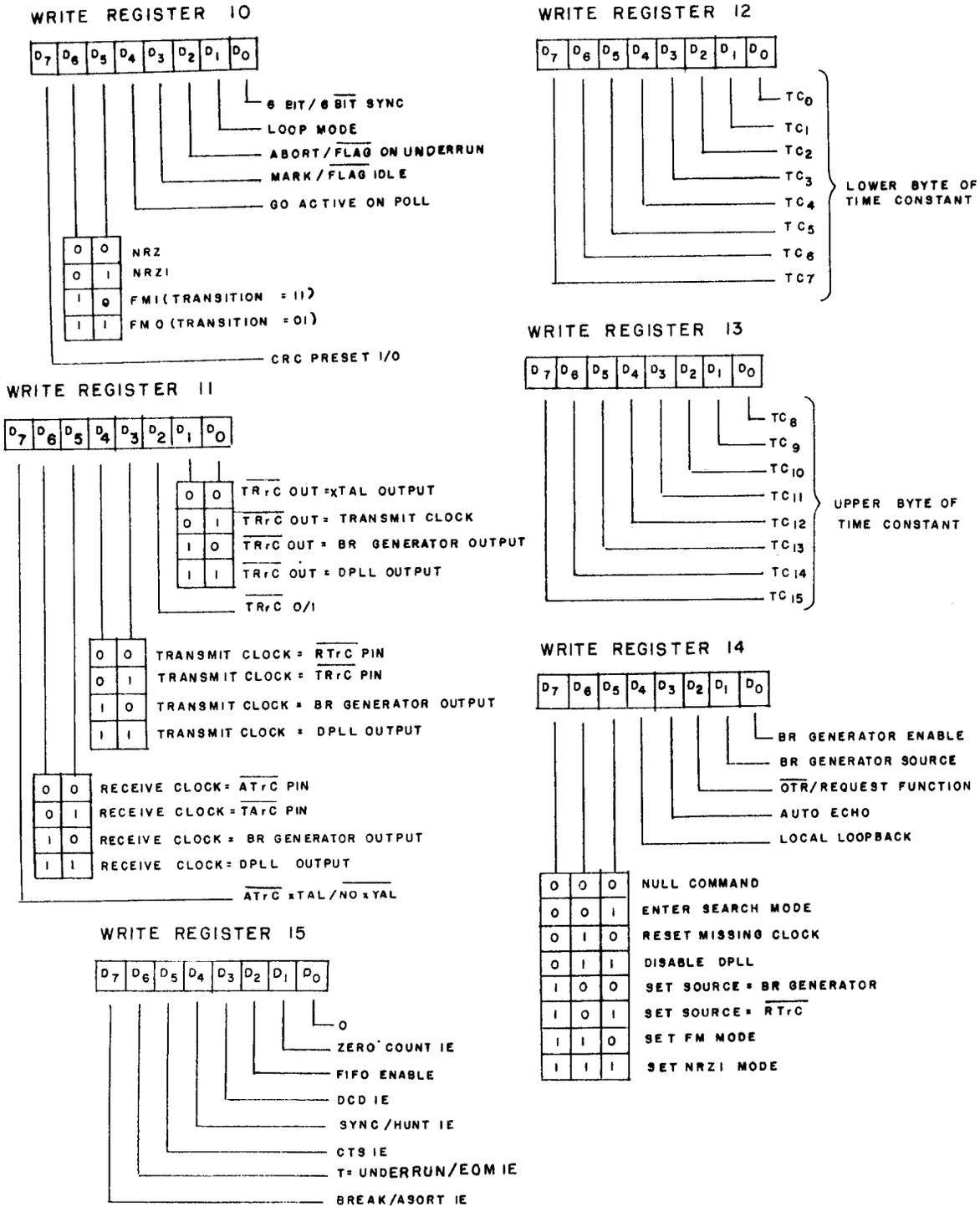
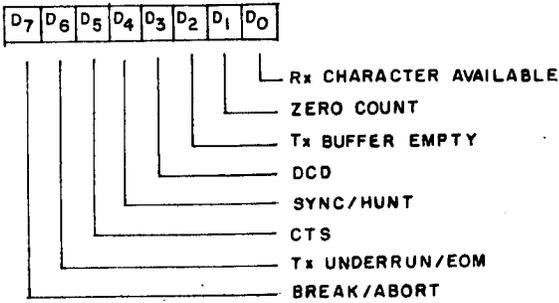
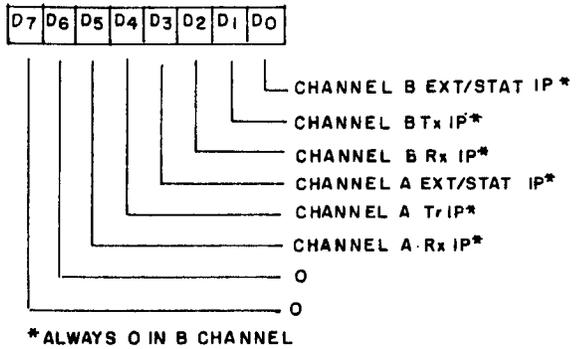


FIGURE 6. Write register bit functions - Continued.

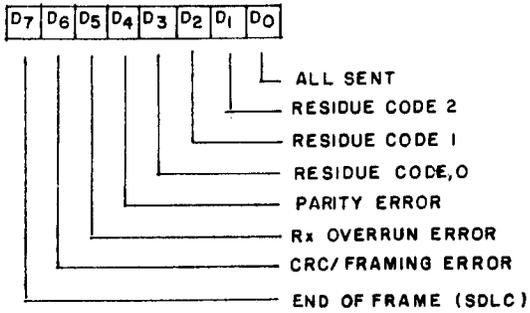
READ REGISTER 0



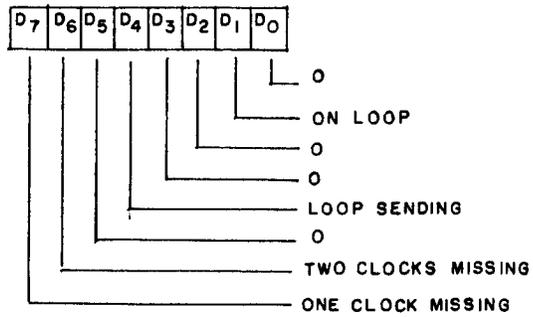
READ REGISTER 3



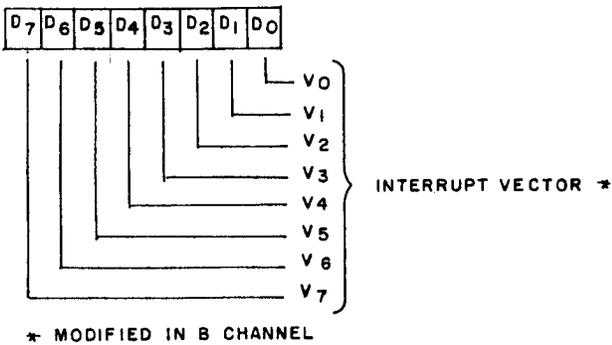
READ REGISTER 1



READ REGISTER 10



READ REGISTER 2



READ REGISTER 12

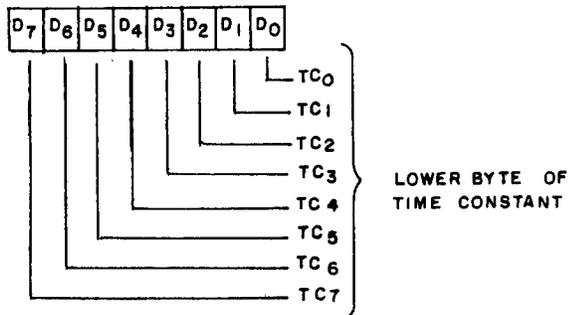


FIGURE 7. Read register bit functions.

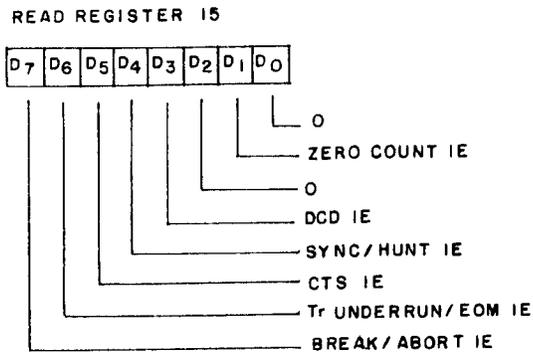
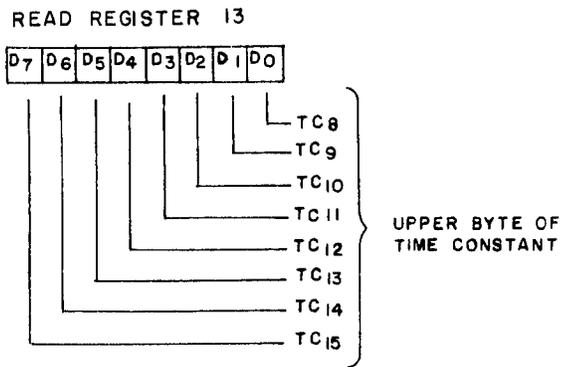


FIGURE 7. Read register bit functions - Continued.

APPENDIX

SYSTEM TIMING

Device types 01 and 02

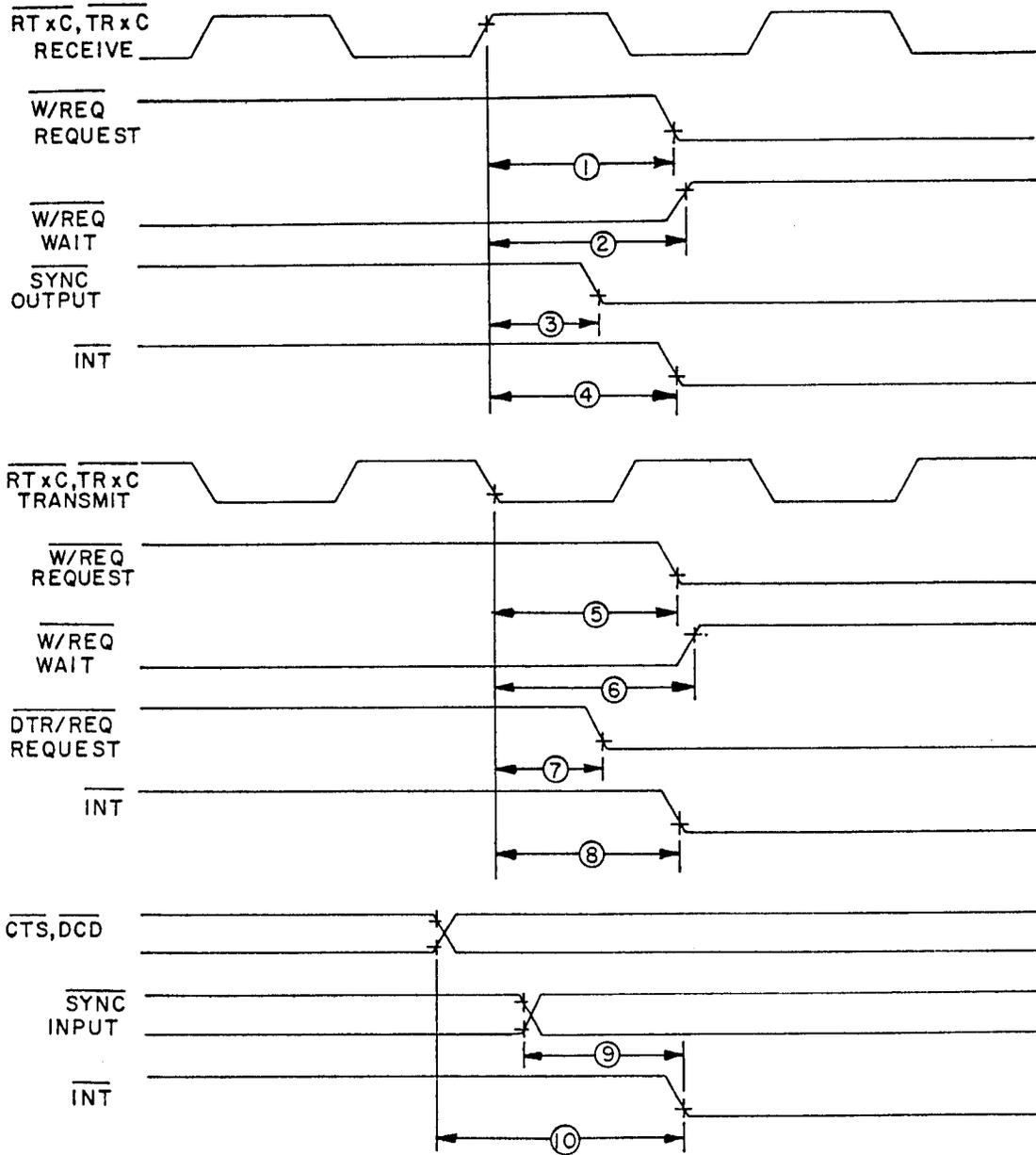


FIGURE 8. System timing.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following modifications and additional criteria shall apply:

- a. Burn-in test method 1015 of MIL-STD-883.
  - (1) Test condition D or E using the burn-in configuration shown on figure 3, or equivalent.
  - (2)  $T_A = +125^{\circ}\text{C}$ .
- b. The percent defective allowable (PDA) for class B devices shall be in accordance with MIL-M-38510. Electrical tests shall be in accordance with table II herein.
- c. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically (i.e., same die, process, and package) to other device types on this specification, the other device type may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I, method 5005 of MIL-STD-883 and as follows:

- a. Electrical tests shall be as specified in table II herein.
- b. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$ ,  $C_{I/O}$  measurements) shall be performed only for initial qualification and after process or package or design changes which may affect design capacitance. Capacitance shall be measured between the designated terminal and  $V_{SS}$  at a frequency of 1 MHz. One pin of each input, output, and input/output (bidirectional, 3-state) type shall be tested on each device. The pin selected for a given type shall be rotated for each subsequent device tested.

- c. Subgroup 12 shall be added to group A inspection requirements for class B devices using an acceptance number of 22 with zero rejects and consist of the procedures, test conditions, and limits specified in table I herein. This inspection will only be performed at a case operating temperature of +125°C and +25°C. This subgroup shall be used for initial qualification only and variable data shall be submitted.
- d. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and acceptance values shown in table Iib of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and acceptance values shown in table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883).
  - (1) Test conditions D or E using the configuration shown on figure 3.
  - (2)  $T_A = +125^\circ\text{C}$  minimum.
- c. Test duration 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical test shall be as specified in table II herein.
- b. The constant acceleration test shall be performed using test condition D of method 2001 of MIL-STD-883.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

Table III, which forms a part of this specification, is not printed herein because of its extreme length. When the sequence or condition of tests and test vectors, which form this table, are needed as part of this inspection they may be obtained in a form compatible with the test system architecture. The preparing activity may be consulted for information on obtaining table III. Group A subgroup assignment is shown in table I.
--

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of the specification.
- b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).
- c. Complete Part or Identifying Number (PIN) (see 6.7).
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to qualifying activity, if applicable.
- e. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirement for product assurance options.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, terms, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

6.3.1 General description. The SCC serial communications controller is a dual channel, multi-protocol data communications peripheral designed for use with 8-bit and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. On-chip features include baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, synchronous byte-oriented protocols, and synchronous bit-oriented protocols such as HDLC and SDLC. This versatile device supports virtually any serial data transfer application (diskette, telecommunications, cassette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 write registers (see figure 6) and 7 read registers (see figure 7) per channel, the user can configure the SCC so that it can handle all asynchronous formats regardless of data size, number of stop bits, or parity requirements. The SCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the SCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation and checking, break and abort generation and detection, and many other protocol-dependent features.

6.3.2 Pinout description. The following section describes the pin functions of the SCC. Figure 1 details the respective pin functions and pin assignments.

$A/\bar{B}$	Channel A/channel B select (input). This signal selects the channel in which the read or write operation occurs.
$\bar{CE}$	Chip enable (input, active low). This signal selects the SCC for a read or write operation.
$D_0 - D_7$	Data bus (bidirectional, 3-state). These lines carry data and commands to and from the SCC.
$D/\bar{C}$	Data/control select (input). This signal defines the type of information transferred to or from the SCC. A high means data is transferred; a low indicates a command.
$\bar{RD}$	Read (input, active low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the interrupt acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
$\bar{WR}$	Write (input, active low). When the SCC is selected, this signal indicates a write operation. The coincidence of $\bar{RD}$ and $\bar{WR}$ is interpreted as a reset.
$\bar{CTS}_A, \bar{CTS}_B$	Clear to send (inputs, active low). If these pins are programmed as auto enables, a low on the inputs enables the respective transmitters. If not programmed as auto enables, they must be general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
$RxDA, RxDB$	Receive data (inputs, active high). These input signals receive serial data at standard TTL levels.

<u>RTxCA</u> , <u>RTxCB</u>	Receive/transmit clocks (inputs, active low). These pins can be programmed in several different modes of operation. In each channel, <u>RTxC</u> may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase-locked loop. These pins can also be programmed for use with the respective <u>SYNC</u> pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
<u>DCDA</u> , <u>DCDB</u>	Data carrier detect (inputs, active low). These pins function as receiver enables if they are programmed for auto enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
<u>DTR/REQA</u> , <u>DTR/REQB</u>	Data terminal ready/request (outputs, active low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as request lines for a DMA controller.
IEI	Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy-chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.
IEO	Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.
INT	Interrupt request (output, open-drain, active low). This signal is activated when the SCC requests an interrupt.
INTACK	Interrupt acknowledge (input, active low). This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy-chain settles. When <u>RD</u> becomes active, the SCC places an vector on the data bus (if IEI is high). <u>INTACK</u> is latched by the rising edge of <u>PCLK</u> .
PCLK	Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

**RTSA, RTSB**

Request to send (outputs, active low). When the request to send (RTS) bit in write register 5 (figure 7) is set, the RTS signal goes low. When the RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

**SYNCA, SYNCB**

Synchronization (inputs or outputs, active low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 (figure 6) but have no other function.

In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, SYNC must be driven low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of SYNC.

In the internal synchronization mode (monosync and bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

**TxDA, TxDB**

Transmit data (outputs, active high). These output signals transmit serial data at standard TTL levels.

**TRxCA, TRxCB**

Transmit/receive clocks (inputs or outputs, active low). These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

**W/REQA, W/REQB**

Wait/request (outputs, open-drain when programmed for a wait function, driven high or low when programmed for a request function). These dual-purpose outputs may be programmed as request lines for a DMA controller or as wait lines to synchronize the CPU to the SCC data rate. The reset state is wait.

6.3.3 Architecture. The SCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to a nonmultiplexed bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (see figure 2).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes 10 control (write) registers, 2 sync-character (write) registers, and 4 status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write only master interrupt control register and three read registers: one containing the vector with status information (channel B only), one containing the vector without status (channel A only), and one containing the interrupt pending bits (channel A only).

The registers for each channel are designated as follows:

WRO-WR15 - - - Write registers 0 through 15.

RRO-RR3, RR10, RR12, RR13, RR15 - - - Read registers 0 through 3,  
10, 12, 13, 15.

Table IV lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR8, but they can be accessed by either channel. All other registers are paired (one for each channel).

6.3.4 Data path. The transmit and receive data path illustrated in figure 5 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the synchronous character registers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the transmit data output (TxD).

TABLE IV. Read and write register functions.

Read register functions	
RR0	Transmit/receive buffer status and external status
RR1	Special receive condition status
RR2	Modified interrupt vector (channel B only) Unmodified interrupt vector (channel A only)
RR3	Interrupt pending bits (channel A only)
RR8	Receive buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/status interrupt information
Write register functions	
WR0	CRC initialize, initialization commands for the various modes. Register pointers.
WR1	Transmit/receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and controls
WR4	Transmit/receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync characters or SDLC address field
WR7	Sync character or SDLC flag
WR8	Transmit buffer
WR9	Master interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receive control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/status interrupt control

6.3.5 Programming. The SCC contains write registers in each channel that are programmed by the system separately to configure the functional personality of the channels. Register addressing is direct for the data registers only, which are selected by a high on the d/c pin. In all other cases (with the exception of WRO and RRO), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WRO and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the SCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WRO (or RRO) is addressed again.

6.3.6 Write registers. The SCC contains 13 write registers (14 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 6 shows the format of each write register.

6.3.7 Read registers. The SCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RRO, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the interrupt pending (IP) bits (channel A). Figure 7 shows the formats for each read register.

The status bits of RRO and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a special receive condition interrupt, all the appropriate error bits can be read from a single register (RR1).

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish "A" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS devices must be handled with certain precautions to avoid damage due to the discharge of accumulated static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a. Devices should be handled on benches with a conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive carriers.
- e. The use of plastic, rubber, or silk in MOS areas should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

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6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	Z85C3006 SCC
02	Z85C3008 SCC

6.7 Part or Identifying Number (PIN). The PIN is created as specified in MIL-M-38510.

## APPENDIX

## SYSTEM TIMING AC CHARACTERISTICS

## 10. SCOPE

10.1 Scope. This appendix contains supplementary timing parameters with associated diagrams for clarification that are to be used as design limits. Due to testing limitations these parameters are impossible to test. This appendix is a mandatory part of the specification and the information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

## 30. SYSTEM TIMING AC CHARACTERISTICS

Symbol	Parameter	Ref no. <u>1/</u>	Device types				Unit
			-01		-02		
			Min	Max	Min	Max	
$t_{dRxC}(REQ)$	$\overline{RxC}^+$ to $\overline{W/REQ}$ valid delay <u>2/</u>	1	8	12	8	12	$t_{cPC}$
$t_{dRxC}(W)$	$\overline{RxC}^+$ to wait inactive delay <u>2/ 3/</u>	2	8	14	8	14	$t_{cPC}$
$t_{dRxC}(SY)$	$\overline{RxC}^+$ to $\overline{SYNC}$ valid delay <u>2/</u>	3	4	7	4	7	$t_{cPC}$
$t_{dRxC}(INT)$	$\overline{RxC}^+$ to $\overline{INT}$ valid delay <u>2/ 3/</u>	4	10	16	10	16	$t_{cPC}$
$t_{dTxC}(REQ)$	$\overline{TxC}^+$ to $\overline{W/REQ}$ valid delay <u>4/</u>	5	5	8	5	8	$t_{cPC}$
$t_{dTxC}(W)$	$\overline{TxC}^+$ to wait inactive delay <u>3/ 4/</u>	6	5	11	5	11	$t_{cPC}$
$t_{dTxC}(DRQ)$	$\overline{TxC}^+$ to $\overline{DTR/REQ}$ valid delay <u>4/</u>	7	4	7	4	7	$t_{cPC}$
$t_{dTxC}(INT)$	$\overline{TxC}^+$ to $\overline{INT}$ valid delay <u>3/ 4/</u>	8	6	10	6	10	$t_{cPC}$
$t_{dSY}(INT)$	$\overline{SYNC}$ transition to $\overline{INT}$ valid delay <u>3/</u>	9	2	6	2	6	$t_{cPC}$

## APPENDIX

## SYSTEM TIMING AC CHARACTERISTICS

Symbol	Parameter	Ref no. <u>1/</u>	Device types				Unit
			-01		-02		
			Min	Max	Min	Max	
$t_{dEXT(INT)}$	$\overline{DCD}$ or $\overline{CTS}$ transition to INT valid delay <u>3/</u>	10	2	6	2	6	$t_{cPC}$

1/ See figure 8, system timing.

2/  $\overline{RxC}$  is  $\overline{RTxC}$  or  $\overline{TRxC}$ , whichever is supplying the receive clock.

3/ Open-drain output, measured with open-drain test load.

4/  $\overline{TxC}$  is  $\overline{TRxC}$  or  $\overline{RTxC}$ , whichever is supplying the transmit clock.

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CONCLUDING MATERIAL

Custodians:

Army - ER  
Navy - EC  
Air Force - 17

Review activities:

Army - AR, MI  
Navy - OS, SH  
Air Force - 11, 19, 85, 99  
DLA - ES

User activities:

Army - SM  
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

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