QUALIFICATION REQUIREMENTS REMOVED

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, MULTIPLIER-ACCUMULATORS/MULTIPLIERS, MONOLITHIC SILICON

This specification is approved for use by the Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, multiplier accumulators and multiplier circuits. Two product assurance classes are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit	Case outlines
01	Multiplier-accumulator, parallel 8 bit	U (C-7)
02	Multiplier-accumulator, parallel 12 bit	U (C-7)
03	Multiplier-accumulator, parallel 16 bit	U (C-7)
04	Multiplier, parallel 8 bit	T (C-5)
05	Multiplier, parallel 12 bit	U (C-7)
06	Multiplier, parallel 16 bit	U (C-7)

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
U	C-7, 68-terminal SQ. CCP (.950" x .950")
T	C-5, 44-terminal SQ. CCP (.650" x .650")

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to 7.0 V dc
Input voltage range	-0.5 to 5.5 V dc
Output voltage range	-0.5 to 5.5 V dc
Storage temperature range	-65°C to +150°C
Junction temperature (T_J) 1/	175°C
Thermal resistance, junction to case (θ_{JC})	
Case U	4.0°C/W
Case T	7.0°C/W

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

Power dissipation (P_D) 2/
Device 01- 2.9 watts
Device 02- 4.7 watts
Device 03- 6.9 watts
Device 04- 2.5 watts
Device 05- 4.1 watts
Device 06- 6.1 watts

1.4 Recommended operating conditions.

Supply voltage - - - - - - - - - - - - - - - - - - 4.5 V dc minimum to 5.5 V dc maximum

Clock pulse width (t_{pw}) measure at 1.5 V level- 30 ns minimum

Operating case temperature range - - - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifictions and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Schematic circuits. The schematic circuit (inputs/outputs only) shall be equivalent in operation as those shown on figure 3.

2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

TABLE I. Electrical performance characteristics.

Parameter	Symbols	Test conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Device types 01 Min	01 Max	02 Min	02 Max	03 Min	03 Max	Unit
High-level input voltage	V_{IH}	V_{CC} = 5.5 V	2.0		2.0		2.0		V
Low-level input voltage	V_{IL}	V_{CC} = 4.5 V		0.8		0.8		0.8	V
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA	2.4		2.4		2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA		0.5		0.5		0.5	V
High-level input current for all inputs	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V		400		400		500	µA
High-level input current for XIN, RND, SUB, ACC, TC, MSP, XTP	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		100	µA
High-level input current for CLK X, TSL, TSM and TSX	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		100	µA
High-level input current for YIN and LSP	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		200	µA
High-level input current for PREL, CLK Y, CLK P	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		200	µA
Low-level input current for XIN, RND, SUB, ACC, TC, MSP and XTP	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		-400		-400		-400	µA
Low-level input current for CLK X, TSL, TSM, TSX	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		-1		-1		-1	mA
Low-level input current for YIN and LSP	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		-400		-400		-800	µA
Low-level input current for PREL, CLK Y, CLK P	I_{IL4}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		-1		-1		-2	mA
Supply current 1/	I_{CC}	V_{CC} = 5.5 V, all inputs = 0, all outputs = "0", three-state controls = 3 V	100	525	200	850	300	1250	mA
Output short circuit current	I_{OS}	V_{CC} = 5.5 V, all outputs = "1" 2/	-1	-40	-1	-40	-1	-40	mA

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbols	Test conditions See figure 5a $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Device types 01 Min	01 Max	02 Min	02 Max	03 Min	03 Max	Unit
Multiply - accumulate time from input register CLK to output register CLK	t_{MA}	V_{CC} = 4.5 V C_L = 40 pF ±10% R_L = 500 Ω ±5%	15	125	15	170	15	200	ns
Output delay	t_{DO} t_{D1}		10 10	45 45	10 10	45 45	10 10	45 45	ns ns
Three state output delay output enable	t_{ENA0} t_{ENA1}		10 10	45 45	10 10	45 45	10 10	45 45	ns ns
Three-state output delay output disable	t_{DIS0} t_{DIS1}		10 10	45 45	10 10	45 45	10 10	45 45	ns ns
Input register set-up time XIN, YIN, TC, RND, ACC, SUB	t_S	V_{CC} = 4.5 V		30		30		30	ns
Input register hold time XIN, YIN, TC, RND, ACC, SUB	t_H	V_{CC} = 4.5 V		3		3		3	ns
Preload register set-up time XTP, MSP, LSP, PREL, TSL, TSM, TSX.	t_{SP}	V_{CC} = 4.5 V		50		50		50	ns
Preload register hold time XTP, MSP, LSP, PREL, TSL, TSM, TSX	t_{HP}	V_{CC} = 4.5 V		3		3		3	ns

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbols	Test conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Device types 04 Min	04 Max	05 Min	05 Max	06 Min	06 Max	Unit
High level input voltage	V_{IH}	V_{CC} = 5.5 V	2.0		2.0		2.0		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		0.8		0.8		0.8	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA	2.4		2.4		2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA		0.5		0.5		0.5	V
High level input current for all inputs	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V		300		300		300	µA
High level input current for RND, XIN, YIN, FT	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		100	µA
High level input current for TCX, TCY, RS	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		100	µA
High level input current for TRIM, TRIL, CLK M, CLK L, CLK X 3/	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		100		100		100	µA
High level input current CLK P	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 2.4 V		200					µA
High level input current CLK Y	I_{IH5}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		100		100		200	µA
Low level input current for XIN, YIN, RND, FT pins	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	-40	-400	-40	-400	-40	-400	µA
Low level input current for TCX, TCY, RS	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V			-40	-800	-40	-800	µA
Low-level input current for CLK X, CLK M, CLK L, TRIL and TRIM 3/	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	-40	-1000	-40	-1000	-40	-1000	µA
Low level input current CLK P	I_{IL4}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	-40	-2000					µA
Low level input current CLK Y	I_{IL5}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	-40	-1000	-40	-1000	-40	-2000	µA
Off-state output current, high level voltage applied, 4/	I_{OZH}	V_{CC} = 5.5 V, V_O = 2.4 V		40		40		40	µA
Off-state output current, low level voltage applied, 4/	I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V		-40		-40		-40	µA
Supply current 1/	I_{CC}	V_{CC} = 5.5 V. All inputs = 0 V. All outputs = "0". Three-state controls = 3 V	100	450	200	750	300	1050	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V. All outputs = "1" 2/	-1	-40	-1	-40	-1	-40	mA

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbols	Test conditions See figure 5b -55°C ≤ T_C ≤ +125°C	Device types 04 Min	04 Max	05 Min	05 Max	06 Min	06 Max	Unit
Multiply time, clocked from input register CLK to output register CLK.	t_{MC}	V_{CC} = 4.5 V C_L = 40 pF ±10% R_L = 500 Ω ±5%	15	115	15	140	15	185	ns
Multiply time, unclocked	t_{MUC}					185		230	ns
Output delay									
	t_{D0}		10	45	10	45	10	45	ns
	t_{D1}		10	45	10	45	10	45	ns
Three-state output delay output enable									
	t_{ENA0}		10	45	10	45	10	45	ns
	t_{ENA1}		10	45	10	45	10	45	ns
Three-state output delay output disable									
	t_{DIS0}		10	45	10	45	10	45	ns
	t_{DIS1}		10	45	10	45	10	45	ns
Input register set-up time XIN, YIN, TCX, TCY, RND	t_S	V_{CC} = 4.5 V		30		30		30	ns
Input register hold time XIN, YIN, TCX, TCY, RND	t_H	V_{CC} = 4.5 V		3		3		3	ns

1/ Worst-case static current.
2/ Not more than one output should be shorted at a time. Short circuit duration should not exceed one second. Data output level may change state under I_{OS} test conditions. In such cases, I_{OS} test limit will be ø mA min.
3/ Input current for CLK X, TRIL, TRIM inputs only for device 04.
4/ MSP outputs only for device 06.

3.2.4 Truth table. The pre-load truth table shall be as specified on figure 4.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended operating case temperature range, unless otherwise specified.

3.5 Data format and functional description. The data format and functional description shall be as specified in the appendix to this specification.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. The subgroup numbers of tables II and III are in accordance with the group A subgroups of method 5005 of MIL-STD-883.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. The "JAN" or "J" certification mark shall not be used.

3.8 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line (not necessarily the line producing the device type described herein).

3.9 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

3.10 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group 100 (technology group A) per appendix E of MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883). Test condition B or F using the burn-in circuits shown on figure 6.

b. Percent defective allowable (PDA). The PDA shall be in accordance with MIL-M-38510.

c. Alternate screening per MIL-STD-883, method 5004, paragraph 3.3 is allowed for class B devices provided prior approval is obtained from the qualifying activity.

d. T_A = +125°C, minimum.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 shall be omitted.

c. Subgroup 7 shall include the functional verification of truth tables (table V).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) 2/	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1, 7	1, 7
Final electrical test parameters (method 5004)	1, 7 1/	1, 7 1/
Group A test requirements (method 5005)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B test requirements (method 5005) subgroup 5	1,2,3,7, 8,9,10,11	---
Group C end-point electrical parameters (method 5005)	1, 7	1, 7
Group D end-point electrical parameters (method 5005)	1, 7	1, 7

1/ PDA applies to subgroup 1 and 7 (see 4.2b).
2/ Subgroup 7 shall be the functional verification of truth tables (Table IV).

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of method 5005 of MIL-STD-883. The following additional criteria shall apply:

a. Steady-state life test (method 1005 of MIL-STD-883) shall be test condition B or F using the life test circuits shown on figure 6.

b. End-point electrical parameters shall be as specified in table II herein.

c. $T_A \geq +125°C$.

4.4.4 Group D inspection. Group D inspection shall consist of the test subgroups and LTPD values shown in table IV of method 5005 of MIL-STD-883.

a. End-point electrical parameters shall be as specified in table II.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

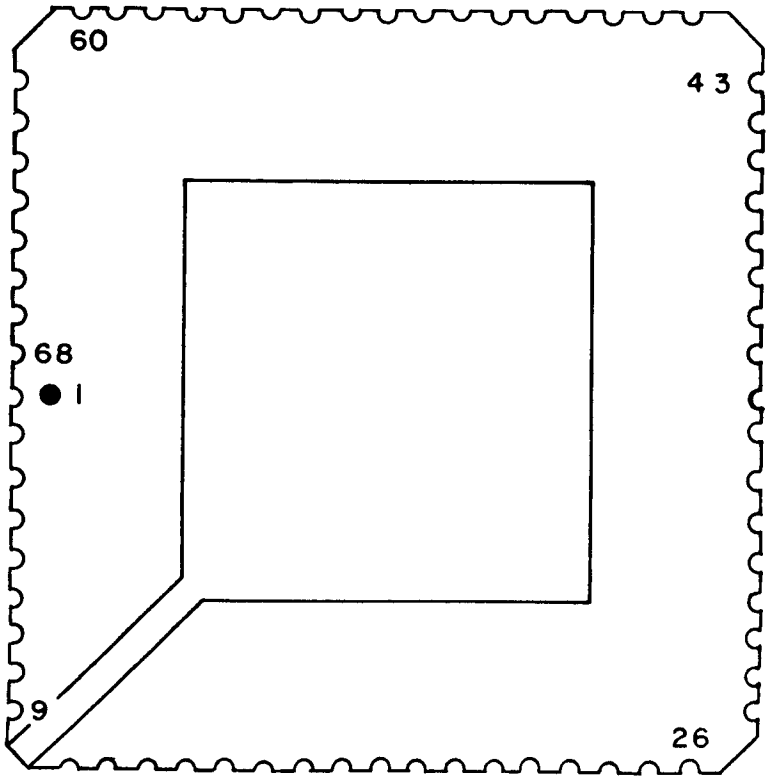
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for the packaging of microcircuits shall be as specified in MIL-M-38510.

Text continued on page 54

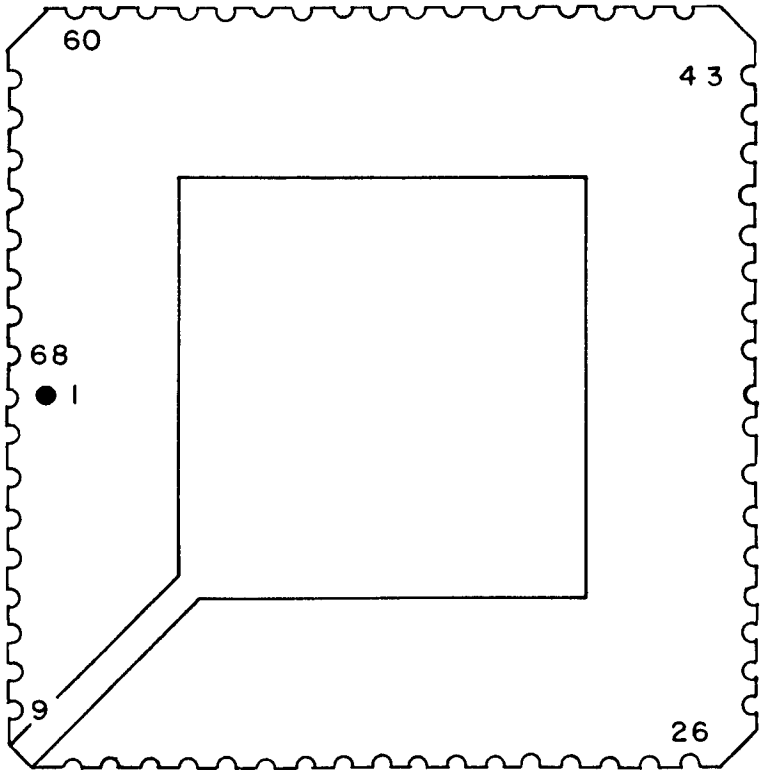
Device type 01



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	P12	18	GND	35	X3	52	Y5
2	P11	19	P4	36	X4	53	Y6
3	P10	20	P3	37	X5	54	Y7
4	P9	21	P2	38	X6	55	TC
5	P8	22	P1	39	X7	56	TSX
6	TSM	23	P0	40	CLK X	57	NC
7	NC	24	TSL	41	CLK Y	58	NC
8	NC	25	NC	42	NC	59	NC
9	NC	26	NC	43	NC	60	NC
10	NC	27	NC	44	NC	61	NC
11	NC	28	NC	45	NC	62	NC
12	CLK P	29	SUB	46	Y0	63	P18
13	PREL	30	ACC	47	Y1	64	P17
14	NC	31	RND	48	Y2	65	P16
15	P7	32	X0	49	Y3	66	P15
16	P6	33	X1	50	Y4	67	P14
17	P5	34	X2	51	VCC	68	P13

FIGURE 1. Terminal connections

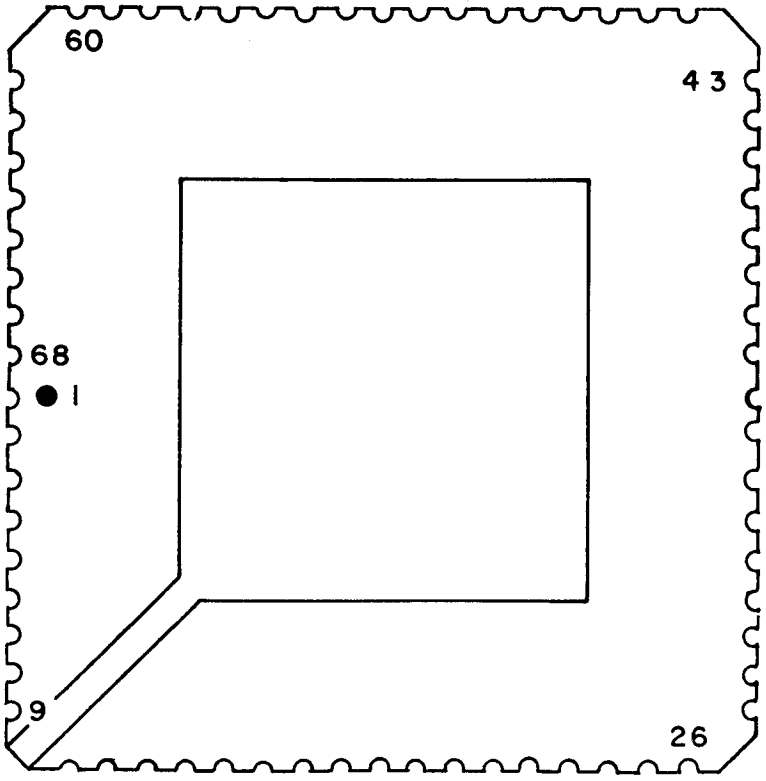
Device type 02



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	18	P19	35	P6	52	X4
2	VCC	19	P18	36	GND	53	X5
3	Y6	20	P17	37	GND	54	X6
4	Y7	21	P16	38	P5	55	X7
5	Y8	22	P15	39	P4	56	X8
6	Y9	23	P14	40	P3	57	X9
7	Y10	24	P13	41	P2	58	X10
8	Y11	25	P12	42	P1	59	X11
9	TC	26	TSM	43	P0	60	CLK X
10	TSX	27	PREL	44	TSL	61	CLK Y
11	P26	28	CLK P	45	RND	62	Y0
12	P25	29	P11	46	SUB	63	Y1
13	P24	30	P10	47	ACC	64	Y2
14	P23	31	P9	48	X0	65	Y3
15	P22	32	P8	49	X1	66	Y4
16	P21	33	P7	50	X2	67	Y5
17	P20	34	GND	51	X3	68	VCC

FIGURE 1. Terminal connections - Continued.

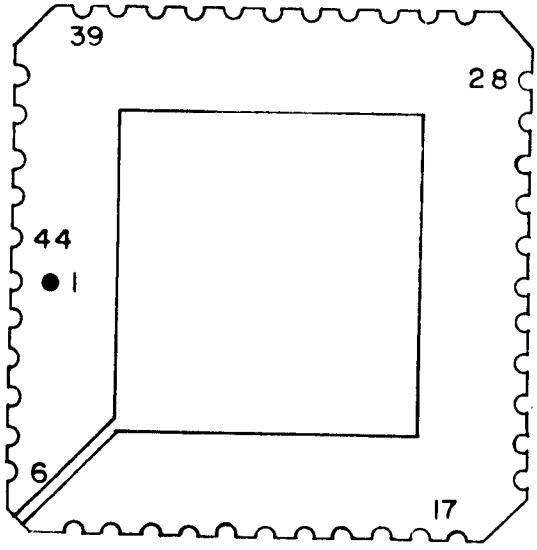
Device type 03



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	X6	18	VCC	35	P25	52	P8,Y8
2	X7	19	VCC	36	P24	53	GND
3	X8	20	VCC	37	P23	54	GND
4	X9	21	TC	38	P22	55	P7,Y7
5	X10	22	TSX	39	P21	56	P6,Y6
6	X11	23	PREL	40	P20	57	P5,Y5
7	X12	24	TSM	41	P19	58	P4,Y4
8	X13	25	CLK P	42	P18	59	P3,Y3
9	X14	26	P34	43	P17	60	P2,Y2
10	X15	27	P33	44	P16	61	P1,Y1
11	TSL	28	P32	45	P15,Y15	62	P0,Y0
12	RND	29	P31	46	P14,Y14	63	X0
13	SUB	30	P30	47	P13,Y13	64	X1
14	ACC	31	P29	48	P12,Y12	65	X2
15	CLK X	32	P28	49	P11,Y11	66	X3
16	CLK Y	33	P27	50	P10,Y10	67	X4
17	VCC	34	P26	51	P9,Y9	68	X5

FIGURE 1. Terminal connections - Continued.

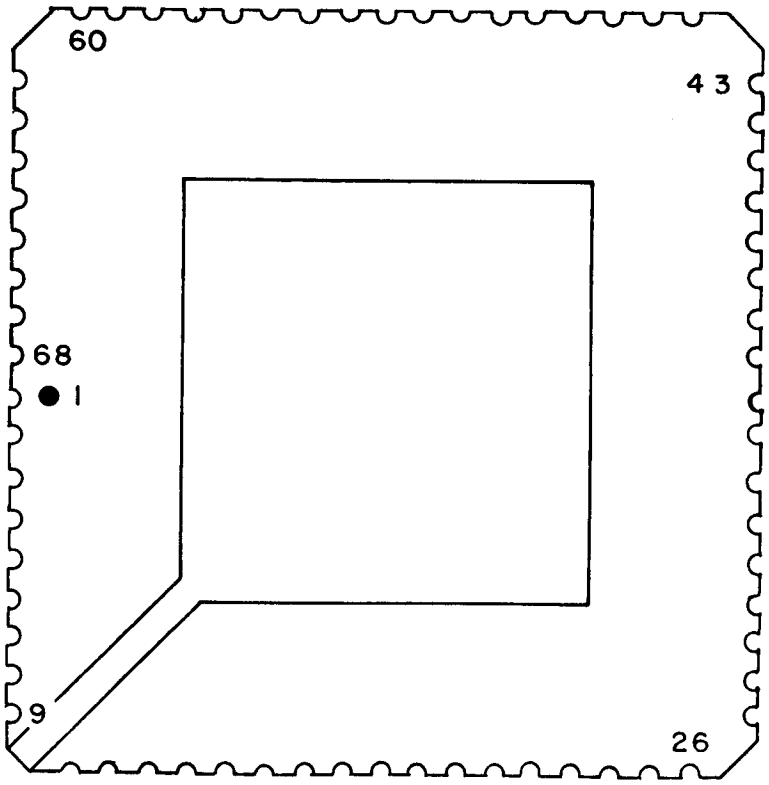
Device type 04



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	P4	12	P10	23	X2	34	VCC
2	P5	13	P11	24	X1	35	Y3
3	P6	14	P12	25	XSGN	36	GND
4	P7	15	P13	26	CLK X	37	Y2
5	CLK P	16	P14	27	CLK Y	38	Y1
6	NC	17	NC	28	NC	39	YSGN
7	TRIM	18	X7	29	RND	40	NC
8	TRIL	19	X6	30	Y7	41	PSGN (MSP)
9	PSGN (LSP)	20	X5	31	Y6	42	P1
10	P8	21	X4	32	Y5	43	P2
11	P9	22	X3	33	Y4	44	P3

FIGURE 1. Terminal connections - Continued.

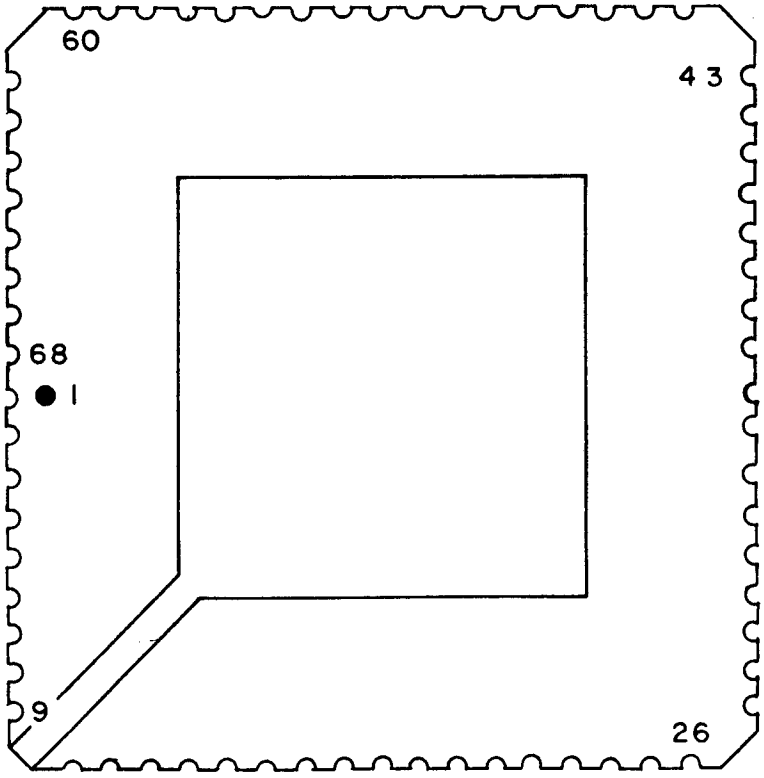
Device type 05



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	P15	18	P8	35	X7	52	VCC
2	P14	19	P7	36	X8	53	Y6
3	P13	20	P6	37	X9	54	Y7
4	P12	21	P5	38	X10	55	Y8
5	NC	22	P4	39	X11	56	Y9
6	CLK M	23	P3	40	CLK X	57	Y10
7	CLK L	24	P2	41	CLK Y	58	Y11
8	RS	25	P1	42	RND	59	TCY
9	FT	26	P0	43	TCX	60	NC
10	GND	27	NC	44	Y0	61	P23
11	GND	28	X0	45	Y1	62	P22
12	TRIM	29	X1	46	Y2	63	P21
13	TRIL	30	X2	47	Y3	64	P20
14	NC	31	X3	48	Y4	65	P19
15	P11	32	X4	49	Y5	66	P18
16	P10	33	X5	50	VCC	67	P17
17	P9	34	X6	51	VCC	68	P16

FIGURE 1. Terminal connections - Continued.

Device type 06



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	VCC	18	P23	35	P7,Y7	52	X5
2	GND	19	P22	36	P6,Y6	53	X6
3	GND	20	P21	37	P5,Y5	54	X7
4	GND	21	P20	38	P4,Y4	55	X8
5	FT	22	P19	39	P3,Y3	56	X9
6	RS	23	P18	40	P2,Y2	57	X10
7	TRIM	24	P17	41	P1,Y1	58	X11
8	CLK M	25	P16	42	P0,Y0	59	X12
9	NC	26	NC	43	NC	60	NC
10	P31	27	P15,Y15	44	CLK Y	61	X13
11	P30	28	P14,Y14	45	CLK L	62	X14
12	P29	29	P13,Y13	46	TRIL	63	X15
13	P28	30	P12,Y12	47	X0	64	CLK X
14	P27	31	P11,Y11	48	X1	65	RND
15	P26	32	P10,Y10	49	X2	66	TCX
16	P25	33	P9,Y9	50	X3	67	TCY
17	P24	34	P8,Y8	51	X4	68	VCC

FIGURE 1. Terminal connections - Continued.

Device type 01

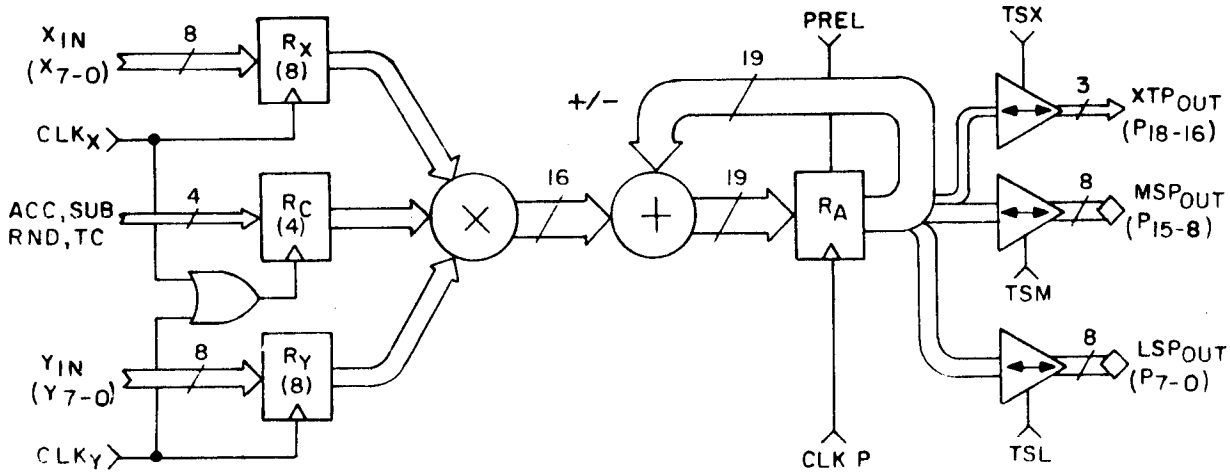


FIGURE 2. Functional block diagram.

Device type 02

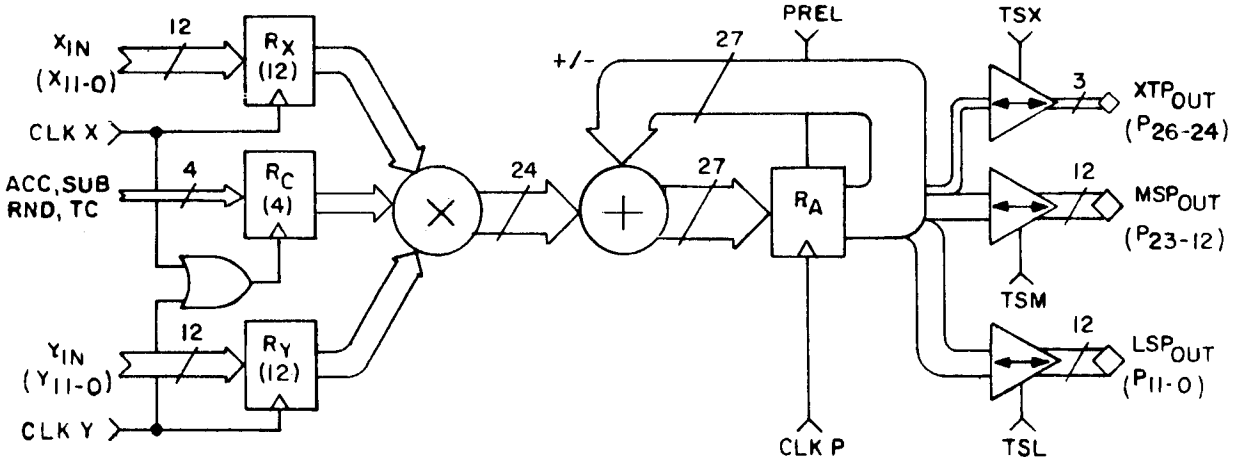


FIGURE 2. Functional block diagram - Continued.

Device type 03

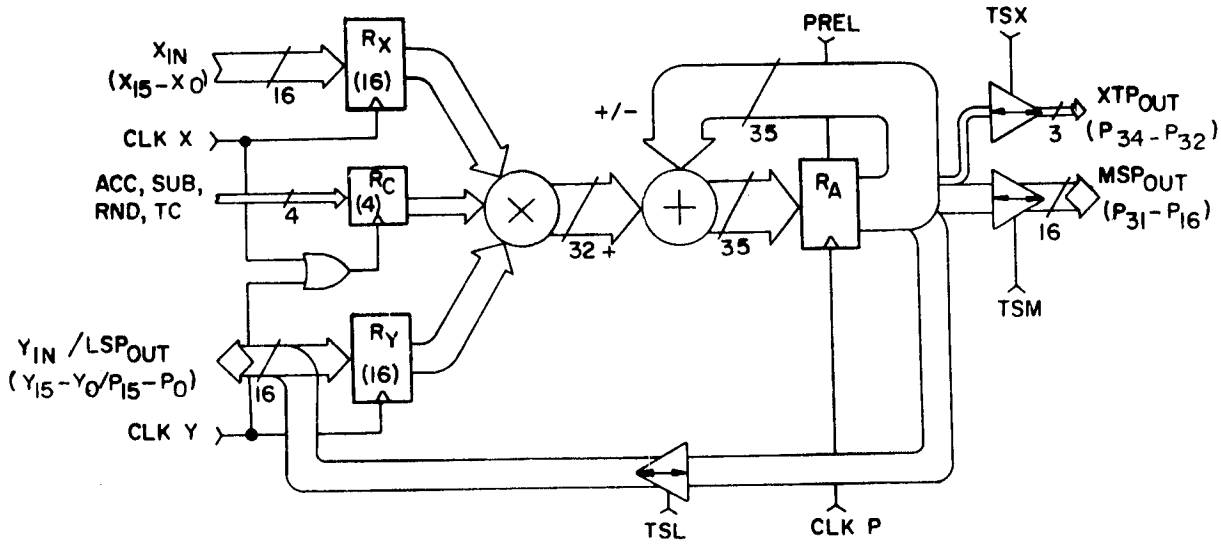
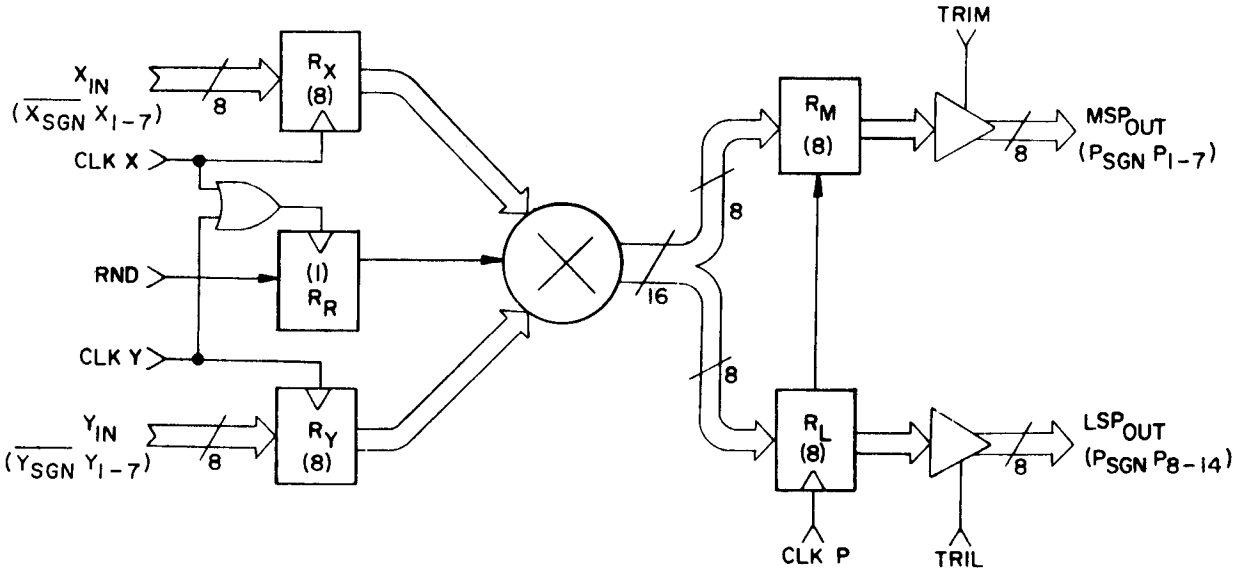


FIGURE 2. Functional block diagram - Continued.

Device 04 1/



1/ For this device, P_{SGN} is the most significant bit, and P_7 is the least significant bit for the output product. (This also applies for the X and Y inputs as well). This numbering order is different from all of the remaining device types.

FIGURE 2. Functional block diagram - Continued.

Device type 05

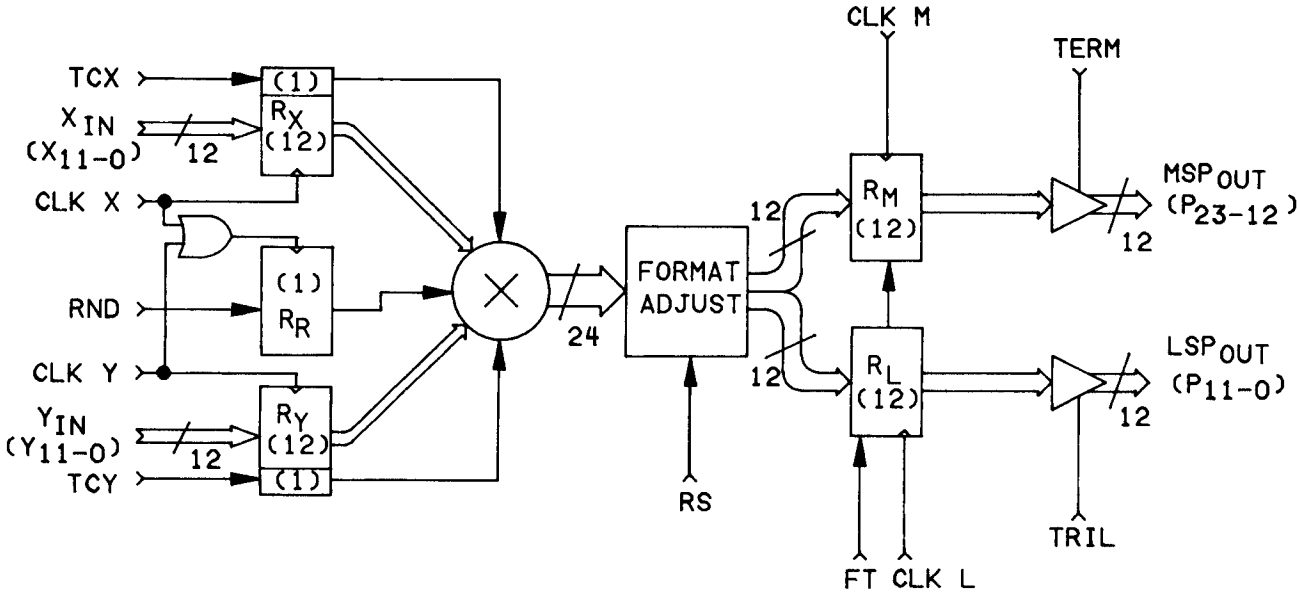


FIGURE 2. Functional block diagram - Continued.

Device type 06

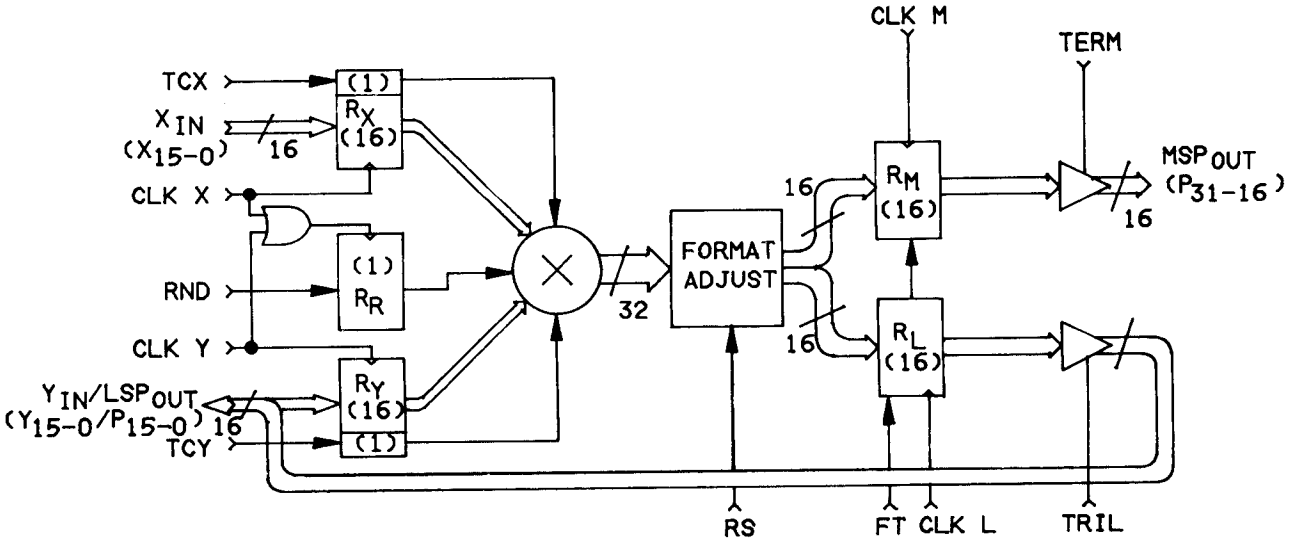


FIGURE 2. Functional block diagram - Continued.

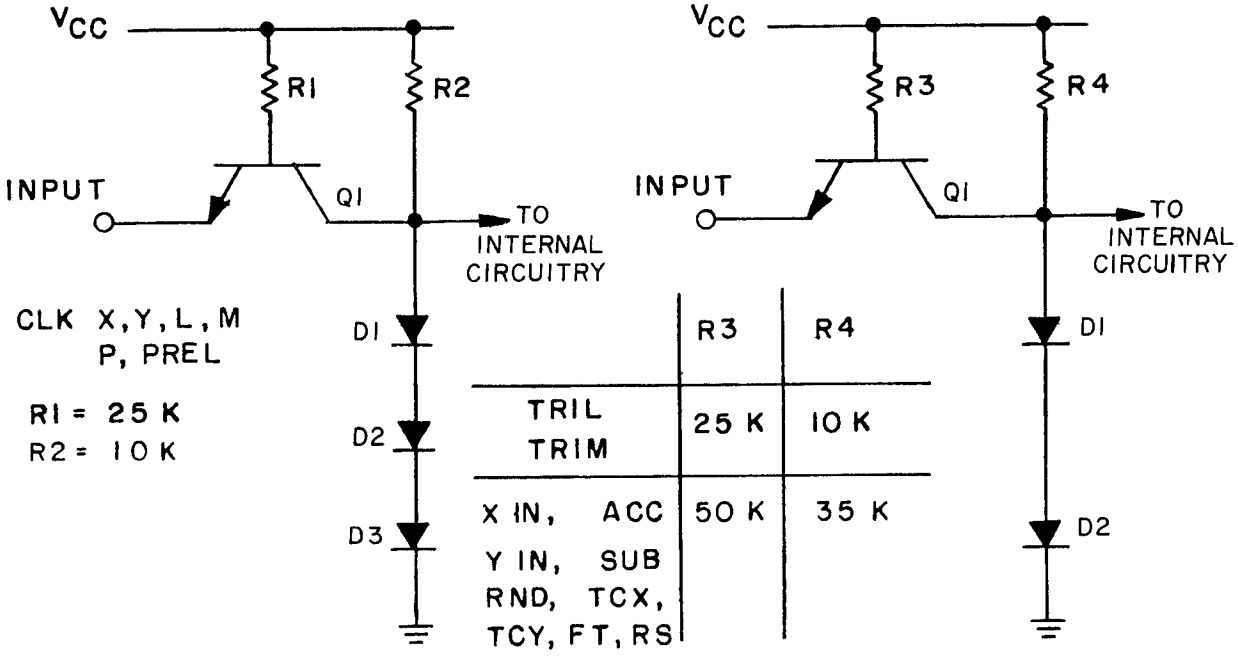


FIGURE 3A. Equivalent input schematics, per input buffer.

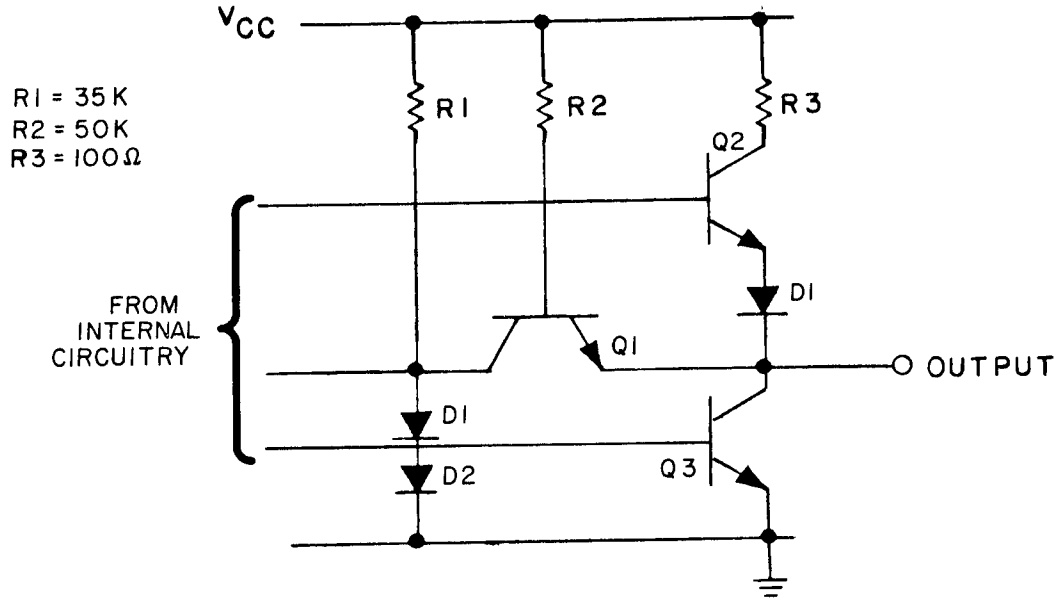


FIGURE 3B. Output/preload input schematic.

Pre-load truth table (device types 01, 02, and 03)

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	HiZ
0	0	1	0	Q	HiZ	Q
0	0	1	1	Q	HiZ	HiZ
0	1	0	0	HiZ	Q	Q
0	1	0	1	HiZ	Q	HiZ
0	1	1	0	HiZ	HiZ	Q
0	1	1	1	HiZ	HiZ	HiZ
1	0	0	0	HiZ	HiZ	HiZ
1	0	0	1	HiZ	HiZ	PL
1	0	1	0	HiZ	PL	HiZ
1	0	1	1	HiZ	PL	PL
1	1	0	0	PL	HiZ	HiZ
1	1	0	1	PL	HiZ	PL
1	1	1	0	PL	PL	HiZ
1	1	1	1	PL	PL	PL

NOTES:

HiZ = Output buffers at high impedance, or output disabled.

Q = Output buffers at low impedance. Contents of accumulator (Q) will be transferred to output register at the rising edge of CLK P.

PL = Output buffers at high impedance, or output disabled. Pre-load data (PD), supplied externally at output pins, will be loaded into the output register at the rising edge of CLK P.

FIGURE 4. Pre-load truth table (device types 01, 02, and 03).

Device types 01, 02, and 03

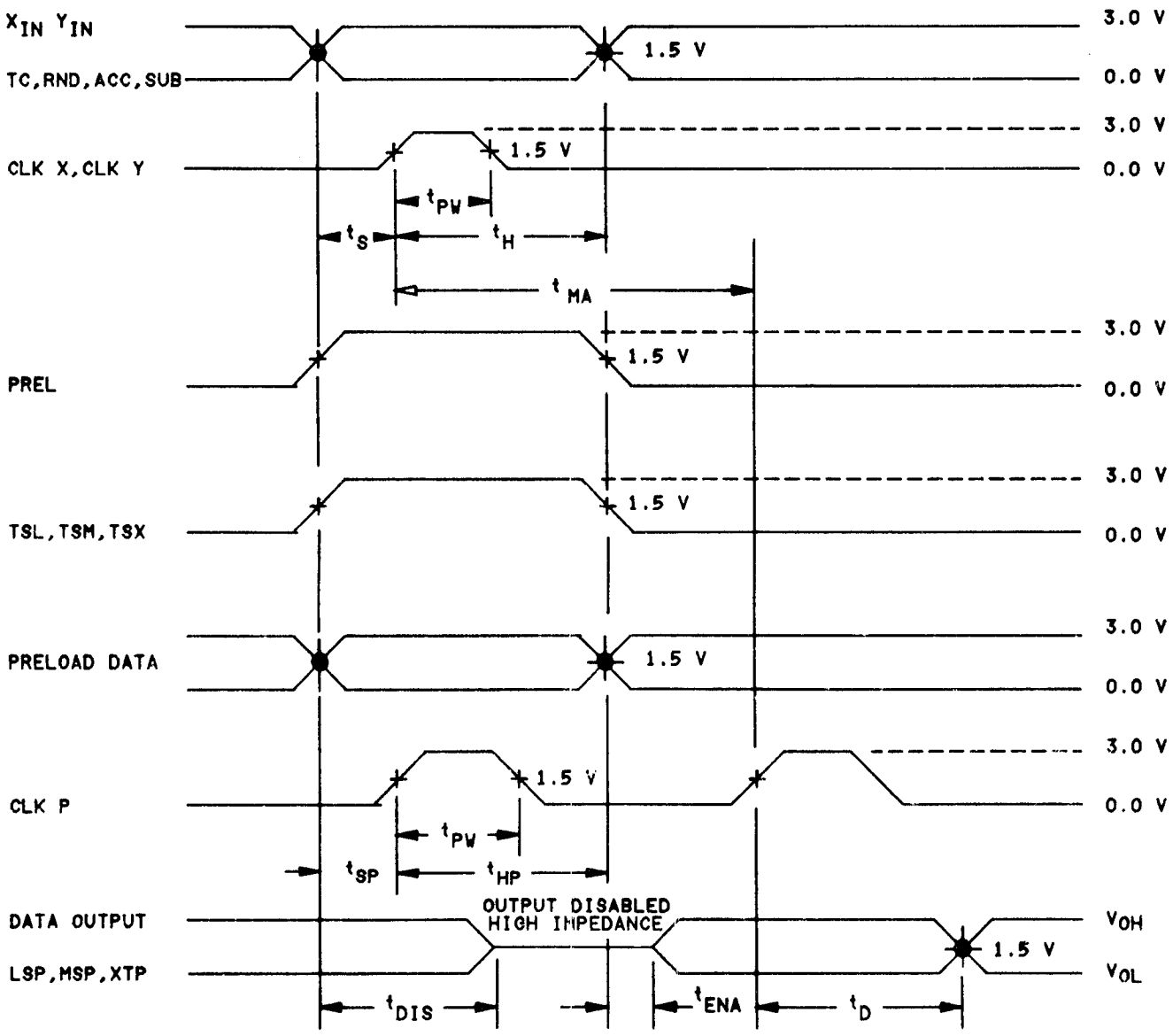


FIGURE 5A. Timing diagram.

Device types 04, 05, and 06

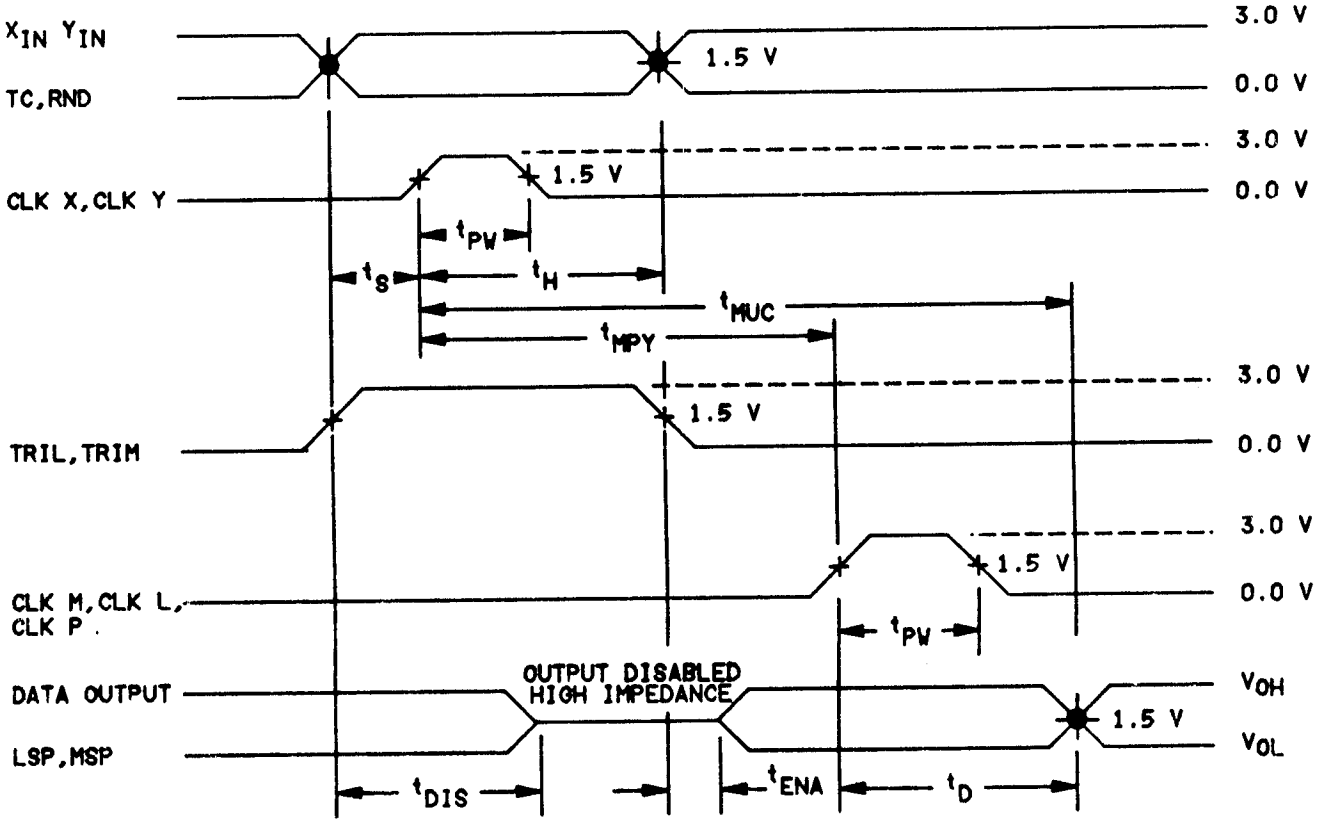
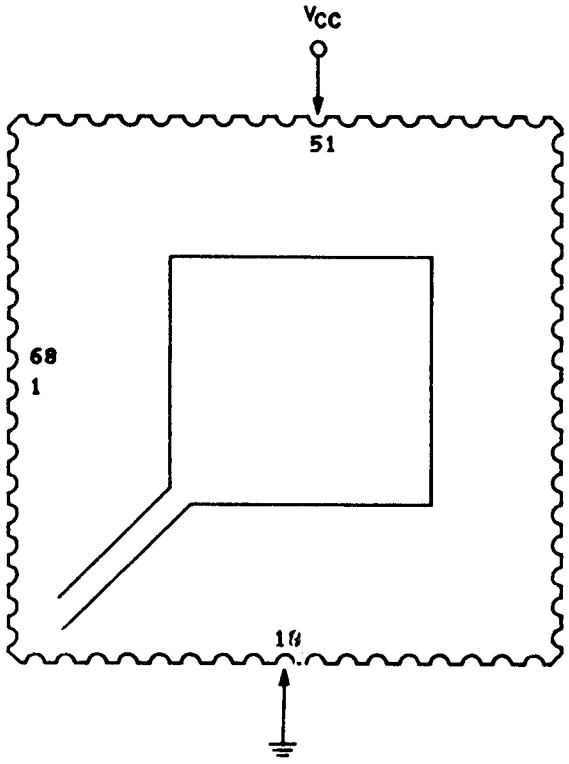


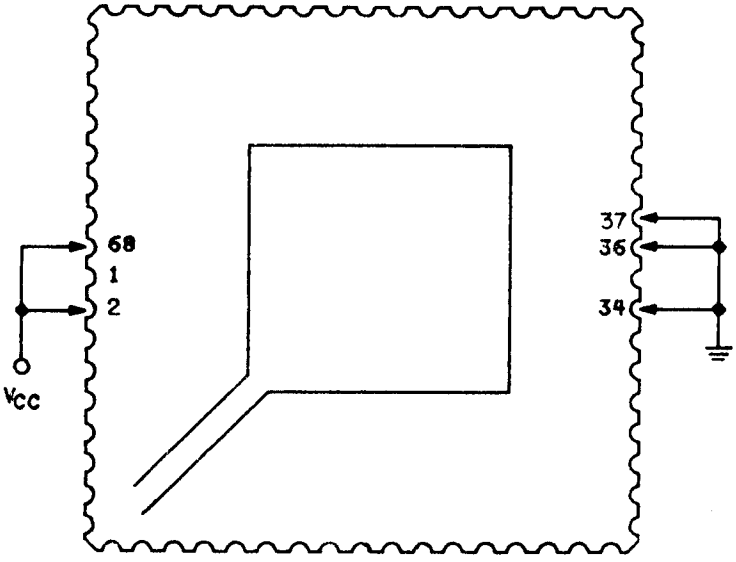
FIGURE 5B. Timing diagram.

Device type 01



PIN	FUNCTION	VOLTS
18	GND	0
51	V_{CC}	5 ±0.25

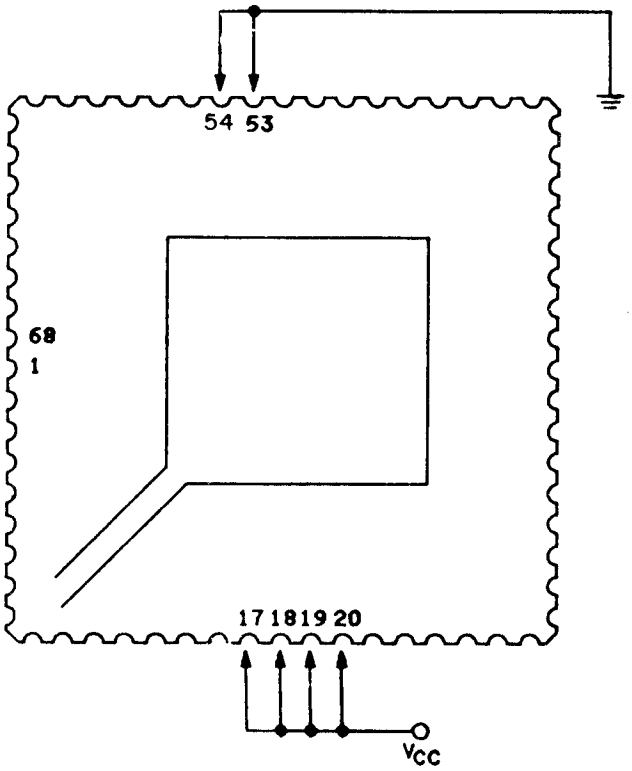
Device type 02



PIN	FUNCTION	VOLTS
2	V_{CC}	5 ±0.25
34	GND	0
36	GND	0
37	GND	0
68	V_{CC}	5 ±0.25

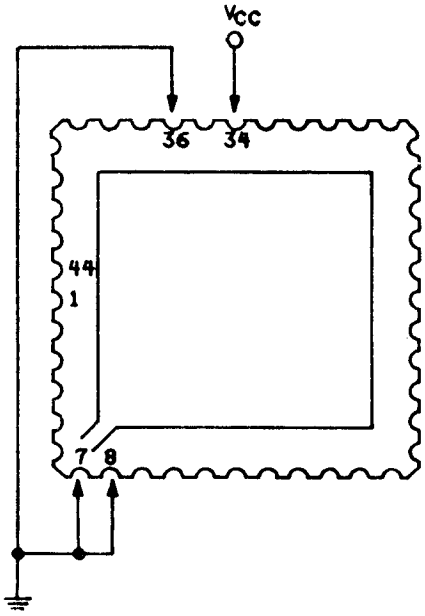
FIGURE 6. Burn-in/life test circuits.

Device type 03



PIN	FUNCTION	VOLTS
17	V_{CC}	5 ±0.25
18	V_{CC}	5 ±0.25
19	V_{CC}	5 ±0.25
20	V_{CC}	5 ±0.25
53	GND	0
54	GND	0

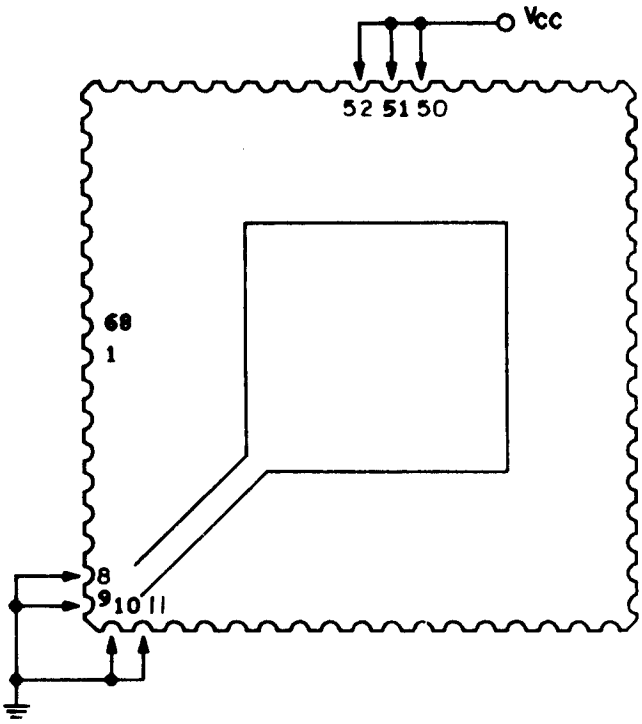
Device type 04



PIN	FUNCTION	VOLTS
7	TRIM	0
8	TRIL	0
34	V_{CC}	5 ±0.25
36	GND	0

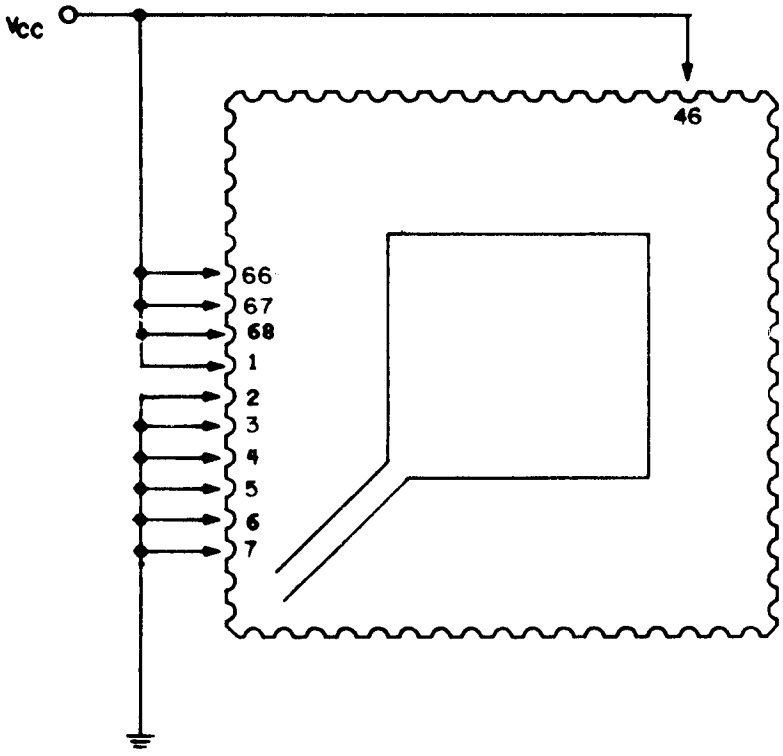
FIGURE 6. Burn-in/life test circuit - Continued.

Device type 05



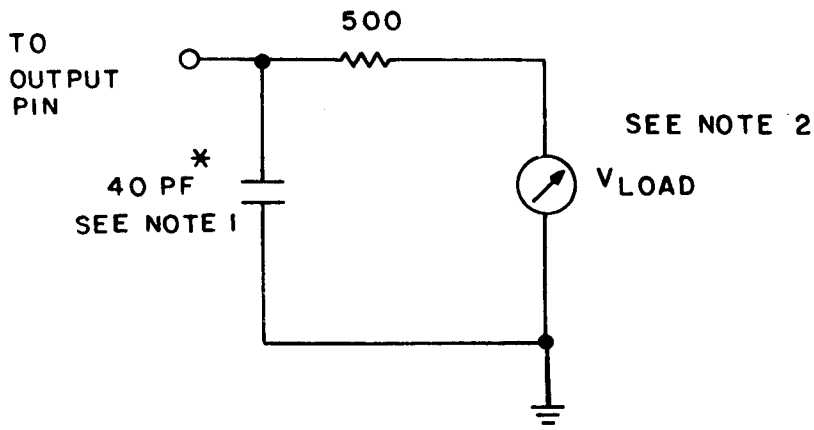
PIN	FUNCTION	VOLTS
8	RS	0
9	FT	0
10	GND	0
11	GND	0
50	V_{CC}	5 ±0.25
51	V_{CC}	5 ±0.25
52	V_{CC}	5 ±0.25

Device type 06



PIN	FUNCTION	VOLTS
1	V_{CC}	5 ±0.25
2	GND	0
3	GND	0
4	GND	0
5	FT	0
6	RS	0
7	TRIM	0
46	TRIL	5 ±0.25
66	TCX	5 ±0.25
67	TCY	5 ±0.25
68	V_{CC}	5 ±0.25

FIGURE 6. Burn-in/life test circuits - Continued.



NOTES:
1. CL = 40 pf ±10%, including scope probe, wiring and stray capacitance without package in test fixture.
2. For V_{LOAD} see table III.

FIGURE 7. AC switching time test load.

TABLE III. Electrical test specifications.

Device types: 01, 02, and 03, Multiplier accumulators
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 01 Min	01 Max	02 Min	02 Max	03 Min	03 Max	Unit
1 T_C = +25°C	1	V_{IH} high level input voltage	V_{CC} = 5.5 V. Perform functional test per table IV.	2.0		2.0		2.0		V
	2	V_{IL} low level input voltage	V_{CC} = 4.5 V. Perform functional test per table IV.		0.8		0.8		0.8	V
	3	I_{OS} short circuit output current	V_{CC} = 5.5 V, all outputs = "1", measure each output pin current at zero output voltage. 1/	-1	-40	-1	-40	-1	-40	mA
	4	V_{OH} high level output voltage	V_{CC} = 4.5 V, I_{OH} = -0.4 mA, V_{IL} = 0 V, V_{IH} = 3 V. 2/	2.4		2.4		2.4		V
	5	V_{OL} low level output voltage	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0 V, V_{IH} = 3 V.		0.5		0.5		0.5	V
	6	I_I high level input current for all inputs	V_{CC} = 5.5 V, pin under test = 5.5 V. All other input pins = 0.4. 3/ 4/		400		400		500	µA
	7	I_{IH1} high level input current for XIN, RND, SUB, ACC, TC, MSP, XTP	V_{CC} = 5.5 V, pin under test = 2.4 V. All other input pins = 0.4 V. 3/		100		100		100	"
	8	I_{IH2} high level input current for CLK X, TSL, TSM, TSX	V_{CC} = 5.5 V, pin under test = 2.4 V. All other inputs pins = 0.4 V.		100		100		100	"
	9	I_{IH3} high level input current for YIN, LSP	V_{CC} = 5.5 V, pin under test = 2.4 V, all other input pins = 0.4 V. 3/ 4/		100		100		200	"
	10	I_{IH4} high level input current for PREL, CLK Y, CLK P	V_{CC} = 5.5 V, pin under test = 2.4 V. All other input pins = 0.4 V.		100		100		200	"
	11	I_{IL1} low level input current XIN, RND, SUB, ACC, TC, MSP, XTP	V_{CC} = 5.5 V, pin under test = 0.4 V. All other inputs = 2.4 V. 3/		-400		-400		-400	"
	12	I_{IL2} low level input current CLK X, TSL, TSM, TSX	V_{CC} = 5.5 V, pin under test = 0.4 V. All other inputs = 2.4 V.		-1		-1		-1	mA

See footnotes at end of device types 01, 02, and 03.

TABLE III. Electrical test specifications - Continued.

Device types: 01, 02, and 03, Multiplier accumulators
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 01 Min	01 Max	02 Min	02 Max	03 Min	03 Max	Unit
1 T_C = +25°C	13	I_{IL3} low level input current YIN, LSP	V_{CC} = 5.5 V, pin under test = 0.4 V. All other inputs = 2.4 V. 3/ 4/	-400		-400		-800		µA
	14	I_{IL4} low level input current PREL, CLK Y, CLK P	V_{CC} = 5.5 V, pin under test = 0.4 V. All other inputs = 2.4 V.	-1		-1		-2		mA
	15	I_{CC} supply current, 5/	V_{CC} = 5.5 V, all inputs = 0 V, all outputs = "0", three-state controls = 3 V.	100	525	200	850	300	1250	mA
2 T_C = +125°C	Same tests, terminal conditions and limits as for subgroup 1 except T_C = +125°C.									
3 T_C = -55°C	Same tests, terminal conditions and limits as for subgroup 1 except omit tests 6 thru 10 and T_C = -55°C.									
7 T_C = +25°C	16	Functional verification	V_{CC} = 5.0 V. Perform functional test pattern per table IV.							
8	Same as for subgroup 7 except T_C = -55°C and T_C = +125°C.									
9 T_C = +25°C	17	t_{MA} Multiply - accumulate time from input register CLK to output register CLK	V_{CC} = 4.5 V. Perform functional test pattern per table IV. Measure delay from 1.5 V level of input clock rising edge to 1.5 V level of output clock rising edge. See figure 5a, see figure 7, V_{LOAD} = 2.2 V.	15	125	15	170	15	200	ns
	18	Output delay t_{DO}	V_{CC} = 4.5 V. Perform functional test pattern per table IV. Measure delay from 1.5 V level of the output clock to the 1.5 V level of each output signal. High and low states measured separately. See figure 5a, see figure 7, V_{LOAD} = 2.2 V.	10	45	10	45	10	45	"
	19	t_{D1}		10	45	10	45	10	45	"
	20	Three state output delay output enable t_{ENA0}	V_{CC} = 4.5 V. Measure from falling edge of TRIM and TRIL to 1.5 V level of the output signal - See figure 5a. The high and low states are measured simultaneously, see figure 7, V_{LOAD} = 1.8 V. NOTE: Only the worst case reading must be reported for test no's 5 and 6 combined.	10	45	10	45	10	45	"
	21	t_{ENA1}		10	45	10	45	10	45	"
	22	Three state output delay-output disable t_{DIS0}	V_{CC} = 4.5 V. Measure from the rising edge of TSL and TSM to V_{OL} + .5 V level (t_{DIS0}) or V_{OH} - .5 V level (t_{DIS1}). See figure 5a. The high and low states are measured separately. See figure 7, V_{LOAD} (t_{DIS0}) = 2.6 V, V_{LOAD} (t_{DIS1}) = 0.0 V.	10	45	10	45	10	45	"
	23	t_{DIS1}		10	45	10	45	10	45	"
	24	t_S input register set up time - XIN, YIN, TC, RND, ACC, SUB	V_{CC} = 4.5 V. Perform functional test pattern per table V. Measure from the leading edge of specified data inputs to the leading edge of CLK X, CLK Y. See figure 5a.		30		30		30	"

See footnotes at end of device types 01, 02, and 03.

TABLE III. Electrical test specifications - Continued.

Device types: 01, 02, and 03, Multiplier accumulators
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 01 Min	01 Max	02 Min	02 Max	03 Min	03 Max	Unit
9 T_C = +25°C	25	t_H input register hold time - XIN, YIN, TC, RND, ACC, SUB	Same conditions as test number 9 except measure from the leading edge of CLK X and CLK Y, to the trailing edge of specified data inputs.		3		3		3	ns
	26	t_{SP} preload register set up time - XTP, MSP, LSP, PREL, TSL, TSM, TSX	Same conditions as test number 9 except measure from the leading edge of CLK P to the leading edge of specified preload inputs.		5		5		5	"
	27	t_{HP} preload register hold time - XTP, MSP, LSP, PREL, TSL, TSM, TSX	Same conditions as test number 9 except measure from the leading edge of CLK P to the trailing edge of specified preload inputs.		3		3		3	"
10 T_C = +125°C	Same tests terminal conditions and limits as for subgroup 9 except T_C = +125°C.									
11 T_C = -55°C	Same tests terminal conditions and limits as for subgroup 9 except T_C = -55°C.									

1/ No more than one output shorted at a time. Short circuit duration not to exceed one second. Data output level may change state under I_{OS} test conditions. In such cases, I_{OS} test limit will be 0 mA min.
2/ V_{IL} = 0.65 V for CLK P input for device 02.
3/ All input pins = 0.4 V except PREL, TSL, TSM and TSX must be at 2.4 V during measurement of MSP, LSP and XTP pins.
4/ TSL must be high during measurement of YIN, for device type 03.
5/ Worst case static current.

TABLE III. Electrical test specifications - Continued.

Device types: 04, 05, and 06, Multiplier
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 04 Min	04 Max	05 Min	05 Max	06 Min	06 Max	Unit
1 T_C = +25°C	1	V_{IH} high level input voltage	V_{CC} = 5.5 V. Perform functional test per table IV.	2.0		2.0		2.0		V
	2	V_{IL} low level input voltage	V_{CC} = 4.5 V. Perform functional test per table IV.		0.8		0.8		0.8	V
	3	I_{OS} short circuit output current	V_{CC} = 5.5 V. All outputs = "1". Measure each output pin current at zero output voltage one at a time. 1/	-1	-40	-1	-40	-1	-40	mA
	4	V_{OH} high level output voltage	V_{CC} = 4.5 V, I_{OH} = -0.4 mA, V_{IL} = 0 V, V_{IH} = 3 V.	2.4		2.4		2.4		V
	5	V_{OL} low level output voltage	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0 V, V_{IH} = 3 V.		0.5		0.5		0.5	V
	6	I_I high level input current for all inputs	V_{CC} = 5.5 V. V_{IH} = 5.5 V on pin under test. All other input pins = 0.4 V. 2/		300		300		300	μA
	7	I_{IH1} high level input current for RND, XIN, YIN, FT	V_{CC} = 5.5 V. Pin under test = 2.4 V. All other inputs at 0.4 V. 2/		100		100		100	"
	8	I_{IH2} high level input current for TCX, TCY, RS	V_{CC} = 5.5 V. Pin under test = 2.4 V. All other inputs at 0.4 V.		100		100		100	"
	9	I_{IH3} high level input current for CLK X, CLK L, CLK M, TRIL, TRIM 3/	V_{CC} = 5.5 V. Pin under test = 2.4 V. All other inputs at 0.4 V.		100		100		100	"
	10	I_{IH4} high level input current for CLK P	V_{CC} = 5.5 V. Pin under test = 2.4 V. All other inputs at 0.4 V.		200		---		---	"
	11	I_{IH5} high level input current CLK Y	V_{CC} = 5.5 V. Pin under test = 2.4 V. All other inputs at 0.4 V.		100		100		200	"
	12	I_{IL1} low level input current for XIN, YIN, RND, FT pins	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V. 2/	-4	-400	-40	-400	-40	-400	"
	13	I_{IL2} low level input currents for TCX, TCY, RS	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V.		---	-40	-800	-40	-800	"

See footnotes at end of device types 04, 05, and 06.

TABLE III. Electrical test specifications - Continued.

Device types: 04, 05, and 06, Multiplier
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 04 Min	04 Max	05 Min	05 Max	06 Min	06 Max	Unit
1 T_C = +25°C	14	I_{IL3} low level input current for CLK X, CLK M, CLK L, TRIL and TRIM 3/	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V.	-40	-1000	-40	-1000	-40	-1000	µA
	15	I_{IL4} low level input currents CLK P	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V.	-40	-2000		---		---	"
	16	I_{IL5} low level input current for CLK Y	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V.	-40	-1000	-40	-1000	-40	-2000	"
	17	I_{OZH} off-state output current, high level voltage applied 4/	V_{CC} = 5.5 V, outputs = "0", three-state controls = 3 V. Force V_O = 2.4 V.		40		40		40	"
	18	I_{OZL} off-state output current low level voltage applied 4/	V_{CC} = 5.5 V. Pin under test = 0.4 V. All other inputs = 2.4 V.		-40		-40		-40	"
	19	I_{CC} supply current 5/	V_{CC} = 5.5 V. All inputs = 0 V. All outputs = "0". Three-state controls = 3 V.	100	450	200	750	300	1050	mA
2 T_C = +125°C	Same tests, terminal conditions and limits as for subgroup 1 except T_C = +125°C.									
3 T_C = -55°C	Same tests, terminal conditions and limits as for subgroup 1 except omit tests 6 thru 11 and T_C = -55°C.									
7 T_C = +25°C	20	Functional verification	V_{CC} = 5.0 V. Perform functional test pattern per table IV.							
8	Same as for subgroup 7 except T_C = -55°C and T_C = +125°C.									
9 T_C = +25°C	21	t_{MC} clocked multiply time from input register CLK to output register CLK	V_{CC} = 4.5 V. Perform functional test pattern per table IV. Measure delay from 1.5 V level of input clock rising edge to 1.5 V level of output clock rising edge. See figure 5b. See figure 7, V_{LOAD} = 2.2 V.	15	115	15	140	15	185	ns
	22	t_{MUC} unclocked multiply time from input register CLK to output signal	V_{CC} = 4.5 V. Perform functional test per table IV. Measure delay from 1.5 V level of input clock rising edge to 1.5 V level of output signal. See figure 5b. See figure 7, V_{LOAD} = 2.2 V.				185		230	"
	23 24	Output delay t_{DO} t_{D1}	V_{CC} = 4.5 V. Perform functional test per table IV. Measure delay from 1.5 V level of the output clock to the 1.5 V level of each output signal. High and low states measured separately. See figure 5b. See figure 7, V_{LOAD} = 2.2 V.	10 10	45 45	10 10	45 45	10 10	45 45	" "

See footnotes at end of device types 04, 05, and 06.

TABLE III. Electrical test specifications - Continued.

Device types: 04, 05, and 06, Multiplier
Tests over recommended temperature range.

Subgroup	Test number	Parameter	Test conditions	Device types 04 Min	04 Max	05 Min	05 Max	06 Min	06 Max	Unit
9 T_C = +25°C	25	Three state output delay-output enable t_{ENA0}	V_{CC} = 4.5 V. Measure from the falling edge of TRIM and TRIL to 1.5 V level of the output signal. High and low states measured simultaneously. See figure 5b. See figure 7, V_{LOAD} = 1.8 V. NOTE: Only the worst case reading must be reported for test no's 6 and 7 combined.	10	45	10	45	10	45	ns
	26	t_{ENA1}		10	45	10	45	10	45	"
	27	Three state output delay-output disable t_{DIS0}	V_{CC} = 4.5 V. Measure from the rising edge of TRIL and TRIM to V_{OL} + .5 V level (t_{DIS0}) or V_{OH} - .5 V level (t_{DIS1}). High and low state measured separately. See figure 5b. See figure 7, V_{LOAD} (t_{DIS0}) = 2.6 V, V_{LOAD} (t_{DIS1}) = 0.0 V.	10	45	10	45	10	45	"
	28	t_{DIS1}		10	45	10	45	10	45	"
	29	t_S input register set up time - XIN, YIN, TCX, TCY, RND	V_{CC} = 4.5 V. Perform functional test pattern per table V. Measure from the leading edge of specified data inputs to the leading edge of CLK X, CLK Y. See figure 5b.		30		30		30	"
	30	t_H input register hold time - XIN, YIN, TCX, TCY, RND	V_{CC} = 4.5 V. Perform functional test pattern per table V. Measure from the leading edge of CLK X and CLK Y, to the trailing edge of specified data inputs.		3		3		3	"
10 T_C = +125°C	Same tests terminal conditions and limits as for subgroup 9 except T_C = +125°C.									
11 T_C = -55°C	Same tests terminal conditions and limits as for subgroup 9 except T_C = -55°C.									

1/ No more than one output shorted at a time. Short circuit duration not to exceed one second. Data output level may change state under I_{OS} test conditions. In such cases, I_{OS} test limit will be ø mA min.
2/ TRIL pin = 2.4 V during measurement of YIN pins on device type 06.
3/ Input current for CLK X, TRIL, TRIM inputs only for device 04.
4/ MSP outputs only for device 06.
5/ Worst case static current.

TABLE IV. Functional test pattern for device type 01.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
1.	110	111	00000	00	00	*MMMMM	*IIIII
2.	001	000	00000	00	00	00000	IIIII
3.	110	111	00000	FF	FF	MMMMM	IIIII
4.	001	000	00000	FF	FF	0FE01	IIIII
5.	110	111	00000	FF	00	MMMMM	IIIII
6.	001	000	00000	FF	000	00000	IIIII
7.	110	111	00000	FF	01	MMMMM	IIIII
8.	001	000	00000	FF	01	000FF	IIIII
9.	110	111	00000	FF	80	MMMMM	IIIII
10.	001	000	00000	FF	80	07F80	IIIII
11.	110	11	00000	60	7F	MMMMM	IIIII
12.	001	000	00000	60	7F	02FA0	IIIII
13.	110	111	00000	70	55	MMMMM	IIIII
14.	001	000	00000	70	55	02530	IIIII
15.	110	111	00000	70	2A	MMMMM	IIIII
16.	001	000	00000	70	2A	01260	IIIII
17.	110	111	00000	48	E0	MMMMM	IIIII
18.	001	000	00000	48	E0	03F00	IIIII
19.	110	111	00000	30	FF	MMMMM	IIIII
20.	001	000	00000	30	FF	02FD0	IIIII
21.	110	111	00000	01	FF	MMMMM	IIIII
22.	001	000	00000	01	FF	000FF	IIIII
23.	110	111	01100	01	FF	MMMMM	IIIII
24.	001	000	01100	01	FF	00000	IIIII
25.	110	111	00000	38	55	MMMMM	IIIII
26.	001	000	00000	38	55	01298	IIIII
27.	110	111	00000	38	15	MMMMM	IIIII
28.	001	000	00000	38	15	00498	IIIII
29.	110	111	00000	78	55	MMMMM	IIIII
30.	001	000	00000	78	55	027D8	IIIII
31.	110	111	00000	78	2A	MMMMM	IIIII
32.	001	000	00000	78	2A	013B0	IIIII
33.	110	111	00000	00	80	MMMMM	IIIII
34.	001	000	00000	00	80	00000	IIIII
35.	110	111	00000	30	60	MMMMM	IIIII
36.	001	000	00000	30	60	01200	*IIIII
37.	110	111	00000	70	60	*MMMMM	IIIII
38.	001	000	00000	70	60	02A00	IIIII
39.	110	111	00000	1C	55	MMMMM	IIIII
40.	001	000	00000	1C	55	0094C	IIIII
41.	110	111	00000	1C	2A	MMMMM	IIIII
42.	001	000	00000	1C	2A	00498	IIIII
43.	110	111	00000	3C	55	MMMMM	IIIII
44.	001	000	00000	3C	55	013EC	IIIII
45.	110	111	00000	3C	2A	MMMMM	IIIII
46.	001	000	00000	3C	2A	009D8	IIIII
47.	110	111	00000	18	60	MMMMM	IIIII
48.	001	000	00000	18	60	00900	IIIII
49.	110	111	00000	38	30	MMMMM	IIIII
50.	001	000	00000	38	30	00A80	IIIII
51.	110	111	00000	0E	55	MMMMM	IIIII
52.	001	000	00000	0E	55	004A6	IIIII
53.	110	111	00000	0E	2A	MMMMM	IIIII
54.	001	000	00000	0E	2A	0024C	IIIII
55.	110	111	00000	1E	55	MMMMM	IIIII
56.	001	000	00000	1E	55	009F6	IIIII
57.	110	111	00000	1E	29	MMMMM	IIIII
58.	001	000	00000	1E	29	004CE	IIIII

See footnotes at end of device type 01.

TABLE IV. Functional test pattern for device type 01 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
59.	110	111	00000	0C	60	MMMMM	*IIIII
60.	001	000	00000	0C	60	00480	IIIII
61.	110	111	00001	00	00	MMMMM	IIIII
62.	001	000	00001	00	00	00000	IIIII
63.	110	111	00001	80	01	MMMMM	IIIII
64.	001	000	00001	80	01	7FF80	IIIII
65.	110	111	00001	80	00	MMMMM	IIIII
66.	001	000	00001	80	00	00000	IIIII
67.	110	111	00001	C0	2A	MMMMM	IIIII
68.	001	000	00001	C0	2A	7F580	IIIII
69.	110	111	00001	C0	55	MMMMM	IIIII
70.	001	000	00001	C0	55	7EAC0	IIIII
71.	110	111	00001	E0	2A	MMMMM	*IIIII
72.	001	000	00001	E0	2A	7FAC0	IIIII
73.	110	111	00001	E0	55	MMMMM	IIIII
74.	001	000	00001	E0	55	7F560	IIIII
75.	110	111	00001	90	A0	MMMMM	IIIII
76.	001	000	00001	90	A0	02A00	IIIII
77.	110	111	00001	C0	C0	MMMMM	IIIII
78.	001	000	00001	C0	C0	01000	IIIII
79.	110	111	00001	48	E0	MMMMM	IIIII
80.	001	000	00001	48	E0	7F700	IIIII
81.	110	111	00001	30	FF	MMMMM	IIIII
82.	001	000	00001	30	FF	7FFD0	IIIII
83.	110	111	00001	70	FF	MMMMM	IIIII
84.	001	000	00001	70	FF	7FF90	IIIII
85.	110	111	00001	00	80	MMMMM	IIIII
86.	001	000	00001	00	80	00000	IIIII
87.	110	111	00001	18	FF	MMMMM	IIIII
88.	001	000	00001	18	FF	7FFE8	IIIII
89.	110	111	00001	38	FF	MMMMM	IIIII
90.	001	000	00001	38	FF	7FFC8	IIIII
91.	110	111	00001	0C	FF	MMMMM	IIIII
92.	001	000	00001	0C	FF	7FFF4	IIIII
93.	110	111	00001	1C	FF	MMMMM	IIIII
94.	001	000	00001	1C	FF	7FFE4	IIIII
95.	110	111	00001	1C	60	MMMMM	IIIII
96.	001	000	00001	1C	60	00A80	IIIII
97.	110	111	00001	06	FF	MMMMM	IIIII
98.	001	000	00001	06	FF	7FFFA	IIIII
99.	110	111	00001	07	55	MMMMM	IIIII
100.	001	000	00001	07	55	00253	IIIII
101.	110	111	00001	07	2A	MMMMM	IIIII
102.	001	000	00001	07	2A	00126	IIIII
103.	110	111	00001	0E	FF	MMMMM	IIIII
104.	001	000	00001	0E	FF	7FFF2	IIIII
105.	110	111	00001	0F	55	MMMMM	IIIII
106.	001	000	00001	0F	55	004FB	IIIII
107.	110	111	00001	0F	2A	*MMMMM	*IIIII
108.	001	000	00001	0F	2A	00276	IIIII
109.	110	111	00001	06	60	MMMMM	IIIII
110.	001	000	00001	06	60	00240	IIIII
111.	110	111	00001	0E	60	MMMMM	IIIII
112.	001	000	00001	0E	60	00540	IIIII
113.	110	111	00001	03	FF	MMMMM	IIIII
114.	001	000	00001	03	FF	7FFFD	IIIII
115.	110	111	00001	03	55	MMMMM	IIIII
116.	001	000	00001	03	55	000FF	IIIII

See footnotes at end of device type 01.

TABLE IV. Functional test pattern for device type 01 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
117.	110	111	00001	03	2A	MMMMM	*IIIII
118.	001	000	00001	03	2A	0007E	IIIII
119.	110	111	00001	07	FF	MMMMM	IIIII
120.	001	000	00001	07	FF	7FFF9	IIIII
121.	110	111	00001	03	60	MMMMM	IIIII
122.	001	000	00001	03	60	00120	IIIII
123.	110	111	00001	07	60	MMMMM	IIIII
124.	001	000	00001	07	60	002A0	IIIII
125.	110	111	00001	01	FF	MMMMM	IIIII
126.	001	000	00001	01	FF	7FFFF	IIIII
127.	110	111	0001	01	55	MMMMM	IIIII
128.	001	000	00001	01	55	00055	IIIII
129.	110	111	00001	01	2A	MMMMM	IIIII
130.	001	000	00001	01	2A	0002A	IIIII
131.	110	111	00001	01	30	MMMMM	IIIII
132.	001	000	00001	01	30	00030	IIIII
133.	110	111	00011	00	00	MMMMM	IIIII
134.	001	000	00011	00	00	00080	IIIII
135.	110	111	00011	78	55	MMMMM	IIIII
136.	001	000	00011	78	55	02858	IIIII
137.	110	111	00011	80	01	MMMMM	IIIII
138.	001	000	00011	80	01	00000	IIIII
139.	110	111	00011	70	60	MMMMM	IIIII
140.	001	000	00011	70	60	02A80	IIIII
141.	110	111	00011	0E	60	*MMMMM	*IIIII
142.	001	000	00011	0E	60	005C0	IIIII
143.	110	111	00001	00	00	MMMMM	IIIII
144.	001	000	00001	00	00	00000	IIIII
145.	110	111	00001	01	20	MMMMM	IIIII
146.	001	000	00001	01	20	00020	IIIII
147.	110	111	00101	01	E0	MMMMM	IIIII
148.	001	000	00101	01	E0	00000	IIIII
149.	110	111	00101	03	55	MMMMM	IIIII
150.	001	000	00101	03	55	000FF	IIIII
151.	110	111	00101	03	55	MMMMM	IIIII
152.	001	000	00101	03	55	001FE	IIIII
153.	110	111	00101	03	55	MMMMM	IIIII
154.	001	000	00101	03	55	002FD	IIIII
155.	110	111	00101	70	60	MMMMM	IIIII
156.	001	000	00101	70	60	02CFD	IIIII
157.	110	111	00101	01	FF	MMMMM	IIIII
158.	001	000	00101	01	DD	02CFC	IIIII
159.	110	111	00101	C0	55	MMMMM	IIIII
160.	001	000	00101	C0	55	017BC	IIIII
161.	110	111	00101	80	80	MMMMM	IIIII
162.	001	000	00101	80	80	057BC	IIIII
163.	110	111	00101	80	80	MMMMM	IIIII
164.	001	000	00101	80	80	097BC	IIIII
165.	110	111	00101	7F	7F	MMMMM	IIIII
166.	001	000	00101	7F	7F	0D6BD	IIIII
167.	110	111	00101	80	80	MMMMM	IIIII
168.	001	000	00101	80	80	116BD	IIIII
169.	110	111	00101	00	00	MMMMM	IIIII
170.	001	000	00101	00	00	116B2	IIIII
171.	110	111	01101	80	80	MMMMM	IIIII
172.	001	000	01101	80	80	72943	IIIII
173.	110	111	01101	01	01	MMMMM	IIIII
174.	001	000	01101	01	01	0D6BE	IIIII

See footnotes at end of device type 01.

TABLE IV. Functional test pattern for device type 01 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
175.	110	111	01101	06	60	MMMMM	*IIIII
176.	001	000	01101	06	60	72B82	IIIII
177.	110	111	01101	00	00	*MMMMM	*IIIII
178.	001	000	01101	00	00	0D47E	IIIII
179.	110	111	00001	00	00	MMMMM	IIIII
180.	001	000	00001	00	00	00000	IIIII
181.	110	111	00001	01	FF	MMMMM	IIIII
182.	001	000	00001	01	FF	7FFFF	IIIII
183.	110	111	00001	00	00	MMMMM	IIIII
184.	001	000	00001	00	00	00000	IIIII
185.	001	111	10001	00	00	MMMMM	7FFFF
186.	000	000	00001	00	00	7FFFF	IIIII
187.	001	000	00001	00	00	00000	IIIII
188.	001	110	10001	00	00	MMMMM	7FFFF
189.	000	000	00001	00	00	7FF00	IIIII
190.	001	000	00001	00	00	00000	IIIII
191.	001	101	10001	00	00	MMMMM	7FFFF
192.	000	000	00001	00	00	700FF	IIIII
193.	001	000	00001	00	00	00000	IIIII
194.	001	011	10001	00	00	MMMMM	7FFFF
195.	000	000	00001	00	00	0FFFF	IIIII
196.	001	000	00001	00	00	00000	IIIII
197.	001	111	10001	00	00	MMMMM	2AAAA
198.	000	000	00001	00	00	2AAAA	IIIII
199.	001	000	00001	00	00	00000	IIIII
200.	001	111	10001	00	00	MMMMM	55555
201.	000	000	00000	00	00	55555	IIIII

1/ MSD = Most significant digit.

2/ The most significant digit (MSD) in the output column represents the extended product (XTP). However, the XTP has only 3 bits, while a hexadecimal digit can represent 4 bits. The notation used in this table appends a 0 to the left of the 3 bits of the XTP output. Therefore, the MSD ranges from 0 to 7, inclusive.

*Note: For outputs M = MASK
For preload outputs I = INHIBIT

TABLE IV. Functional test pattern for device type 02.

Line	CCC LLL KKK XYP	TTT SSS SML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
1.	110	111	00000	000	000	*MMMMMMM	*IIIIIII
2.	001	000	00000	000	000	0000000	IIIIIII
3.	110	111	00000	FFF	FFF	MMMMMMM	IIIIIII
4.	001	000	00000	FFF	FFF	0FFE001	IIIIIII
5.	110	111	00000	FFF	000	MMMMMMM	IIIIIII
6.	001	000	00000	FFF	000	0000000	IIIIIII
7.	110	111	00000	C30	FFF	MMMMMMM	IIIIIII
8.	001	000	00000	C30	FFF	0C2F3D0	IIIIIII
9.	110	111	00000	E38	AAA	MMMMMMM	IIIIIII
10.	001	000	00000	E38	AAA	097A130	IIIIIII
11.	110	111	00000	E38	555	MMMMMMM	IIIIIII
12.	001	000	00000	E38	555	04BD098	IIIIIII
13.	110	111	00000	924	C30	MMMMMMM	IIIIIII
14.	001	000	00000	924	C30	06F66C0	IIIIIII
15.	110	111	00000	618	FFF	MMMMMMM	IIIIIII
16.	001	000	00000	618	FFF	06179E8	IIIIIII
17.	110	111	00000	71C	AAA	MMMMMMM	IIIIIII
18.	001	000	00000	71C	AAA	04BD098	IIIIIII
19.	110	111	00000	71C	28A	MMMMMMM	IIIIIII
20.	001	000	00000	71C	28A	0120D18	IIIIIII
21.	110	111	00000	F3C	AAA	MMMMMMM	IIIIIII
22.	001	000	00000	F3C	AAA	0A275D8	IIIIIII
23.	110	111	00000	F3C	555	MMMMMMM	IIIIIII
24.	001	000	00000	F3C	555	0513AEC	IIIIIII
25.	110	111	00000	618	C30	MMMMMMM	IIIIIII
26.	001	000	00000	618	C30	04A4480	IIIIIII
27.	110	111	00000	E38	C30	MMMMMMM	IIIIIII
28.	001	000	00000	E38	C30	0AD4A80	IIIIIII
29.	110	111	00000	38E	AAA	MMMMMMM	IIIIIII
30.	001	000	00000	38E	AAA	025E84C	IIIIIII
31.	110	111	00000	38E	555	MMMMMMM	IIIIIII
32.	001	000	00000	38E	555	012F426	IIIIIII
33.	110	111	00000	79E	AAA	MMMMMMM	IIIIIII
34.	001	000	00000	79E	AAA	0513AEC	IIIIIII
35.	110	111	00000	79E	555	MMMMMMM	IIIIIII
36.	001	000	00000	79E	555	0289D76	*IIIIIII
37.	110	111	00000	30C	C30	*MMMMMMM	IIIIIII
38.	001	000	00000	30C	C30	0252240	IIIIIII
39.	110	111	00000	71C	618	MMMMMMM	IIIIIII
40.	001	000	00000	71C	618	02B52A0	IIIIIII
41.	110	111	00000	1C7	AAA	MMMMMMM	IIIIIII
42.	001	000	00000	1C7	AAA	012F426	IIIIIII
43.	110	111	00000	1C7	555	MMMMMMM	IIIIIII
44.	001	000	00000	1C7	555	0097A13	IIIIIII
45.	110	111	00000	3CF	AAA	MMMMMMM	IIIIIII
46.	001	111	00000	3CF	AAA	0289D76	IIIIIII
47.	110	111	00000	3CF	514	MMMMMMM	IIIIIII
48.	001	000	00000	3CF	514	013572C	IIIIIII
49.	110	111	00000	186	C30	MMMMMMM	IIIIIII
50.	001	000	00000	186	C30	0129120	IIIIIII
51.	110	111	00001	000	000	MMMMMMM	IIIIIII
52.	001	000	00001	000	000	0000000	IIIIIII
53.	110	111	00001	820	555	MMMMMMM	IIIIIII
54.	001	000	00001	820	555	7D602A0	IIIIIII
55.	110	111	00001	820	AAA	MMMMMMM	IIIIIII
56.	001	000	00001	820	AAA	02A0540	IIIIIII
57.	110	111	00001	C30	555	MMMMMMM	IIIIIII
58.	001	000	00001	C30	555	7EBABF0	IIIIIII

See footnotes at end of device type 02.

TABLE IV. Functional test pattern for device type 02 - Continued.

Line	CCC LLL KKK XYP	TTT SSS SML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
59.	110	111	00001	C30	AAA	MMMMMMM	*IIIIIII
60.	001	000	00001	C30	AAA	01457E0	IIIIIII
61.	110	111	00001	208	410	MMMMMMM	IIIIIII
62.	001	000	00001	208	410	0084080	IIIIIII
63.	110	111	00001	820	820	MMMMMMM	IIIIIII
64.	001	000	00001	820	820	03E0400	IIIIIII
65.	110	111	00001	924	C30	MMMMMMM	IIIIIII
66.	001	000	00001	924	C30	01A26C0	IIIIIII
67.	110	111	00001	618	FFF	MMMMMMM	IIIIIII
68.	001	000	00001	618	FFF	7FFF9E8	IIIIIII
69.	110	111	00001	E38	FFF	MMMMMMM	IIIIIII
70.	001	000	00001	E38	FFF	00001C8	*IIIIIII
71.	110	111	00001	30C	FFF	*MMMMMMM	IIIIIII
72.	001	000	00001	30C	FFF	7FFFCF4	IIIIIII
73.	110	111	00001	71C	FFF	MMMMMMM	IIIIIII
74.	001	000	00001	71C	FFF	7FFF8E4	IIIIIII
75.	110	111	00001	186	FFF	MMMMMMM	IIIIIII
76.	001	000	00001	186	FFF	7FFFE7A	IIIIIII
77.	110	111	00001	38E	FFF	MMMMMMM	IIIIIII
78.	001	000	00001	38E	FFF	7FFFC72	IIIIIII
79.	110	111	00001	38E	C30	MMMMMMM	IIIIIII
80.	001	000	00001	38E	C30	7F272A0	IIIIIII
81.	110	111	00001	0C3	FFF	MMMMMMM	IIIIIII
82.	001	000	00001	0C3	FFF	7FFFF3D	IIIIIII
83.	110	111	00001	0C3	AAA	MMMMMMM	IIIIIII
84.	001	000	00001	0C3	AAA	7FBEF7E	IIIIIII
85.	110	111	00001	0C3	555	MMMMMMM	IIIIIII
86.	001	000	00001	0C3	555	0040FBF	IIIIIII
87.	110	111	00001	1C7	FFF	MMMMMMM	IIIIIII
88.	001	000	00001	1C7	FFF	7FFFE39	IIIIIII
89.	110	111	00001	1C7	AAA	MMMMMMM	IIIIIII
90.	001	000	00001	1C7	AAA	7F68426	IIIIIII
91.	110	111	00001	1C7	555	MMMMMMM	IIIIIII
92.	001	000	00001	1C7	555	0097A13	IIIIIII
93.	110	111	00001	0C3	C30	MMMMMMM	IIIIIII
94.	001	000	00001	0C3	C30	7FD1890	IIIIIII
95.	110	111	00001	1C7	C30	MMMMMMM	IIIIIII
96.	001	000	00001	1C7	C30	7F93950	IIIIIII
97.	110	111	00001	041	FFF	MMMMMMM	IIIIIII
98.	001	000	00001	041	FFF	7FFFFBF	IIIIIII
99.	110	111	00001	041	AAA	MMMMMMM	IIIIIII
100.	001	000	00001	041	AAA	7FEA52A	IIIIIII
101.	110	111	00001	041	555	MMMMMMM	IIIIIII
102.	001	000	00001	041	555	0015A95	IIIIIII
103.	110	111	00001	0C3	FFF	MMMMMMM	IIIIIII
104.	001	000	00001	0C3	FFF	7FFFF3D	IIIIIII
105.	110	111	00001	041	C30	*MMMMMMM	*IIIIIII
106.	001	000	00001	041	C30	7FF0830	IIIIIII
107.	110	111	00001	0C3	C30	MMMMMMM	IIIIIII
108.	001	000	00001	0C3	C30	7FD1890	IIIIIII
109.	110	111	00001	000	000	MMMMMMM	IIIIIII
110.	001	000	00001	000	000	0000000	IIIIIII
111.	110	111	00011	F3C	AAA	MMMMMMM	IIIIIII
112.	001	000	00011	F3C	AAA	0041DD8	IIIIIII
113.	110	111	00011	000	000	MMMMMMM	IIIIIII
114.	001	000	00011	000	000	0000800	IIIIIII
115.	110	111	00011	E38	C30	MMMMMMM	IIIIIII
116.	001	000	00011	E38	C30	006D280	IIIIIII

See footnotes at end of device type 02.

TABLE IV. Functional test pattern for device type 02 - Continued.

Line	CCC LLL KKK XYP	TTT SSS ML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
117.	110	111	00011	1C7	C30	MMMMMMM	*IIIIIII
118.	001	000	00011	1C7	C30	7F94150	IIIIIII
119.	110	111	00001	000	000	MMMMMMM	IIIIIII
120.	001	000	00001	000	000	0000000	IIIIIII
121.	110	111	00101	001	FFF	MMMMMMM	IIIIIII
122.	001	000	00101	001	FFF	7FFFFFF	IIIIIII
123.	110	111	00101	001	001	MMMMMMM	IIIIIII
124.	110	000	00101	001	001	0000000	IIIIIII
125.	110	111	00101	000	555	MMMMMMM	IIIIIII
126.	001	000	00101	000	555	0000000	IIIIIII
127.	110	111	01101	F3C	AAA	MMMMMMM	IIIIIII
128.	001	000	01101	F3C	AAA	00415D8	IIIIIII
129.	110	111	01101	C30	FFF	MMMMMMM	IIIIIII
130.	001	000	01101	C30	FFF	7F3EDF8	IIIIIII
131.	110	111	01101	FFF	000	MMMMMMM	IIIIIII
132.	001	000	01101	FFF	000	0041208	IIIIIII
133.	110	111	00001	000	000	MMMMMMM	IIIIIII
134.	001	000	00001	000	000	0000000	IIIIIII
135.	110	111	00001	001	FFF	MMMMMMM	IIIIIII
136.	001	000	00001	001	FFF	7FFFFFF	IIIIIII
137.	110	111	00001	000	000	MMMMMMM	IIIIIII
138.	001	000	00001	000	000	0000000	IIIIIII
139.	110	000	00001	000	000	MMMMMMM	IIIIIII
140.	001	000	00001	000	000	0000000	IIIIIII
141.	001	111	10000	*III	*III	*MMMMMMM	0000000
142.	000	000	00000	III	III	0000000	*IIIIIII
143.	001	001	10000	III	III	MMMMMMM	0000FFF
144.	000	000	00000	III	III	0000FFF	IIIIIII
145.	001	010	10000	III	III	MMMMMMM	0FFF000
146.	000	000	00000	III	III	0FFFFFF	IIIIIII
147.	001	100	10000	III	III	MMMMMMM	7000000
148.	000	000	00000	III	III	7FFFFFF	IIIIIII
149.	001	111	10000	III	III	MMMMMMM	0000000
150.	000	000	00000	III	III	0000000	IIIIIII
151.	001	111	10000	III	III	MMMMMMM	7FFFFFF
152.	000	000	00000	III	III	7FFFFFF	IIIIIII
153.	001	001	10000	III	III	MMMMMMM	7FFF000
154.	000	000	00000	III	III	7FFF000	IIIIIII
155.	001	010	10000	III	III	MMMMMMM	7000FFF
156.	000	000	00000	III	III	7000000	IIIIIII
157.	001	100	10000	III	III	MMMMMMM	0FFFFFF
158.	000	000	00000	III	III	0000000	IIIIIII
159.	110	111	00001	000	000	MMMMMMM	IIIIIII
160.	001	000	00001	000	000	0000000	IIIIIII
161.	001	001	10000	III	III	MMMMMMM	0000FFF
162.	001	010	10000	III	III	MMMMMMM	0FFF000
163.	001	100	10000	III	III	MMMMMMM	7000000
164.	000	000	00000	III	III	7FFFFFF	IIIIIII
165.	001	001	10000	III	III	MMMMMMM	7FFF000
166.	001	010	10000	III	III	MMMMMMM	7000FFF
167.	001	100	10000	III	III	MMMMMMM	0FFFFFF

See footnotes at end of device type 02.

TABLE IV. Functional test pattern for device type 02 - Continued.

Line	CCC LLL KKK XYP	TTT SSS ML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD M S D 1/
168.	000	000	00000	III	III	0000000	IIIIIII
169.	001	111	10000	III	III	MMMMMMM	2AAAAAA
170.	000	000	00000	III	III	2AAAAAA	IIIIIII
171.	001	111	10000	III	III	MMMMMMM	5555555
172.	000	000	00000	III	III	5555555	IIIIIII

1/ MSD = Most significant digit.

2/ The most significant digit (MSD) in the output column represents the extended product (XTP). However, the XTP has only 3 bits, while a hexadecimal digit can represent 4 bits. The notation used in this table appends a 0 to the left of the 3 bits of the XTP output. Therefore, the MSD ranges from 0 to 7, inclusive.

*Note: For outputs M = MASK
For preload outputs and some X and Y inputs I = INHIBIT

TABLE IV. Functional test pattern for device type 03.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD 1/
1.	110	111	00000	0000	0000	*MMMMMMMMM	IIIII
2.	001	000	00000	0000	*IIII	000000000	IIIII
3.	110	111	00000	FFFF	FFFF	MMMMMMMMM	IIIII
4.	001	000	00000	FFFF	IIII	0FFFE0001	IIIII
5.	110	111	00000	FFFF	0000	MMMMMMMMM	IIIII
6.	001	000	00000	FFFF	IIII	000000000	IIIII
7.	110	111	00000	FFFF	0101	MMMMMMMMM	IIIII
8.	001	000	00000	FFFF	IIII	00100FEFF	IIIII
9.	110	111	00000	FFFF	8080	MMMMMMMMM	IIIII
10.	001	000	00000	FFFF	IIII	0807F7F80	IIIII
11.	110	111	00000	6060	7F7F	MMMMMMMMM	IIIII
12.	001	000	00000	6060	IIII	02FFF6FA0	IIIII
13.	110	111	00000	7070	5555	MMMMMMMMM	IIIII
14.	001	000	00000	7070	IIII	0257A8530	IIIII
15.	110	111	00000	7070	2A2A	MMMMMMMMM	IIIII
16.	001	000	00000	7070	IIII	01284D260	IIIII
17.	110	111	00000	4848	E0E0	MMMMMMMMM	IIIII
18.	001	000	00000	4848	IIII	03F7E3F00	IIIII
19.	110	111	00000	3030	FFFF	MMMMMMMMM	IIIII
20.	001	000	00000	3030	IIII	0302FCFD0	IIIII
21.	110	111	00000	3838	5555	MMMMMMMMM	IIIII
22.	001	000	00000	3838	IIII	012BD4298	IIIII
23.	110	111	00000	3838	1515	MMMMMMMMM	IIIII
24.	001	000	00000	3838	IIII	004A13498	IIIII
25.	110	111	00000	7878	5555	MMMMMMMMM	IIIII
26.	001	000	00000	7878	IIII	02827D7D8	IIIII
27.	110	111	00000	7878	2A2A	MMMMMMMMM	IIIII
28.	001	000	00000	7878	IIII	013D773B0	IIIII
29.	110	111	00000	0000	8080	MMMMMMMMM	IIIII
30.	001	000	00000	0000	IIII	000000000	IIIII
31.	110	111	00000	3030	6060	MMMMMMMMM	IIIII
32.	001	000	00000	3030	IIII	012241200	IIIII
33.	110	111	00000	7070	6060	*MMMMMMMMM	IIIII
34.	001	000	00000	7070	*IIII	02A542A00	IIIII
35.	110	111	00000	1C1C	5555	MMMMMMMMM	IIIII
36.	001	000	00000	1C1C	IIII	0095EA14C	IIIII
37.	110	111	00000	1C1C	2A2A	MMMMMMMMM	IIIII
38.	001	000	00000	1C1C	IIII	004A13498	IIIII
39.	110	111	00000	3C3C	5555	MMMMMMMMM	IIIII
40.	001	000	00000	3C3C	IIII	01413EBEC	IIIII
41.	110	111	00000	3C3C	2A2A	MMMMMMMMM	IIIII
42.	001	000	00000	3C3C	IIII	009EBB9D8	IIIII
43.	110	111	00000	1818	6060	MMMMMMMMM	IIIII
44.	001	000	00000	1818	IIII	009120900	IIIII
45.	110	111	00000	3838	3030	MMMMMMMMM	IIIII
46.	001	000	00000	3838	IIII	00A950A80	IIIII
47.	110	111	00000	0E0E	5555	MMMMMMMMM	IIIII
48.	001	000	00000	0E0E	IIII	004AF50A6	IIIII
49.	110	111	00000	0E0E	2A2A	MMMMMMMMM	IIIII
50.	001	000	00000	0E0E	IIII	002509A4C	IIIII
51.	110	111	00000	1E1E	5555	MMMMMMMMM	IIIII
52.	001	000	00000	1E1E	IIII	00A09F5F6	IIIII
53.	110	111	00000	1E1E	2929	MMMMMMMMM	IIIII
54.	001	000	00000	1E1E	IIII	004D7A0CE	IIIII
55.	110	111	00000	0C0C	6060	MMMMMMMMM	IIIII
56.	001	000	00000	0C0C	IIII	004890480	IIIII
57.	110	111	00000	0000	0000	MMMMMMMMM	IIIII
58.	001	000	00000	0000	IIII	000000000	IIIII

See footnotes at end of device type 03.

TABLE IV. Functional test pattern for device type 03 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD 1/
59.	110	111	00001	8080	0101	MMMMMMMMM	IIIII
60.	001	000	00001	8080	IIII	7FF800080	IIIII
61.	110	111	00001	8080	0000	MMMMMMMMM	IIIII
62.	001	000	00001	8080	IIII	000000000	IIIII
63.	110	111	00001	C0C0	2A2A	MMMMMMMMM	IIIII
64.	001	000	00001	C0C0	IIII	7F5951F80	IIIII
65.	110	111	00001	C0C0	5555	MMMMMMMMM	IIIII
66.	001	000	00001	C0C0	IIII	7EAEABFC0	IIIII
67.	110	111	00001	E0E0	2A2A	*MMMMMMMMM	IIIII
68.	001	000	00001	E0E0	*IIII	7FADFA4C0	IIIII
69.	110	111	00001	E0E0	5555	MMMMMMMMM	IIIII
70.	001	000	00001	E0E0	IIII	7F5A00A60	IIIII
71.	110	111	00001	9090	A0A0	MMMMMMMMM	IIIII
72.	001	000	00001	9090	IIII	029845A00	IIIII
73.	110	111	00001	C0C0	C0C0	MMMMMMMMM	IIIII
74.	001	000	00001	C0C0	IIII	00FA09000	IIIII
75.	110	111	00001	4848	E0E0	MMMMMMMMM	IIIII
76.	001	000	00001	4848	IIII	7F7363F00	IIIII
77.	110	111	00001	3030	FFFF	MMMMMMMMM	IIIII
78.	001	000	00001	3030	IIII	7FFFFCFD0	IIIII
79.	110	111	00001	7070	FFFF	MMMMMMMMM	IIIII
80.	001	000	00001	7070	IIII	7FFFF8F90	IIIII
81.	110	111	00001	0000	8080	MMMMMMMMM	IIIII
82.	001	000	00001	0000	IIII	000000000	IIIII
83.	110	111	00001	1818	FFFF	MMMMMMMMM	IIIII
84.	001	000	00001	1818	IIII	7FFFFE7E8	IIIII
85.	110	111	00001	3838	FFFF	MMMMMMMMM	IIIII
86.	001	000	00001	3838	IIII	7FFFFC7C8	IIIII
87.	110	111	00001	0C0C	FFFF	MMMMMMMMM	IIIII
88.	001	000	00001	0C0C	IIII	7FFFFF3F4	IIIII
89.	110	111	00001	1C1C	FFFF	MMMMMMMMM	IIIII
90.	001	000	00001	1C1C	IIII	7FFFFE3E4	IIIII
91.	110	111	00001	1C1C	6060	MMMMMMMMM	IIIII
92.	001	000	00001	1C1C	IIII	00A950A80	IIIII
93.	110	111	00001	0606	FFFF	MMMMMMMMM	IIIII
94.	001	000	00001	0606	IIII	7FFFFF9FA	IIIII
95.	110	111	00001	0707	5555	MMMMMMMMM	IIIII
96.	001	000	00001	0707	IIII	00257A853	IIIII
97.	110	111	00001	0707	2A2A	MMMMMMMMM	IIIII
98.	001	000	00001	0707	IIII	001284D26	IIIII
99.	110	111	00001	0E0E	FFFF	*MMMMMMMMM	IIIII
100.	001	000	00001	0E0E	*IIII	7FFFFF1F2	IIIII
101.	110	111	00001	0F0F	5555	MMMMMMMMM	IIIII
102.	001	000	00001	0F0F	IIII	00504FAFB	IIIII
103.	110	111	00001	0F0F	2A2A	MMMMMMMMM	IIIII
104.	001	000	00001	0F0F	IIII	0027AEE76	IIIII
105.	110	111	00001	0606	6060	MMMMMMMMM	IIIII
106.	001	000	00001	0606	IIII	002448240	IIIII
107.	110	111	00001	0E0E	6060	MMMMMMMMM	IIIII
108.	001	000	00001	0E0E	IIII	0054A8540	IIIII
109.	110	111	00001	0303	FFFF	MMMMMMMMM	IIIII
110.	001	000	00001	0303	IIII	7FFFFFCFD	IIIII
111.	110	111	00001	0303	5555	MMMMMMMMM	IIIII
112.	001	000	00001	0303	IIII	00100FEFF	IIIII
113.	110	111	00001	0303	2A2A	MMMMMMMMM	IIIII
114.	001	000	00001	0303	IIII	0007EFC7E	IIIII
115.	110	111	00001	0707	FFFF	MMMMMMMMM	IIIII
116.	001	000	00001	0707	IIII	7FFFFF8F9	IIIII

See footnotes at end of device type 03.

TABLE IV. Functional test pattern for device type 03 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD 1/
117.	110	111	00001	0303	6060	MMMMMMMMM	IIIII
118.	001	000	00001	0303	IIII	001224120	IIIII
119.	110	111	00001	0707	6060	MMMMMMMMM	IIIII
120.	001	000	00001	0707	IIII	002A542A0	IIIII
121.	110	111	00001	0101	FFFF	MMMMMMMMM	IIIII
122.	001	000	00001	0101	IIII	7FFFFFEFF	IIIII
123.	110	111	00001	0101	5555	MMMMMMMMM	IIIII
124.	001	000	00001	0101	IIII	00055AA55	IIIII
125.	110	111	00001	0101	2A2A	MMMMMMMMM	IIIII
126.	001	000	00001	0101	IIII	0002A542A	IIIII
127.	110	111	00001	0101	3030	MMMMMMMMM	IIIII
128.	001	000	00001	0101	IIII	000306030	IIIII
129.	110	111	00001	0000	0000	MMMMMMMMM	IIIII
130.	001	000	00001	0000	IIII	000000000	IIIII
131.	110	111	00011	7878	5555	MMMMMMMMM	IIIII
132.	001	000	00011	7878	*IIII	0282857D8	IIIII
133.	110	111	00011	8080	0101	*MMMMMMMMM	IIIII
134.	001	000	00011	8080	IIII	7FF808080	IIIII
135.	110	111	00011	7070	6060	MMMMMMMMM	IIIII
136.	001	000	00011	7070	IIII	02A54AA00	IIIII
137.	110	111	00011	0E0E	6060	MMMMMMMMM	IIIII
138.	001	000	00011	0E0E	IIII	0054B0540	IIIII
139.	110	111	00001	0000	0000	MMMMMMMMM	IIIII
140.	001	000	00101	0000	IIII	000000000	IIIII
141.	110	111	00101	0001	FFFF	MMMMMMMMM	IIIII
142.	001	000	00101	0001	IIII	7FFFFFFFF	IIIII
143.	110	111	00101	0001	0001	MMMMMMMMM	IIIII
144.	001	000	00101	0001	IIII	000000000	IIIII
145.	110	111	00101	0101	5555	MMMMMMMMM	IIIII
146.	001	000	00101	0101	IIII	00055AA55	IIIII
147.	110	111	00101	0101	2A2A	MMMMMMMMM	IIIII
148.	001	000	00101	0101	IIII	0007FFE7F	IIIII
149.	110	111	01001	7070	6060	MMMMMMMMM	IIIII
150.	001	000	01101	7070	IIII	02A542A00	IIIII
151.	110	111	01101	7878	5555	MMMMMMMMM	IIIII
152.	001	000	01101	7878	IIII	7FDD3ADD8	IIIII
153.	110	111	01101	6060	7E7E	MMMMMMMMM	IIIII
154.	001	000	01101	6060	IIII	031CB0168	IIIII
155.	110	111	01101	FFFF	0001	MMMMMMMMM	IIIII
156.	001	000	01101	FFFF	IIII	7CE34FE97	IIIII
157.	110	111	00001	0000	0000	MMMMMMMMM	IIIII
158.	001	000	00001	0000	IIII	000000000	IIIII
159.	110	111	00001	0001	FFFF	MMMMMMMMM	IIIII
160.	001	000	00001	IIII	IIII	7FFFFFFFF	IIIII
161.	110	111	00001	0000	0000	MMMMMMMMM	IIIII
162.	001	000	00000	0000	IIII	000000000	IIIII
163.	001	111	10000	IIII	0000	MMMMMMMMM	00000
164.	000	000	00000	IIII	IIII	000000000	IIIII
165.	001	001	10000	IIII	FFFF	*MMMMMMMMM	00000
166.	000	000	00000	IIII	*IIII	00000FFFF	IIIII
167.	001	010	10000	IIII	0000	MMMMMMMMM	0FFFF
168.	000	000	00000	IIII	IIII	0FFFFFFFF	IIIII
169.	001	100	10000	IIII	0000	MMMMMMMMM	70000
170.	000	000	00000	IIII	IIII	7FFFFFFFF	IIIII
171.	001	111	10000	IIII	0000	MMMMMMMMM	00000
172.	000	000	00000	IIII	IIII	000000000	IIIII
173.	001	111	10000	IIII	FFFF	MMMMMMMMM	7FFFF
174.	000	000	00000	IIII	IIII	7FFFFFFFF	IIIII

See footnotes at end of device type 03.

TABLE IV. Functional test pattern for device type 03 - Continued.

Line	CCC LLL KKK XYP	TTT SSS XML	PSART RUCNC EBCD L	X-INPUTS M S D 1/	Y-INPUTS M S D 1/	OUTPUTS M S D 1/ 2/	PRELOAD 1/
175.	001	001	10000	IIII	0000	MMMMMMMMM	7FFFF
176.	000	000	00000	IIII	IIII	7FFFF0000	IIIII
177.	001	010	10000	IIII	FFFF	MMMMMMMMM	70000
178.	000	000	00000	IIII	IIII	700000000	IIIII
179.	001	100	10000	IIII	FFFF	MMMMMMMMM	0FFFF
180.	000	000	00000	IIII	IIII	000000000	IIIII
181.	001	111	10000	IIII	0000	MMMMMMMMM	00000
182.	000	000	00000	IIII	IIII	000000000	IIIII
183.	001	111	10000	IIII	5555	MMMMMMMMM	55555
184.	000	000	00000	IIII	IIII	555555555	IIIII
185.	001	111	10000	IIII	AAAA	MMMMMMMMM	2AAAA
186.	000	000	00000	IIII	IIII	2AAAAAAAA	IIIII
187.	110	111	00001	0000	0000	MMMMMMMMM	IIIII
188.	001	000	00000	0000	IIII	000000000	IIIII
189.	001	111	10000	IIII	0000	MMMMMMMMM	00000
190.	000	000	00000	IIII	IIII	000000000	IIIII
191.	001	001	10000	IIII	FFFF	*MMMMMMMMM	IIIII
192.	000	000	00000	IIII	*IIII	00000FFFF	IIIII
193.	001	010	10000	IIII	IIII	MMMMMMMMM	IFFFF
194.	000	000	00000	IIII	IIII	0FFFFFFFF	IIIII
195.	001	100	10000	IIII	IIII	MMMMMMMMM	7IIII
196.	000	000	00000	IIII	IIII	7FFFFFFFF	IIIII
197.	001	111	10000	IIII	0000	MMMMMMMMM	00000
198.	000	000	00000	IIII	IIII	000000000	IIIII
199.	001	111	10000	IIII	FFFF	MMMMMMMMM	7FFFF
200.	000	000	00000	IIII	IIII	7FFFFFFFF	IIIII
201.	001	001	10000	IIII	0000	MMMMMMMMM	IIIII
202.	000	000	00000	IIII	IIII	7FFFF0000	IIIII
203.	001	010	10000	IIII	IIII	MMMMMMMMM	I0000
204.	000	000	00000	IIII	IIII	700000000	IIIII
205.	001	100	10000	IIII	IIII	MMMMMMMMM	0IIII
206.	000	000	00000	IIII	IIII	000000000	IIIII
207.	001	111	10000	IIII	0000	MMMMMMMMM	00000
208.	000	000	00000	IIII	IIII	000000000	IIIII
209.	001	111	10000	IIII	5555	MMMMMMMMM	55555
210.	000	000	00000	IIII	IIII	555555555	IIIII
211.	001	111	10000	IIII	AAAA	MMMMMMMMM	2AAAA
212.	000	000	00000	IIII	IIII	2AAAAAAAA	IIIII

1/ MSD = Most significant digit.

2/ The most significant digit (MSD) in the output column represents the extended product (XTP). However, the XTP has only 3 bits, while a hexadecimal digit can represent 4 bits. The notation used in this table appends a 0 to the left of the 3 bits of the XTP output. Therefore, the MSD ranges from 0 to 7, inclusive.

Note: For X inputs, X inputs, and Preload outputs, I = INHIBIT
For outputs M = MASK

TABLE IV. Functional test pattern for device type 04.

Line	Inputs			Outputs 1/	
	RND	XIN	YIN	MSP	LSP
1.	0	00	00	00	00
2.	0	80	00	00	00
3.	0	80	01	FF	80
4.	0	C0	2A	EB	80
5.	0	C0	55	D5	C0
6.	0	E0	2A	F5	C0
7.	0	E0	55	EA	E0
8.	0	90	A0	54	00
9.	0	C0	C0	20	00
10.	0	60	7F	5F	20
11.	0	70	55	4A	30
12.	0	70	0A	24	60
13.	0	48	E0	EE	80
14.	0	30	FF	FF	00
15.	0	08	55	25	08
16.	0	08	0A	12	30
17.	0	70	FF	FF	90
18.	0	70	55	4F	58
19.	0	70	2A	27	30
20.	0	00	00	00	00
21.	0	30	60	24	00
22.	0	70	60	54	00
23.	0	18	FF	FF	E8
24.	0	1C	55	12	4C
25.	0	1C	2A	09	18
26.	0	38	FF	FF	C8
27.	0	3C	55	27	6C
28.	0	3C	2A	13	58
29.	0	18	60	12	00
30.	0	38	60	2A	00
31.	0	0C	FF	FF	F4
32.	0	0E	55	09	26
33.	0	0E	2A	04	4C
34.	0	1C	FF	FF	E4
35.	0	1E	55	13	76
36.	0	1E	2A	09	6C
37.	0	0C	60	09	00
38.	0	1C	60	15	00
39.	0	06	FF	FF	FA
40.	0	07	55	04	53
41.	0	07	2A	02	26
42.	0	0E	FF	FF	F2
43.	0	0F	55	09	7B
44.	0	0F	2A	04	76
45.	0	06	60	04	40
46.	0	0F	60	0A	40
47.	0	03	FF	FF	FD
48.	0	03	55	01	7F
49.	0	03	2A	00	7F
50.	0	07	FF	FF	F9
51.	0	03	60	02	20
52.	0	07	60	05	20
53.	0	00	00	00	00
54.	0	01	FF	FF	FF
55.	0	00	00	00	00

See footnote at end of device type 04.

TABLE IV. Functional test pattern for device type 04 - Continued.

Line	Inputs			Outputs 1/	
	RND	XIN	YIN	MSP	LSP
56.	0	01	55	00	55
57.	0	01	2A	00	2A
58.	0	01	60	00	60
59.	1	01	55	01	15
60.	1	01	2A	00	6A
61.	1	01	60	01	20
62.	0	FF	D5	00	2B
63.	0	7F	EA	EA	96
64.	0	FF	D5	00	2B

1/ MSP = Most significant product.
LSP = Least significant product.

TABLE IV. Functional test pattern for device type 05.

Line	CC LL KK XY	CC LL KK ML	TT RR II ML	TTR CCNFR XYDTS	Inputs XIN	Inputs YIN	Outputs 1/ MSP	Outputs 1/ LSP
1.	11	11	00	00001	000	000	000	000
2.	11	11	00	00001	FFF	FFF	FFE	001
3.	11	11	00	00001	FFF	000	000	000
4.	11	11	00	00001	000	FFF	000	000
5.	11	11	00	00001	AAA	AAA	716	8EF
6.	11	11	00	00001	555	555	1C6	E39
7.	11	11	00	00001	AAA	555	38D	C72
8.	11	11	00	00001	555	AAA	38D	C72
9.	11	11	00	00001	AAA	FC0	A7F	580
10.	11	11	00	00001	FC0	AAA	A7F	580
11.	11	11	00	00001	DB6	249	1F5	4E6
12.	11	11	00	00001	249	DB6	1F5	4E6
13.	11	11	00	00001	EEE	EEE	DEE	544
14.	11	11	00	00001	EF7	EF7	DFF	251
15.	11	11	00	00001	EC7	EC7	DA5	EB1
16.	11	11	00	00001	A95	DB6	911	6EE
17.	11	11	00	00001	B6D	AAA	79D	862
18.	11	11	00	00001	A95	B6D	78E	871
19.	11	11	00	00001	56A	492	18B	E74
20.	11	11	00	00001	000	000	000	000
21.	11	11	00	11001	7FF	FFF	FFF	801
22.	11	11	00	11001	AAA	555	E38	C72
23.	11	11	00	11001	EEE	AAA	56	60C
24.	11	11	00	11001	249	DB6	FAC	4E6
25.	11	11	00	11001	B9D	A95	17C	461
26.	11	11	00	11001	56A	492	18B	E74
27.	11	11	00	11001	B6D	56A	E73	C22
28.	11	11	00	11001	492	B6D	EB1	82A
29.	11	11	00	11001	EF7	555	FA7	B03
30.	11	11	00	11001	FFF	7FF	FFF	801
31.	11	11	00	11001	800	FFF	000	800
32.	11	11	00	11001	FFF	FFF	000	001
33.	11	11	00	11001	000	AAA	000	000
34.	11	11	00	11001	FFF	001	FFF	FFF
35.	11	11	00	11001	000	000	000	000
36.	11	11	00	11001	800	800	400	000
37.	11	11	00	11101	FFF	001	000	7FF
38.	11	11	00	11101	000	000	000	800
39.	11	11	00	11000	AAA	555	C71	C72
40.	11	11	00	11000	EEE	AAA	B6	60C
41.	11	11	00	11000	B6D	56A	CE7	C22
42.	11	11	00	11000	800	800	800	800
43.	11	11	00	11000	000	000	000	400
44.	11	00	00	11011	7FF	FFF	FFF	801
45.	11	00	00	11011	AAA	555	E38	C72
46.	11	00	00	11011	000	FFF	000	000
47.	11	11	00	11001	000	FFF	000	000
48.	11	00	00	11001	001	FFF	000	000
49.	11	11	00	11001	FFF	001	FFF	FFF
50.	11	11	11	11001	000	000	FFF	FFF

1/ MSP = Most significant product.
LSP = Least significant product.

TABLE IV. Functional test pattern for device type 06.

Line	CCCC LLLL KKKK XYML	TT RR II ML	TTRFR CCNTS XYD	X-INPUTS M S B	Y-INPUTS M S B	OUTPUTS M S P 1/	OUTPUTS L S P 1/
1.	1100	11	00001	0000	0000	MMMM	*MMMM
2.	0011	00	00001	0000	*IIII	0000	0000
3.	1100	11	00001	FFFF	FFFF	MMMM	MMMM
4.	0011	00	00001	FFFF	IIII	FFFE	0001
5.	1100	11	00001	FFFF	0000	MMMM	MMMM
6.	0011	00	00001	FFFF	IIII	0000	0000
7.	1100	11	00001	FFFF	0101	MMMM	MMMM
8.	0011	00	00001	FFFF	IIII	0100	FEFF
9.	1100	11	00001	FFFF	8080	MMMM	MMMM
10.	0011	00	00001	FFFF	IIII	807F	7F80
11.	1100	11	00001	6060	7F7F	MMMM	MMMM
12.	0011	00	00001	6060	IIII	2FFF	6FA0
13.	1100	11	00001	7070	5555	MMMM	MMMM
14.	0011	00	00001	7070	IIII	257A	8530
15.	1100	11	00001	7070	2A2A	MMMM	MMMM
16.	0011	00	00001	7070	IIII	1284	D260
17.	1100	11	00001	4848	E0E0	MMMM	MMMM
18.	0011	00	00001	4848	IIII	3F7E	3F00
19.	1100	11	00001	3030	FFFF	MMMM	MMMM
20.	0011	00	00001	3030	IIII	302F	CFD0
21.	1100	11	00001	3838	5555	MMMM	MMMM
22.	0011	00	00001	3838	IIII	12BD	4298
23.	1100	11	00001	3838	1515	MMMM	MMMM
24.	0011	00	00001	3838	IIII	04A1	3498
25.	1100	11	00001	7878	5555	MMMM	MMMM
26.	0011	00	00001	7878	IIII	2827	D7D8
27.	1100	11	00001	7878	2A2A	MMMM	MMMM
28.	0011	00	00001	7878	IIII	13D7	73B0
29.	1100	11	00001	0000	8080	MMMM	MMMM
30.	0011	00	00001	0000	IIII	0000	0000
31.	1100	11	00001	3030	6060	MMMM	MMMM
32.	0011	00	00001	3030	IIII	1224	1200
33.	1100	11	00001	7070	6060	MMMM	MMMM
34.	0011	00	00001	7070	IIII	2A54	2A00
35.	1100	11	00001	1C1C	5555	MMMM	MMMM
36.	0011	00	00001	1C1C	*IIII	095E	A14C
37.	1100	11	00001	1C1C	2A2A	*MMMM	MMMM
38.	0011	00	00001	1C1C	IIII	04A1	3498
39.	1100	11	00001	3C3C	5555	MMMM	MMMM
40.	0011	00	00001	3C3C	IIII	1413	EREC
41.	1100	11	00001	3C3C	2A2A	MMMM	MMMM
42.	0011	00	00001	3C3C	IIII	09EB	B9D8
43.	1100	11	00001	1818	6060	MMMM	MMMM
44.	0011	00	00001	1818	IIII	0912	0900
45.	1100	11	00001	3838	3030	MMMM	MMMM
46.	0011	00	00001	3838	IIII	0A95	0A80
47.	1100	11	00001	0E0E	5555	MMMM	MMMM
48.	0011	00	00001	0E0E	IIII	04AF	50A6
49.	1100	11	00001	0E0E	2A2A	MMMM	MMMM
50.	0011	00	00001	0E0E	IIII	0250	9A4C
51.	1100	11	00001	1E1E	5555	MMMM	MMMM
52.	0011	00	00001	1E1E	IIII	0A09	F5F6
53.	1100	11	00001	1E1E	2929	MMMM	MMMM
54.	0011	00	00001	1E1E	IIII	04D7	A0CE
55.	1100	11	00001	0C0C	6060	MMMM	MMMM
56.	0011	00	00001	0C0C	IIII	0489	0480
57.	1100	11	00001	0000	0000	MMMM	MMMM
58.	0011	00	00001	0000	IIII	0000	0000

See footnote at end of device type 06.

TABLE IV. Functional test pattern for device type 06 - Continued.

Line	CCCC LLLL KKKK XYML	TT RR II ML	TTRFR CCNTS XYD	X-INPUTS M S B	Y-INPUTS M S B	OUTPUTS M S P 1/	OUTPUTS L S P 1/
59.	1100	11	11001	8080	0101	MMMM	MMMM
60.	0011	00	11001	8080	IIII	FF80	0080
61.	1100	11	11001	8080	0000	MMMM	MMMM
62.	0011	00	11001	8080	IIII	0000	0000
63.	1100	11	11001	C0C0	2A2A	MMMM	MMMM
64.	0011	00	11001	C0C0	IIII	F595	1F80
65.	1100	11	11001	C0C0	5555	MMMM	MMMM
66.	0011	00	11001	C0C0	IIII	EAEA	BFC0
67.	1100	11	11001	E0E0	2A2A	MMMM	MMMM
68.	0011	00	11001	E0E0	IIII	FADF	A4C0
69.	1100	11	11001	E0E0	5555	MMMM	MMMM
70.	0011	00	11001	E0E0	IIII	F5A0	0A60
71.	1100	11	11001	9090	A0A0	*MMMM	MMMM
72.	0011	00	11001	9090	*IIII	2984	5A00
73.	1100	11	11001	C0C0	C0C0	MMMM	MMMM
74.	0011	00	11001	C0C0	IIII	0FA0	9000
75.	1100	11	11001	4848	E0E0	MMMM	MMMM
76.	0011	00	11001	4848	IIII	F736	3F00
77.	1100	11	11001	3030	FFFF	MMMM	MMMM
78.	0011	00	11001	3030	IIII	FFFF	CFD0
79.	1100	11	11001	7070	FFFF	MMMM	MMMM
80.	0011	00	11001	7070	IIII	FFFF	8F90
81.	1100	11	11001	0000	8080	MMMM	MMMM
82.	0011	00	11001	0000	IIII	0000	0000
83.	1100	11	11001	1818	FFFF	MMMM	MMMM
84.	0011	00	11001	1818	IIII	FFFF	E7E8
85.	1100	11	11001	3838	FFFF	MMMM	MMMM
86.	0011	00	11001	3838	IIII	FFFF	C7C8
87.	1100	11	11001	0C0C	FFFF	MMMM	MMMM
88.	0011	00	11001	0C0C	IIII	FFFF	F3F4
89.	1100	11	11001	1C1C	FFFF	MMMM	MMMM
90.	0011	00	11001	1C1C	IIII	FFFF	E3E4
91.	1100	11	11001	1C1C	6060	MMMM	MMMM
92.	0011	00	11001	1C1C	IIII	0A95	0A80
93.	1100	11	11001	0606	FFFF	MMMM	MMMM
94.	0011	00	11001	0606	IIII	FFFF	F9FA
95.	1100	11	11001	0707	5555	MMMM	MMMM
96.	0011	00	11001	0707	IIII	0257	A853
97.	1100	11	11001	0707	2A2A	MMMM	MMMM
98.	0011	00	11001	0707	IIII	0128	4D26
99.	1100	11	11001	0E0E	FFFF	MMMM	MMMM
100.	0011	00	11001	0E0E	IIII	FFFF	F1F2
101.	1100	11	11001	0F0F	5555	MMMM	MMMM
102.	0011	00	11001	0F0F	IIII	0504	FAFB
103.	1100	11	11001	0F0F	2A2A	MMMM	MMMM
104.	0011	00	11001	0F0F	IIII	027A	EE76
105.	1100	11	11001	0606	6060	MMMM	MMMM
106.	0011	00	11001	0606	*IIII	0244	8240
107.	1100	11	11001	0E0E	6060	*MMMM	MMMM
108.	0011	00	11001	0E0E	IIII	054A	8540
109.	1100	11	11001	0303	FFFF	MMMM	MMMM
110.	0011	00	11001	0303	IIII	FFFF	FCFD
111.	1100	11	11001	0303	5555	MMMM	MMMM
112.	0011	00	11001	0303	IIII	0100	FEFF
113.	1100	11	11001	0303	2A2A	MMMM	MMMM
114.	0011	00	11001	0303	IIII	007E	FC7E
115.	1100	11	11001	0707	FFFF	MMMM	MMMM
116.	0011	00	11001	0707	IIII	FFFF	F8F9

See footnote at end of device type 06.

TABLE IV. Functional test pattern for device type 06 - Continued.

Line	CCCC LLLL KKKK XYML	TT RR II ML	TTRFR CCNTS XYD	X-INPUTS M S B	Y-INPUTS M S B	OUTPUTS M S P 1/	OUTPUTS L S P 1/
117.	1100	11	11001	0303	6060	MMMM	MMMM
118.	0011	00	11001	0303	IIII	0122	4120
119.	1100	11	11001	0707	6060	MMMM	MMMM
120.	0011	00	11001	0707	IIII	02A5	42A0
121.	1100	11	11001	0101	FFFF	MMMM	MMMM
122.	0011	00	11001	0101	IIII	FFFF	FEFF
123.	1100	11	11001	0101	5555	MMMM	MMMM
124.	0011	00	11001	0101	IIII	0055	AA55
125.	1100	11	11001	0101	2A2A	MMMM	MMMM
126.	0011	00	11001	0101	IIII	002A	542A
127.	1100	11	11001	0101	3030	MMMM	MMMM
128.	0011	00	11001	0101	IIII	0030	6030
129.	1100	11	11001	0000	0000	MMMM	MMMM
130.	0011	00	11001	0000	IIII	0000	0000
131.	1100	11	11101	7878	5555	MMMM	MMMM
132.	0011	00	11101	7878	IIII	2828	57D8
133.	1100	11	11101	8080	0101	MMMM	MMMM
134.	0011	00	11101	8080	IIII	FF80	8080
135.	1100	11	11101	7070	6060	MMMM	MMMM
136.	0011	00	11101	7070	IIII	2A54	AA00
137.	1100	11	11101	0E0E	6060	MMMM	MMMM
138.	0011	00	11101	0E0E	IIII	054B	0540
139.	1100	11	11100	E000	2AAA	MMMM	MMMM
140.	0011	00	11100	E000	IIII	F555	C000
141.	1100	11	11000	E000	5555	MMMM	MMMM
142.	0011	00	11000	E000	IIII	EAAA	E000
143.	1100	11	11000	9000	A000	MMMM	MMMM
144.	0011	00	11000	9000	IIII	5400	0000
145.	1100	11	11000	C000	C000	MMMM	MMMM
146.	0011	00	11000	C000	IIII	2000	0000
147.	1100	11	11000	6000	7FFF	MMMM	MMMM
148.	0011	00	11000	6000	IIII	5FFF	2000
149.	1100	11	11000	0780	5555	MMMM	MMMM
150.	0011	00	11000	0780	IIII	04FF	7D80
151.	1100	11	11000	0780	2AAA	MMMM	MMMM
152.	0011	00	11000	0780	IIII	027F	7B00
153.	1100	11	11000	0300	6000	MMMM	MMMM
154.	0011	00	11000	0300	IIII	0240	0000
155.	1100	11	11000	0700	6000	MMMM	MMMM
156.	0011	00	11000	0700	IIII	0540	0000
157.	1100	11	11000	0180	FFFF	MMMM	MMMM
158.	0011	00	11000	0180	IIII	FFFF	FE80
159.	1100	11	11000	000C	6000	MMMM	MMMM
160.	0011	00	11000	000C	IIII	0009	0000
161.	1100	11	11000	000C	6000	MMMM	MMMM
162.	0011	00	11000	000C	IIII	0015	0000
163.	1100	11	11000	0006	FFFF	MMMM	MMMM
164.	0011	00	11000	0006	IIII	FFFF	FFFA
165.	1100	11	11000	0007	5555	MMMM	MMMM
166.	0011	00	11000	0007	IIII	0004	5553
167.	1100	11	11000	0007	2AAA	MMMM	MMMM
168.	0011	00	11000	0007	IIII	0002	2AA6
169.	1100	11	11000	0007	6DB6	MMMM	MMMM
170.	0011	00	11000	0007	IIII	0005	7FFA
171.	1100	11	11000	0007	36DB	MMMM	MMMM
172.	0011	00	11000	0007	IIII	0002	7FFD
173.	1100	11	11000	0007	1B6C	MMMM	MMMM
174.	0011	00	11000	0007	IIII	0001	3FF4

See footnote at end of device type 06.

TABLE IV. Functional test pattern for device type 06 - Continued.

Line	CCCC LLLL KKKK XYML	TT RR II ML	TTRFR CCNTS XYD	X-INPUTS M S B	Y-INPUTS M S B	OUTPUTS M S P 1/	OUTPUTS L S P 1/
175.	1100	11	11000	0000	0000	MMMM	MMMM
176.	0011	00	11000	0000	IIII	0000	0000
177.	1100	11	11100	FFFF	0001	*MMMM	MMMM
178.	0011	00	11100	FFFF	*IIII	0000	3FFF
179.	1100	11	11100	FFB6	E0F1	MMMM	MMMM
180.	0011	00	11100	FFB6	IIII	0012	3A56
181.	1100	11	11100	FFD3	CDC5	MMMM	MMMM
182.	0011	00	11100	FFD3	IIII	0012	145F
183.	1100	11	11100	FFD5	ADB6	MMMM	MMMM
184.	0011	00	11100	FFD5	IIII	001C	126E
185.	1100	11	11100	FFD8	CAE0	MMMM	MMMM
186.	0011	00	11100	FFD8	IIII	0011	0D00
187.	1100	11	11100	FFDB	E8F4	MMMM	MMMM
188.	0011	00	11100	FFDB	IIII	0007	14BC
189.	1100	11	11100	FFE1	C0BC	MMMM	MMMM
190.	0011	00	11100	FFE1	IIII	000F	693C
191.	1100	11	11000	0001	0000	MMMM	MMMM
192.	0011	00	11000	0001	IIII	0000	0000
193.	1100	11	11000	FFFF	0001	MMMM	MMMM
194.	0011	00	11000	0001	IIII	FFFF	FFFF
195.	1100	11	11000	0001	0000	MMMM	MMMM
196.	0011	00	00000	0001	IIII	0000	0000
197.	1100	11	00011	6060	7F7F	MMMM	MMMM
198.	0000	00	00011	6060	IIII	2FFF	6FA0
199.	1100	11	00011	7070	5555	MMMM	MMMM
200.	0000	00	00011	7070	IIII	257A	8530
201.	1100	11	00011	7070	2A2A	MMMM	MMMM
202.	0000	00	00011	7070	IIII	1284	D260
203.	1100	11	00011	4848	E0E0	MMMM	MMMM
204.	0000	00	00011	4848	IIII	3F7E	3F00
205.	1100	11	00011	3030	FFFF	MMMM	MMMM
206.	0000	00	00011	3030	IIII	302F	CFD0
207.	1100	11	00011	3838	5555	MMMM	MMMM
208.	0000	00	00011	3838	IIII	12BD	4298
209.	1100	11	00011	3838	1515	MMMM	MMMM
210.	0000	00	00011	3838	IIII	04A1	3498
211.	1100	00	11000	FFFF	0001	MMMM	MMMM
212.	0011	11	11000	FFFF	IIII	FFFF	FFFF
213.	1100	00	11000	0000	IIII	*MMMM	MMMM
214.	0011	00	11000	0000	*IIII	FFFF	FFFF
215.	1100	00	11000	FFFF	0001	MMMM	MMMM
216.	0000	11	11000	FFFF	IIII	0000	0000

1/ MSP = Most significant product.
LSP = Least significant product.

Note: For Y inputs I = INHIBIT
For outputs M = MASK

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to acquiring activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

6.3.1 Pin definitions for device types 01, 02, 03. The following describes the function of each pin of the multiplier-accumulator devices.

Data input (XIN, YIN)

XIN and YIN are parallel input words where X_0 and Y_0 are least significant bits and X_{N-1} and Y_{N-1} are most significant bits. Data inputs are loaded into the X register and Y register at the rising edge of CLK X and CLK Y, respectively.

Data output (P_0 to P_{2N+2})

P_0 is the least significant bit and P_{2N+2} is the most significant bit. The product is divided into least significant product (LSP: P_0 to P_{N-1}), most significant product (MSP: P_N to P_{2N-1}) and extended product (XTP: P_{2N} to P_{2N+2}). The product generated is loaded into the output registers at the rising edge of CLK P.

Pre-load data (PD_0 to PD_{2N+2})

Data applied externally to output pins, to initialize output register to a given value at the rising edge of CLK P.

PD_0 to PD_{2N+2} are provided to output pins P_0 to P_{2N+2} respectively, where PD_0 is the least significant bit and PD_{2N+2} is the most significant bit.

Two's complement control (TC)

When TC is high, the inputs are N-bit two's complement numbers. When TC is low the inputs are N-bit unsigned magnitude numbers. The TC signal is loaded into the instruction register at the rising edge of the logical OR of CLK X, CLK Y. The TC signal must be valid over the same period that the input data is valid.

Round control (RND)

When RND is high a "1" is added to the most significant bit of the LSP to round up the product in MSP and XTP rather than truncate it.

The RND signal is loaded into the instruction register at the rising edge of the logical OR of CLK X, CLK Y. The RND signal must be valid over the same period that the input data is valid.

Accumulation control (ACC)

When ACC is high and SUB is low, the contents of the output registers are added to the next product generated and their sum is stored back into the output registers at the rising edge of the next CLK P.

When ACC is low, multiplication without accumulation is performed and the next product generated will be stored into the output registers directly.

The ACC signal is loaded into the instruction register at the rising edge of the logical OR of CLK X, CLK Y. The ACC signal must be valid over the same period that the input data is valid.

Subtraction control (SUB)

When ACC and SUB are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLK P.

When ACC is high and SUB is low, addition is performed insted of subtraction.

The SUB signal is loaded into the instruction register at the rising edge of either CLK X or CLK Y. The SUB signal must be valid over the same period that the input data is valid.

Three-state least, most, and extended control (TSL, TSM, TSX)

The LSP, MSP, or XTP output buffers are at high impedance, or output disabled, when TSL, TSM, or TSX is high, respectively. These are direct, non-registered control signals.

Pre-load control (PREL)

All appropriate output buffers are at high impedance, or output disabled, when PREL is high. When TSL, TSM, or TSX also are high, the initial contents of their corresponding output register can be pre-set to the Pre-Load Data applied to the output pins at the rising edge of CLK P. If TSL, TSM, or TSX is low while PREL is high, the contents of the respective output register remains unchanged.

Clocks (CLK X, CLK Y, CLK P)

The X, Y, and output registers are each clocked on the rising edge by their respective clocks. The clock for the instruction register is the logical OR of CLK X, CLK Y.

6.3.3 Pin definitions, for device types 04, 05, 06. The following describes the function of each pin of the multiplier devices.

Data input (XIN, YIN)

XIN and YIN are parallel input words where X_0 and Y_0 are least significant bits and X_{N-1} and Y_{N-1} are most significant bits. Data inputs are loaded into the X register and Y register at the rising edge of CLK X and CLK Y, respectively.

Data output (P_0 to P_{2N})

P_0 is the least significant bit and P_{2N} is the most significant bit. The product is divided into least significant product (LSP: P_0 to P_{N-1}) and most significant product (MSP: P_N to P_{2N-1}). The product generated is loaded into the output registers at the rising edge of CLK P (04 only), or CLK L and CLK M (05 and 06 only).

Round control (RND) (04 only)

When RND is high, a "1" is added to the most significant bit of the LSP to round up the product in MSP rather than truncate it.

The RND signal is loaded into the instruction register at the rising edge of either CLK X or CLK Y. The RND signal must be valid over the same period that the input data is valid.

Round control (RND) (05 and 06 only)

When RND is 1 and RS is 0, a one will be added to P10 for the 05 multiplier, or P14 for the 06 multiplier.

When RND is 1 and RS is 1, a one will be added to P11 for the 05 multiplier, or P15 for the 06 multiplier.

Two's complement controls (TCX and TCY) (05 and 06 only)

When TCX or TCY are high, the respective input work is designated a two's complement number. When TCX or TCY are low, the respective input word is designated an unsigned magnitude number.

The TCX and TCY signals are loaded into the instruction register at the rising edge of the logical OR of CLK X, CLK Y. The TCX and TCY signals must be valid over the same period that the input data is valid.

Feed-through (FT) (05 and 06 only)

When FT is high, the output registers are mode transparent and the product is brought asynchronously to the output pins if TRIL and TRIM are low. When FT is low, the output registers are clocked on the positive edge of CLK M or CLK L. FT is not a registered input.

Right shift (RS) (05 and 06 only)

When RS is 1, the MSP is shifted down on bit, relative to the input format.

When RS is 0, the MSP has the same format as the input. See the Input/Output formats in the appendix for further details. RS must be stable for 30 nanoseconds before the rising edge of CLK L or CLK M, if the multiplier is in the clocked mode.

TRIL, TRIM: Three State Controls, LSP and MSP respectively.

CLK L + CLK M (05 and 06 only): Register clocks, LSP and MSP respectively.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead finish C (see 3.3).

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	TDC1008C1V
02	TDC1009C1V
03	TDC1010C1V
04	MPY008HC2V
05	MPY012HC1V
06	MPY016HC1V

6.6 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

Custodians:
Air Force - 17
Army - ER
Navy - EC

Review activities:
Air Force - 11, 19, 85, 99
Army - AR, MI
Navy - OS, SH, TD
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-0955-4)