MIL-M-38510/504A(USAF)
AMENDMENT 3
10 NOVEMBER 1996
SUPERSEDING
AMENDMENT 2
11 SEPTEMBER 1986

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR PROGRAMMABLE LOGIC, MONOLITHIC SILICON

This amendment forms a part of Military Specification MIL-M-38510/504A(USAF), dated 30 August 1984, and is approved for use by the Department of the Air Force, and is available for use by all Departments and Angencies of the Department of Defense.

PAGE 1

1.1, 3rd sentence: Delete "(TD-W), platinum silicide, and nichrome" and substitute "(TiW)".

1.2.3, Case outlline 2: Delete "CCP" and substitute "chip carrier package".

1.3, Thermal resistance: Delete "2/".

PAGE 2

1.4, following minimum high-level input voltage: Insert "(V_{IH})".
following maximum low-level input voltage: Insert "(V_{IL})".
following case operating temperature range: Insert "(T_C)".

PAGE 3

* TABLE I, V_{OH} min now reads 2.4 V for all devices; divide Device Type and Limits Min and Max boxes horizontally, in the upper box under Device type insert 01-06, and in the upper Min box insert 2.4. In the bottom box under Device type insert 07-10, and in the bottom Min box insert 2.3.

* TABLE I, I_{CC} for devices 07,08,09,10 now reads 90 mA; the change is to place the 07 device by itself with a limit of 105 mA and keep the other devices (08,09, and 10) with the limit at 90 mA.

The attached insertable replacements pages listed below are replacements for stipulated pages. When the new pages have been entered in the document, insert the amendment as the cover sheet to the specification.

Replacement page	Page replaced
27	27
28	28
59	59
60	60
61	61
62	62
63	63
64	64
65	65
66	66

PAGE 14

Figure 3, second truth table: Delete "Device type 05" and substitute "Device type 06".

PAGE 31

TABLE III, I_{OS}: Add "11/" in the symbol column.

PAGE 32

TABLE III, functional tests, pin 20: Delete "4.5 V" and substitute "5.5 V".

PAGE 33

TABLE III, V_{OL}, test no. 11, pin 11: Delete "6/" and substitute "1/".

PAGE 34

TABLE III, I_{OS}, test no. 57, pin 11: Delete "6/" and substitute "1/".

TABLE III, I_{OS}: Add "11/" in the symbol column.

PAGE 35

TABLE III. t_{PLZ} and t_{PHZ}. pin 11: Delete "." (2 places). and substitute "7/" (2 places).

TABLE III, f_{MAX}, pin 11: Add "6/"

TABLE III. f_{MAX}. measured terminal column: Delete ".", and substitute "All registered outputs".

PAGE 36

TABLE III, I_{IL}, test no. 40, measured terminal column: Delete "I/O_1", and substitute "I/O_7".

TABLE III, V_{OL}, test no. 13, pin 11: Delete "6/" and substitute "1/".

PAGE 37

TABLE III, I_{OS}: Add "11/" in the symbol column.

TABLE III, I_{OS}, test no. 63, pin 11: Delete "6/" and substitute "1/".

PAGE 38

TABLE III, t_{PHZ} and t_{PLZ}, test nos. 95 and 96, pin 11: Delete "." (2 places), and substitute "7/" (2 places).

TABLE III, f_{MAX}: pin 11: Add "5/".

TABLE III, f_{MAX}, measured terminal column: Delete "all", and substitute "All registered outputs".

PAGE 39

TABLE III, V_{OL}, test nos. 17 through 20, measured terminal column: Delete "I_2, I_3, I_4, I_5, and substitute "O_2, O_3, O_4, O5" respectively.

PAGE 40

TABLE III, I_{IH}, test no. 54, pin 11: Add "2.4 V".

TABLE III, I_I, test nos. 67 and 68, measured terminal column: Delete "I/O_2, I/O_3", and substitute "I/O_6, I/O_7" respectively.

TABLE III, IOS: Add "11/" in the symbol column.

TABLE III, I_{OS}, test no. 69, pin 20: Delete "-", and substitute "5.0 V".

TABLE III, I_{OZH}, test no. 77, pin 20: Delete "-", and substitute "5.5 V".

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TABLE III, t_{PHZ} and t_{PLZ}, test nos. 99 and 100, pin 11: Delete "-" (2 places), and substitute "7/" (2 places).

TABLE III, t_{MAX}: pin 11: Add "5/".

TABLE III, f_{MAX}: pin 14: Delete "3/", and substitute "5/".

TABLE III, f_{MAX}, measured terminal column: Delete "all", and substitute "All registered outputs".

PAGE 47

TABLE III, IOS: Add "11/" in the symbol column.
I_{CC}: delete the 90 mA value and replace with 105 mA value.

PAGE 48

TABLE III, t_{PHL}, pins 12 through 18: Delete "8/" and substitute "9/".

PAGE 50

TABLE III, I_{OS}: Add "11/" in the symbol column.

PAGE 51

TABLE III, f_{MAX}: pin 11: Delete "-", and substitute "5/ 6/".

TABLE III, t_{PLZ} and t_{PHZ}, pin 11: Delete "-" (2 places), and substitute "7/" (2 places).

TABLE III, fMAX, measured terminal column: Delete "-", and substitute "All registered outputs".

PAGE 52

TABLE III, I_{IL}, test no. 40, measured terminal column: Delete "I/O_1", and substitute "I/O_7".

PAGE 53

TABLE III, I_{OS}: Add "11/" in the symbol column.

PAGE 54

TABLE III, f_{MAX}: pin 11: Add "5/".

TABLE III, f_{MAX}, measured terminal column: Delete "all", and substitute "All registered outputs".

PAGE 55

TABLE III, V_{OL}, test nos. 17 through 20, measured terminal column: Delete "I_2, I_3, I_4, I_5, and substitute "O_2, O_3, O_4, O_5" respectively.

PAGE 56

TABLE III, I_I, test nos. 67 and 68, measured terminal column: Delete "I/O_2, I/O_3", and substitute "I/O_6, I/O_7" respectively.

TABLE III, IOS: Add "11/" in the symbol column.

TABLE III, I_{OS}, test no. 69, pin 20: Delete "-", and substitute "5.0 V".

TABLE III, I_{OZH}, test no. 77, pin 20: Delete "-", and substitute "5.5 V".

PAGE 57

TABLE III, f_{MAX}: pin 20: Delete "5/", and substitute "4.5 V".

TABLE III, t_{PHZ} and t_{PLZ}, test nos. 99 and 100, pin 11: Delete "-" (2 places), and substitute "7/" (2 places).

TABLE III, f_{MAX}: pin 11: Add "5/".

TABLE III, f_{MAX}, measured terminal column: Delete "all", and substitute "All registered outputs".

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Footnote 1/, delete and substitute the following:

"1/ For programmed devices select an appropriate set of inputs to acquire the desired output states.

For unprogrammed devices circuit A, for V_{OL}, V_{OH}, and I_{OS} use conditions defined for the programming procedure as follows:

V_{OL}:

a. 11.5 V on pins 1-9; 0 V on pins 12-15; and a clock pulse on pin 11. Outputs are on pins 16-19.

b. 11.5 V on pins 2-9 and pin 11; 0 V on pins 16-19 and a clock pulse on pin 1. Outputs are on pin 12-15.

V_{OH}:

a. 11.5 V on pin 1; 0 V on pins 2-9; a clock pulse on pin 11. Pins 12-15 are high impedance. Outputs are on pins 16-19.

b. 11.5 V on pin 11; 0 V on pins 2-9; a clock pulse on pin 1. Pins 16-19 are high impedance. Outputs are on pins 12-15.

I_{OS}:

Applying the proper output test, generate the output condition as specified for V_{OH}. Short only one output at a time. Duration of the short should not exceed 1 second.

For unprogrammed devices circuit B, for V_{OL}, V_{OH}, I_{OS}, use conditions defined for the programming procedures as follows:

V_{OL}:

a. 11.5 V on pins 1-9; 5 V on pins 12-15; and a clock pulse on pin 11. Outputs are on pins 16-19.

b. 11.5 V on pins 2-9 and pin 11; 5 V on pins 16-19 and a clock pulse on pin 1. Outputs are on pins 12-15.

V_{OH}:

a. 11.5 V on pins 1-9 and pins 13-15, 5 V on pin 12, and a clock pulse on pin 11. Outputs are on pins 16-19.

b. 11.5 V on pins 2-9 and pin 11, and pins 16-18, 5 V on pins 19; a clock pulse on pin 1. Outputs are on pins 12-15.

I_{OS}:

Applying the proper output test, generate the output condition as specified for V_{OH}. Short only one output at a time. Duration of the short should not exceed 1 second.

For unprogrammed devices circuit C, for V_{OL}, V_{OH}, I_{OZH}, I_{OZL}, and I_{OS}, use conditions defined for the programming procedures as follows:

V_{OL}:

a. 10.5 V on pins 2-9, GND on pins 10 and 11, and a clock pulse on pin 1. Outputs are on pins 13, 15, 17, 19.

b. 10.5 V on pins 3-9, GND on pins 2, 10, and 11, and a clock pulse on pin 1. Outputs are on pins 12 and 14.

c. 10.5 V on pins 3-9, GND on pins 1, 2, 10, and 11. *Outputs are on pins 16 and 18.*

V_{OH}:

a. 10.5 V on pin 11, GND on pins 2-10, and a clock pulse on pin 1. Outputs are on pins 12 - 15.

b. 10.5 V on pin 1, GND on pins 2-10, and a clock pulse on pin 11. Outputs are on pins 16 - 19.

I_{OZH}:

a. GND on pins 1-11, outputs are on pins 12-19 for device types 01 and 07. Outputs are on pins 12, 19 for device types 03 and 09. Outputs are on pins 12, 13, 18, and 19 for device types 04 and 10.

b. GND on pins 1-10, 2.0 V on pin 11, outputs are on pins 12-19 for device types 02 and 08, 13-18 for device types 03 and 09. Outputs are on pins 14-17 for device types 04 and 10.

I_{OZL}:

a. GND on pins 2-11, and a clock pulse on pin 1. *Outputs are on pins 12 and 19 for device types 01 and 07.*

b. GND on pins 2-10, 2.0 V on pin 11, and a clock pulse on pin 1. Outputs are on pins 12-19 for device types 02 and 08. Outputs are on pins 13-18 for device types 03 and 09. Outputs are on pins 14-17 for device types 04 and 10.

I_{OS}:

Applying the proper output test, generate the output condition as specified for V_{OH}. Short only one output at a time. Duration of the short should not exceed 1 second.

Add footnote 11/ as follows:

"11/" For circuit C, I_{OS} test may be replaced with an equivalent I_O test as follows: pins 12-19, delete "GND and substitute "2.25 V"; pin 20 V_{CC}; delete "5.0 V", substitute "5.5 V"; and in the limits columns, delete min/max of "-30/-250" and substitute "-15/-125".

4.6, delete and substitute the following:

"4.6 Programming/verifying procedure for circuits A, B, and C. The programming specifications on figure 8a, figure 9, and table IV for circuit A; figure 8b, figure 9, and table V for circuit B; and figure 8c, figure 9, and table VI for circuit C, and the following procedures shall be used for programming the device."

4.6.1c, delete and substitute:

"c. Select and input line by specifying inputs and L/R as shown in table VII for circuits A, B, and C."

4.6.1d, delete and substitute:

"d. Select a product line by specifying A_0, A_1, and A_2 one-of-eight. Select as shown in table VIII for circuits A, B, and C."

4.6.1e, delete and substitute:

"e. Pulse the CLOCK pin and verify (with CLOCK at V_{IL}) that the output pins, O0 through O3, are in the state corresponding to an unblown fuse. Use the minimum timing conditions as specified on figure 8a for circuit A, figure 8b for circuit B, and figure 8c for circuit C.
- For verified unblown condition, continue procedure from C through E.
- For verified blown condition, stop procedure."

4.6.1f, delete and substitute:

"f. Program the fuse by pulsing the output pins of the selected group -one at a time- to V_{IHH}, see figure 8a for circuit A, figure 8b for circuit B, and figure 8c for circuit C."

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6.5, delete the exsisting cross reference information and substitute as follows:

" Military device type	Generic-industry type/manufacturer	Circuit designator	Fusible link	Symbol/ CAGE number
01	PAL16L8A/Monolithic Memories	A	TiW	CECD/50364
01	PAL16L8A/National	B	TiW	CCXP/27014
01	PAL16L8A/Texas Instruments	C	TiW	CGO/01295
02	PAL16R8A/Monolithic Memories	A	TiW	---
02	PAL16R8A/National	B	TiW	---
02	PAL16R8A/Texas Instruments	C	TiW	---
03	PAL16R6A/Monolithic Memories	A	TiW	---
03	PAL16R6A/National	B	TiW	---
03	PAL16R6A/Texas Instruments	C	TiW	---
04	PAL16R4A/Monolithic Memories	A	TiW	---
04	PAL16R4A/National	B	TiW	---
04	PAL16R4A/Texas Instruments	C	TiW	---
05	PAL16X4/Monolithic Memories	A	TiW	---
05	PAL16X4/National	B	TiW	---
06	PAL16A4/Monolithic Memories	A	TiW	---
06	PAL16A4/National	B	TiW	---
07	PAL16L8A-2/Monolithic Memories	A	TiW	---
07	PAL16L8A-2/Texas Instruments	C	TiW	---
08	PAL16R8A-2/Monolithic Memories	A	TiW	---
08	PAL16R8A-2/Texas Instruments	C	TiW	---
09	PAL16R6A-2/Monolithic Memories	A	TiW	---
09	PAL16R6A-2/Texas Instruments	C	TiW	---
10	PAL16R4A-2/Monolithic Memories	A	TiW	---
10	PAL16R4A-2/Texas Instruments	C	TiW	---

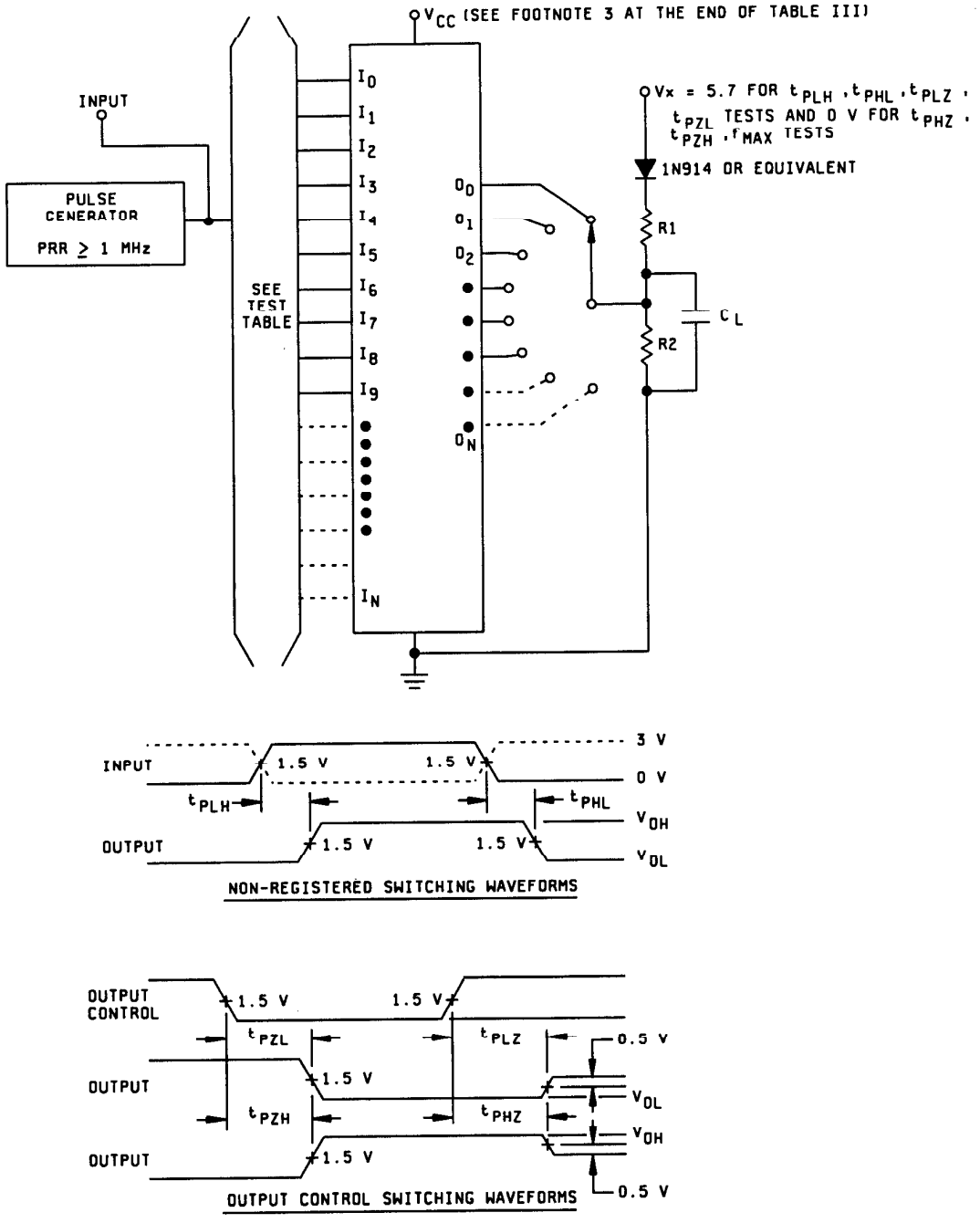
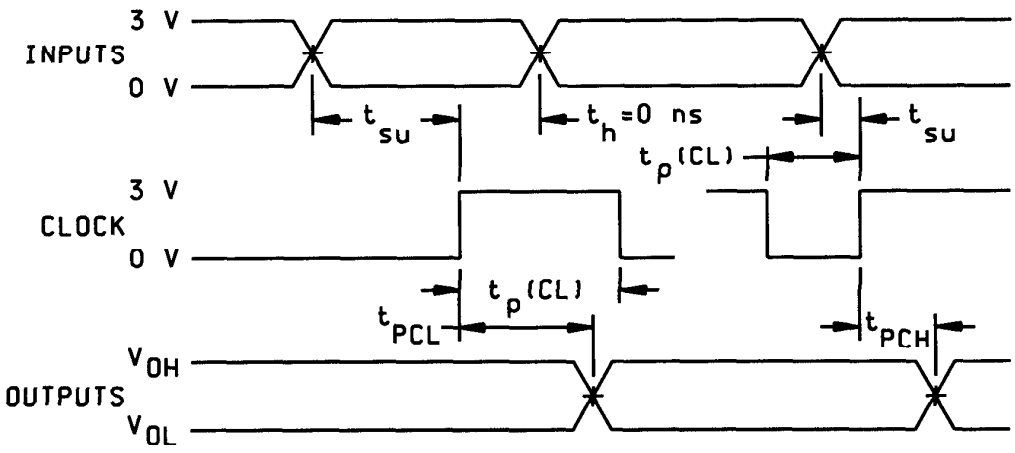


FIGURE 6. Switching time test circuit and waveforms.



REGISTERED SWITCHING WAVEFORM

NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent test which apply to the specific program configuration for the resulting PAL.
2. CL = 50 pF minimum, including jig and probe capacitance; R1 = 365Ω ±2 percent; R2 = 715Ω ±2 percent.
3. Outputs may be under load simultaneously.
4. Verification of limit conditions t_P(CL), t_{SU}, and t_h = 0 ns may be conducted by simultaneously setting the condition to the specified limit values of table III and observing for proper output state change.

FIGURE 6. Switching time test circuit and waveforms - Continued.

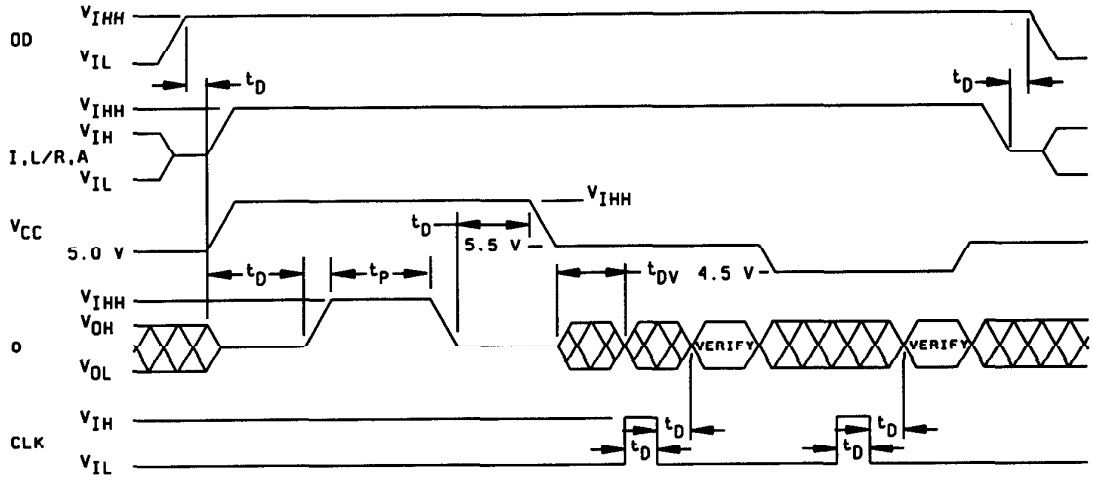


FIGURE 8a. Programming waveforms for circuit A.

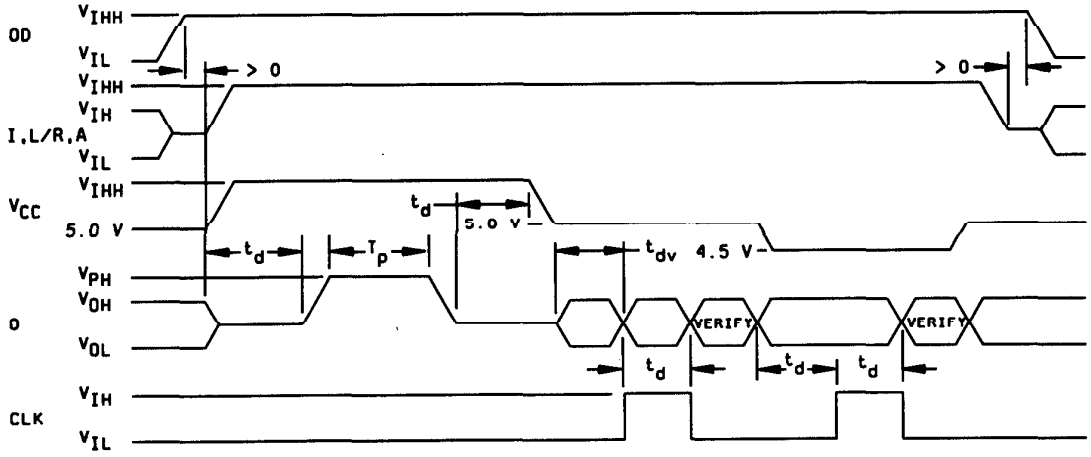


FIGURE 8b. Programming waveforms for circuit B.

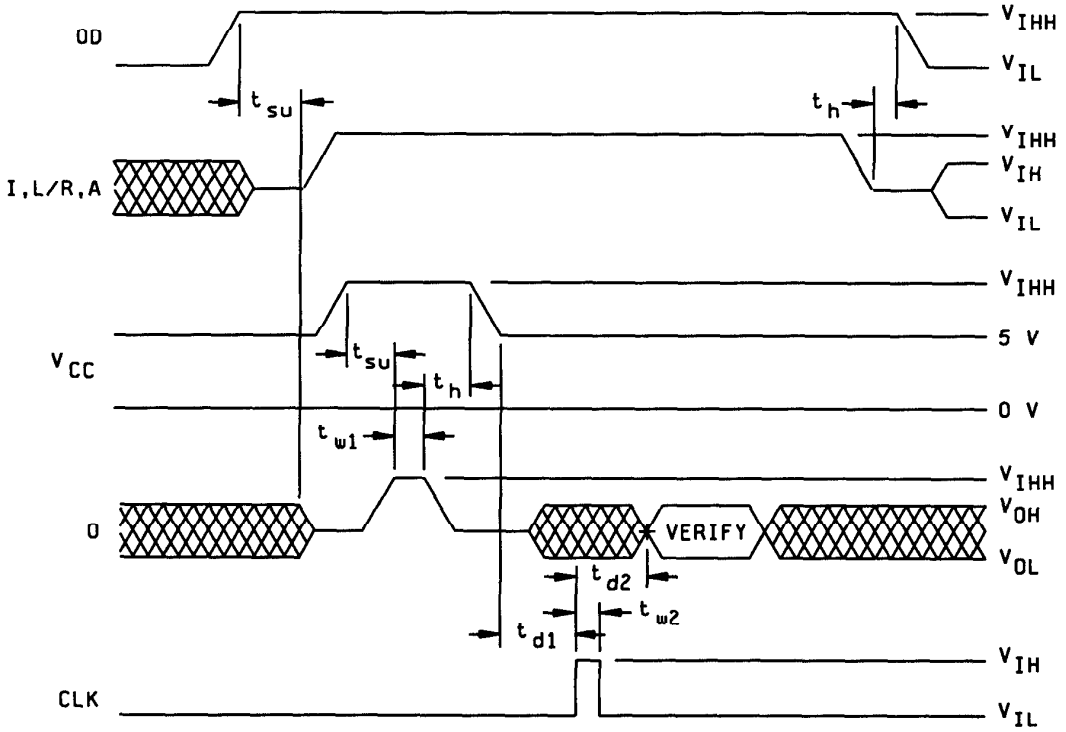
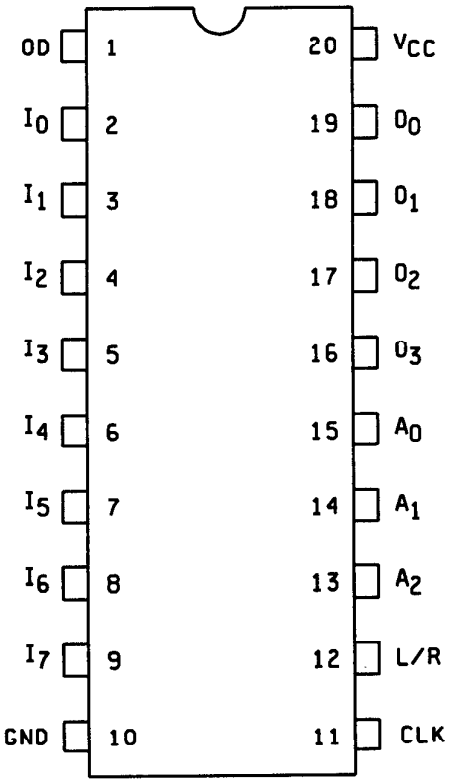


FIGURE 8c. Programming waveforms for circuit C.

PRODUCTS 0 THRU 31

TOP VIEW



PRODUCTS 32 THRU 63

TOP VIEW

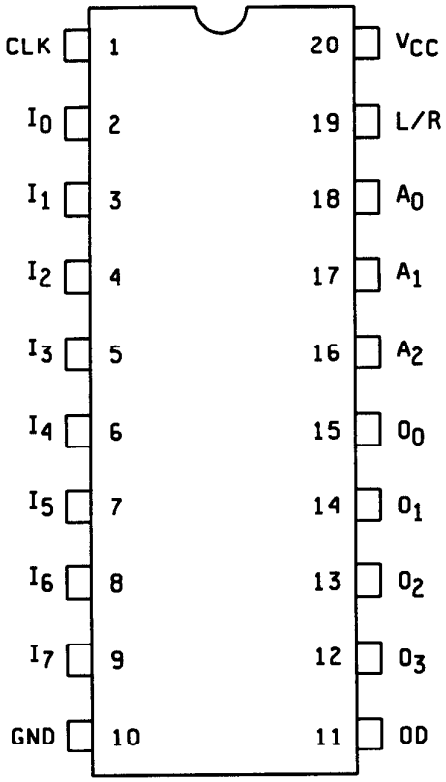


FIGURE 9. Programming pin identification for circuit A, B, and C.

TABLE IV. Programming characteristics for circuit A.

Symbol	Parameters		Limits			Units
			Min	Typ	Max	
V_{IHH}	Program - level input voltage		11.5	11.75	12.0	V
I_{IHH}	Program - level input current	Output program pulse	---	---	50	mA
		Output disable, OD	---	---	50	
		All other inputs	---	---	10	mA
I_{CCH}	Program supply current		---	---	900	mA
t_P	Program pulse width		10	20	50	μs
t_d	Delay time		100	---	---	ns
---	Program pulse duty cycle		---	---	20	%
V_P	Program/verify-protect-input voltage		18	18.5	19	V
I_P	Program/verify-protect-input current		---	---	400	mA
t_{PP}	Security fuse programming pulse width		10	40	70	μs
	Security fuse programming duty cycle		---	---	50	%
t_{RP}	Rise time of output programming and address pulses		1	1.5	10	V/μs
t_{RP}	Rise time of security fuse programming pulses		1	1.5	10	V/μs
V_{CCPP}	V_{CC} value during security fuse programming		5.75	6.0	6.25	V
	V_{CC} value for first verify		4.75	5.0	5.25	
	V_{CC} value for high V_{CC} verify		5.4	5.5	5.6	
	V_{CC} value for low V_{CC} verify		4.4	4.5	4.6	

TABLE V. Programming characteristics for circuit B.

Symbol	Parameters		Limits			Units
			Min	Typ	Max	
V_{IHH}	Program - level input voltage		11.0	11.5	12.0	V
I_{IHH}	Program - level input current	Output program pulse			50	mA
		OD, L/R			25	
		All other inputs			5	
I_{CCH}	Program supply current				400	mA
t_P	Program pulse width		10		50	μs
t_d	Delay time		100			ns
	Program pulse duty cycle				25	%
V_P	Program/verify-protect-input voltage			20		V
I_P	Program/verify-protect-input current				400	mA
t_{dv}	Delay time to verify		100			μs
V_{PH}	Programming pulse		11.0	11.5	12.0	V

TABLE VI. Programming characteristics for circuit C.

Symbol	Parameters		Limits			Units
			Min	Typ	Max	
V_{CC}	Verify - level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	Output PGM, pulse		20	50	mA
		OD, L/R		*10*	*25*	
		All other inputs		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program pulse duration at PO pins		10		50	μs
t_{w2}	Pusle duration at PGM verify		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from VCC to 5 V to PGM verify ↑		100			μs
t_{d2}	Delay time from PGM verify ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA

TABLE VII. Input line select for circuits A, B, and C.

Input line number	Pin identification								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V).

TABLE VIII. Product line select for circuits A, B, and C.

Product line number	Pin identification						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V).

The margins of this amendment are marked with asterisks to indicate where changes (additions, modifications, corrections, deletions) from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

Custodians:
Air Force - 17

Preparing activity:
DLA - ES

(Project 5962-1726)