INCH-POUND

MIL-M-38510/552
20 JANUARY 1989

# MILITARY SPECIFICATION

## MICROCIRCUITS, DIGITAL, CMOS, TIMING CONTROL UNIT, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

## 1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic silicon, CMOS, timing control unit (TCU) microcircuit. One product assurance class is provided and is reflected in the complete Part or Identifying Number (PIN) (see 6.7).

1.2 Classification.

1.2.1 Device type. The device type shall be as follows:

| Device type | Frequency | Circuit |
|---|---|---|
| 01 | 10.0 MHz | Timing control unit |

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

| Letter | Case outline (see MIL-M-38510, appendix C) |
|---|---|
| J | D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range | -0.3 V dc to +7.0 V dc |
| Input voltage range | -0.5 V to $V_{CC}$ +0.5 V |
| Output voltage range | -0.5 V to $V_{CC}$ +0.5 V |
| Maximum power dissipation | 1.0 W |
| Storage temperature range | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | 300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-M-38510, appendix C |
| Maximum junction temperature ($T_J$) | 130°C |

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5962

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1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | 4.75 V dc to 5.25 V dc |
| Case operating temperature range | -55°C to +125°C |
| Minimum high level input voltage ($V_{IH}$) except XIN and $\overline{RSTI}$ | 2.4 V |
| Maximum low level input voltage ($V_{IL}$) except XIN and $\overline{RSTI}$ | 0.8 V |
| Minimum high level input voltage XIN | 3.8 V |
| Maximum low level input voltage XIN | 1.0 V |
| Oscillation frequency | 10.0 MHz |

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| High level output voltage All outputs except XOUT, PHI1, PHI2 | $V_{OH}$ | | | $V_{CC} = 4.75$ V $I_{OH} = -1$ mA 2/ | 4.27 | | V |
| | | | | $V_{CC} = 5.25$ V $I_{OH} = -1$ mA 2/ | 4.72 | | |
| Low level output voltage All outputs except XOUT, PHI1, PHI2 | $V_{OL}$ | | | $I_{OL} = 2$ mA 2/ | | 0.5 | V |
| High level input voltage all except $\overline{RSTI}$ and XIN | $V_{IH}$ | | | 2/ | 2.4 | 5.75 | V |
| Low level input voltage all except $\overline{RSTI}$ and XIN | $V_{IL}$ | | | 2/ | -0.5 | 0.8 | V |
| $\overline{RSTI}$ rising threshold voltage | $V_{T+}$ | | | 2/ | 2.0 | 3.5 | V |
| $\overline{RSTI}$ hysteresis voltage | $V_{HYS}$ | | | 2/ | 0.8 | 1.8 | V |
| XIN input high voltage | $V_{XH}$ | | | $V_{CC} = 4.75$ V 2/ | 3.8 | | V |
| | | | | $V_{CC} = 5.25$ V 2/ | 4.2 | | |
| XIN input low voltage | $V_{XL}$ | | | $V_{CC} = 4.75$ V 2/ | | 0.94 | V |
| | | | | $V_{CC} = 5.25$ V 2/ | | 1.05 | |
| Low level output voltage PHI1 and PHI2 | $V_{OL}$ | | | $I_{OL} = 1$ mA 2/ | | 0.5 | V |
| High level output voltage PHI1 and PHI2 | $V_{OH}$ | | | $V_{CC} = 4.75$ V 2/ | 4.51 | | V |
| | | | | $V_{CC} = 5.25$ V 2/ | 4.98 | | V |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Input low current | $I_{IL}$ | | | $V_{IN}$ = 0.4 V 2/ | -20 | | µA |
| Input high current | $I_{IH}$ | | | $V_{IN}$ = 5.25 V 2/ | | 20 | µA |
| Three-state output leakage current high ($\overline{RD}$, $\overline{WR}$) | $I_{OZH}$ | | | $V_{OUT}$ = 5.25 V 2/ | | 20 | µA |
| Three-state output leakage current low ($\overline{RD}$, $\overline{WR}$) | $I_{OZL}$ | | | $V_{OUT}$ = 0.4 V 2/ | -20 | | µA |
| Supply current | $I_{CC}$ | | | f = 10 MHz 2/ | | 120 | mA |
| Clock period | $t_{CP}$ 3/ | A | 9 | PHI1 R.E. to next PHI1 R.E. 2/ | 100 | | ns |
| Clock high time for PHI1 and PHI2 | $t_{CLh}$ 3/ | A | 10 | 90% $V_{CC}$ on PHI1 R.E. to 90% $V_{CC}$ on PHI1 F.E. and 90% $V_{CC}$ on PHI2 R.E. to 90% $V_{CC}$ on PHI2 F.E. 2/ | 35 | 48 | ns |
| Clock low time | $t_{CLl}$ 3/ | A | 13 | 10% $V_{CC}$ on PHI1 F.E. to 10% $V_{CC}$ on PHI1 R.E. 2/ | 43 | 60 | ns |
| Clock pulse width PHI1 | $t_{CLw(1)}$ 3/ | A | 53 | At 2.0 V on PHI1 2/ | 40 | 52 | ns |
| Clock pulse width PHI2 | $t_{CLw(2)}$ 3/ | A | 54 | At 2.0 V on PHI2 2/ | 40 | 52 | ns |
| PHI1, PHI2 asymmetry | $t_{CLwas}$ | | | At 2.0 V on PHI1, PHI2 2/ | -5 | 5 | ns |
| Clock rise time | $t_{CLR}$ 3/ | A | 12 | 10% $V_{CC}$ on PHI1 R.E. to 90% $V_{CC}$ on PHI1 R.E. | | 8 4/ | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Clock fall time | $t_{CLF}$ 3/ | A | 11 | 90% $V_{CC}$ on PHI1 F.E. to 10% $V_{CC}$ on PHI1 F.E. | | 8 4/ | ns |
| Clock non-overlap time | $t_{nOVL}$ 3/ 4/ | A | 14 | 10% $V_{CC}$ on PHI1 to 10% $V_{CC}$ on PHI2 | -2 | 2 | ns |
| Non-overlap asymmetry | $t_{nOVLas}$ 3/ 4/ | | | At 10% $V_{CC}$ of PHI1, PHI2 2/ | -4 | 4 | ns |
| XIN high time (external output) | $t_{Xh}$ | A | 1 | At 80% $V_{CC}$ on XIN (both edges) 2/ | 16 | | ns |
| XIN low time (external output) | $t_{Xl}$ | A | 2 | At 20% $V_{CC}$ on XIN (both edges) 2/ | 16 | | ns |
| XIN to FCLK R.E. delay | $t_{XFr}$ | A | 3 | 80% $V_{CC}$ on XIN R.E. to FCLK R.E. 2/ | 3 | 29 | ns |
| XIN to FCLK F.E. delay | $t_{XFf}$ | A | 4 | 20% $V_{CC}$ on XIN F.E. to FCLK F.E. 2/ | 3 | 29 | ns |
| XIN to CTTL R.E. delay | $t_{XCr}$ 5/ | A | 5 | 80% $V_{CC}$ on XIN R.E. to CTTL R.E. 2/ | 3 | 34 | ns |
| XIN to PHI1 R.E. delay | $t_{XPr}$ 3/ | A | 8 | 80% $V_{CC}$ on XIN R.E. to PHI1 R.E. 2/ | 3 | 32 | ns |
| FCLK to CTTL R.E. delay | $t_{FCr}$ 5/ | A | 6 | FCLK R.E. to CTTL R.E. 2/ | -2 | 6 | ns |
| FCLK to CTTL F.E. delay | $t_{FCf}$ | A | 7 | FCLK R.E. to CTTL R.E. 2/ | -3 | 4 | ns |
| FCLK to PHI1 R.E. delay | $t_{FPr}$ 3/ | B | 16 | FCLK R.E. to PHI1 R.E. 2/ | -1 | 4 | ns |
| FCLK to PHI1 F.E. delay | $t_{FPf}$ 3/ | B | 17 | FCLK R.E. to PHI1 F.E. 2/ | -4 | -3 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| FCLK to pulse width with crystal | $t_{Fw}$ | B | 15 | At 50% $V_{CC}$ on FCLK (both edges) 2/ | 16 | 25 | ns |
| PHI2 R.E. to CTTL F.E. delay | $t_{PCf}$ 5/ | B | 18 | PHI2 R.E. to CTTL F.E. 2/ | -3 | 4 | ns |
| PHI1 to CTTL R.E. delay | $t_{PCr}$ | B | 19 | PHI1 R.E. to CTTL R.E. 2/ | -3 | 5 | ns |
| CTTL rise time | $t_{CTR}$ | B | 21 | 10% to 90% $V_{CC}$ on CTTL R.E. 2/ | | 5 4/ | ns |
| CTTL fall time | $t_{CTF}$ | B | 22 | 90% to 10% $V_{CC}$ on CTTL F.E. 2/ | | 5 4/ | ns |
| $\overline{RSTO}$ R.E. delay | $t_{RSTr}$ | F | 31 | After PHI1 R.E. 2/ | | 21 | ns |
| $\overline{RSTI}$ setup time | $t_{RSTs}$ | F | 30 | Before PHI1 R.E. 2/ | 20 | | ns |
| $\overline{ADS}$ setup time | $t_{ADs}$ | F | 32 | Before PHI1 R.E. 2/ | 30 | | ns |
| $\overline{ADS}$ pulse width | $t_{ADw}$ | F | 33 | $\overline{ADS}$ L.E. + $\overline{ADS}$ T.E. 2/ | 25 | | ns |
| $\overline{DDIN}$ setup time | $t_{DDs}$ | F | 34 | Before PHI1 R.E. 2/ | 15 | | ns |
| $\overline{TSO}$ L.E. delay | $t_{Tf}$ | C&E | 23 | After PHI1 R.E. 2/ | | 12 | ns |
| $\overline{TSO}$ T.E. delay | $t_{Tr}$ | C&E | 24 | After PHI1 R.E. 2/ | | 18 | ns |
| CTTL pulse width | $t_{CTw}$ | A | 20 | At 50% $V_{CC}$ on CTTL (both edges) 2/ | 43 | 51 | ns |
| $\overline{RD}/\overline{WR}$ L.E. delay (fast cycle) | $t_{RWf(F)}$ | E | 25 | After PHI1 R.E. 2/ | | 35 | ns |
| $\overline{RD}/\overline{WR}$ L.E. delay (peripheral cycle) | $t_{RWf(S)}$ | C | 35 | After PHI1 R.E. 2/ | | 25 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{RD}/\overline{WR}$ T.E. delay | $t_{RWr}$ | C & E | 26 | After PHI1 R.E. 2/ | | 25 | ns |
| $\overline{DBE}$ L.E. delay (write cycle) | $t_{DBf(W)}$ | C & E | 27 | After PHI1 R.E. 2/ | | 28 | ns |
| $\overline{DBE}$ L.E. delay (read cycle) | $t_{DBf(R)}$ | C & E | 28 | After PHI2 R.E. 2/ | | 21 | ns |
| $\overline{DBE}$ T.E. delay | $t_{DBr}$ | C & E | 29 | After PHI2 R.E. 2/ | | 23 | ns |
| $\overline{RD}$, $\overline{WR}$ low level to 3-state | $t_{PLZ}$ | D | 36 | After $\overline{RWEN}$/SYNC R.E. 2/ | | 30 | ns |
| $\overline{RD}$, $\overline{WR}$ high level to 3-state | $t_{PHZ}$ | D | 39 | After $\overline{RWEN}$/SYNC R.E. 2/ | | 30 | ns |
| $\overline{RD}$, $\overline{WR}$ 3-state to low level | $t_{PZL}$ | D | 37 | After $\overline{RWEN}$/SYNC F.E. 2/ | | 25 | ns |
| $\overline{RD}$, $\overline{WR}$ 3-state to high level | $t_{PZH}$ | D | 38 | After $\overline{RWEN}$/SYNC F.E. 2/ | | 25 | ns |
| $\overline{CWAIT}$ setup time (cycle hold) | $t_{CWs(H)}$ | G | 41 | Before PHI1 R.E. 2/ | 30 | | ns |
| $\overline{CWAIT}$ hold time (cycle hold) | $t_{CWh(H)}$ | G | 42 | After PHI1 R.E. 2/ | 0 | | ns |
| $\overline{CWAIT}$ setup time (wait states) | $t_{CWs(W)}$ | G & H | 40 | Before PHI2 R.E. 2/ | 10 | | ns |
| $\overline{CWAIT}$ hold time (wait states) | $t_{CWh(W)}$ | H | 44 | After PHI2 R.E. 2/ | 20 | | ns |
| $\overline{WAITn}$ setup time | $t_{Ws}$ | H | 45 | Before PHI2 R.E. 2/ | 7 | | ns |
| $\overline{WAITn}$ hold time | $t_{Wh}$ | H | 46 | After PHI2 R.E. 2/ | 20 | | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Fig. 5 | Ref. no. 1/ | Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5.0$ V ±5% | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{PER}$ setup time | $t_{Ps}$ | I | 49 | Before PHI1 R.E. 2/ | 7 | | ns |
| $\overline{PER}$ hold time | $t_{Ph}$ | I | 48 | After PHI1 R.E. 2/ | 30 | | ns |
| RDY delay | $t_{Rd}$ | H & I | 47 | After PHI2 R.E. 2/ | | 25 | ns |
| SYNC setup time | $t_{Sys}$ | J | 50 | Before XIN R.E. 2/ | 6 | | ns |
| SYNC hold time | $t_{Syh}$ | J | 51 | After XIN R.E. 2/ | 0 | | ns |
| CTTL/SYNC inversion delay | $t_{CS}$ | J | 52 | CTTL (master) to $\overline{RWEN}$/SYNC (slave) 2/ | | 10 | ns |
| Capacitance input | $C_I$ | | | 6/ | | 30 | pF |
| Capacitance output | $C_O$ | | | 6/ | | 40 | pF |
| Capacitance clock | $C_{clk}$ | | | 6/ | | 30 | pF |

1/ The reference number refers to the position where the parameter appears on figure 5.

2/ Timing measurements are made at 10% and 90% of $V_{CC}$, unless otherwise specified. DC voltages are verified at a test frequency of 1 MHz. AC test voltage levels are $V_{IL}$ = 0.4 V and $V_{IH}$ = 3.0 V except $X_{IN}$ and RSTI which are $V_{IL}$ = 0.5 V and $V_{IH}$ = 4.2 V. All output voltage levels are $V_{OL}$ = 1.6 V and $V_{OH}$ = 2.0 V. AC test are performed at 10 MHz and $C_L$ = 30 pF. R.E. = Rising edge, T.E. = trailing edge, F.E. = falling edge, and L.E. = leading edge.

3/ PHI1 and PHI2 are interchangeable for the following parameters: $t_{Cp}$, $t_{CLh}$, $t_{CL1}$, $t_{CLw}$, $t_{CLR}$, $t_{CLF}$, $t_{nOVL}$, $t_{XPr}$, $t_{FPr}$, $t_{FPf}$.

4/ This limit guaranteed to limit specified herein by characterization data.

5/ Parameters $t_{XCr}$, $t_{FCr}$, $t_{PCf}$, and $t_{CTh}$ are measured with 30 pF load on CTTL.

6/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz, and $T_C = +25^{\circ}C$. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Functional description, terms, and symbols. The functional description, terms, and symbols shall be as specified in 6.4.

3.2.4 Case outlines. The case outline shall be as specified in MIL-M-38510, appendix C, and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table III herein, for the applicable device type and device class. The electrical tests for each subgroup are described in table III, herein and table VI, test vectors which form a part of the manufacturing test type.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.6.1 Total dose radiation hardness identifier. The total dose radiation hardness identifier shall be in accordance with MIL-M-38510, and as specified herein.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

   1. Test condition D, using the circuit shown on figure 3, or equivalent.

   2. $T_A = +125°C$.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) is specified as 10% for class B devices based on failures from group A, subgroups 1 and 7 tests, after cool down as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre-burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta ($\Delta$) limits specified in table II, footnote 3 herein, or electrical parameter limits specified in table III, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

TABLE II. Electrical test requirements.

| Line no. | MIL-STD-883 test requirements | Subgroups (see table III) Class B devices |
|---|---|---|
| 1 | Interim electrical parameters (method 5004) | 1, 7 |
| 2 | Dynamic burn-in (method 1015) | Required |
| 3 | Same as line 1 | *1Δ 2/ 3/ |
| 4 | Final electrical test parameters (method 5004) | *1, 2, 3, *7, 8, 9, 10, 11 1/ 4/ |
| 5 | Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10, 11, 5/ |
| 6 | Group B end-point electrical parameters | See 4.4.2 |
| 7 | Group C end-point electrical parameters (method 5005) 2/ | 1, 2, 3, 7, 8 |
| 8 | Group D end-point electrical parameters (method 5005) | 1, 2, 3, 7, 8 |

1/ (*) PDA applies to subgroups 1 and 7 (see 4.2c).

2/ (Δ) indicates a delta limit shall be required only on table III, subgroup 1 and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

3/ Delta limit at 25°C for $I_{CC}$ is 12 mA.

4/ The device manufacturer may, at his option, either complete the required electrical parameter measurements (subgroup 1), including delta measurements within 96 hours after burn-in completion (removal of bias); or may complete the required electrical measurements (subgroup 1) without delta measurements within 24 hours after burn-in completion (removal of bias).

5/ Capacitance testing (see 4.4.1b).

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designed may be H ≥ 2.0 V, L ≤ 0.7 V, or open)

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 1 $\overline{DBE}$ | 2 $\overline{RWEN}$/SYNC | 3 $\overline{RD}$ | 4 $\overline{WR}$ | 5 $\overline{DDIN}$ | 6 $\overline{ADS}$ | 7 $\overline{RSTI}$ | 8 $\overline{RSTO}$ | 9 RDY | 10 PHI2 | 11 PHI1 | 12 GND | 13 XIN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1<br>$T_C$ = 25°C | $I_{IL}$ | 3009 | 1 | | | | | | | | | | | | 0.0 V | 0.0 V |
| | | | 2 | | | | | | | 0.0 V | | | | | " | |
| | | | 3 | | 0.0 V | | | | | | | | | | " | |
| | | | 4 | | | | | | 0.0 V | | | | | | " | |
| | | | 5 | | | | | 0.0 V | | | | | | | " | |
| | | | 6 | | | | | | | | | | | | " | |
| | | | 7 | | | | | | | | | | | | " | |
| | | | 8 | | | | | | | | | | | | " | |
| | | | 9 | | | | | | | | | | | | " | |
| | | | 10 | | | | | | | | | | | | " | |
| | | | 11 | | | | | | | | | | | | " | |
| | $I_{IH}$ | 3010 | 12 | | | | | | | | | | | | " | 5.25 V |
| | | | 13 | | | | | | | 5.25 V | | | | | " | |
| | | | 14 | | 5.25 V | | | | | | | | | | " | |
| | | | 15 | | | | | | 5.25 V | | | | | | " | |
| | | | 16 | | | | | 5.25 V | | | | | | | " | |
| | | | 17 | | | | | | | | | | | | " | |
| | | | 18 | | | | | | | | | | | | " | |
| | | | 19 | | | | | | | | | | | | " | |
| | | | 20 | | | | | | | | | | | | " | |
| | | | 21 | | | | | | | | | | | | " | |
| | | | 22 | | | | | | | | | | | | " | |
| | $I_{OZL}$ 1/ | | 23 | | | | 0.4 V | | | | | | | | " | |
| | | | 24 | | | | | 0.4 V | | | | | | | " | |
| | $I_{OZH}$ 1/ | | 25 | | | | 5.25 V | | | | | | | | " | |
| | | | 26 | | | | | 5.25 V | | | | | | | " | |
| | $V_{OL}$ 1/ | 3007 | 27 | | | | | | | | 2 mA | | | | " | |
| | | | 28 | | | 2 mA | | | | | | | | | " | |
| | | | 29 | | | | 2 mA | | | | | | | | " | |
| | | | 30 | | 2 mA | | | | | | | | | | " | |
| | | | 31 | | | | | | | | | | | | " | |
| | | | 32 | | | | | | | | | 2 mA | | | " | |
| | | | 33 | | | | | | | | | | | | " | |
| | | | 34 | | | | | | | | | | | 1 mA | " | |
| | | | 35 | | | | | | | | | | 1 mA | | " | |
| | | | 36 | | | | | | | | | | | | " | |
| | | | 37 | | | | | | | | | | | | " | |
| | $V_{OH}$ 1/ | 3006 | 38 | | | | | | | | -1 mA | | | | " | |
| | | | 39 | | | -1 mA | | | | | | | | | " | |
| | | | 40 | | | | -1 mA | | | | | | | | " | |
| | | | 41 | | -1 mA | | | | | | | | | | " | |
| | | | 42 | | | | | | | | | | | | " | |
| | | | 43 | | | | | | | | | -1 mA | | | " | |
| | | | 44 | | | | | | | | | | | | " | |
| | | | 45 | | | | | | | | | | | -1 mA | " | |
| | | | 46 | | | | | | | | | | -1 mA | | " | |
| | | | 47 | | | | | | | | | | | | " | |
| | | | 48 | | | | | | | | | | | | " | |
| | $V_{T+}$ 1/ 2/ | 3006 | 49 | | | | | | | | | | | | " | |
| | $V_{HYS}$ 1/ 3/ | 3006 | 50 | | | | | | | | | | | | " | |
| | $I_{CC}$ | 3005 | 51 | | | | | | | | | | | | " | 4/ |

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designed may be H ≥ 2.0 V, L ≤ 0.7 V, or open)

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 14 XOUT | 15 FCLK | 16 CTTL | 17 $\overline{TSO}$ | 18 $\overline{WAIT8}$ | 19 $\overline{WAIT4}$ | 20 $\overline{WAIT2}$ | 21 $\overline{WAIT1}$ | 22 $\overline{CWAIT}$ | 23 $\overline{PER}$ | 24 $V_{CC}$ | Measured terminal | Test limits Min | Test limits Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 $T_C$ = 25°C | $I_{IL}$ | 3009 | 1 | | | | | | | | | | | 5.25 V | XIN | -10 | | μA |
| | | | 2 | | | | | | | | | | | " | $\overline{RST1}$ | " | | " |
| | | | 3 | | | | | | | | | | | " | RWEN/SYNC | " | | " |
| | | | 4 | | | | | | | | | | | " | $\overline{ADS}$ | " | | " |
| | | | 5 | | | | | | | | | | | " | $\overline{DDIN}$ | " | | " |
| | | | 6 | | | | | | | | | | 0.0 V | " | $\overline{PER}$ | " | | " |
| | | | 7 | | | | | | | | | 0.0 V | | " | $\overline{CWAIT}$ | " | | " |
| | | | 8 | | | | | | | | 0.0 V | | | " | $\overline{WAIT1}$ | " | | " |
| | | | 9 | | | | | | | 0.0 V | | | | " | $\overline{WAIT2}$ | " | | " |
| | | | 10 | | | | | | 0.0 V | | | | | " | $\overline{WAIT4}$ | " | | " |
| | | | 11 | | | | | 0.0 V | | | | | | " | $\overline{WAIT8}$ | " | | |
| | $I_{IH}$ | 3010 | 12 | | | | | | | | | | | " | XIN | | 10 | " |
| | | | 13 | | | | | | | | | | | " | $\overline{RST1}$ | | " | " |
| | | | 14 | | | | | | | | | | | " | RWEN/SYNC | | " | " |
| | | | 15 | | | | | | | | | | | " | $\overline{ADS}$ | | " | " |
| | | | 16 | | | | | | | | | | | " | $\overline{DDIN}$ | | " | " |
| | | | 17 | | | | | | | | | | 5.25 V | " | $\overline{PER}$ | | " | " |
| | | | 18 | | | | | | | | | 5.25 V | | " | $\overline{CWAIT}$ | | " | " |
| | | | 19 | | | | | | | | 5.25 V | | | " | $\overline{WAIT1}$ | | " | " |
| | | | 20 | | | | | | | 5.25 V | | | | " | $\overline{WAIT2}$ | | " | " |
| | | | 21 | | | | | | 5.25 V | | | | | " | $\overline{WAIT4}$ | | " | " |
| | | | 22 | | | | | 5.25 V | | | | | | " | $\overline{WAIT8}$ | | " | " |
| | $I_{OZL}$ 1/ | | 23 | | | | | | | | | | | " | $\overline{RD}$ | -20 | | " |
| | | | 24 | | | | | | | | | | | " | $\overline{WR}$ | -20 | | " |
| | $I_{OZH}$ 1/ | | 25 | | | | | | | | | | | " | $\overline{RD}$ | | 20 | " |
| | | | 26 | | | | | | | | | | | " | $\overline{WR}$ | | 20 | " |
| | $V_{OL}$ 1/ | 3007 | 27 | | | | | | | | | | | " | $\overline{RST0}$ | | 0.50 | V |
| | | | 28 | | | | | | | | | | | " | $\overline{RD}$ | | " | " |
| | | | 29 | | | | | | | | | | | " | $\overline{WR}$ | | " | " |
| | | | 30 | | | | | | | | | | | " | $\overline{DBE}$ | | " | " |
| | | | 31 | | | | 2 mA | | | | | | | " | $\overline{TSO}$ | | " | " |
| | | | 32 | | | | | | | | | | | " | $\overline{RDY}$ | | " | " |
| | | | 33 | | 2 mA | | | | | | | | | " | FCLK | | " | " |
| | | | 34 | | | | | | | | | | | " | PHI1 | | " | " |
| | | | 35 | | | | | | | | | | | " | PHI2 | | " | " |
| | | | 36 | | | 2 mA | | | | | | | | " | CTTL | | " | " |
| | | | 37 | 2 mA | | | | | | | | | | " | XOUT | | " | " |
| | $V_{OH}$ 1/ | 3006 | 38 | | | | | | | | | | | 4.75 V | $\overline{RST0}$ | 4.275 | | " |
| | | | 39 | | | | | | | | | | | " | $\overline{RD}$ | " | | " |
| | | | 40 | | | | | | | | | | | " | $\overline{WR}$ | " | | " |
| | | | 41 | | | | | | | | | | | " | $\overline{DBE}$ | " | | " |
| | | | 42 | | | | -1 mA | | | | | | | " | $\overline{TSO}$ | " | | " |
| | | | 43 | | | | | | | | | | | " | $\overline{RDY}$ | " | | " |
| | | | 44 | | -1 mA | | | | | | | | | " | FCLK | " | | " |
| | | | 45 | | | | | | | | | | | " | PHI1 | " | | " |
| | | | 46 | | | | | | | | | | | " | PHI2 | " | | " |
| | | | 47 | | | -1 mA | | | | | | | | " | CTTL | " | | " |
| | | | 48 | -1 mA | | | | | | | | | | " | XOUT | " | | " |
| | $V_{T+}$ 1/ 2/ | 3006 | 49 | | | | | | | | | | | 5.00 V | $\overline{RST1}$ | 2.0 | 3.5 | " |
| | $V_{HYS}$ 1/ 3/ | 3006 | 50 | | | | | | | | | | | 5.00 V | $\overline{RST1}$ | 0.8 | 1.8 | " |
| | $I_{CC}$ | 3005 | 51 | | | | | | | | | | | 5.25 V | $V_{CC}$ | | 120 | mA |

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designed may be H ≥ 2.0 V, L ≤ 0.7 V, or open)

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 1 $\overline{DBE}$ | 2 $\overline{RWEN}$/SYNC | 3 $\overline{RD}$ | 4 $\overline{WR}$ | 5 $\overline{DDIN}$ | 6 $\overline{ADS}$ | 7 $\overline{RSTI}$ | 8 $\overline{RSTO}$ | 9 RDY | 10 PHI2 | 11 PHI1 | 12 GND | 13 XIN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 $T_C$ = 125°C | | | 52-102 | Tests 52-102: Repeat tests 1 through 51, $T_C$ = +125°C. For test limits, see table I. | | | | | | | | | | | | |
| 3 $T_C$ = -55°C | | | 103-153 | Tests 103-153: Repeat tests 1 through 51, $T_C$ = -55°C. For test limits, see table I. | | | | | | | | | | | | |
| 4 $T_C$ = 25°C | $C_O$ | 3012 | 154 | 5/ 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V |
| | | | 155 | | " | 5/ 0.0 V | " | " | " | " | " | " | " | " | " | " |
| | | | 156 | | " | " | 5/ 0.0 V | " | " | " | " | " | " | " | " | " |
| | | | 157 | | " | " | " | " | " | " | 5/ 0.0 V | " | " | " | " | " |
| | | | 158 | | " | " | " | " | " | " | " | 5/ 0.0 V | " | " | " | " |
| | | | 159 | | " | " | " | " | " | " | " | " | 5/ 0.0 V | " | " | " |
| | | | 160 | | " | " | " | " | " | " | " | " | " | 5/ 0.0 V | " | " |
| | | | 161 | | " | " | " | " | " | " | " | " | " | " | 5/ 0.0 V | " |
| | | | 162 | | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 163 | | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 164 | | " | " | " | " | " | " | " | " | " | " | " | " |
| | $C_I$ | 3012 | 165 | 0 0 V | 5/ 0.0 V | " | " | " | " | " | " | " | " | " | " | " |
| | | | 166 | " | " | " | " | 5/ 0.0 V | " | " | " | " | " | " | " | " |
| | | | 167 | " | " | " | " | " | 5/ 0.0 V | " | " | " | " | " | " | " |
| | | | 168 | " | " | " | " | " | " | 5/ 0.0 V | " | " | " | " | " | " |
| | | | 169 | " | " | " | " | " | " | " | " | " | " | " | " | 5/ 0.0 V |
| | | | 170 | " | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 171 | " | " | " | " | " | " | " | " | " | 0.0 V | 5/ 0.0 V | " | " |
| | | | 172 | " | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 173 | " | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 174 | " | " | " | " | " | " | " | " | " | " | " | " | " |
| | | | 175 | " | " | " | " | " | " | " | " | " | " | " | " | " |
| 7 $T_C$ = 25°C | 6/ 7/ 8/ | 3014 | 176 | Functional testing. | | | | | | | | | | | | |
| 8 $T_C$ = 125°C $T_C$ = -55°C | 6/ 7/ 8/ | 3014 | 177 | Functional testing. Same tests, terminal conditions and limits as subgroup 7 except $T_C$ = 125°C and -55°C. | | | | | | | | | | | | |
| 9 $T_C$ = 25°C | 6/ 7/ 8/ 9/ | 3014 | 178-230 | Switching tests (see table IV). | | | | | | | | | | | | |
| 10 $T_C$ = 125°C | 6/ 8/ 9/ | 3014 | 231-283 | Switching tests. Repeat tests, 178 through 230 except $T_C$ = 125°C | | | | | | | | | | | | |
| 11 $T_C$ = -55°C | 6/ 7/ 9/ | 3014 | 284-336 | Switching tests. Repeat tests, 178 through 230 except $T_C$ = -55°C | | | | | | | | | | | | |

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designed may be H ≥ 2.0 V, L ≤ 0.7 V, or open)

| Subgroup | Symbol | MIL-STD-883 method | Test no. | 14 XOUT | 15 FCLK | 16 CTTL | 17 $\overline{TSO}$ | 18 $\overline{WAIT8}$ | 19 $\overline{WAIT4}$ | 20 $\overline{WAIT2}$ | 21 $\overline{WAIT1}$ | 22 $\overline{CWAIT}$ | 23 $\overline{PER}$ | 24 $V_{CC}$ | Measured terminal | Test limits Min | Test limits Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 $T_C$ = 125°C | | | 52-102 | Tests 52-102: Repeat tests 1 through 51, $T_C$ = +125°C | | | | | | | | | | | | | | |
| 3 $T_C$ = -55°C | | | 103-153 | Tests 103-153: Repeat tests 1 through 51, $T_C$ = -55°C | | | | | | | | | | | | | | |
| 4 $T_C$ = 25°C | $C_O$ | 3012 | 154 | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | 0.0 V | $\overline{DBE}$ | | 40 | pF |
| | | | 155 | " | " | " | " | " | " | " | " | " | " | " | $\overline{RD}$ | | " | " |
| | | | 156 | " | " | " | " | " | " | " | " | " | " | " | $\overline{WR}$ | | " | " |
| | | | 157 | " | " | " | " | " | " | " | " | " | " | " | $\overline{RSTO}$ | | " | " |
| | | | 158 | " | " | " | " | " | " | " | " | " | " | " | RDY | | " | " |
| | | | 159 | " | " | " | " | " | " | " | " | " | " | " | PHI2 | | " | " |
| | | | 160 | " | " | " | " | " | " | " | " | " | " | " | PHI1 | | " | " |
| | | | 161 | 5/ | " | " | " | " | " | " | " | " | " | " | XOUT | | " | " |
| | | | 162 | 0.0 V | 5/ | " | " | " | " | " | " | " | " | " | FCLK | | " | " |
| | | | 163 | " | 0.0 V | 5/ | " | " | " | " | " | " | " | " | CTTL | | " | " |
| | | | 164 | " | " | 0.0 V | 5/ | " | " | " | " | " | " | " | $\overline{TSO}$ | | " | " |
| | $C_I$ | 3012 | 165 | " | " | " | 0.0 V | " | " | " | " | " | " | " | $\overline{RWEN}$/SYNC | | 30 | " |
| | | | 166 | " | " | " | " | " | " | " | " | " | " | " | $\overline{DDIN}$ | | " | " |
| | | | 167 | " | " | " | " | " | " | " | " | " | " | " | $\overline{ADS}$ | | " | " |
| | | | 168 | " | " | " | " | " | " | " | " | " | " | " | $\overline{RSTI}$ | | " | " |
| | | | 169 | " | " | " | " | " | " | " | " | " | " | " | XIN | | " | " |
| | | | 170 | " | " | " | " | " | " | " | 5/ | " | " | " | $\overline{WAIT1}$ | | " | " |
| | | | 171 | " | " | " | " | " | " | 5/ | 0.0 V | " | " | " | $\overline{WAIT2}$ | | " | " |
| | | | 172 | " | " | " | " | " | 5/ | 0.0 V | " | " | " | " | $\overline{WAIT4}$ | | " | " |
| | | | 173 | " | " | " | " | 5/ | 0.0 V | " | " | " | " | " | $\overline{WAIT8}$ | | " | " |
| | | | 174 | " | " | " | " | 0.0 V | " | " | " | 5/ | " | " | $\overline{CWAIT}$ | | " | " |
| | | | 175 | " | " | " | " | 0.0 V | " | " | " | 0.0 V | 5/ | " | $\overline{PER}$ | | " | " |
| 7 $T_C$ = 25°C | 6/ 7/ 8/ | 3014 | 176 | Functional testing | | | | | | | | | | | | | | |
| 8 $T_C$ = 125°C $T_C$ = -55°C | 6/ 7/ 8/ | 3014 | 177 | Functional testing. Same tests, terminal conditions and limits as subgroup 7 except $T_C$ = 125°C and -55°C | | | | | | | | | | | | | | |
| 9 $T_C$ = 25°C | 6/ 7/ 8/ 9/ | 3014 | 178-230 | Switching tests (see table IV). | | | | | | | | | | | | | | |
| 10 $T_C$ = 125°C | 6/ 8/ 9/ | 3014 | 231-283 | Switching tests. Repeat tests, 178 through 230 except $T_C$ = 125°C | | | | | | | | | | | | | | |
| 11 $T_C$ = -55°C | 6/ 7/ 9/ | 3014 | 284-336 | Switching tests. Repeat tests, 178 through 230 except $T_C$ = -55°C | | | | | | | | | | | | | | |

See footnotes at end of table.

1/ $V_{T(+)}$, $V_{HYS}$, $V_{XH}$, $V_{OL}$, $I_{OZL}$, $I_{OZH}$ and $V_{OH}$ are tested with the same conditions as subgroups 7 and 8.

2/ Increment input in 50 mV steps beginning 100 mV above the maximum limit specified until the output changes from GND to $V_{CC}$. The input voltage where this transition occurs is $V_{T+}$.

3/ $V_{HYS} = (V_{T+})-(V_{T-})$. See table I for $V_{HYS}$ limits.

4/ Apply 20 MHz signal to XIN.

5/ The capacitance measurements should be made between the indicated terminal and ground at frequency of 1 MHz. The dc bias of the measuring instrument should be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms. The tests will be conducted in accordance with MIL-STD-883, method 3012.

6/ For functional tests, input/output conditions A, B, and C, appear in table V.

7/ Table VI functional tests shall be repeated for input/output conditions A, B, and C of table V (see 6.3).

8/ When patterns are applied as specified for subgroups 7 and 8, they verify the dynamic, functional output threshold and switching parameters at $T_C$ = +25°C, -55°C, and +125°C (see 6.3).

9/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.

10/ $\overline{RSTO}$ goes high on the first rising edge of PHI1 after $\overline{RSTI}$ goes high.

TABLE IV. Switching tests for group A inspection for device type 01.

| Test number | Symbol | Terminals | Figure 5 | Reference number 1/ | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| 178 | $t_{Cp}$ | PHI1 | A | 9 | 100 | 48 | ns |
| 179 | $t_{CLh}$ | PHI1 | A | 10 | 35 | 47 | ns |
| 180 | $t_{CLl}$ | PHI1 | A | 13 | 43 | 60 | ns |
| 181 | $t_{CLw(1,2)}$ | PHI1/PHI2 | A | 54 & 53 | 40 | 52 | ns |
| 182 | $t_{CLwas}$ | PHI1/PHI2 | | | -5 | 5 | ns |
| 183 | $t_{CLR}$ | PHI1 | A | 12 | | 7 | ns |
| 184 | $t_{CLF}$ | PHI1 | A | 11 | | 7 | ns |
| 185 | $t_{nOVL}$ | PHI2 | A | 14 | -2 | 5 | ns |
| 186 | $t_{nOVLas}$ | PHI1/PHI2 | | | -4 | 4 | ns |
| 187 | $t_{Xh}$ | XIN | A | 1 | 16 | | ns |
| 188 | $t_{Xl}$ | XIN | A | 2 | 16 | | ns |
| 189 | $t_{XFr}$ | XIN/FCLK | A | 3 | 6 | 29 | ns |
| 190 | $t_{XFf}$ | XIN/FCLK | A | 4 | 6 | 29 | ns |
| 191 | $t_{XCr}$ | XIN/CTTL | A | 5 | 6 | 34 | ns |
| 192 | $t_{XPr}$ | XIN/PHI1 | A | 8 | 3 | 32 | ns |
| 193 | $t_{FCr}$ | FCLK/CTTL | A | 6 | 2 | 6 | ns |
| 194 | $t_{FCf}$ | FCLK/CTTL | A | 7 | -3 | 4 | ns |
| 195 | $t_{FPr}$ | FCLK/PHI1 | B | 16 | -7 | 4 | ns |
| 196 | $t_{FPf}$ | FCLK/PHI1 | B | 17 | -4 | -3 | ns |
| 197 | $t_{CWh(W)}$ | PHI2/$\overline{CWAIT}$ | H | 44 | 20 | 30 | ns |
| 198 | $t_{PCf}$ | PHI2/CTTL | B | 18 | -3 | 4 | ns |
| 199 | $t_{CTw}$ | CTTL | A | 20 | 43 | 51 | ns |
| 200 | $t_{PCr}$ | PHI1/CTTL | B | 19 | -3 | 5 | ns |
| 201 | $t_{CTr}$ | CTTL | B | 21 | | 5 | ns |
| 202 | $t_{CTF}$ | CTTL | B | 22 | | 5 | ns |
| 203 | $t_{RSTr}$ | PHI1/$\overline{RSTO}$ | F | 31 | | 21 | ns |
| 204 | $t_{RSTs}$ | $\overline{RSTI}$/PHI1 | F | 30 | 20 | | ns |
| 205 | $t_{ADs}$ | $\overline{ADS}$/PHI1 | F | 32 | 30 | | ns |
| 206 | $t_{ADw}$ | $\overline{ADS}$ | F | 33 | 25 | | ns |
| 207 | $t_{DDs}$ | $\overline{DDIN}$/PHI1 | F | 34 | 15 | | ns |
| 208 | $t_{Tf}$ | PHI1/$\overline{TSO}$ | C & E | 23 | | 12 | ns |
| 209 | $t_{Tr}$ | PHI1/$\overline{TSO}$ | C & E | 24 | | 18 | ns |
| 210 | $t_{RWF(F)}$ | PHI1/$\overline{RD}$,$\overline{WR}$ | E | 25 | | 35 | ns |
| 211 | $t_{RWf(S)}$ | PHI1/$\overline{RD}$,$\overline{WR}$ | C | 35 | | 25 | ns |
| 212 | $t_{RWr}$ | PHI1/$\overline{RD}$,$\overline{WR}$ | C & E | 26 | | 25 | ns |
| 213 | $t_{DBf(W)}$ | PHI1/$\overline{DBE}$ | C & E | 27 | | 28 | ns |
| 214 | $t_{DBf(R)}$ | PHI2/$\overline{DBE}$ | C & E | 28 | | 21 | ns |
| 215 | $t_{DBr}$ | PHI2/$\overline{DBE}$ | C & E | 29 | | 23 | ns |
| 216 | $t_{PLz}$ | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | D | 36 | | 30 | ns |
| 217 | $t_{PHz}$ | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | D | 39 | | 30 | ns |
| 218 | $t_{PZL}$ | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | D | 37 | | 25 | ns |
| 219 | $t_{PZH}$ | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | D | 38 | | 25 | ns |
| 220 | $t_{CWs(H)}$ | $\overline{CWAIT}$/PHI1 | G | 41 | 30 | | ns |
| 221 | $t_{CWh(H)}$ | PHI1/$\overline{CWAIT}$ | G | 42 | 0 | | ns |
| 222 | $t_{CWs(W)}$ | $\overline{CWAIT}$/PHI2 | G & H | 40 | 10 | | ns |

See footnote at end of table.

TABLE IV. Switching tests for group A inspection for device type 01 - Continued.

| Test number | Symbol | Terminals | Figure 5 | Reference number 1/ | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| 223 | $t_{Ws}$ | $\overline{WAITn}$/PHI2 | H | 45 | 7 | | ns |
| 224 | $t_{Wh}$ | PHI2/$\overline{WAITn}$ | H | 46 | 20 | | ns |
| 225 | $t_{Ps}$ | $\overline{PER}$/PHI1 | I | 49 | 7 | | ns |
| 226 | $t_{Ph}$ | PHI1/$\overline{PER}$ | I | 48 | 30 | | ns |
| 227 | $t_{Ph}$ | PHI2/RDY | H & I | 47 | | 25 | ns |
| 228 | $t_{Sgs}$ | ($\overline{RWEN}$/SYNC)/FCLK | J | 50 | 6 | | ns |
| 229 | $t_{Syh}$ | FCLKN/$\overline{RWEN}$/SYNC | J | 51 | 0 | | ns |
| 230 | $t_{Cs}$ | CTTL/($\overline{RWEN}$/SYNC) | J | 52 | | 10 | ns |

1/ The reference number refers to the position where the parameter being measured appears on figure 5.

TABLE V. Input and output conditions for table III for device type 01.

| Symbol | Figure 5 | Reference number 1/ | Terminals | Test conditions 2/ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | A | B | C | |
| $V_{CC}$ | | | $V_{CC}$ | 5.25 | 4.75 | 5.25 | V |
| $V_{OH}$ | | | All logic outputs except XOUT | 2.0 | 2.0 | 2.0 | V |
| $V_{OL}$ | | | All logic outputs except XOUT | 1.6 | 1.6 | 1.6 | V |
| $V_{IH}$ | | | All logic inputs except $\overline{RSTI}$ and XIN | 3.0 | 3.0 | 5.75 | V |
| $V_{IL}$ | | | All logic inputs except $\overline{RSTI}$ and XIN | 0.4 | 0.4 | -0.5 | V |
| $V_{T+}$ | | | | 4.2 | 4.2 | 4.2 | V |
| $V_{HYS}$ | | | | 1.80 | 1.80 | 1.80 | V |
| $V_{XH}$ | | | XIN | 4.7 | 4.2 | 5.75 | V |
| $V_{XL}$ | | | XIN | 0.5 | 0.5 | -0.5 | V |
| $t_{CP}$ | A | 9 | PHI1 | 100 | 100 | 100 | ns |
| $t_{CLh}$ | A | 10 | PHI1 | 35 | 35 | 35 | ns |
| $t_{CLl}$ | A | 13 | PHI1 | 60 | 60 | 60 | ns |
| $t_{CLw}$ (1,2) | A | 53 & 54 | PHI1 and PHI2 | 52 | 52 | 52 | ns |
| $t_{CLR}$ | A | 12 | PHI1 | 8 | 8 | 8 | ns |
| $t_{CLF}$ | A | 11 | PHI1 | 8 | 8 | 8 | ns |
| $t_{nOVL}$ | A | 14 | PHI1 and PHI2 | -2 | -2 | -2 | ns |

See footnotes at end of table.

TABLE V. Input and output conditions for table III for device type 01 - Continued.

| Symbol | Figure 5 | Reference number 1/ | Terminals | Test conditions 2/ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | A | B | C | |
| $t_{Xh}$ | A | 1 | XIN | 16 | 16 | 16 | ns |
| $t_{Xl}$ | A | 2 | XIN | 16 | 16 | 16 | ns |
| $t_{XFr}$ | A | 3 | XIN/FCLK | 29 | 29 | 29 | ns |
| $t_{XFf}$ | A | 4 | XIN/FCLK | 29 | 29 | 29 | ns |
| $t_{XCr}$ | A | 5 | XIN/CTTL | 34 | 34 | 34 | ns |
| $t_{XPr}$ | A | 8 | XIN/PHI1 | 32 | 32 | 32 | ns |
| $t_{FCr}$ | A | 6 | FCLK/CTTL | 6 | 6 | 6 | ns |
| $t_{FCf}$ | A | 7 | FCLK/CTTL | 4 | 4 | 4 | ns |
| $t_{FPr}$ | B | 16 | PHI1/FCLK | 4 | 4 | 4 | ns |
| $t_{FPf}$ | B | 17 | FCLK/PHI1 | 2 | 2 | 2 | ns |
| $t_{PCf}$ | B | 18 | PHI2/CTTL | 4 | 4 | 4 | ns |
| $t_{PCr}$ | B | 19 | PHI1/CTTL | 5 | 5 | 5 | ns |
| $t_{CTR}$ | B | 21 | CTTL | 5 | 5 | 5 | ns |
| $t_{CTF}$ | B | 22 | CTTL | 5 | 5 | 5 | ns |
| $t_{RSTr}$ | F | 31 | PHI1/$\overline{RSTO}$ | 21 | 21 | 21 | ns |
| $t_{RSTs}$ | F | 30 | PHI1/$\overline{RSTI}$ | 20 | 20 | 20 | ns |

See footnotes at end of table.

TABLE V. Input and output conditions for table III for device type 01 - Continued.

| Symbol | Figure 5 | Reference number 1/ | Terminals | Test conditions 2/ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | A | B | C | |
| $t_{ADs}$ | F | 32 | PHI1/$\overline{ADS}$ | 30 | 30 | 30 | ns |
| $t_{ADw}$ | F | 33 | $\overline{ADS}$ | 25 | 25 | 25 | ns |
| $t_{DDs}$ | F | 34 | PHI1/$\overline{DDIN}$ (T2) | 15 | 15 | 15 | ns |
| $t_{Tf}$ | C & E | 23 | PHI1/$\overline{TSO}$ | 12 | 12 | 12 | ns |
| $t_{Tr}$ | C & E | 24 | PHI1/$\overline{TSO}$ | 18 | 18 | 18 | ns |
| $t_{RWf(F)}$ | E | 25 | PHI1/($\overline{RD}$/$\overline{WR}$) | 35 | 35 | 35 | ns |
| $t_{RWf(S)}$ | C | 35 | PHI1/($\overline{RD}$/$\overline{WR}$) | 25 | 25 | 25 | ns |
| $t_{RWr}$ | C & E | 26 | PHI1/($\overline{WR}$/$\overline{RD}$) | 25 | 25 | 25 | ns |
| $t_{DBf(W)}$ | C & E | 27 | PHI1/$\overline{DBE}$ | 28 | 28 | 28 | ns |
| $t_{DBf(R)}$ | C & E | 28 | PHI2/$\overline{DBE}$ | 21 | 21 | 21 | ns |
| $t_{DBr}$ | C & E | 29 | PHI2/$\overline{DBE}$ | 23 | 23 | 23 | ns |
| $t_{PLZ}$ | D | 36 | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | 30 | 30 | 30 | ns |
| $t_{PHZ}$ | D | 39 | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | 30 | 30 | 30 | ns |
| $t_{PZL}$ | D | 37 | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | 25 | 25 | 25 | ns |
| $t_{PZH}$ | D | 38 | ($\overline{RWEN}$/SYNC)/($\overline{WR}$ & $\overline{RD}$) | 25 | 25 | 25 | ns |
| $t_{CWs(H)}$ | G | 41 | $\overline{CWAIT}$/PHI1 | 30 | 30 | 30 | ns |
| $t_{CTV}$ | B | 20 | CTTL | 43 | 43 | 43 | ns |

See footnotes at end of table.

TABLE V. Input and output conditions for table III for device type 01 - Continued.

| Symbol | Figure 5 | Reference number 1/ | Terminals | Test conditions 2/ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | A | B | C | |
| $t_{CWh(H)}$ | G | 42 | PHI1/$\overline{CWAIT}$ | 0 | 0 | 0 | ns |
| $t_{CWs(W)}$ | G & H | 40 | $\overline{CWAIT}$/PHI2 | 10 | 10 | 10 | ns |
| $t_{CWh(W)}$ | H | 44 | PHI2/$\overline{CWAIT}$ | 20 | 20 | 20 | ns |
| $t_{Ws}$ | H | 45 | $\overline{WAITn}$/PHI2 | 7 | 7 | 7 | ns |
| $t_{Wh}$ | H | 46 | PHI2/$\overline{WAITn}$ | 20 | 20 | 20 | ns |
| $t_{Ps}$ | I | 49 | $\overline{PER}$/PHI1 | 7 | 7 | 7 | ns |
| $t_{Ph}$ | I | 48 | PHI1/$\overline{PER}$ | 30 | 30 | 30 | ns |
| $t_{Rd}$ | H & I | 47 | PHI2/RDY | 25 | 25 | 25 | ns |
| $t_{SYs}$ | J | 50 | ($\overline{RWEN}$/SYNC)/FCLK | 6 | 6 | 6 | ns |
| $t_{SYh}$ | J | 51 | FCLK/($\overline{RWEN}$/SYNC) | 0 | 0 | 0 | ns |
| $t_{CS}$ | J | 52 | CTTL/($\overline{RWEN}$/SYNC) | 10 | 10 | 10 | ns |

1/ The reference numbers refer to the position where the parameter being measured appears on figure 5.

2/ Test conditions:

A - - - $V_{CC}$ = 5.25 V, f = 10 MHz

B - - - $V_{CC}$ = 4.75 V, f = 10 MHz

C - - - $V_{CC}$ = 5.25 V, f = 10 MHz
$V_{IH}$ = 5.75 V, and $V_{IL}$ = -0.5 V

Device type 01

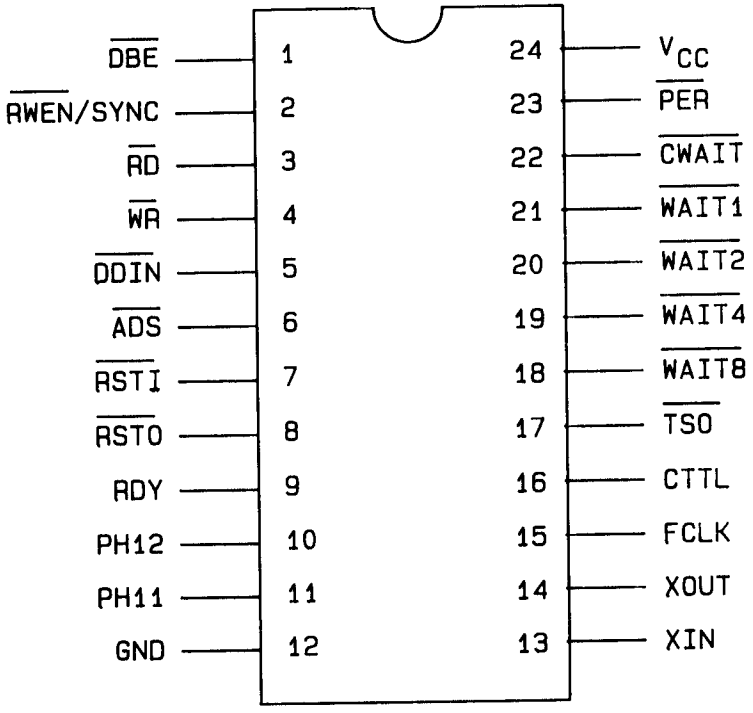



FIGURE 1. Terminal connections.

**Device type 01**

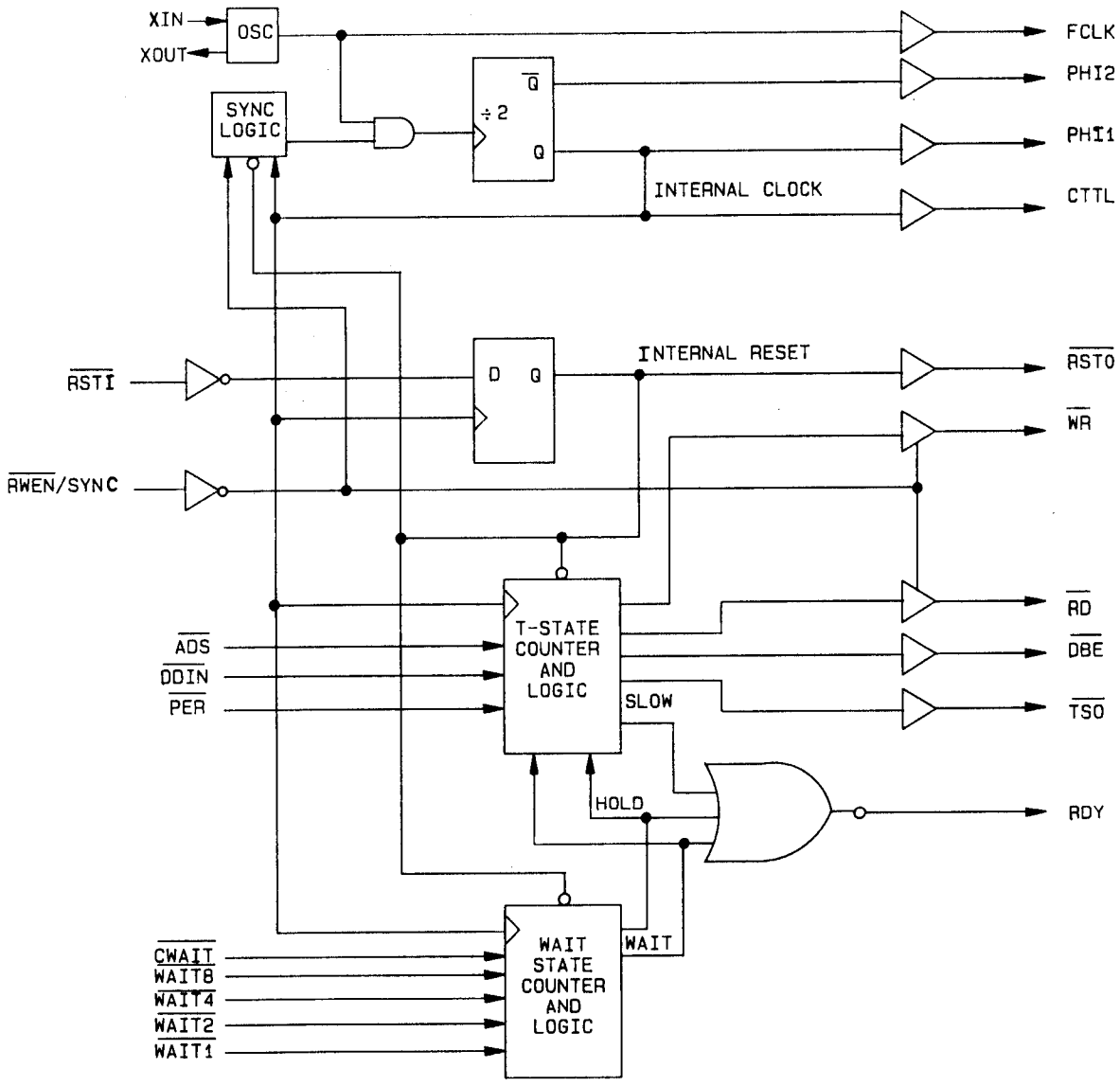
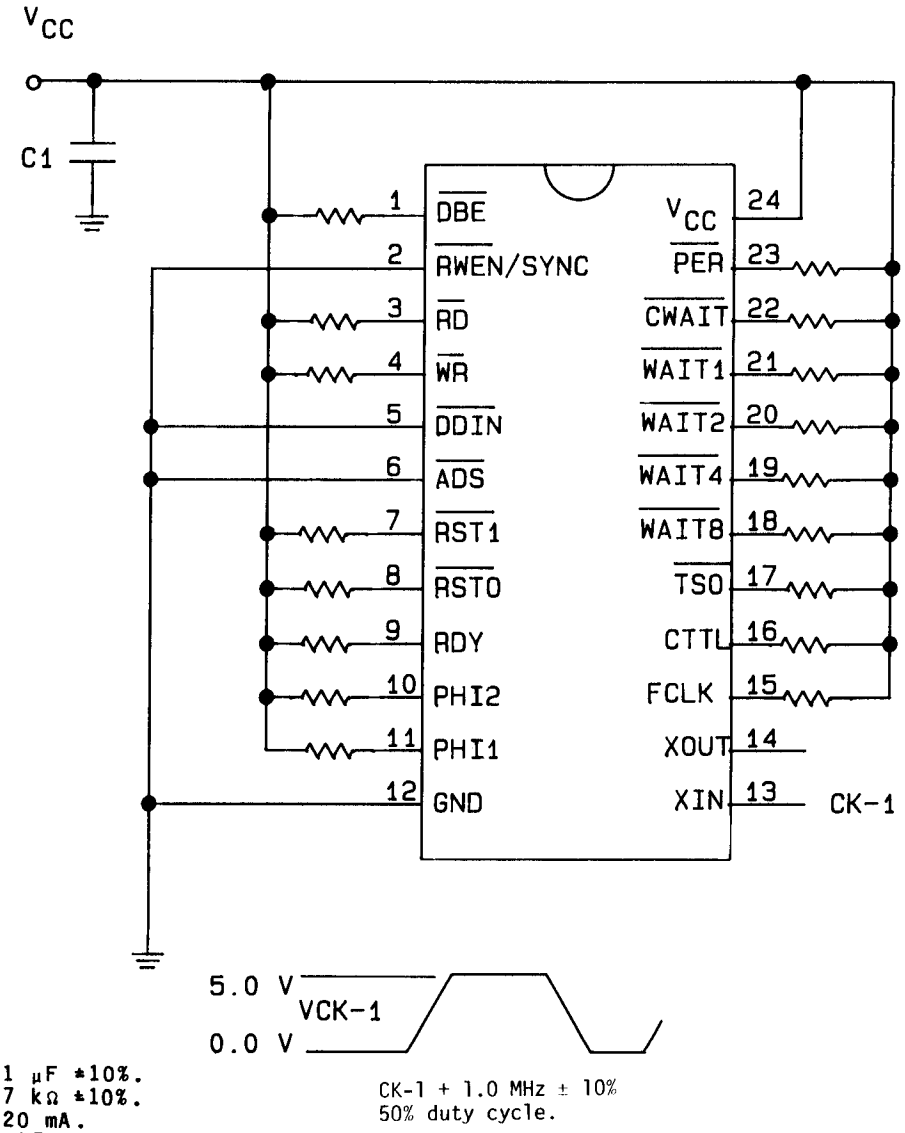
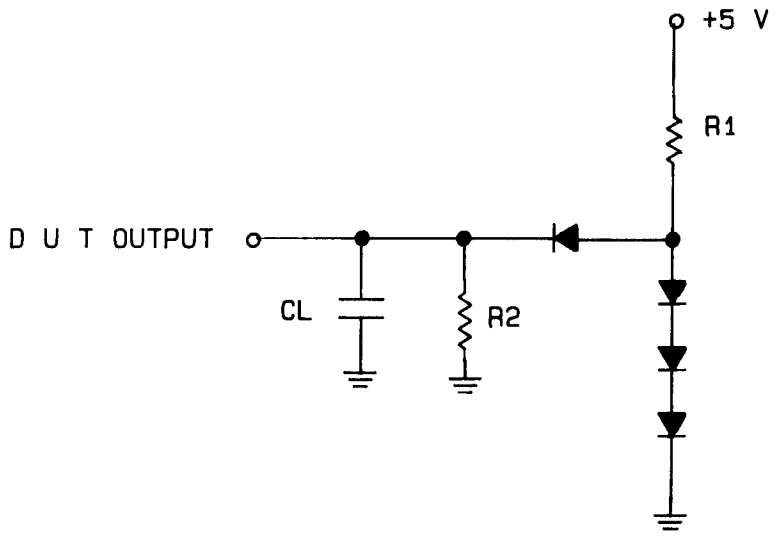



FIGURE 2. Functional block diagram.




Notes:
1. C1 = 0.1 µF ±10%.
2. R1 = 2.7 kΩ ±10%.
3. $I_{CC}$ = 120 mA.
4. $V_{CC}$ = 5.25 V.
5. Power/Socket = 0.65 W.
6. $V_{CK-1} \leq V_{CC}$.
7. Both $V_{CC}$ and $V_{CK}$-1 are sequenced. ($V_{CC}$ should be turned on before $V_{CK}$-1 and to be turned off in reversed order.)

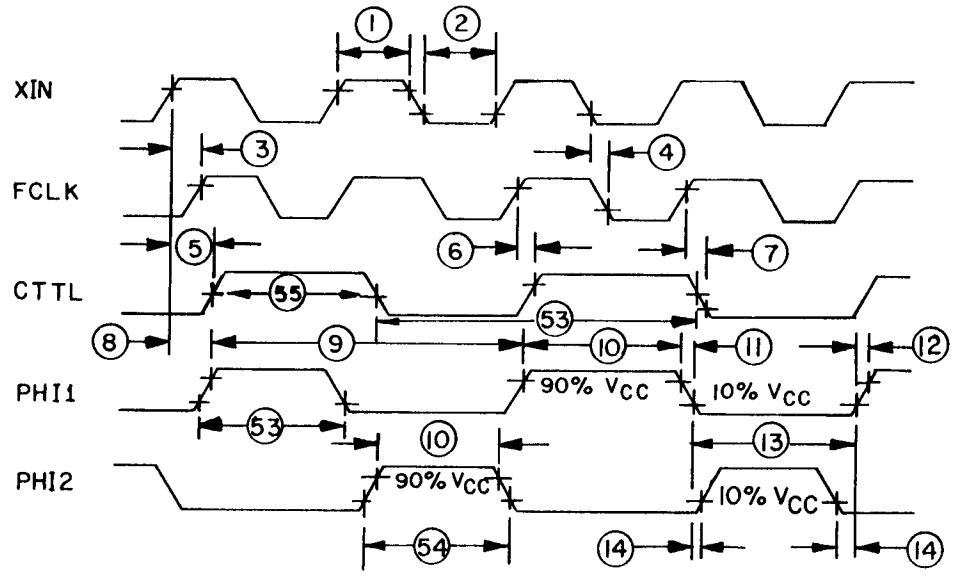
FIGURE 3. Dynamic burn-in and life test circuit.



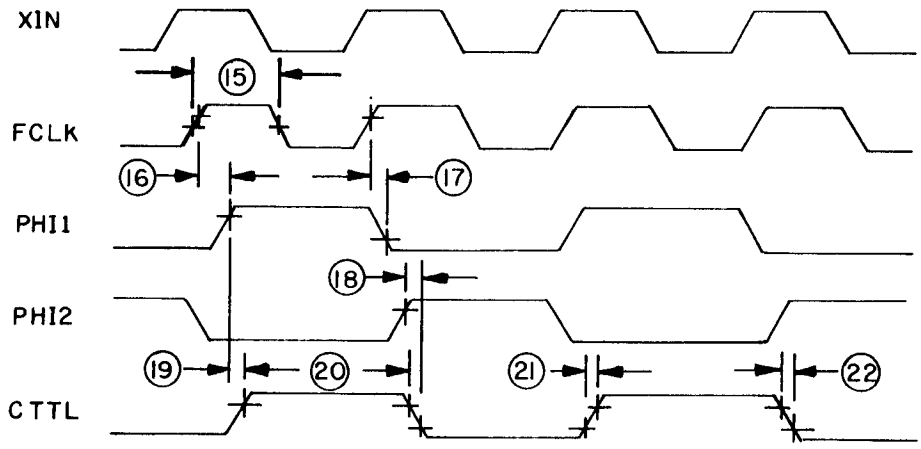

R1 = 1.90 kΩ
R2 = 4.5 kΩ
CL = 50 pF on RDY, $\overline{DBE}$, $\overline{TSO}$, CTTL
CL = 75 pF on $\overline{WR}$, $\overline{RD}$
CL = 100 pF on FCLK
CL = 170 pF on PHI1, PHI2
CL = includes all stray capacitance

NOTE: Equivalent circuit may be used.

FIGURE 4. Output load circuit for ac, functional, and three-state tests.

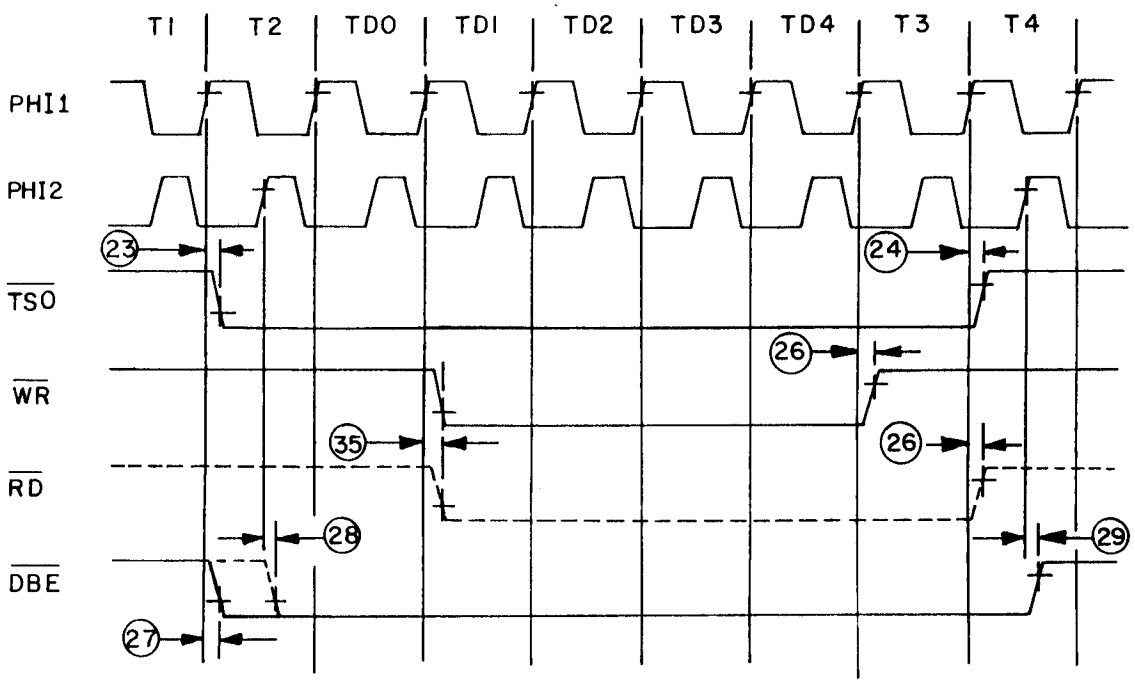



(A) Clock signals

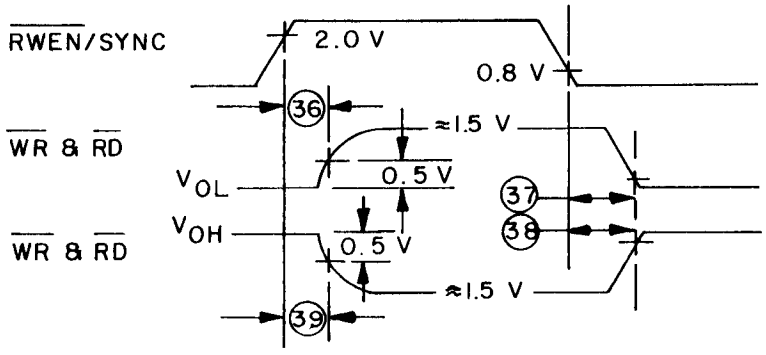



(B) Clock signals

FIGURE 5. Timing diagrams.

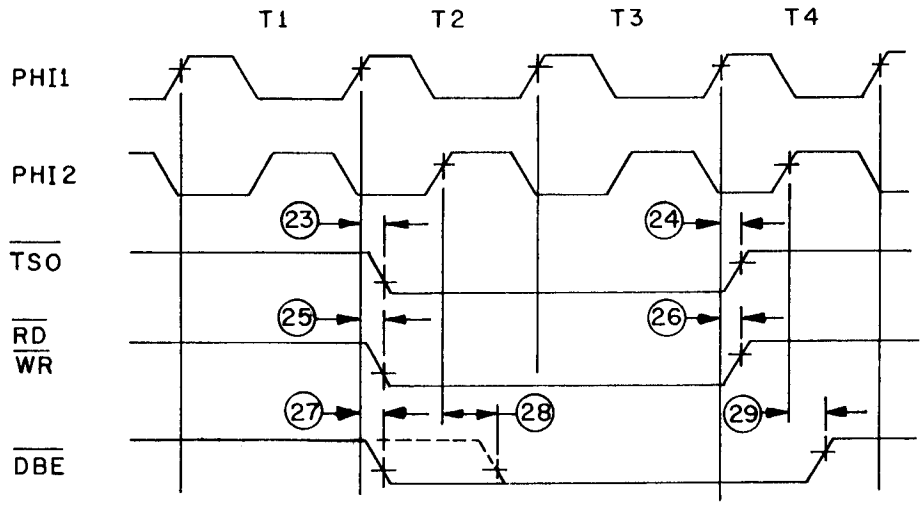



(C) Control outputs (peripheral cycle)

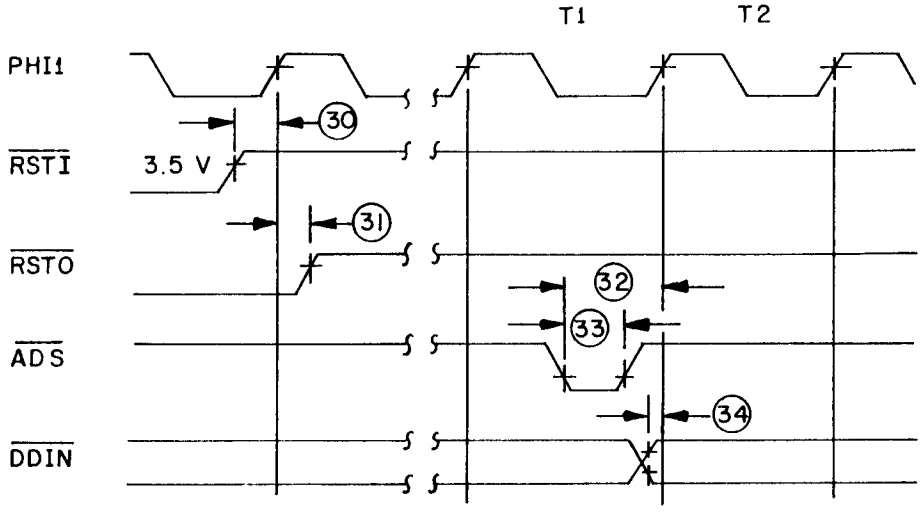



(D) Control outputs (three-state timing)

FIGURE 5. Timing diagrams - Continued.

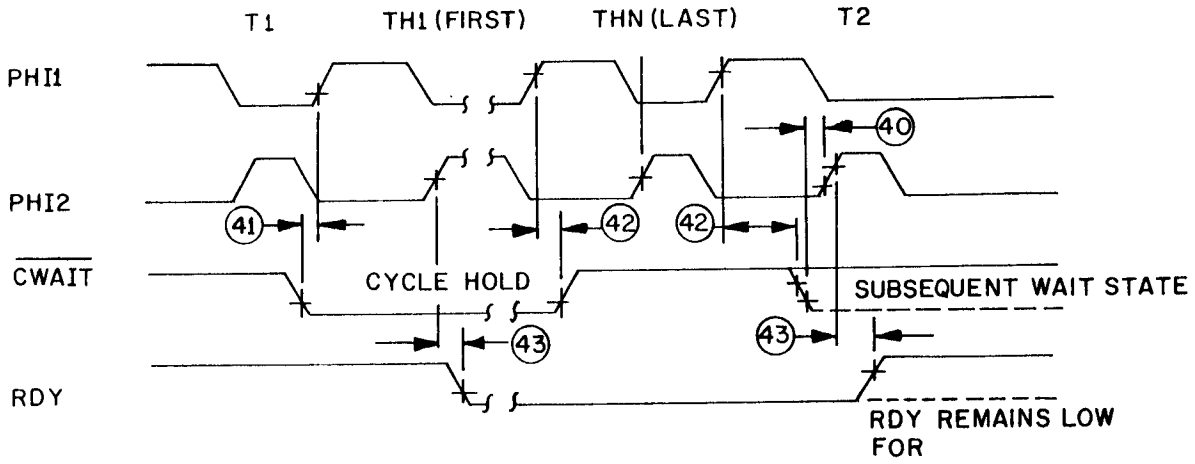



(E) Control inputs (fast cycle)

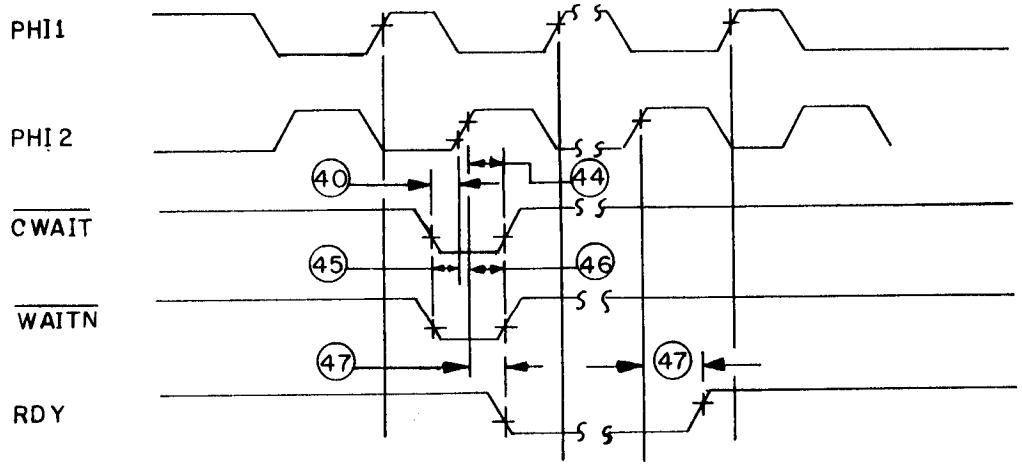



(F) Control inputs

FIGURE 5. Timing diagrams - Continued.

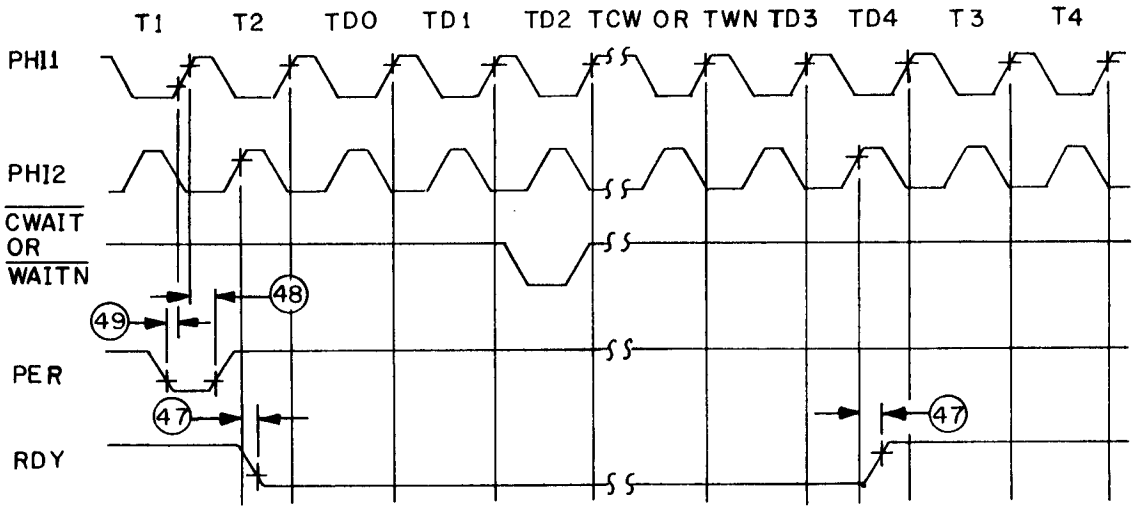



(G) Cycle hold



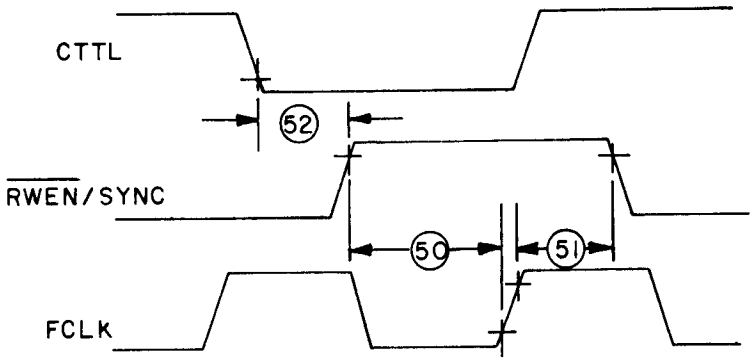

(H) Wait state (fast cycle)

FIGURE 5. Timing diagrams - Continued.



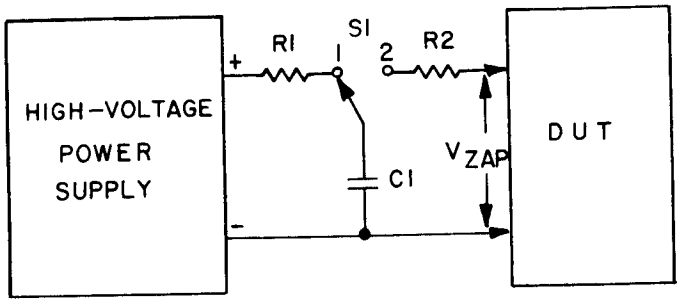

(I) Wait state (peripheral cycle)

FIGURE 5. Timing diagrams - Continued.




(J) Synchronization timing

FIGURE 5. Timing diagrams - Continued.




NOTES:

1. R1 = 3 Gohm maximum to 800 kΩ minimum.
2. R2 = 1.5 kΩ ±10%.
3. C1 = 100 pF ±10%.
4. S1 = Hg-wetted 'bounceless' relay break before make type.
5. All pins of DUT no associated with $V_{ZAP}$ test shall be open (NC).
6. Devices shall be tested to MIL-STD-885, method 3015 requirements (see 4.6.2).

FIGURE 6. High voltage ($V_{ZAP}$) test circuit.

TABLE VI. Test vectors.

| |
|---|
| Table VI, not printed herein, is a computer listing for use with table III. Each vector identifies activity states by pin number. See 6.3 for information on obtaining the complete table in a compatible output format. When the vectors are performed as specified in table III for subgroups 7, 8, 9, 10, and 11 they verify the dynamic, functional, threshold, and switching parameters at +25°C, -55°C, and +125°C. |

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). In addition, the qualification outlined below shall be performed through the use of the identified qualification vehicle.

| Qualification phase | Qualification vehicle |
|---|---|
| Control and stability | Process monitor die (PM) |

4.3.1 Process control and stability. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's process monitor (PM). The PM (either a drop-in or fabricated in the Kerf) is to be designed so that the dc process parameters (ac parameters may be included as a manufacturer's option) may be measured in wafer form or packaged device form. The PM design must be submitted to the qualifying activity for approval prior to use for qualification and must contain as a minimum the following structures:

N channel device (minimum geometry)
P channel device (minimum geometry)
Sheet resistance measurement structure
Metal step coverage structure
Field threshold device
Intermetal oxide integrity structure
Contact chains (to be of sufficient length to be representative of the contact resistance typically found on a device, with diagnostic taps to isolate failures).
  Metal to poly
  Metal to diffusion

For qualification, PM's on a minimum of three different lots (minimum of four PM's per wafer) shall be measured to ensure the establishment of a statistically valid data base upon which a decision can be made as to whether the manufacturer's process is stable and under control.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and quality/accept number values shown in table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be performed in accordance with table II herein.

b. Subgroup 4($C_O$, $C_I$ and $C_{CLK}$) capacitance measurements shall be performed only for initial qualification and after process or design changes which may affect device capacitance.

c. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

d. Dynamic and functional testing shall be performed using circuit configuration shown on figure 4, utilizing the waveforms on figure 5.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table IIB of method 5005 of MIL-STD-883, and as follows: A special subgroup 9 shall be added to the group B inspection requirements for class B. This subgroup shall consist of the test, conditions, and limits specified in 4.6.2.

4.4.3 Groups C and D inspection. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV of method 5005 of MIL-STD-883 and as follows.

a. End-point electrical tests shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883).

1. Test condition D using the circuit shown on figure 3.

2. $T_A$ = +125°C minimum.

3. Test duration, 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.4.4 Group E inspection. Group E inspection is required only for device types intended to be marked as radiation hardened (see 3.6.1). When group E testing is performed, it shall be in accordance with table V of method 5005 of MIL-STD-883.

4.5 Inspection of packaging. Inspection of packaging shall be as specified in MIL-M-38510.

4.6 Methods of inspection. Methods of inspection shall be as follows.

4.6.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and are positive when flowing into the referenced terminal.

4.6.2 High voltage ($V_{ZAP}$) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 400 V from a 100 pF source in the following test sequence:

a. $V_{ZAP}$ test circuit is shown on figure 6.

b. Measure $I_{IH}$ and $I_{IL}$ at one input terminal of the device under test at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of $I_{IH}$ and $I_{IL}$ shall be as specified in table III.

c. Apply the test voltage ($V_{ZAP}$ = 400 V) to the same terminal selected for leakage current measurements. Apply $V_{ZAP}$ in a 2-pulse sequence as follows and in accordance with the test circuit shown on figure 6.

(1) Input (-) to GND.

(2) Input (+) to GND.

d. Within 24 hours repeat the $I_{IH}$ and $I_{IL}$ measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of specified limits is defective.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. In addition, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage (see 6.6).

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory).

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition document must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. Complete Part or Identifying Number (see 6.7).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirements for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to qualifying activity, if applicable.

g. Requirement for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

h. Requirements for product assurance options.

i. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.

k. Requirements for "JAN" marking.

6.3 Test vector table. Table VI (test vectors) which forms a part of this specification is not printed herein because of its extreme length and complexity. When the test vectors are presented in hardcopy form, it requires conversion to online format. When the entire sequence of vector groups are needed for an inspection, a test program output should be obtained in a form compatible with test system architecture. The preparing activity, or Defense Electronics Supply Center as its agent, may be consulted for obtaining such output information. For reference purposes, Rome Air Development Center (RADC-RBRM) and Defense Electronics Supply Center (DESC-ECS) each maintain a limited quantity of dated, hardcopy printouts of this table.

6.4 Functional description, terms and symbols. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

6.4.1 Functional description. The timing control unit (TCU) is a 24-pin device using a CMOS technology. It provides a two-phase clock, system control logic, and cycle extension for compatible 32-bit microprocessors. The TCU input clock can be provided by either a crystal or an external clock signal whose frequency is twice the system clock frequency.

The two-phase clock (PHI1 and PHI2) are used mainly for the central processing unit (CPU) and memory management unit (MMU); also, the TCU produces two system clocks (FCLK and CTTL) for general use within the system. FCLK is a fast clock whose frequency is the same as the input clock (20 MHz), while CTTL is a replica of PHI1. The system control logic ($\overline{RSTO}$, $\overline{WR}$, $\overline{RD}$, $\overline{DBE}$, $\overline{TSO}$, and RDY) provides accurate bus control signals and very controllable bus cycle timing.

6.4.2 Terms and definitions.

| | |
|---|---|
| $\overline{RSTI}$ (Reset, input) | Active low. Schmit triggered asynchronous signal used to generate system reset. |
| $\overline{ADS}$ (Address strobe) | Active low. Identifies the first timing state (T1) of a bus cycle. |
| $\overline{DDIN}$ (Data direction) | Active low. Indicates the direction of the data transfer during a bus cycle. Implies a read when low and a write when high. |
| $\overline{RWEN}$/SYNC (Read/Write enable and synchronization) | 3-state the $\overline{RD}$ and $\overline{WR}$ outputs when high and enables them when low. Also used to synchronize the phase of the TCU clock signals, when two or more TCU's are used. |
| XIN (Crystal or external clock source) | Input from a crystal or an external clock source. |

| | |
|---|---|
| $\overline{CWAIT}$ (Continuous wait) | Active low. Initiates a continuous wait if sampled when low in the middle of T2. If $\overline{CWAIT}$ is low at the end of T1, it initiates a cycle hold. |
| $\overline{WAIT1}$, $\overline{WAIT2}$, $\overline{WAIT4}$, $\overline{WAIT8}$ (4-bit wait state) | Active low. These inputs (collectively called $\overline{WAITn}$) allow from zero to 15 wait states to be specified. They are binary weighted. |
| $\overline{PER}$ (Peripheral cycle) | Active low. If active, causes the TCU to insert five wait cycles into a normal bus cycle. It also causes the read and write signals to be reshaped to meet the setup and hold timing requirements of slower MOS peripherals. |
| $\overline{RSTO}$ (Reset output) | Active low. This signals becomes active when $\overline{RSTI}$ is low, initiates a system reset. $\overline{RSTO}$ goes high on the first rising edge of PHI1 after $\overline{RSTI}$ goes high. |
| $\overline{RD}$ (Read strobe) | 3-state active low. Identifies a read cycle. It is decoded from $\overline{DDIN}$ and 3-state by $\overline{RWEN}$/SYNC. |
| $\overline{WR}$ (Write strobe) | 3-state active low. Identifies a write cycle. It is decoded from $\overline{DDIN}$ and TRI-STATE by $\overline{RWEN}$/SYNC. |
| $\overline{DBE}$ (Data bus enable) | Active low. This signal is used to control data bus buffers. It is low when the data buffers are to be enabled. |
| $\overline{TSO}$ (Timing state output) | Active low. The falling edge of $\overline{TSO}$ signals the beginning of T2 of a bus cycle. The rising edge of $\overline{TSO}$ signals the beginning of T4. |
| RDY (Ready) | Active high. This signal will go low and remain low as long as wait states are to be inserted in a bus cycle. |
| FCLK (Fast clock) | This is a clock running at the same frequency as the crystal or external source. Its frequency is twice that of the CPU clocks. |
| PHI1 and PHI2 (CPU clocks) | These outputs provide the CPU with two-phase, non-overlapping clock signals. Their frequency is half that of the crystal or the external source. |
| CTTL (TTL system clock) | This is a system version of the PHI1 clock. Hence it operates at the CPU clock frequency. |
| XOUT (Crystal output) | This line is used as a return path for the crystal (if used). It must be open when an external clock source is used to drive XIN. |

6.5 Logistic support. Lead material and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for government logistic support will be acquired to device class B for the Department of Defense (see 1.2.2), and lead finish "C" (see 3.3). Longer length leads and lead forming shall not affect the PIN.

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. These CMOS devices are fabricated with silicon gate technology including input protection, which reduces the susceptibility to damage; however, the following practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Devices should be stored in conductive foam or carriers.

e. Avoid uses of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50%, if practical.

6.7 Part or Identifying Number (PIN). The PIN shall be in accordance with MIL-M-38510.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry part. Generic-industry microcircuit types may not have equivalent operational performance characteristics, due to military temperature ranges, reliability factors equivalent to MIL-M-38510 device type, or slight differences in case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

| Military device type | Generic-industry type |
|---|---|
| 01 | 32C201-10 |

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - Ar, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1136)