INCH-POUND

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MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS, REMOTE TERMINAL INTERFACE MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS remote terminal interface (RTI). One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit organization
01	Remote terminal interface (clock duty cycle logical high 10 percent to 35 percent)
02	Remote terminal interface (clock duty cycle logical high 40 percent to 60 percent)

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Case outline	Case outline (see MIL-M-38510, appendix C)
X	C-8 (84-terminal, 1.15" x 1.15"), square chip carrier package.
Z	P-BC (84-pin, 1.135" square x .345"), pin grid array package.

1.3 Absolute maximum ratings. (Referenced to V_{SS}.)

Supply voltage range	-0.3 V to +7.0 V
Input or output voltage range	-0.3 V to (V_{DD} +0.3 V)
Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
Maximum junction temperature (T_J) 1/	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	20°C/W
Maximum power dissipation (P_D)	300 mW

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5962

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1.4 Recommended operating conditions.

Operating supply voltage (V_{DD})	4.5 V minimum to 5.5 V maximum
Minimum high level input voltage:	
Logic inputs (V_{IH})	2.0 V
Clock inputs	2.0 V
Maximum low level input voltage:	
Logic inputs (V_{IL})	0.8 V
Clock inputs	0.8 V
Frequency of operation	12 MHz ±0.01 percent
Operating case temperature (T_C)	-55°C to +125°C
Duty cycle:	
Device type 01	10 percent to 35 percent
Device type 02	40 percent to 60 percent

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1553 - Digital Time Division Command and Response Multiplex Data BUS.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be as specified in 1.2.3 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Input protection circuit. The input protection circuit shall be as specified on figure 3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and shall apply over the operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table III. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, by device class, as specified in table II.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Device type	Group A subgroup	Limits Min	Limits Max	Unit
Input leakage for inputs without pull-up resistors	I_{ILW}	V_{IN} = GND	All	1,2,3	-10		µA 2/
Input leakage for inputs without pull-down resistors	I_{IHW}	V_{IN} = 5.5 V	All	1,2,3		10	µA 2/
Input leakge current for inputs with pull-up resistors	I_{ILP}	V_{SS} = GND; V_{IN} = GND(PU)	All	1,2,3	-2.75	-0.11	mA 2/
Input leakage current for inputs with pull-down resistors	I_{IHP}	V_{SS} = GND; V_{IN} = $V_{DD(PD)}$	All	1,2,3	0.11	2.75	mA 2/
Output leakage current (three-state)	$I_{LOZ(H)}$	$V_{ADDROUT}$ = 5.5 V; V_{ADOEN} = V_{OH}	All	1,2,3	-10	10	µA
Output leakage current (three-state)	$I_{LOZ(L)}$	$V_{ADDROUT}$ = 0.0 V; V_{ADOEN} = V_{OH}	All	1,2,3	-10	10	µA
Output leakage current (bi-direct)	$I_{LB(H)}$	V_{DT} = 5.5 V; V_{MRST} = V_{OL}	All	1,2,3	-10	10	µA
Output leakage current (bi-direct)	$I_{LB(L)}$	V_{DT} = 0.0 V; V_{MRST} = V_{OL}	All	1,2,3	-10	10	µA
Low level output voltage	V_{OL}	I_{OL} = 4.0 mA	All	1,2,3		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^\circ C \leq T_C \leq +125^\circ C$ unless otherwise specified	Device type	Group A subgroup	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -0.4 mA	All	1,2,3	2.4		V
Low level input voltage 3/	V_{IL}		All	1,2,3		0.8	V
High level input voltage 3/	V_{IH}		All	1,2,3	2.0		V
Input clamp voltage (positive) 3/	V_{IC^+}	V_{DD} = GND; I_{IN} = 1 mA $T_C = +25^\circ C$	All	1	0.4	1.8	V
Input clamp voltage (negative) 3/	V_{IC^-}	V_{DD} = OPEN; I_{IN} = -1 mA $T_C = +25^\circ C$	All	1	-0.4	-1.8	V
Input capacitance 4/	C_I	V_I = 0.0 V; F = 1 MHz; $T_C = +25^\circ C$		4		10	pF 5/
Output capacitance 4/	C_O	V_O = 0.0 V; F = 1 MHz; $T_C = +25^\circ C$		4		20	pF 5/
Bidirect capacitance 4/	C_B	V_O = 0.0 V; F = 1 MHz; $T_C = +25^\circ C$		4		25	pF 5/
Quiescent current 6/	I_{DD}			1,2,3		50	mA
$\overline{CS}$(L) to $\overline{RCS}$(L)	t_{PHL1}	See figure 6	All	9,10,11		48	ns
$\overline{CS}$(H) to $\overline{RCS}$(H)	t_{PLH2}		All	9,10,11		40	ns
RD/$\overline{WR}$(L) to RRD/$\overline{RWR}$(L)	t_{PHL3}		All	9,10,11		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 7/	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroup	Limits Min	Limits Max	Unit
RD/$\overline{WR}$(H) to RRD/$\overline{RWR}$(H)	t_{PLH4}	See figure 6	All	9,10,11		35	ns
$\overline{CS}$(L) to ADDR OUT(H)	t_{PLH5}		All	9,10,11	6	52	ns
$\overline{CS}$(L) to ADDR OUT(L) 8/	t_{PHL5}		All		6	52	ns
ADDR IN(L) to ADDR OUT(L)	t_{PHL6}		All	9,10,11		44	ns
ADDR IN(H) to ADDR OUT(H)	t_{PLH6}		All	9,10,11		44	ns
$\overline{ADOEN}$(H) to ADDR OUT(H) to Hi-Z 9/	t_{PLZ7}		All			42	ns
$\overline{ADOEN}$(H) to ADDR OUT(L) to Hi-Z 9/	t_{PHZ7}		All			42	ns
$\overline{ADOEN}$(L) to ADDR OUT(H) 8/	t_{PLH8}		All		6	50	ns
$\overline{ADOEN}$(L) to ADDR OUT(L)	t_{PHL8}		All	9,10,11	6	50	ns
$\overline{CS}$(L) to $\overline{MEMCK}$(L)($\overline{MEMCK}$ not recognized) 9/ 10/	t_{SHL9}		All		13		ns
$\overline{CS}$(H) to $\overline{MEMCK}$(L)($\overline{MEMCK}$ recognized) 9/ 11/	t_{HHL10}		All		10		ns
DMARQ(H) to $\overline{MEMCK}$(L) 9/	t_{SHL12}	See figure 7	All		0		ns
$\overline{MEMCK}$(L) to $\overline{RCS}$(L)	t_{PHL13}		All	9,10,11		67	ns
$\overline{MEMCK}$(H) to $\overline{RCS}$(H)	t_{PLH14}		All	9,10,11		61	ns
$\overline{MEMCK}$(L) to RRD/$\overline{RWR}$(L)	t_{PHL15}		All	9,10,11		61	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 7/	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Group A subgroup	Limits Min	Limits Max	Unit
$\overline{MEMCK}$(H) to RRD/$\overline{RWR}$(H)	t_{PLH16}	See figure 7	All	9,10,11		58	ns
$\overline{MEMCK}$ pulse width during receive 12/ 13/	t_{PW17}		All	7,8	83		ns
$\overline{MEMCK}$(L) to DATA bus(H) during receive	t_{PZH18}		All	9,10,11		115	ns
$\overline{MEMCK}$(L) to DATA bus(L) during receive	t_{PZL18}		All	9,10,11		115	ns
$\overline{RCS}$, RRD/$\overline{RWR}$(H) to DATA bus(L) to high Z 9/	t_{PLZ19}		All		5	101	ns
$\overline{RCS}$, RRD/$\overline{RWR}$(H) to DATA bus(H) to high Z 9/	t_{PHZ19}		All		5	101	ns
DMARQ(H) to $\overline{MEMCK}$(L) 9/ (setup)	t_{SHL21}	See figure 8	All	7,8	0	14.9	µs
$\overline{MEMCK}$(L) to $\overline{RCS}$(L)	t_{PHL22}		All	9,10,11		67	ns
$\overline{MEMCK}$(H) to $\overline{RCS}$(H)	t_{PLH23}		All	9,10,11		61	ns
$\overline{MEMCK}$ pulse width during transmit	t_{PWL24}		All	7,8	50		ns
Input DATA valid before $\overline{MEMCK}$(H) (setup)	t_{SLH25}		All	7,8	45		ns
Input DATA valid after $\overline{RCS}$(H) (hold)	t_{HLH26}		All		5		ns
DMARQ(H) to $\overline{MEMCK}$(H) response, xmit	t_{OILH27}		All	7,8		18.3	µs
Input DATA valid (setup) before control write(H)	t_{SLH28} 14/	See figure 9	All	7,8	20		ns
Input DATA valid (hold) after control write(H)	t_{HLH29} 14/		All	7,8	25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 7/	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Group A subgroup	Limits Min	Limits Max	Unit
ADDR IN 0 = 0 (setup time before control write (L) so software reset is not recognized	t_{SHL30} 14/	See figure 9	All	7,8	20		ns
ADDR IN 0 = 0 (hold time after control write (H) so software reset is not recognized	t_{HLH31} 14/		All	7,8	20		ns
($\overline{CTRL}$ + $\overline{CS}$) (L) to DATA bus (H) while ADDR IN 0 = 1 or 0	t_{PZH32}	See figure 10	All	9,10,11		132	ns
($\overline{CTRL}$ + $\overline{CS}$) (L) to DATA bus (L) while ADDR IN 0 = 1 or 0	t_{PZL32}		All	9,10,11		132	ns
ADDR IN 0 (valid) to DATA bus (H) while ($\overline{CTRL}$ + $\overline{CS}$) = 0	t_{PLH33}		All	9,10,11		70	ns
ADDR IN 0 (valid) to DATA bus (L) while ($\overline{CTRL}$ + $\overline{CS}$) = 0	t_{PHL33}		All	9,10,11		70	ns
($\overline{CTRL}$ + $\overline{CS}$)(H) to DATA(L) Bus Hi-Z 9/	t_{PLZ34}		All			101	ns
($\overline{CTRL}$ + $\overline{CS}$)(H) to DATA(H) Bus Hi-Z 9/	t_{PHZ34}		All			101	ns
Status (H) before $\overline{TIMERON}$ (L) 9/	t_{OOHL35}	See figure 11	All		4	31	ns
$\overline{TIMERON}$ (L) before first output biphase transition 9/	t_{OOLH36}		All		1.2		µs
$\overline{TIMERON}$ low pulse width (during time out) 9/	t_{PWL37}		All			730	µs 15/
$\overline{COMSTR}$ (L) to $\overline{TIMERON}$ (H) (reset) 9/	t_{OOLH38}					31	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Output levels are tested in static (dc) state and are specified over the voltage range of V_{DD}. V_{DD} = 5.0 V ±10 percent, unless otherwise specified.

2/ Refer to figure 1 for identification of inputs with pull-up or pull-down resistors.

3/ These tests are performed as go-no-go tests.

4/ See 4.4.1c.

5/ Capacitance is measured between the designated terminal and V_{SS} at frequency of 1 MHz and a signal amplitude of 50 mV rms maximum.

6/ Measured at the test vector determined to be worse case. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge.

7/ The symbols used herein are defined by the following:

t_{PXXY} = propagation delay
t_{PWXY} = pulse width
t_{OOXXY} = output to output relationship
t_{OIXXY} = output to input relationship in accordance with MIL-STD-1553
t_{SXXY} = setup condition
t_{HXXY} = hold condition

8/ t_{PHL5} and t_{PLH8} are not tested but guaranteed. t_{PLH5} and t_{PHL8} are tested and are the worse case transitions.

9/ Supplied as a design limit but not guaranteed or tested.

10/ t_{SHL9} is interpreted as follows: In order for $\overline{MEMCK}$ to be ignored during a DMARQ cycle, $\overline{CS}$ must be asserted no later than 13 ns before $\overline{MEMCK}$ falls.

11/ t_{HHL10} is interpreted as follows: In order for $\overline{MEMCK}$ to be recognized after a $\overline{CS}$ cycle, 10 ns must pass after $\overline{CS}$ is negated before $\overline{MEMCK}$ can fall.

12/ Allows a 20 ns data valid set before $\overline{RCS}$ and RRD/$\overline{RWR}$ go high.

13/ The sum of t_{SHL12} and t_{PW17} must not exceed 18.8 µs.

14/ Logical OR result of ($\overline{CTRL}$ + $\overline{CS}$ + RD/$\overline{WR}$).

15/ F = 12.00 MHz and T_C = +25°C.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.2.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically (i.e., same die, process, and package) to other device types on this specification, the other device types may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table I)
	Class B devices
Interim electrical test parameters (method 5004)	2, 8 1/
Final electrical test parameters (method 5004)	1,2/ 2, 3, 7,2/ 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4,3/ 7, 8, 9, 10, 11
Group B test requirements (method 5005)	1 4/
Group C end-point electrical parameters (method 5005)	1, 2, 7, 8 1/
Group D end-point electrical parameters (method 5005)	1, 2, 7, 8 1/

1/ Maximum temperature only.
2/ PDA applies to subgroups 1 and 7 (see 4.3b).
3/ See 4.4.1c.
4/ Subgroup 1 applies only to electrostatic discharge sensitivity test.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following modifications and additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, using burn-in circuit shown on figure 4.

(2) T_A = +125°C minimum.

b. The percent defective allowable (PDA) for class B devices shall be in accordance with MIL-M-38510. Electrical tests shall be in accordance with table II herein.

c. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

d. The constant acceleration test in accordance with method 5004 shall be performed using test condition D.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I, method 5005 of MIL-STD-883 and as follows:

a. Electrical tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for initial qualification and after process or design changes which may affect input/output capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. One pin of each input and output buffer (driver) type shall be tested on each device. The pin selected for a given buffer type shall be rotated for each subsequent device tested.

d. Instruction mnemonics for the functional tests of subgroups 7 and 8 and switching tests of subgroups 9, 10, and 11 shall be as specified in table III.

e. Test vectors for subgroups 7 through 11 shall be as defined in table III.

f. The output/load circuit for subgroups 7 through 11 shall be as shown on figure 5.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. The ESDS testing in MIL-STD-883, method 3015, required by group B tests for class B and S devices, is modified as follows:

(1) For use in this specification, method 3015, table I pin combination number (4) shall be "input (B) to V + (A)" and combination number (5) shall be "output (B) to V + (A)".

(2) The reverse polarity procedure shall be applicable to all pin combinations.

(3) Only those devices that pass the ESDS test in accordance with MIL-STD-883, method 3015, at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.

(4) ESD tests shall be performed on a special subgroup for qualification and after input or output buffer design changes. During testing, each pin combination shall be required on only one pin of each input and output driver (buffer) type.

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II.

b. Steady-state life test (method 1005 of MIL-STD-883, test condition A) conditions:

(1) Use the burn-in board configuration shown on figure 4.

(2) T_A = +125°C minimum.

c. Test duration, 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.4.5 Constant acceleration. The constant acceleration tests of groups C and D shall be performed using test condition D.

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                                 |-------------------------|
BIPHASE IN  A - Z  ----->|  39(G9)          (A1)74  |<--->  0    (LSB)
                0  ----->|  37(H10)         (B3)73  |<--->  1
                                 |                         |
BIPHASE OUT A - Z  <-----|  28(K8)          (A2)72  |<--->  2
                0  <-----|  27(L8)          (A3)71  |<--->  3
                                 |                         |
BIPHASE IN  B - Z  ----->|  34(J10)         (B4)70  |<--->  4
                0  ----->|  33(K10)         (A4)69  |<--->  5
                                 |                         |
BIPHASE OUT B - Z  <-----|  30(L10)         (C5)68  |<--->  6
                0  <-----|  32(L11)         (B5)67  |<--->  7 ---DATA I/O
                                 |                  (A5)66  |<--->  8
                                 |                  (A6)65  |<--->  9
                                 |                  (C7)63  |<---> 10
          STATUS  <-----|  23(J7)          (B6)61  |<---> 11
          BRDCST  <-----|  36(J11)         (A8)59  |<---> 12
             RCV  <-----|  51(B11)         (A9)57  |<---> 13
            XMIT  <-----|  38(H11)        (A10)55  |<---> 14
          CH A/B  <-----|  26(L6)         (A11)53  |<---> 15
        MES ERR   <-----|  49(D10)                 |
                                 |                  (K3)13  |<----  0    (LSB)
         (LSB)  0  <-----|  14(L2)          (K1) 9  |<----  1
                1  <-----|  16(K4)          (H2) 7  |<----  2
       MC/SA--- 2  <-----|  17(L4)          (G3) 5  |<----  3
                3  <-----|  18(J5)          (G1) 3  |<----  4
                4  <-----|  19(K5)          (F3) 1  |<----  5 ---ADDR IN
           MC/SA  <-----|  21(K6)          (E1)83  |<----  6
         ILL COMM  ----->|  20(L5)*         (F2)81  |<----  7
                                 |                  (D2)79  |<----  8
         EXT TEST  ----->|  29(L9)*         (B1)77  |<----  9
EXT TST CH SEL A/B ----->|  31(K9)**        (B2)75  |<---- 10
                                 |                         |
         (LSB)  0  ----->|  64(C6)**        (L1)11  |---->  0    (LSB)
                1  ----->|  62(A7)**        (J2)10  |---->  1
          TA--- 2  ----->|  60(B7)**        (J1) 8  |---->  2
                3  ----->|  58(B8)**        (H1) 6  |---->  3
                4  ----->|  56(B9)**        (G2) 4  |---->  4
     TALEN/PARITY  ----->|  52(C10)**       (F1) 2  |---->  5 ---ADDR OUT
                                 |                  (E3)84  |---->  6
          12 MHz  ----->|  35(K11)         (E2)82  |---->  7
                                 |                  (D1)80  |---->  8
            MRST  ----->|  40(G10)**       (C1)78  |---->  9
                                 |                  (C2)76  |----> 10
           2 MHz  <-----|  24(L7)                  |
                                 |                  (L3)15  |<---  ADDOEN
          COMSTR  <---- |  22(J6)          (E9)44  |<---- CS
                                 |                 (E10)46  |<---- RD/WR
            BCEN  ----->|  25(K7)**       (C11)50  |<---- CTRL
                                 |                 (D11)48  |<---- MEMCK
            VDD  ------|  54(B10)        (F11)47  |----> DMARQ
                                 |                  (F9)43  |----> RCS
        VSS(GND)  -----|  12(K2)         (E11)45  |----> RRD/RWR
        VSS(GND)  -----|  42(F10)                 |
                                 |                  (G11)41  |----> TIMERON
                                 |-------------------------|
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NOTES:
1. Pin internally pulled-down.
2. Pin internally pulled-up.
3. () Pin grid array lead identification listed in parentheses.

FIGURE 1. UT 1553B RTI functional pin description.

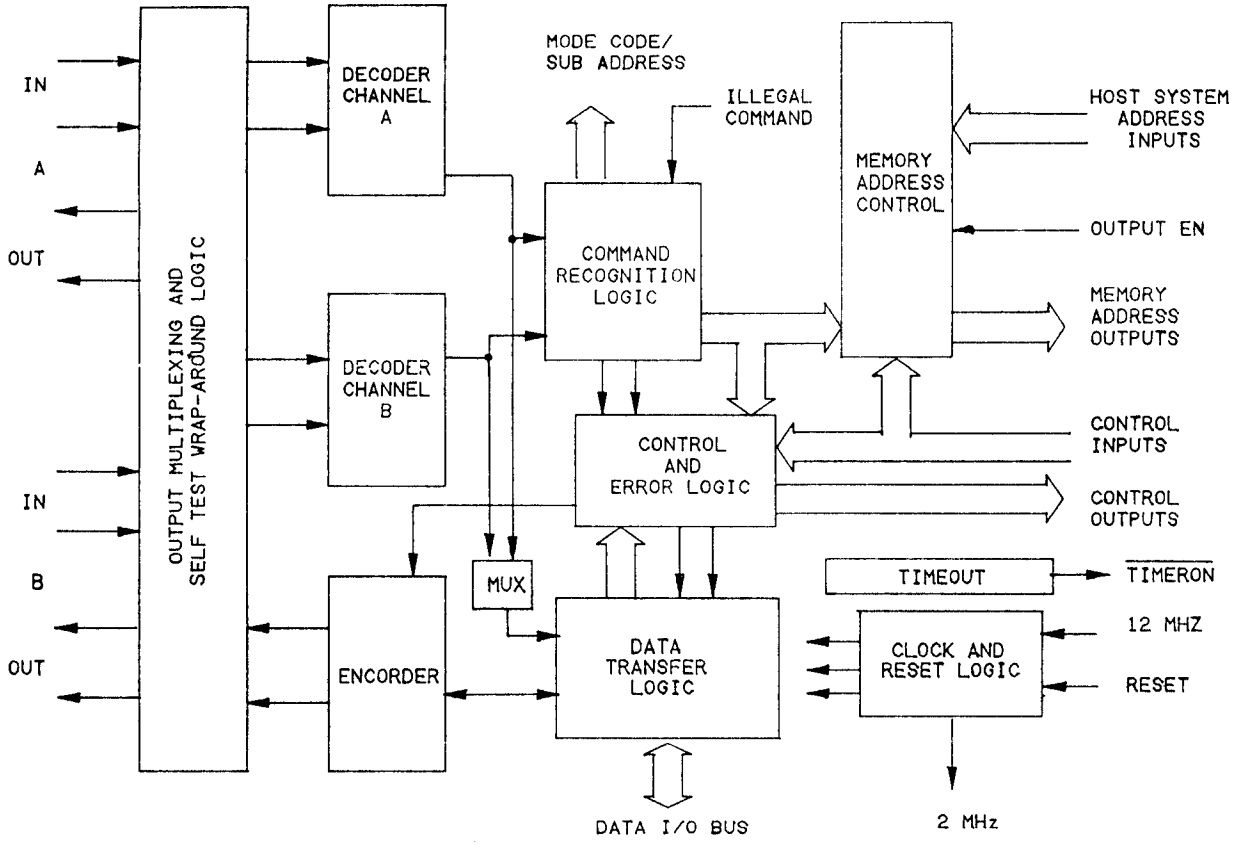
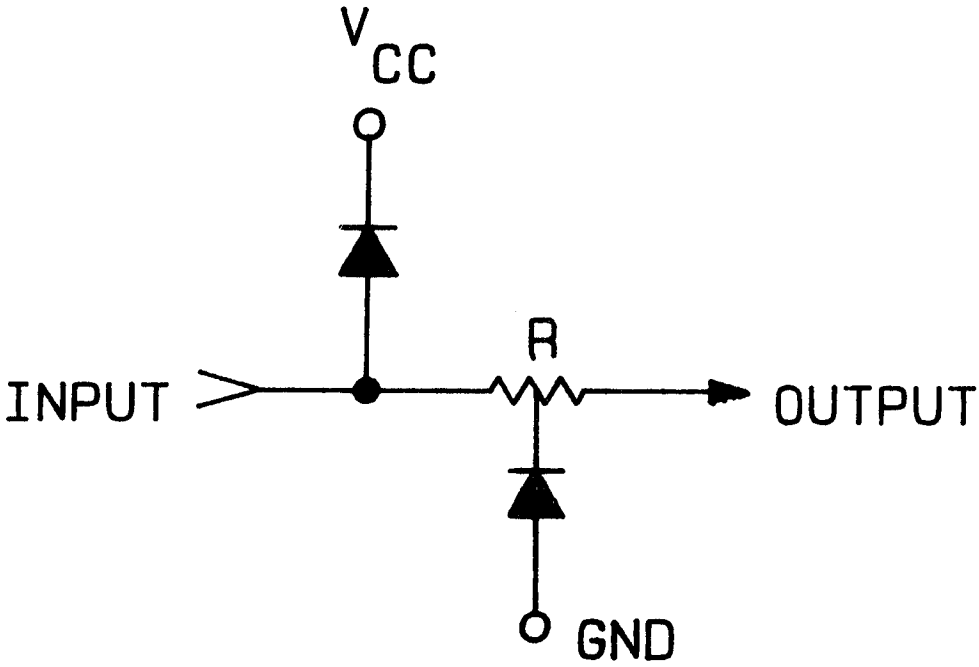
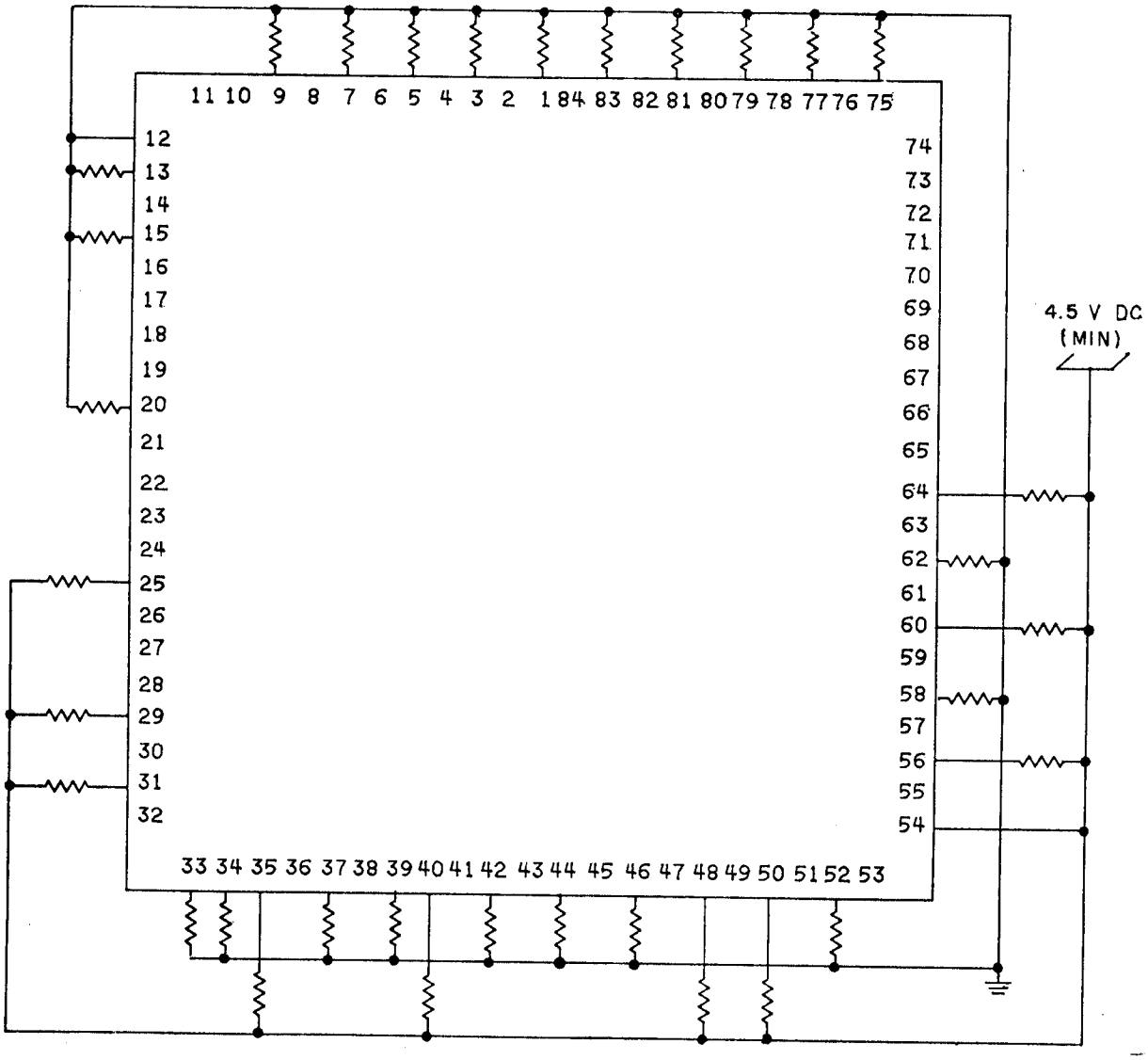


FIGURE 2. Function block diagram.



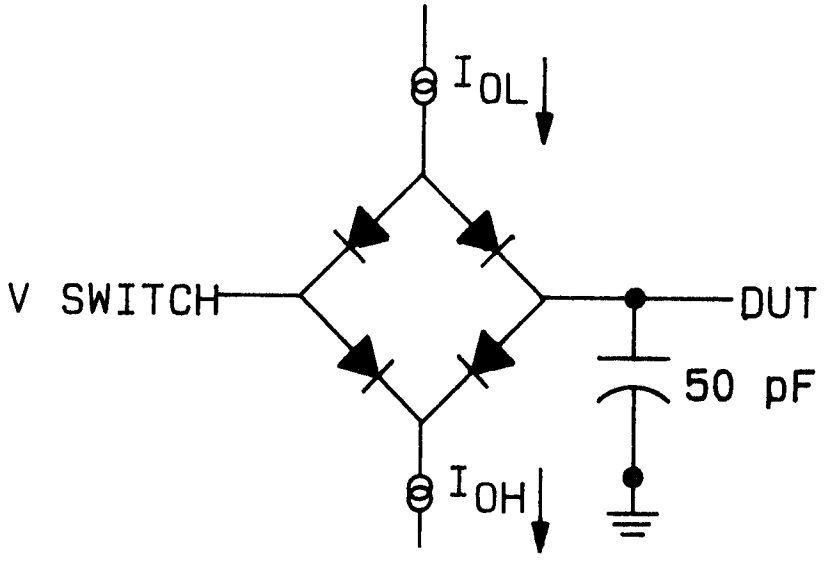
NOTES:
1. All device inputs shall be protected from transients such as electrostatic discharge by the diode resistor circuit shown. This circuit is intrinsic to the device.
2. R = 40Ω typical.

FIGURE 3. Input protection circuit.



NOTES:
1. All resistor values are 2.5 k ±10 percent.
2. See figure 1 for PGA lead identification.

FIGURE 4. Burn-in and steady-state life test circuit.



$$V\ SWITCH = (V_{OL}\ MAX + V_{OH}\ MIN)/2$$

FIGURE 5. Output test circuit for ac and functional tests.

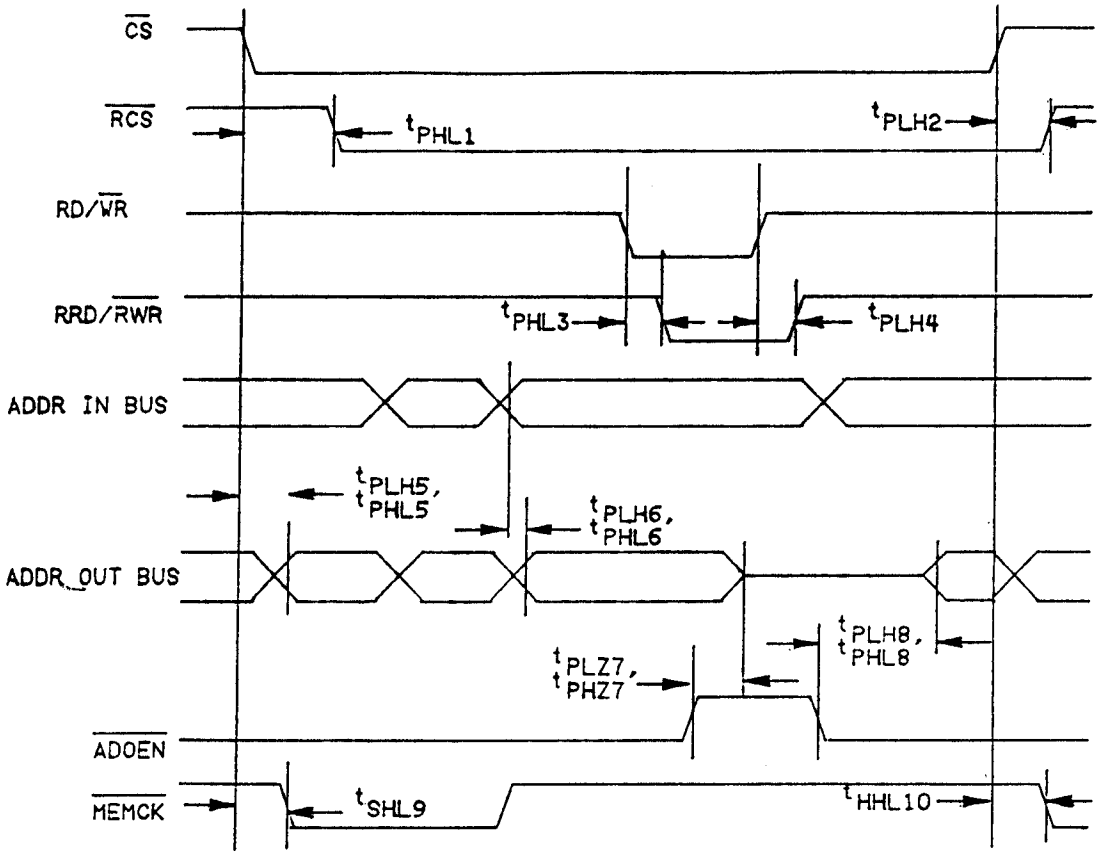


FIGURE 6. Processor-to-RAM propagation delay limits.

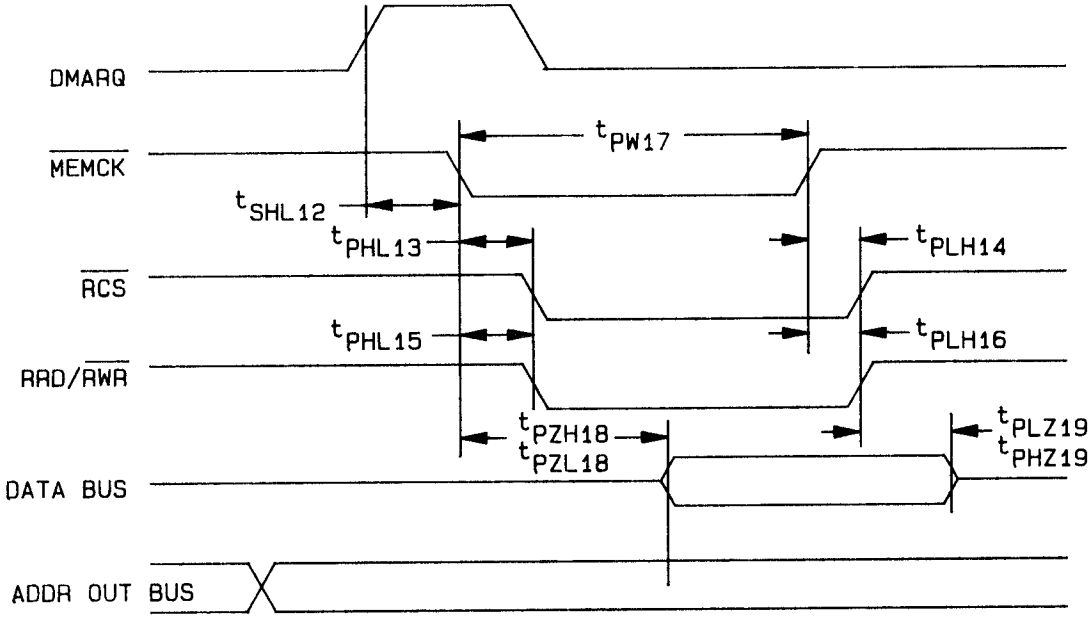


FIGURE 7. Timing limits for received data storage.

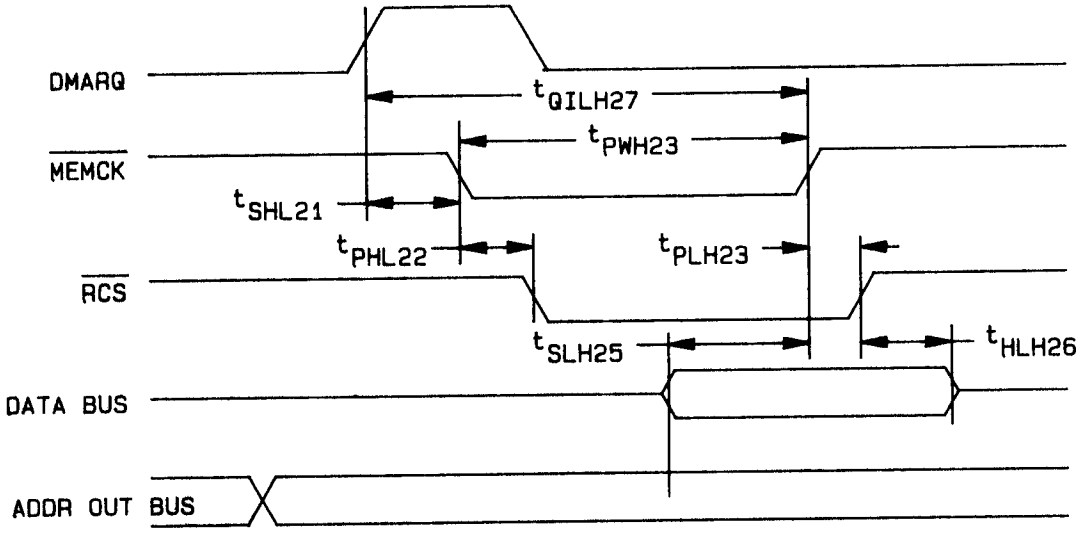
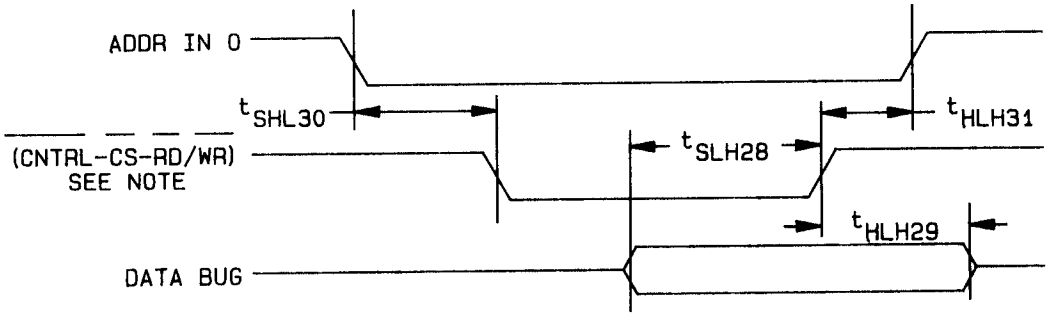
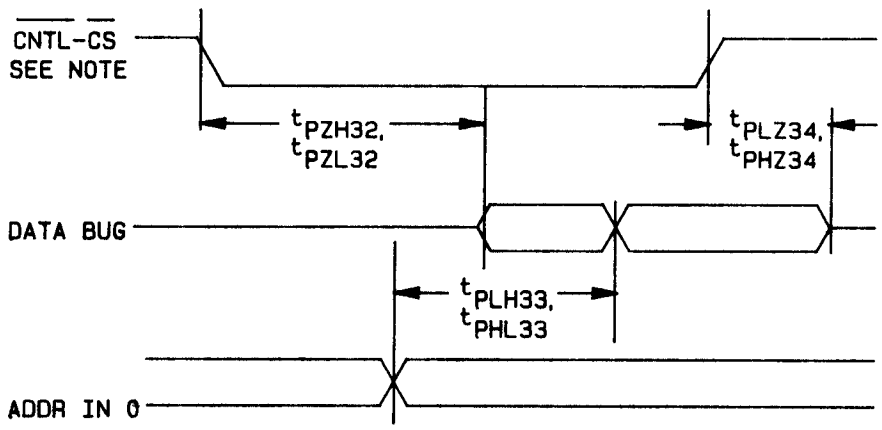


FIGURE 8. Timing limits for transmit data retrieval.



SEE NOTE: CONTROL WRITE=LOGICAL "OR" RESULT

FIGURE 9. Control register write timing limits.



NOTE: LOGICAL "OR" RESULT

FIGURE 10. System register/last command register read timing limits.

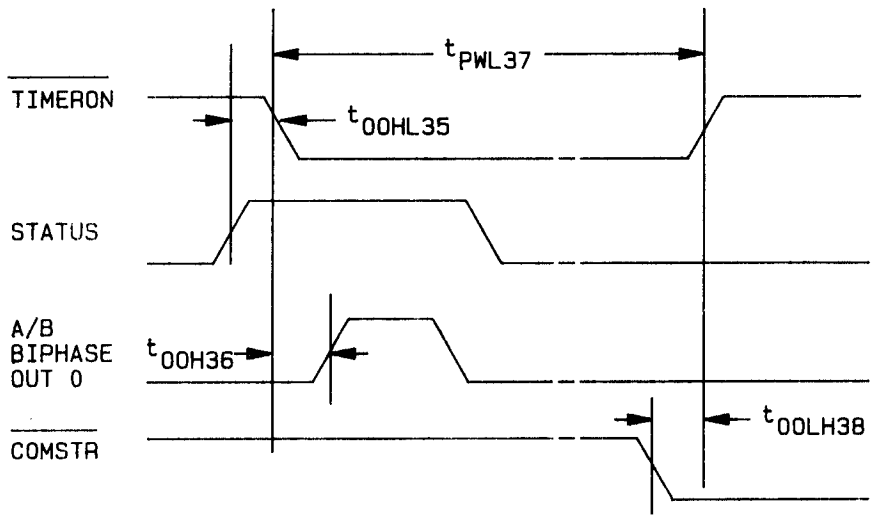


FIGURE 11. RT fail-safe timer signal relationships.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Quiescent supply current I_{DD} test. When performing quiescent supply current measurements, I_{DD}, the meter shall be placed so that all currents flow through the meter.

TABLE III

Table III which forms a part of this specification, is not printed herein because of its extreme length; and, even when presented as hard copy, it requires conversion to on-line format. When the sequence or conditions of tests and test vectors are needed as part of inspection, it may be obtained in a form compatible with test system architecture (magnetic tape format usually preferred). The preparing activity (or Defense Electronics Supply Center, as its agent) may be consulted for information on obtaining table III. Group A subgroup assignment is shown on table I.

Functional tests are performed under the following conditions for group A subgroups 7 and 8.

Symbol	Parameter	Unit
V_{DD}	4.5 and 5.5	Volts
V_{SS}	0	Volts
V_{IH}	V_{OH} minimum**	Volts
V_{IL}	V_{OL} maximum**	Volts
V_{OH}	$\geq$(V_{OH} minimum + V_{OL} maximum)/2	Volts
V_{OL}	$\leq$(V_{OH} minimum + V_{OL} maximum)/2	Volts
F	12	MHz

** Values of V_{OH} and V_{OL} may be obtained from table I.

Switching tests are performed with $V_{IH} = V_{DD}$ and $V_{IL} = 0$ V as input test conditions.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. PIN (see 1.2).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirements for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

h. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

i. Requirements for product assurance options.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

6.3.1 Pinout description.

DATA I/O 0-15	16-bit bidirectional data port for all data transfer between the RTI and host system.
ADDR IN 0-10	11-bit host system address input if it is in transparent memory mode. Not used in DMA configuration.
ADDR OUT 0-10	11-bit three-state address output. Contains processor or RTI-generated address ($\overline{CS}$ selects processor address).
$\overline{ADOEN}$	Address out enable. Causes ADDR OUT lines to be active when low, high impedance when high.
$\overline{CS}$	Processor chip select. Active low input for host system access of transparent memory or the RTI registers.

RD/$\overline{WR}$	Processor read/write. High input in conjunction with $\overline{CS}$ for host system read of transparent memory, system register or last command read function. Low input in conjunction with $\overline{CS}$ for host system write to transparent memory or control register.
$\overline{CTRL}$	Control select. Active low in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ for host system access to the RTI registers. This signal is also used to latch terminal address input lines (if $\overline{TALEN}$/PARITY = 1) and to generate programmable reset.
$\overline{MEMCK}$	Memory clock (DMA acknowledge). Active low synchronizing input used to generate reads or writes to memory.
DMARQ	Direct memory access request. Active high output requests RTI access of memory.
$\overline{RCS}$	Ram chip select. Active low output enables memory access.
RRD/$\overline{RWR}$	RAM read/write. High output enables memory read, low output enables memory write (in conjunction with $\overline{RCS}$). Quiescent state = high.
$\overline{TIMERON}$	Active low pulse of 730 microseconds maximum duration started by the rising edge of STATUS which is used with external logic to provide a less than 800 microseconds fail-safe timer. This pulse is reset when $\overline{COMSTR}$ goes low or during a master reset. During external self-test, the timer will not recognize the $\overline{COMSTR}$ signal and will be allowed to timeout in order to test the external fail-safe hardware.
V_{DD}, GND	Power supply inputs.
$\overline{BCEN}$	Broadcast enable. Active low input enables broadcast commands.
$\overline{COMSTR}$	Command strobe. An active low output of 500 nanoseconds duration identifying receipt of a valid command and that all the RTI indicators ($\overline{MC}$/SA, MCSA 0-4, $\overline{XMIT}$, $\overline{RCV}$, $\overline{BRDCST}$) are valid.
2 MHZ	2 megahertz free running clock output.
$\overline{MRST}$	Master reset. Active low signal that initializes all internal nodes, must be followed by host system write to control register to enable the communication channels.
12 MHZ	12 megahertz clock input.
$\overline{TALEN}$/PARITY	Terminal address latch enable/parity. The function of the $\overline{TALEN}$/PARITY signal is dependent upon the state of the external test (EXTST, pin 29) and external test channel select (EXT TST CH SEL A/$\overline{B}$, pin 31) signals. In all cases, if $\overline{TALEN}$/PARITY is low, the terminal address will be strobed onto the TA lines (TA0-TA4); otherwise, the terminal address can only be loaded via a control register write.

EXT TEST	EXT TST CH SEL A/$\overline{B}$	Function of $\overline{TALEN}$/PARITY.
0	0	External terminal address latch control only. Terminal address parity is not checked.
0	1	Odd parity bit for the terminal address and external terminal address latch control. Terminal address parity is checked.
1	0	External terminal address latch control only. Terminal address parity is not checked.
1	1	External terminal address latch control only. Terminal address parity is checked.

TA0-TA4 — 5-bit terminal address input. These lines are strobed into the internal terminal address latch during a control register load ($\overline{TALEN}$/PARITY = 1) or when $\overline{TALEN}$/PARITY is low.

EXT TST CH SEL A/$\overline{B}$ — External test channel select. See table for $\overline{TALEN}$/PARITY.

EXT TST — External test. Used for off-board device testing. Test function should not be used in system (Remote Terminal) implementations. See table for $\overline{TALEN}$/PARITY function. Can also be used to test external fail-safe hardware (see TIMERON description).

ILL COMM — Illegal command. Input to identify present command as illegal. Used in conjunction with RTI indicators (see $\overline{COMSTR}$ description) to decode system dependent illegal commands.

$\overline{MC}$/SA — Mode code/subaddress. Used to determine if MCSA lines contain mode code or subaddress information. When low, the output indicates if most recent command is a mode command.

MCSA 0-4 — 5-bit mode code/subaddress output. If $\overline{MC}$/SA is low these lines contain the 5 least significant bits of the most recent command, the mode code. Otherwise, they contain the next 5 bits, the subaddress.

MES ERR — Message error. Active high output identifying that the message error bit has been set due to receipt of an illegal or invalid command, or error during message sequence.

CH A/$\overline{B}$ — Channel A/$\overline{B}$. Output identifying the channel on which the most recent valid command was received. Channel A = 1, channel B = 0.

$\overline{XMIT}$ — Active low output identifies a transmit command message transfer is in process by the RTI.

$\overline{RCV}$ — Active low output identifies a receive command message transfer is in process by the RTI.

$\overline{BRDCST}$ — Active low output identifies receipt of a broadcast command.

STATUS — Active high output indicates that the RTI is in the process of transmitting its status word.

BIPHASE IN 0 A, B
BIPHASE IN Z A, B — Manchester II encoded biphase serial data inputs for channels A and B. The biphase one inputs may be used as uniphase inputs if the associated biphase zero input is held at a logic high.

BIPHASE OUT 0 A, B
BIPHASE OUT Z A, B — Manchester II encoded biphase serial data outputs for channels A and B.

6.3.2 Terminology.

Host	The device or system that controls the operation of the Remote Terminal Interface (e.g., microprocessor).
Assert	An active high signal that is asserted means that it has been placed at a logic 1. An active low signal that is asserted is placed at logic 0.
Negate	An active high signal is negated when it is brought back to a logic 0. An active low signal is negated when brought back to a logic 1.
Status word	The "status word" is the MIL-STD-1553B (see figure 13) response word that is transmitted by the Remote Terminal. The following bits in a status word are not supported by the RTI and are always at a logic 0: a. Dynamic bus control acceptance b. Instrumentation c. All reserved
System register	The system register is a 16-bit word obtained from RTI's data bus and reflects the current state of the RTI.
Control register	The control register is an 8-bit word that is written to the RTI via its data bus to control its operation and certain bits of the 1553 status word.
Last command register	The last command register is a 16-bit word obtained from the RTI's data bus and contains five system status bits and the last 11 bits of the last command that was processed in accordance with the protocol.

6.3.3 Interface architecture.

6.3.3.1 Decoders. The RTI contains two separate free-running decoders to insure that all redundancy requirements of MIL-STD-1553B are met. See figure 2. Each decoder receives, decodes, and verifies biphase Manchester II data. Proper frequency and edge skew are also verified.

6.3.3.2 Command recognition logic. The command recognition logic monitors the output of both decoders at all times. Recognition of a valid command causes a reset of present interface activity followed by execution of the command. This meets the requirement for superseding valid commands.

6.3.3.3 Encoder. The encoder receives serial data from the data transfer logic, converts it to Manchester II form with proper sync and parity, and passes it to the output and self-test logic.

6.3.3.4 Data transfer logic. The data transfer logic provides double buffered 16-bit parallel-to-serial and serial-to-parallel conversion during reception and transmission of data.

6.3.3.5 Memory address control. The memory address control logic controls the output of the three-state address lines during memory access. In DMA system implementions, the memory address control provides interface-generated addresses. In transparent dual-port memory implementations, the memory address control logic provides either interface-generated or host system addressing.

6.3.3.6 Control and error logic. The control and error logic performs the following four major functions:

a. Interface control for proper processing of MIL-STD-1553 commands.

b. Error checking of both MIL-STD-1553 data and RTI operation.

c. Memory control (DMA or transparent) for proper data transfer.

d. Operational status and control handshaking with host system.

6.3.3.7 Output multiplexing and self testing logic. This logic directs the output of the encoder to one of four places:

a. Channel A outputs

b. Channel B outputs

c. Channel A decoders during self-test

d. Channel B decoders during self-test

6.3.3.8 Clock and reset logic. The RTI requires a 12 MHz input clock to operate properly. It provides a 2 MHz output for the system designer's use. The device provides a hardware reset pin as well as software-generated reset.

6.3.3.9 Timer logic. The RTI has a built-in 730 microsecond timer that is activated when the encoder is about to transmit. The timer is reset upon receipt of a valid command or a master reset.

6.3.4 Initializing the RTI.

a. During power-up the master reset ($\overline{MRST}$) pin must be asserted to put the RTI in a known state. After a reset, the control register is cleared which means that both communication channels A and B are disabled. Therefore, a control register write (see 6.3.9) must be performed to at least enable the communication channels and allow the RTI to start receiving commands.

b. A software reset is also available so that the host can selectively initialize the RTI. This is accomplished by simultaneously asserting $\overline{CS}$ and $\overline{CNTRL}$, RD/$\overline{WR}$ = 0, and ADDR IN 0 = 1.

6.3.5 Receive operation.

a. The receive operation is illustrated via the following example (see figure 12). Detailed timing parameters are given in figure 7, and the appendix (figures 15, 16, and 17).

b. A receive command word and its associated data words (five in this example) are sent contiguously by the bus controller (BC) to the RTI's biphase inputs, as follows (hexadecimal notation). See figure 13.

A8C5	TA = 10101, T/R = 0, SA = 00110, WC = 00101
000A	first data word
000B	second data word
000C	third data word
000D	fourth data word
000E	fifth data word

c. After command word validation, the command strobe ($\overline{COMSTR}$) line is pulsed low and the RTI's receive output ($\overline{RCV}$) will also go low to indicate to the host that a receive operation is in effect. The subaddress will also be valid in the mode code/subaddress MCSA lines. The command word is stored internally in the last command register.

d. After validating the first incoming data word, the RTI will assert the DMA request (DMARQ) line to notify the host that it has to do a memory transfer.

e. The host responds to the DMA request by asserting the RTI's memory clock ($\overline{MEMCK}$) input. This action causes the RTI's emory access control lines RAM chip-select ($\overline{RCS}$) and RAM read/write (RRD/$\overline{RWR}$) to go low. The RTI will also put the data word in the data bus (DT bus). Memory addresses (ADDR OUT bus) are generated automatically by the RTI (see item 6.3.5j).

f. The host will then negate $\overline{MEMCK}$ after it has determined that the memory devices have read in the data word from the RTI's DT bus. This action causes the RTI's memory access control lines ($\overline{RCS}$ and RRD/$\overline{RWR}$) to go high and the DT bus to be three-stated (high impedance state).

g. The sequence above will be repeated until all data words are received by the RTI. After the last data word is processed, the status word is transmitted to the bus controller via the RTI's biphase outputs. The RTI's status (STATUS) line will also go high to indicate to the host that the status word is being transmitted.

h. The RTI is capable of processing the maximum word count (32) and all subaddresses (01 through 1E).

i. If the busy bit of the status register is set, all DMARQ assertions are suppressed although a status word will be transmitted.

j. During this receive operation, the contents of the address (ADO) and data (DT) busses will be as follows:

address	data	comments
0C4	000A	first data word
0C3	000B	second data word
0C2	000C	third data word
0C1	000D	fourth data word
0C0	000E	fifth data word

k. Notice that the adddresses generated by the RTI are derived directly from the least 11 bits of the command word. The addresses will always count down to zero. For example, if 32 words were received, the first address will be 0DF (00011011111).

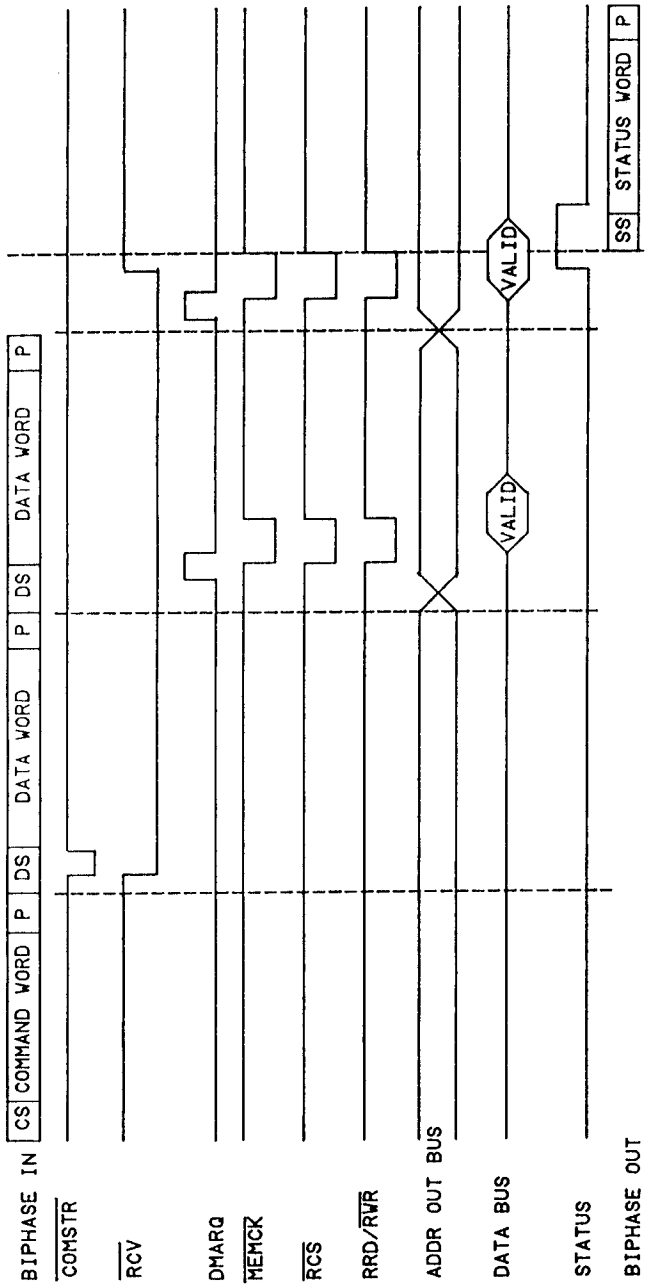
l. With an 11-bit address field, the RTI is capable of accessing 2048 memory locations. Since the T/R bit of command word is the most significant bit of this address field, the 2K memory space is divided into transmit and receive blocks of 1K each. Therefore, for data "wrap-around" applications (transmitting data that was previously received), ADDR OUT 10 must be tied high or low.

6.3.6 Transmit operation. The transmit operation is shown on figure 14 and is similar to the receive operation discussed above except for the following:

a. In accordance with the protocol, the status word will be transmitted first by the RTI before the data word(s).

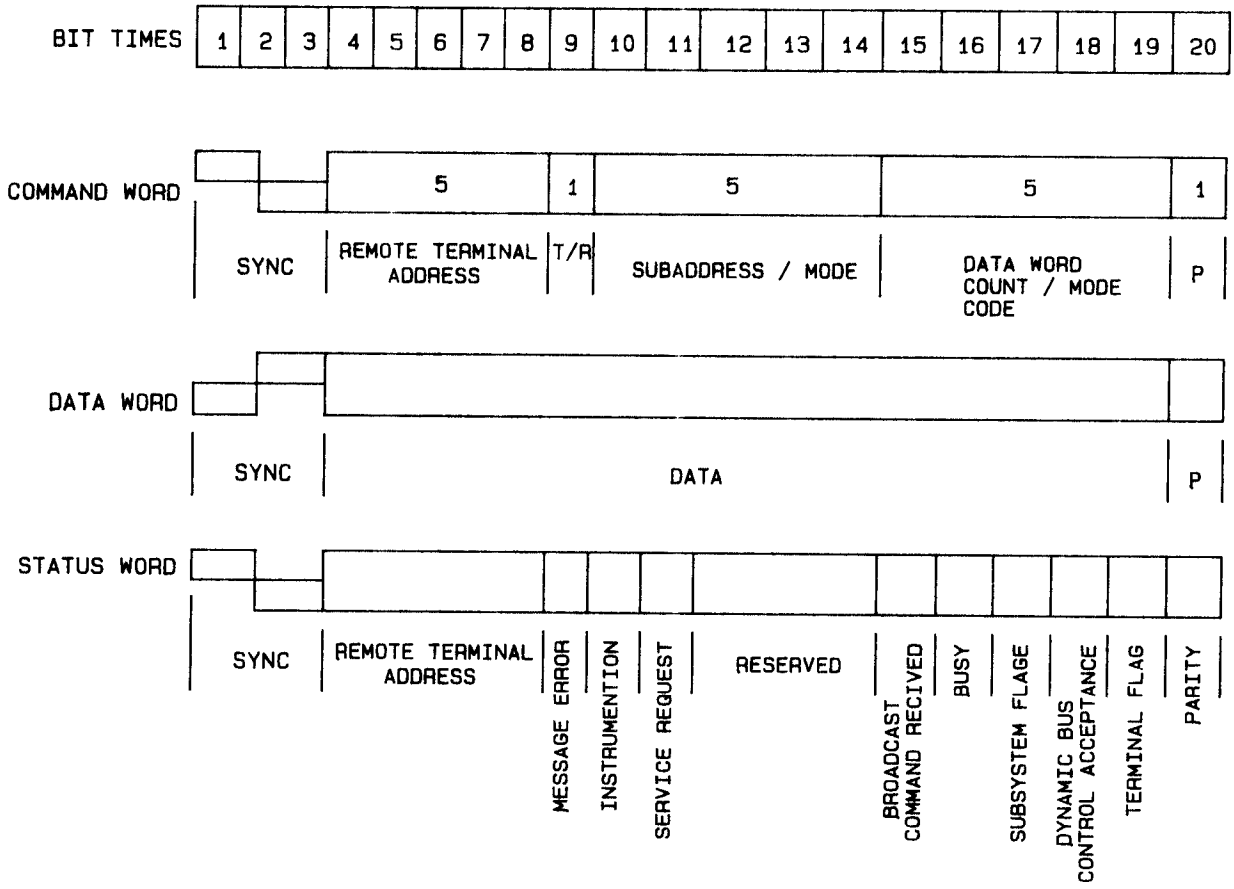
b. The RTI will be reading data from memory for transmission (RRD/$\overline{RWR}$ = 1).

c. The RTI will assert the transmit output ($\overline{XMIT}$) rather than $\overline{RCV}$.



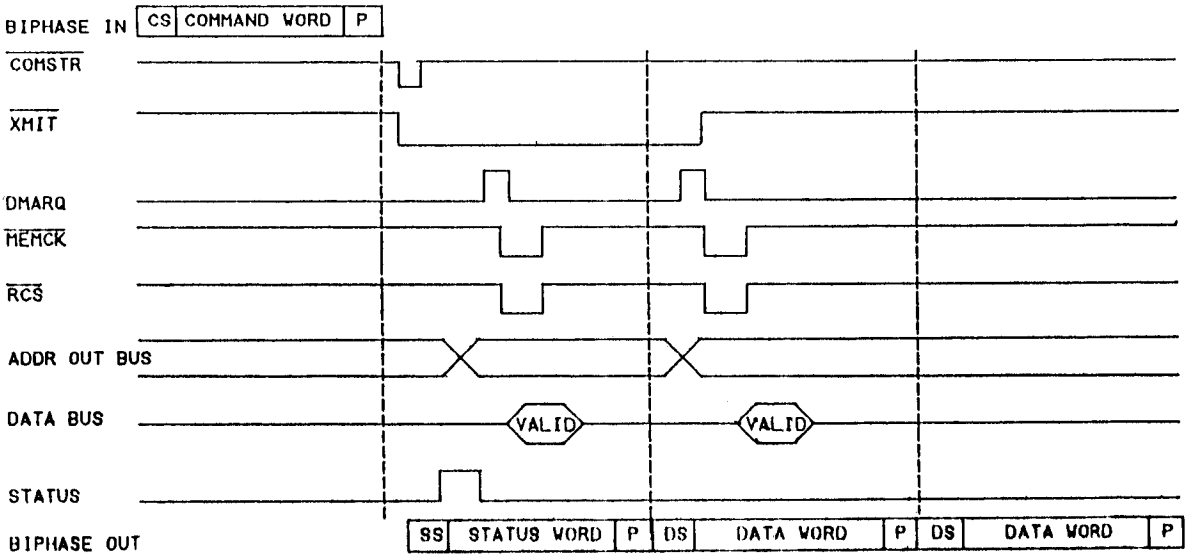
NOTES:
1. CS = Command sync.
2. DS = Data sync.
3. SS = Status sync.
4. P = parity bit.

FIGURE 12. Receive command with two data words.



NOTES:
1. T/R = transmit/receive
2. P = parity

FIGURE 13. MIL-STD-1553 word formats.



NOTES:
1. CS = Command sync.
2. DC = Data sync.
3. SS = Status sync.
4. P = parity bit.
5. RRD/RWR = 1.

FIGURE 14. Transmit two data words command.

The automatic address generation scheme (see 6.3.5g) also applies to a transmit operation. Detailed timing parameters for transmit operation are given in figure 8, and the appendix (figures 15, 18, and 19).

6.3.7 Mode code processing.

a. The RTI will accept both 0 and 1F in the mode/subaddress field of the command word as mode indicators. The RTI will internally decode the following mode codes as illegal:

(1) Dynamic bus control (0).

(2) Selected transmitter shutdown (14).

(3) Override selected transmitter shutdown (15).

(4) All reserved codes.

If the RTI receives one of the above mode commands, it will respond by transmitting the status word with the message error (ME) bit set. The message error (MES ERR) output and the message error latch in the system register will also be set.

b. During mode command processing, the mode code will be valid in the mode code/subaddress MCSA lines and the mode/subaddress ($\overline{MC}$/SA) line will be low. The host can use these lines to decode a mode command it cannot support (but accepted by the RTI) and assert the illegal command (ILL COMM) line. If this should happen, the RTI will respond by transmitting the status word with the ME bit set.

c. Mode commands which involve data transfers are processed just like normal (nonmode) receive and transmit commands. The only difference will be that the memory address will be the last 11 bits of the command word. For example, the memory address generated by the mode command "synchronize with data word" will be 011 (0 00000 10001). Notice that the RTI will always generate 0 in the mode field of the address whether it received an 0 or 1F mode indicator.

d. The RTI will not generate DMA requests for "transmit status word" and "transmit last command" since the status and last command words are stored internally.

e. The following mode commands require assistance from the host:

(1) Synchronize.

(2) Initiate self-test.

(3) Reset remote terminal.

For example, although the RTI will accept and respond to a "reset remote terminal" mode command, it will not perform a reset operation. It will be up to the host to interpret the mode command and take appropriate action.

f. The data word associated with the following mode commands are not defined or interpreted by the RTI:

(1) Transmit vector word.

(2) Synchronize with data word.

(3) Transmit BIT (built-in-test) word.

For example, although the RTI will accept and respond to a "synchronize with data word" and store the data word in memory, it is up to the host to interpret the contents of this data word. Likewise, the RTI will retrieve a word from memory during a "transmit BIT word" command. However, it is up to the host to define the contents of this word.

6.3.8 Broadcast commands.

a. The RTI will accept all valid and legal mode and nonmode broadcast commands in all message formats. Upon receipt of a broadcast command, the RTI will assert its broadcast ($\overline{BRDCST}$) line.

b. In order for the RTI to process broadcast commands, its broadcast enable ($\overline{BCEN}$) input must be low.

6.3.9 Control register writes.

a. The RTI is controlled via an 8-bit control register which is defined in table IV. A control register write is performed by simultaneously asserting the $\overline{CTRL}$ and $\overline{CS}$ signals, RD/$\overline{WR}$ = 0, and ADDR IN 0 = 0 (least significant bit of the address input bus). Detailed timing parameters for a control register write are given on figure 9.

b. A control register write may be performed anytime; however, toggling status word bits are subject to the following conditions:

c. A control register write can be done to assert a status word bit (service request, subsystem flag, busy, or terminal flag). However, note that if a control register write is performed on or before the status (STATUS) line goes high, the transmitted status word will reflect the updated contents of the control register. If the control register is done after STATUS goes low, the transmitted status word will not reflect the updated control register.

d. To remove or negate a status word bit, the control register write must be completed 50 ns before the rising edge of the command strobe ($\overline{COMSTR}$) pulse in order for the current status word to be updated. Otherwise, the status word will be updated only on the receipt of the next command word.

e. Under certain conditions, the external terminal address lines can only be enabled by doing a control register write.

6.3.10 System register access.

a. The status of the RTI can be obtained from a 16-bit system register which is defined in table V. A system register read is performed by asserting $\overline{CTRL}$ and $\overline{CS}$ at the same time (RD/$\overline{WR}$ = 1) and placing the least significant bit of the address input bus (ADDR IN) at a logic 0. Detailed timing parameters for a system register read are given on figure 10.

b. Although a system register read can be done anytime, it is recommended that it be done after STATUS goes to a logic 1. The valid message latch is set at this time indicating that a valid message has been received. After the system register read, the valid message latch is reset.

TABLE IV. Control register.

Bit 0	Channel A enable. A logic 1 will enable channel A.
Bit 1	Channel B enable. A logic 1 will enable channel B.
Bit 2	Terminal flag. A logic 1 will cause the terminal flag bit of the status word to be asserted. The terminal flag bit of the status word will actually be asserted if the RTI had not received an "inhibit terminal flag" mode command.
Bit 3	System busy. A logic 1 will assert the busy bit of the status register and will suppress all DMA requests by the RTI.
Bit 4	Subsystem flag. A logic 1 will assert the subsystem flag of the status register.
Bit 5	Internal test channel select. A logic 1 selects channel A; a logic 0 selects channel B.
Bit 6	Internal test. A logic 1 places the RTI into self-test mode.
Bit 7	Service request. A logic 1 will assert the service request bit of the status register.
Bit 8 . . . Bit 15	don't cares.

TABLE V. System register.

Bit 0	Mode code/subaddress bit 0.
Bit 1	Mode code/subaddress bit 1.
Bit 2	Mode code/subaddress bit 2.
Bit 3	Mode code/subaddress bit 3.
Bit 4	Mode code/subaddress bit 4.
Bit 5	Mode code/subaddress. A logic 1 indicates the last command was a normal transmit or receive command (non-mode) and that bits 4 through 0 above comprise the subaddress field of that command. A logic 0 indicates that the last command was a mode command and that bits 4 through 0 above comprise the mode code field of that command.
*Bit 6	Channel A or B. A logic 1 indicates that the most recent command arrived on channel A; a logic 0 indicates that it arrived on channel B.
Bit 7	Channel B enabled. A logic 1 indicates that channel B is enabled for both transmission and reception.
Bit 8	Channel A enabled. A logic 1 indicates that channel A is enabled for both transmission and reception.
*Bit 9	Terminal flag enabled. A logic 1 indicates that the RTI has not received an "inhibit terminal flag bit" mode code and the host is able to set the terminal flag bit of the status register. A logic 0 indicates that the host is disabled from setting the terminal flag bit of the status word. In this situation, the host can only set the status word terminal flag by either receiving an "override inhibit terminal flag bit" mode code or through a master reset.
*Bit 10	Busy. A logic 1 indicates that the host has enabled the busy bit of the control register and status word.
*Bit 11	Self-test. A logic 1 indicates that the RTI is currently in either the internal or external self-test mode.
Bit 12	Bad terminal address parity. A logic 1 indicates that the RTI has detected a parity error on the terminal address. It also indicates that the RTI has disabled the communication channels and is unable to receive commands.
Bit 13	Message error latch. A logic 1 indicates that at some time a message error condition has occurred. This bit will not return to a logic 0 until the system register has been read.
Bit 14	Valid message latch. A logic 1 indicates that at some time a valid message has been received. This bit will not return to a logic 0 until the system register has been read.
Bit 15	Terminal active. A logic 1 indicates that the RTI is currently processing a transmit or receive instruction. This bit is the logical NAND of the RTI's external $\overline{XMT}$ and $\overline{RCV}$ pins.

* These bits are also available in the last command register.

6.3.11 Last command register access.

a. The last command register of the RTI is defined in table VI. A last command register read is performed by asserting $\overline{CTRL}$ and $\overline{CS}$ at the same time (RD/$\overline{WR}$ = 1) and placing the least significant bit of the address input bus (ADDR IN) at logic 1. Detailed timing parameters for a last command register read are identical to a system register read given in figure 10.

b. A last command register read can be done anytime. However, the last command register is updated during $\overline{COMSTR}$ time except when the RTI receives a "transmit last command."

6.3.12 External illegal command decoding.

a. As mentioned in 6.3.5c, the host has the option of asserting the ILL COMM line if it cannot support a valid command it has received. On receipt of an illegal command, the RTI will set the message error bit in the status word, set the message error output (MES ERR), and set the message error latch in the system register.

The following RTI outputs may be used to externally decode an illegal command; mode code or subaddress indicator ($\overline{MC}$/SA), mode code, or subaddress bus (MCSA 0-4), the transmit indicator ($\overline{XMIT}$), the receive indicator ($\overline{RCV}$), and the broadcast indicator ($\overline{BRDCST}$) and command strobe ($\overline{COMSTR}$).

b. For proper external illegal command decoding; the following timing guidelines should be followed:

(1) The ILL COMM line must be asserted within 3.3 μs after STATUS goes to a logic 1 if the host intends to respond with the ME bit of the status word at a logic 1, except when the illegal command is mode code 2, 4, 5, 6, 7, or 18, in which case the ILL COMM line must be valid 178 ns after $\overline{COMSTR}$ goes to a logic 1.

(2) The minimum pulse width for the ILL COMM signal is 1 μs.

(3) For illegal receive commands, the ILL COMM line must be asserted within 18.2 μs after the $\overline{COMSTR}$ pulse in order for DMA requests to be suppressed. In addition, the ILL COMM line must be at a logic 1 throughout the reception of the message until STATUS is asserted. This does not apply to illegal transmit commands since the status word is transmitted first provided conditions 6.3.12b(1) and 6.3.12b(2) above are met.

(4) The above timing conditions also apply when the host externally decodes an illegal broadcast command. However, caution must be exercised since the status word transmission is suppressed and the STATUS line stays at a logic 0 giving no external hardware indication that the message has been completely received. The host will have to continually monitor the valid message bit of the system register to obtain this information. The host must remove the illegal command condition so that the next command will not be falsely decoded as illegal.

6.3.13 Self-test.

a. The RTI can be placed in a self-test condition by asserting the EXT TEST pin or writing a logic 1 into bit 7 of the control register. A self-test condition will cause the encoder output to be fed back to decoder A or B depending on the status of the EXT TST CH SEL (external test channel select) pin or bit 6 of control register.

b. When external self-test is enabled, any transmission by the RTI will appear on its biphase outputs. During an internal self-test, the biphase outputs are disabled.

c. During self-test, the biphase input channels are disabled. Therefore, the RTI will not be able to receive commands. It is not necessary to enable the channels in the control register to perform a self-test.

TABLE VI. Last command register.

Bit 0	Last command word bit 0.
Bit 1	Last command word bit 1.
Bit 2	Last command word bit 2.
Bit 3	Last command word bit 3.
Bit 4	Last command word bit 4.
Bit 5	Last command word bit 5.
Bit 6	Last command word bit 6.
Bit 7	Last command word bit 7.
Bit 8	Last command word bit 8.
Bit 9	Last command word bit 9.
Bit 10	Last command word bit 10.
*Bit 11	Busy. A logic 1 indicates that the host has enabled the busy bit of the control register and status word.
*Bit 12	Self-test. A logic 1 indicates that the RTI is currently in either the internal or external self-test mode.
*Bit 13	Terminal flag enabled. A logic 1 indicates that the RTI has not received an "inhibit terminal flag bit" mode code and the host is able to set the terminal flag bit of the status register. A logic 0 indicates that the host is disabled from setting the terminal flag bit of the status word. In this situation, the host can only set the status word terminal flag by either receiving an "override inhibit terminal flag bit" mode code or through a master reset.
*Bit 14	Channel A or B. A logic 1 indicates that the most recent command arrived on channel A; a logic 0 indicates that it arrived on channel B.
Bit 15	Illegal command. A logic 1 indicates that the last command received was either decoded internally or externally as an illegal command.

* These bits are also available in the system register.

d. When the RTI is placed in a self-test condition, it will immediately begin transmitting the status word. The state of the status word is not altered when the RTI is placed in self-test. Since the status word and the command word sync pulses are identical, the decoder will interpret the status word being fed back to it as a command word.

e. Any error condition during self-test will cause a status word transmission in order to prevent the RTI from hanging up.

f. The actual self-test should be controlled by the host; the RTI has no predefined self-test routine. The status word from the encoder being fed back to the decoder can be modified by control register writes. The self-test can be monitored via the system and/or last command registers. Only transmit commands can be used during self-test to check for data transfers between RTI and memory. This is because a receive command (which was a status word from the encoder) will effectively cancel the transmission of the associated data words.

g. There are two ways to get out of self-test. The first is via a master reset. The second is to negate the EXT TEST pin or the self-test bit in the control register. This does not actually stop the self-test but causes the encoder-to- decoder link to be severed on the next valid command generated by the self-test.

6.3.14 Transparent memory access.

a. A host performs a "transparent" memory access when it does a memory transfer to or from a memory device whose address and control lines are connected to the RTI. The host does this by asserting the $\overline{CS}$ and RD/$\overline{WR}$ pins and placing an 11-bit address on the RTI's address input pins. The signal $\overline{CTRL}$ must remain at a logic 1 at all times during transparent memory access to prevent the RTI from performing a control register write, a system register read, a last command register read, or a software master reset.

b. The $\overline{CS}$ pin when at a logic 0 will prevent the RTI itself from doing a memory access; this means that the data bus will remain at high impedance and the address outputs and RAM read/write (RRD/$\overline{RWR}$) will reflect the state of the address inputs and RD/$\overline{WR}$ lines respectively.

c. The RTI will still be able to assert the DMARQ line while $\overline{CS}$ is at a logic 0 although $\overline{MEMCK}$ transitions will not be recognized. This implies that the RTI can still process incoming commands while it is being used by the host. Note that the RTI recognizes $\overline{MEMCK}$ transitions only; therefore, if $\overline{MEMCK}$ is asserted (in response to DMARQ) while $\overline{CS}$ is at logic 0, it will have to be negated and reasserted when $\overline{CS}$ goes high.

6.3.15 Terminal fail-safe operation.

a. The RTI has a built in counter that will time out in 730 µs. Detailed timing parameters are shown on figure 12. This timer is activated whenever the encoder is enabled and is about to transmit information on the biphase outputs. This is indicated by the signal $\overline{TIMERON}$ going to a logic 0.

b. When the RTI receives a valid command, it will reset the timer during $\overline{COMSTR}$ time and return signal $\overline{TIMERON}$ back to a logic 1. The timer will also reset when it has reached its timeout period or when the RTI is reset.

c. During external test, the timer will not recognize the $\overline{COMSTR}$ signal and will be allowed to time out so that the host will be able to test its external fail-safe hardware.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (finish A for Cerquad) (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	UT1553BRTI
02	UT1553BRTIA

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation to static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive foam or carriers.

e. The use of plastic, rubber, or silk in MOS areas should be avoided.

f. Relative humidity should be maintained above 50 percent, if practical.

g. Operator should be grounded when handling devices.

6.7 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX

DESIGN LIMIT TIMING PARAMETERS

10. SCOPE

10.1 Scope. This appendix contains supplementary timing parameters with associated diagrams for clarification that are to be used as design limits. Due to testing limitations, these parameters cannot be tested, many of these timings are such that it is impractical to do so. This appendix is a mandatory part of the specification and the information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. DESIGN LIMIT TIMING PARAMETERS 1/

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{PLH39} t_{PHL39}	Command word mid-parity bit to CH A/$\overline{B}$ valid	2.58	2.66	µs	15	
t_{PHL40}	Command word mid-parity bit to $\overline{COMSTR}$(L) and $\overline{RCV}$(L) or $\overline{XMIT}$(L)	3.58	3.67	µs	15, 18, 20	
t_{WL41}	$\overline{COMSTR}$ low pulse width	499	502	ns	15	
t_{PHL42}	$\overline{BRDCST}$, $\overline{MC}$/SA, MCSA, ADDR OUT valid before $\overline{COMSTR}$(L) (set-up)	430		ns	15	2/
t_{PHL43}	$\overline{COMSTR}$(L) to MES ERR	745	750	ns	15	3/
t_{PLH44}	Received data word mid-parity bit to DMARQ(H)	3.58	3.68	µs	16, 17	
t_{OOLH45}	ADDR OUT valid before DMARQ(H)	0.9		µs	16	
t_{PHL46}	1553B response time BIPHASE to BIPHASE OUT	8.80	9.37	µs	17, 18, 20	4/
t_{PLH47}	STATUS(H), RCV(H) before BIPHASE OUT(H)	1.24	1.25	µs	17, 18, 20	
t_{WH48}	STATUS high pulse width	4.48	4.98	µs	17, 18, 20	
t_{PLH49}	Transmit command mid-parity bit to DMARQ(H) for first word to be transmitted	12.05	12.16	µs	18	
t_{PLH50}	DMARQ(H) lead time before mid-data sync of data word to be transmitted	17.15	17.18	µs	19	5/

See footnotes at end of table.

APPENDIX

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{PLH51}	DMARQ(H) to next DMARQ(H) during transmit		19.92	µs	19	5/
t_{PLH52}	$\overline{XMIT}$(H) after last DMARQ(H)	460	500	ns	19	
t_{WL53}	$\overline{XMIT}$ low pulse width for mode codes without data words	1.0		µs	20	
t_{PLH54}	Illegal mode command mid-parity bit to MES ERR(H)	6.57	6.68	µs	20	6/
t_{PLH55}	Data word mid-parity bit to MES ERR(H) timeout for missing data words during receive	23.50	23.63	µs	21	
t_{PLH56}	Receive command mid-parity bit to MES ERR(H) timeout for no response from the transmitter during RT to RT	55.4	55.5	µs	22	7/

1/ These additional timing parameters are meant to supplement those given in table I. These timing parameters were derived from logic simulations (fast and slow conditions) and are not tested or guaranteed.

2/ The ADDR OUT will contain the 11-bit command word.

3/ MES ERR was high from a previous command. This is part of the status word reset requirements given in MIL-STD-1553. MES ERR will remain high if the current command is a transmit status word or a transmit last command mode code.

4/ In accordance with MIL-STD-1553.

5/ This is true only if DMARQ is acknowledged (via $\overline{MEMCK}$ by the host within the time constraints given in table I. If these time constraints are exceeded, the RTI will be forced to introduce gaps between the transmitted data words which will be a violation of MIL-STD-1553 with respect to data contiguity.

6/ This refers to mode codes internally decoded within the RTI as illegal.

7/ See notice 2 of MIL-STD-1553.

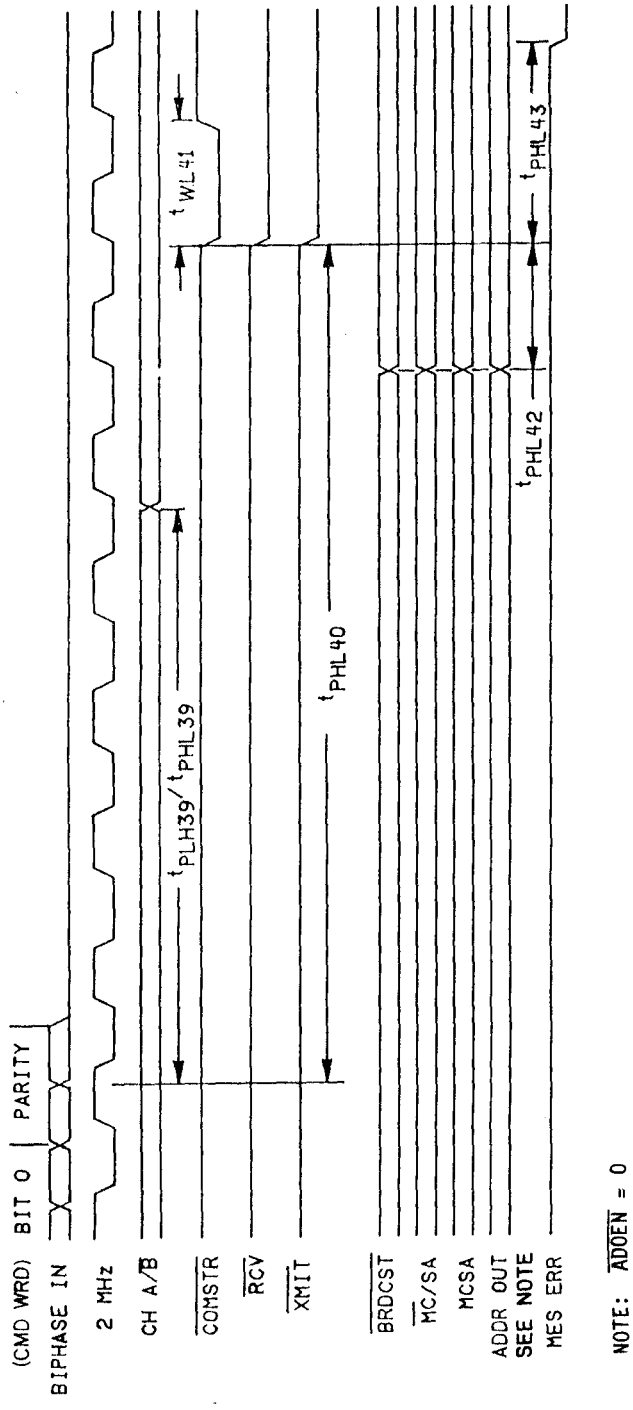


FIGURE 15. Command word validation timing.

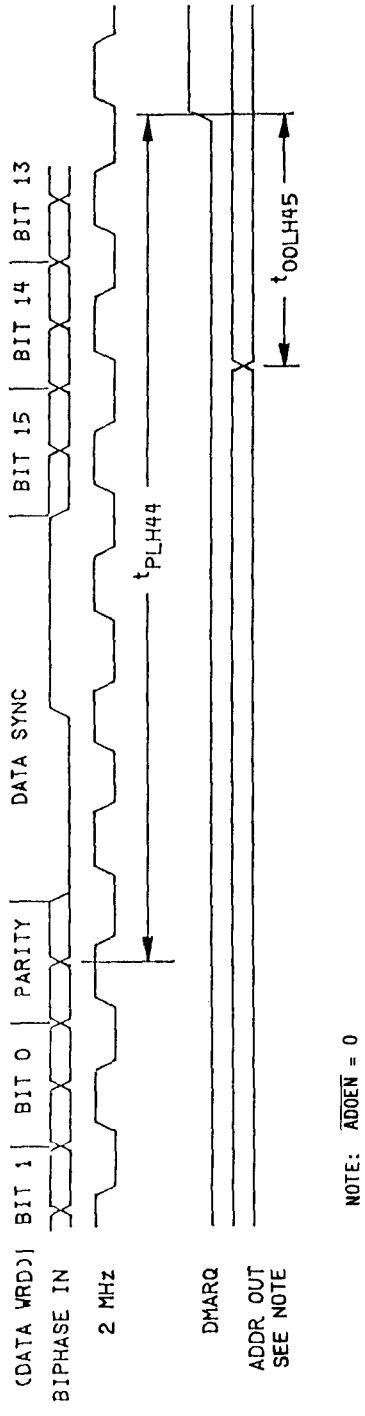


FIGURE 16. Received data work validation timing.

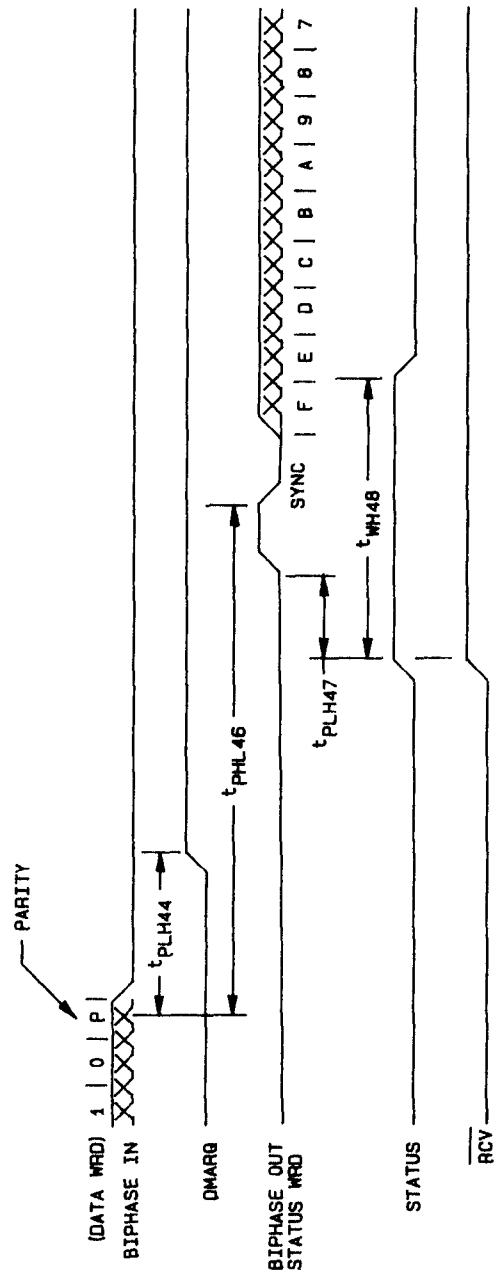


FIGURE 17. Received last data word validation and response timing.

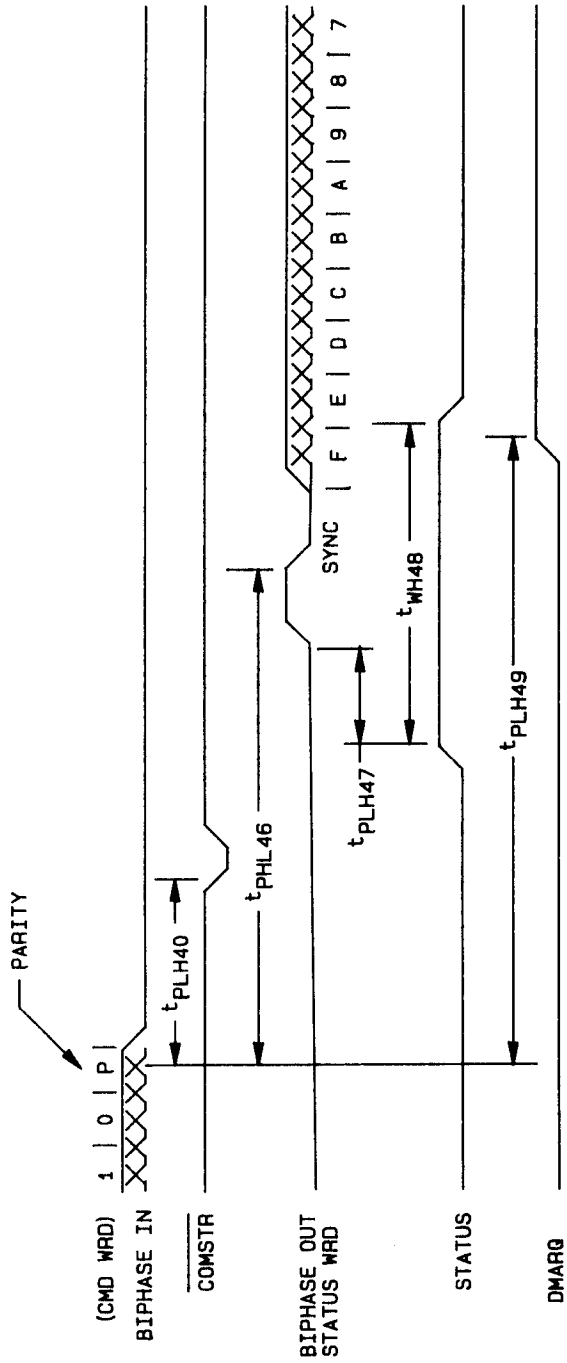


FIGURE 18. Transmit command response timing.

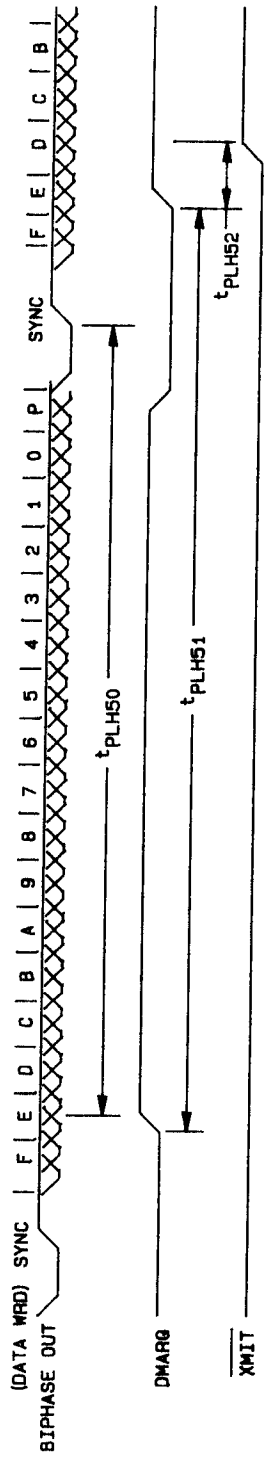


FIGURE 19. Transmitted data timing.

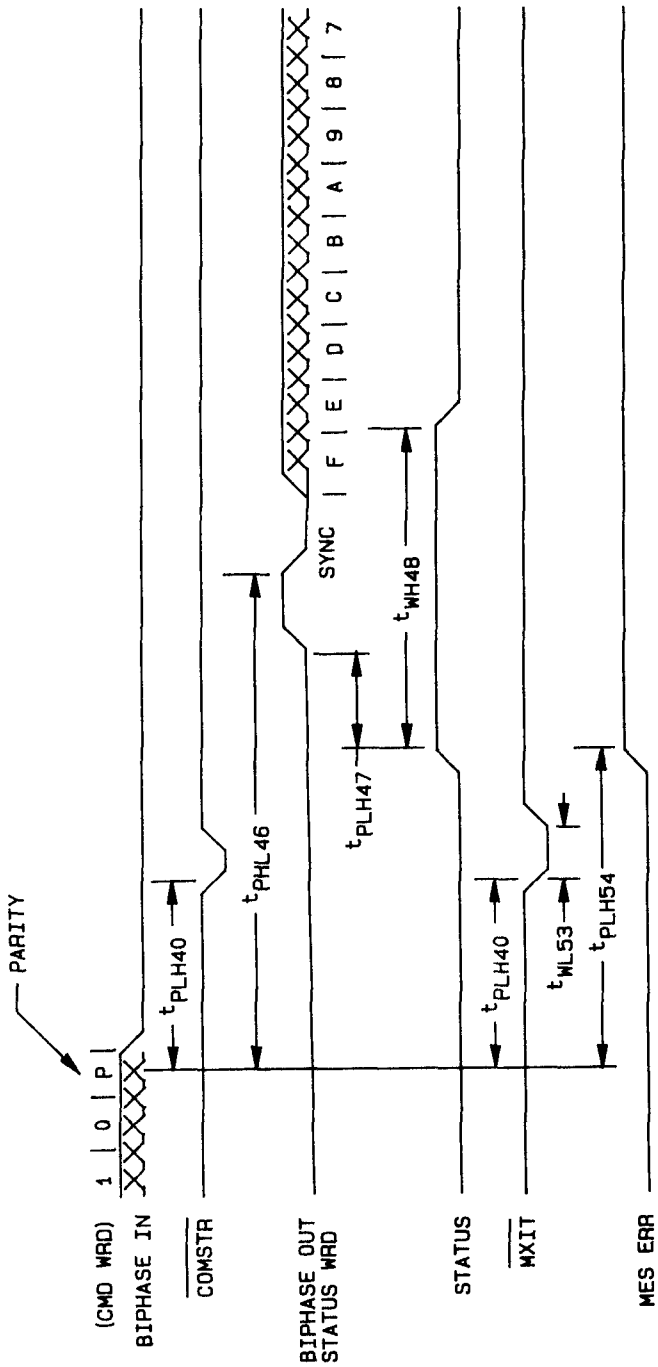


FIGURE 20. Mode command response timing.

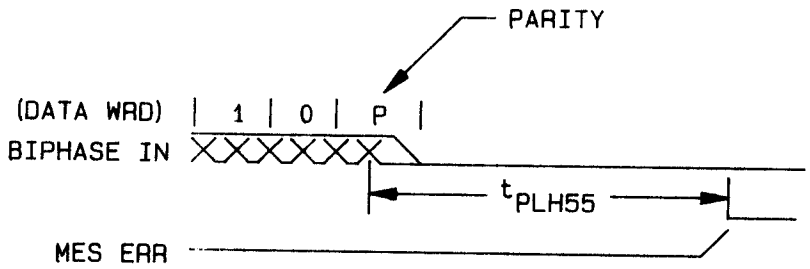


FIGURE 21. Message error timeout during normal receive due to missing data words from bus controller.

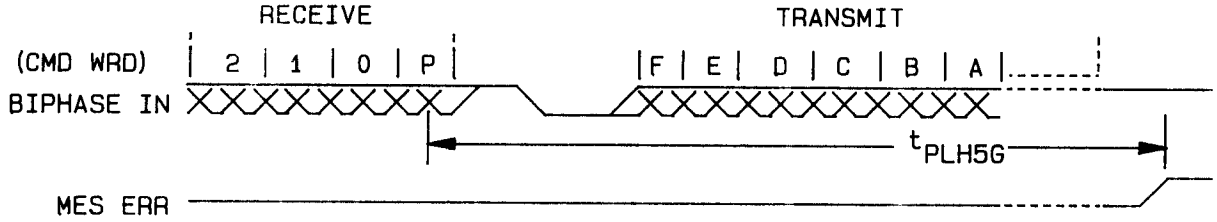


FIGURE 22. Message error timeout during remote terminal to remote terminal receive (due to no response from the transmitter).

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1230)