

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL,

BINARY FULL ADDERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, full adder microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	2-Bit full adder
02	4-Bit full adder
03	Dual full adder
04	Gated full adder

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>MIL-M-38510, appendix C case outline</u>
A	F-1 (14-pin, 1/4" x 1/4", flat-pack)
B	F-3 (14-pin, 1/4" x 1/8", flat-pack)
C	D-1 (14-pin, 1/4" x 3/4", dual-in-line)
D	F-2 (14-pin, 1/4" x 3/8", flat-pack)
E	D-2 (16-pin, 1/4" x 7/8", dual-in-line)
F	F-5 (16-pin, 1/4" x 3/8", flat-pack)

1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.5 Vdc to 7.0 Vdc
Input voltage range	- - - - -	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range	- - - - -	-65 °C to 150 °C
Maximum power dissipation 1/	- - - - -	$P_D = 275 \text{ mWdc}$ for types 01 and 03 $P_D = 550 \text{ mWdc}$ for type 02 $P_D = 165 \text{ mWdc}$ for type 04
Lead temp. (soldering 10 secs)	- - - - -	300 °C
Thermal resistance, junction to case	- - -	$\theta_{JC} = 0.09 \text{ °C/mW}$ for flat pack $\theta_{JC} = 0.08 \text{ °C/mW}$ for dual-in-line pack
Junction temperature	- - - - -	$T_J = 175 \text{ °C}$

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for five (5) seconds duration.

1.4 Recommended operating conditions.

Supply voltage	- - - - -	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	- - - - -	2.0 Vdc
Maximum low level input voltage	- - - - -	0.8 Vdc
Normalized fanout (each input)	1/ - - - -	10 maximum for sum outputs 5 maximum for carry outputs
Ambient operating temperature range	- - -	-55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. Case outlines shall be as specified in 1.2.3.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagram shall be as specified on figure 3.

3.2.5 Schematic circuit. The schematic circuit shall be as specified on figure 4.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range, unless otherwise specified.

1/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IN} = 0.8 V or 2.0 V 3/	All	2.4	---	Volts
Low-level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IN} = 2.0 V or 0.8 V 4/	All	---	0.4	Volts
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -12 mA, T _A = 25°C	All	---	-1.5	Volts
High-level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.4 V 2/ A ₁ , B ₁ , A ₂ , B ₂ , C ₀ A ₁ , B ₁ , A ₃ , B ₃ , C ₀ A ₂ , B ₂ , A ₄ , B ₄ A ₂ , B ₂ A ₁ , A ₂ , B ₁ , B ₂ , A _C , B _C	01 02 02 03 04	---	160 160 40 40 15	μA
High-level input current	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 5.5 V 2/	01, 02	---	400	μA
High-level input current	I _{IH3}	V _{CC} = 5.5 V V _{IN} = 2.4 V 2/ A ₁ , B ₁ , A ₂ , B ₂ , C ₁ , C ₂ C _N	03 04	---	160 200	μA
High-level input current	I _{IH4}	V _{CC} = 5.5 V, V _{IN} = 5.5 V 2/	03 04	---	400 1	μA mA
Low-level input current	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V 1/ A ₁ , B ₁ , C ₀ A ₁ , B ₁ , A ₃ , B ₃ , C ₀ A ₂ , B ₂ , A ₁ , A ₂ , B ₁ , B ₂ , A _C , B _C	01 02 03 04	-1.4 -0.8 -0.4 ---	-6.4 -6.4 -1.3 -1.6	mA
Low-level input current	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.4 V 1/ A ₂ , B ₂ , A ₂ , B ₂ , A ₄ , B ₄ A ₁ , B ₁ , C ₁ A*, B*	01 02 03 04	-0.7 -0.7 -1.2 ---	-3.2 -3.2 -5.6 -2.6	mA
Low-level input current	I _{IL3}	V _{CC} = 5.5 V, V _{IN} = 0.4 V 1/ A ₂ , B ₂ , C ₂ C _N	03 04	-1.2 ---	-5.6 -8.0	mA mA
Short-circuit output current at Σ	I _{OS1}	V _{CC} = 5.5 V, V _{IN} = 4.5 V, V _{OUT} = 0 V 5/	01 02 03 04	-20 -20 -30 -20	-70 -55 -100 -57	mA
Short-circuit output current at C	I _{OS2}	V _{CC} = 5.5 V, V _{IN} = 4.5 V, V _{OUT} = 0 V 5/	01, 02, 04	-20	-70	mA
Short-circuit output current at A* or B*	I _{OS3}	V _{CC} = 5.5 V, V _{IN} = 0 V, V _{OUT} = 0 V 5/	04	-0.9	-2.9	mA
Supply current	I _{CC}	V _{CC} = 5.5 V, V _{IN} = 4.5 V	01 02 03 04	---	50 100 55 31	mA
Propagation delay time, high-to-low-level, C ₀ to Σ1	t _{PHL1}	C _L = 50 pF, R _L = 390 Ω	01 02	3 3	61 51	ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Propagation delay time, low-to-high-level, C ₀ to Σ ₁	tPLH1	C _L = 50 pF, R _L = 390 Ω	01 02	3	56 39	ns
Propagation delay time, high-to-low-level, B ₂ to Σ ₂	tPHL2	C _L = 50 pF, R _L = 390 Ω		01 02	3 3	
Propagation delay time, low-to-high-level, B ₂ to Σ ₂	tPLH2	C _L = 50 pF, R _L = 390 Ω	01 02	3	65 45	ns
Propagation delay time, high-to-low-level, C ₀ to Σ ₂	tPHL3	C _L = 50 pF, R _L = 390 Ω		01 02	3 3	
Propagation delay time, low-to-high-level, C ₀ to Σ ₂	tPLH3	C _L = 50 pF, R _L = 390 Ω	01 02	3	62 51	ns
Propagation delay time, high-to-low-level, C ₀ to C ₂	tPHL4	C _L = 50 pF, R _L = 800 Ω		01	3	
Propagation delay time, low-to-high-level, C ₀ to C ₂	tPLH4	C _L = 50 pF, R _L = 800 Ω	01	3	43	ns
Propagation delay time, high-to-low-level, C ₀ to Σ ₃	tPHL4	C _L = 50 pF, R _L = 390 Ω	02	3	77	ns
Propagation delay time, low-to-high-level, C ₀ to Σ ₃	tPLH4	C _L = 50 pF, R _L = 390 Ω	02	3	62	ns
Propagation delay time, high-to-low-level, C ₀ to Σ ₄	tPHL5	C _L = 50 pF, R _L = 390 Ω	02	3	71	ns
Propagation delay time, low-to-high-level, C ₀ to Σ ₄	tPLH5	C _L = 50 pF, R _L = 390 Ω	02	3	72	ns
Propagation delay time, high-to-low-level, C ₀ to C ₄	tPHL6	C _L = 50 pF, R _L = 800 Ω	02	3	55	ns
Propagation delay time, low-to-high-level, C ₀ to C ₄	tPLH6	C _L = 50 pF, R _L = 800 Ω	02	3	63	ns
Propagation delay time, high-to-low-level, A ₂ to Σ ₂	tPHL7	C _L = 50 pF, R _L = 390 Ω	02	3	40	ns
Propagation delay time, low-to-high-level, A ₂ to Σ ₂	tPLH7	C _L = 50 pF, R _L = 390 Ω	02	3	45	ns
Propagation delay time, high-to-low-level, A ₄ to Σ ₄	tPHL8	C _L = 50 pF, R _L = 390 Ω	02	3	40	ns
Propagation delay time, low-to-high-level, A ₄ to Σ ₄	tPLH8	C _L = 50 pF, R _L = 390 Ω	02	3	45	ns
Propagation delay time, high-to-low-level, B ₄ to Σ ₄	tPHL9	C _L = 50 pF, R _L = 390 Ω	02	3	40	ns
Propagation delay time, low-to-high-level, B ₄ to Σ ₄	tPLH9	C _L = 50 pF, R _L = 390 Ω	02	3	45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions	Device type	Limits Min	Limits Max	Unit
Propagation delay time, high-to-low-level, C_1 to Σ_1	t _{PHL1}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	9	59	ns
Propagation delay time, low-to-high-level, C_1 to Σ_1	t _{PLH1}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	9	60	ns
Propagation delay time, high-to-low-level, C_1 to $\bar{\Sigma}_1$	t _{PHL2}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	6	39	ns
Propagation delay time, low-to-high-level, C_1 to $\bar{\Sigma}_1$	t _{PLH2}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	6	39	ns
Propagation delay time, high-to-low-level, C_1 to \bar{C}_{01}	t _{PHL3}	$C_L = 50 \text{ pF}$, $R_L = 800 \Omega$	03	3	21	ns
Propagation delay time, low-to-high-level, C_1 to \bar{C}_{01}	t _{PLH3}	$C_L = 50 \text{ pF}$, $R_L = 800 \Omega$	03	3	21	ns
Propagation delay time, high-to-low-level, A_2 to Σ_2	t _{PHL4}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	11	67	ns
Propagation delay time, low-to-high-level, A_2 to Σ_2	t _{PLH4}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	11	69	ns
Propagation delay time, high-to-low-level, A_2 to Σ_2	t _{PHL5}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	8	48	ns
Propagation delay time, low-to-high-level, A_2 to Σ_2	t _{PLH5}	$C_L = 50 \text{ pF}$, $R_L = 390 \Omega$	03	8	49	ns
Propagation delay time, high-to-low-level, A_2 to \bar{C}_{02}	t _{PHL6}	$C_L = 50 \text{ pF}$, $R_L = 800 \Omega$	03	5	28	ns
Propagation delay time, low-to-high-level, A_2 to \bar{C}_{02}	t _{PLH6}	$C_L = 50 \text{ pF}$, $R_L = 800 \Omega$	03	5	29	ns
Propagation delay time, high-to-low-level, C_n to \bar{C}_{n+1}	t _{PHL1}	$C_L = 50 \text{ pF}$, $R_L = 780 \Omega$	04	---	18	ns
Propagation delay time, low-to-high-level, C_n to \bar{C}_{n+1}	t _{PLH1}	$C_L = 50 \text{ pF}$, $R_L = 780 \Omega$	04	---	33	ns
Propagation delay time, high-to-low-level, B_C to \bar{C}_{n+1}	t _{PHL2}	$C_L = 50 \text{ pF}$, $R_L = 780 \Omega$	04	---	90	ns
Propagation delay time, low-to-high-level, B_C to \bar{C}_{n+1}	t _{PLH2}	$C_L = 50 \text{ pF}$, $R_L = 780 \Omega$	04	---	45	ns
Propagation delay time, high-to-low-level, A_C to Σ	t _{PHL3}	$C_L = 50 \text{ pF}$, $R_L = 400 \Omega$	04	---	127	ns
Propagation delay time, low-to-high-level, A_C to Σ	t _{PLH3}	$C_L = 50 \text{ pF}$, $R_L = 400 \Omega$	04	---	112	ns
Propagation delay time, high-to-low-level, B_C to Σ	t _{PHL4}	$C_L = 50 \text{ pF}$, $R_L = 400 \Omega$	04	---	120	ns
Propagation delay time, low-to-high-level, B_C to Σ	t _{PLH4}	$C_L = 50 \text{ pF}$, $R_L = 400 \Omega$	04	---	90	ns
Propagation delay time, high-to-low-level, A_1 to A^*	t _{PHL5}	$C_L = 50 \text{ pF}$	04	---	45	ns
Propagation delay time, low-to-high-level, A_1 to A^*	t _{PLH5}	$C_L = 50 \text{ pF}$	04	---	105	ns
Propagation delay time, high-to-low-level, B_1 to B^*	t _{PHL6}	$C_L = 50 \text{ pF}$	04	---	45	ns
Propagation delay time, low-to-high-level, B_1 to B^*	t _{PLH6}	$C_L = 50 \text{ pF}$	04	---	105	ns

See footnotes on page 6.

- 1/ All unspecified inputs at 5.5 volts.
- 2/ All unspecified inputs grounded.
- 3/ I_{OH} for each sum output is -0.4 mA (types 01, 02 and 04) and -0.8 mA (type 03) and for each carry output it is -0.2 mA (types 01, 02 and 04) and -0.56 mA (type 03). I_{OH} for A* or B* is -0.12 mA (type 04).
- 4/ I_{OL} for each sum output is 16 mA and for each carry output it is 8 mA. I_{OL} for A* or B* is 4.8 mA (type 04).
- 5/ Not more than one output should be shorted at one time.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification and quality conformance, by device class are specified in table II. (Subgroups 7 and 8 testing requires only a summary of attributes data.)

TABLE II. Electrical test requirements.

MIL-STD-883 Test requirement	Subgroups (see table III)		
	Class A Devices	Class B Devices	Class C Devices
Interim electrical parameters (Pre Burn-In) (Method 5004)	1	1	None
Final electrical test parameters (Method 5004)	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9	1, 7
Group A test requirements (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9 10, 11	1, 2, 3, 7, 9
Groups C and D end point electrical parameters (Method 5005)	1, 2, 3	1, 2, 3	1
Additional electrical subgroups for Group C periodic inspections	None	None	10, 11

* PDA applies to subgroup 1 (see 4.3(d)).

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container:

(a) Country of origin.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 4. (See MIL-M-38510 Appendix E.)

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and Method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, and 4.4.3).

4.3 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- (a) Burn-in test (Method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$ minimum.
- (b) Reverse bias burn-in and interim electrical test in accordance with 3.1.12 of Method 5004 of MIL-STD-883 may be omitted.
- (c) Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- (d) Percent defective allowable (PDA) - The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with Method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of Method 5005 of MIL-STD-883 and as follows:

- (a) Tests shall be as specified in table II.
- (b) Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of Method 5005 of MIL-STD-883.

4.4.3 Groups C and D inspections. Groups C and D inspections shall be in accordance with tables III and IV of Method 5005 of MIL-STD-883 and as follows:

- (a) End point electrical parameters shall be as specified in table II.
- (b) Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- (c) Operating life-test (Method 1005 of MIL-STD-883) conditions, or equivalent:
 - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by Appendix B of MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables and as follows.

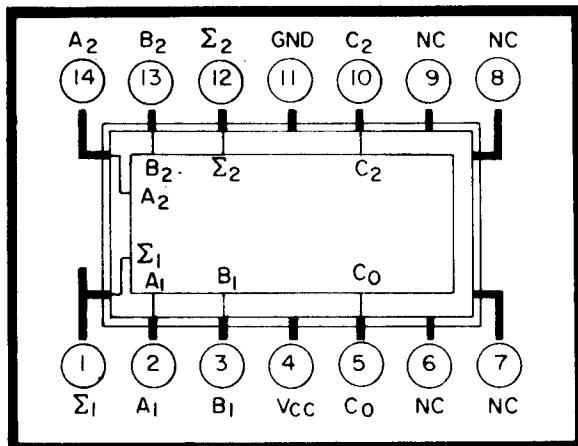
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

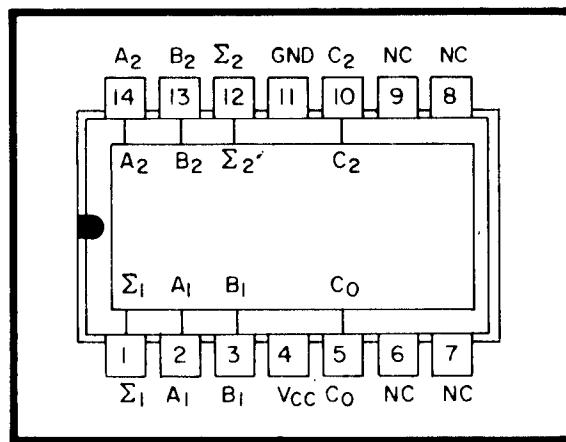
4.6 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

Device type 01

Case A, B and D

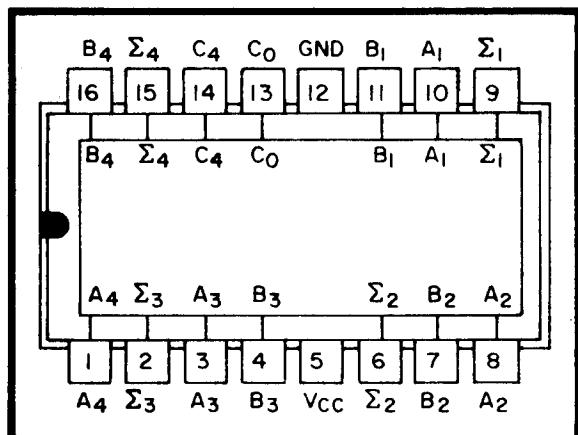


Case C



Device type 02

Case E and F



Device type 03

Case E and F

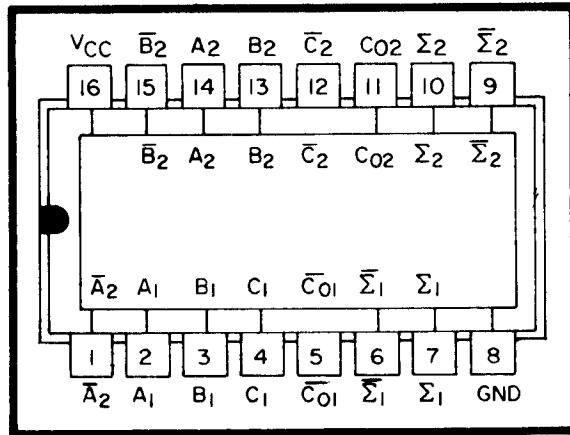
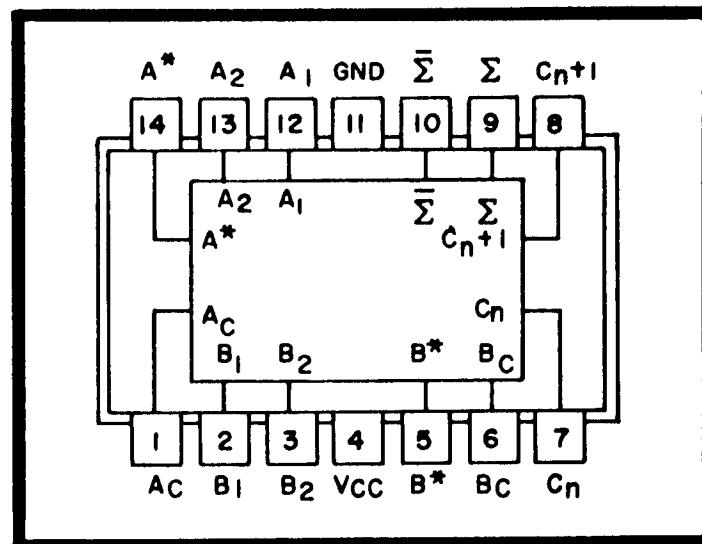


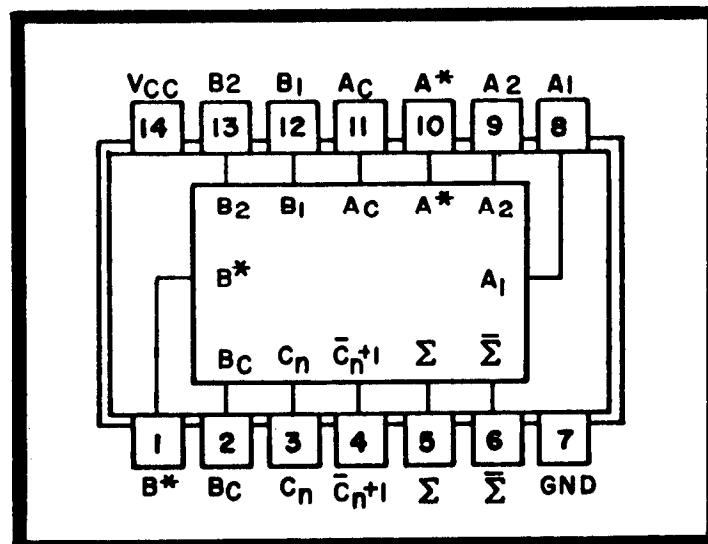
FIGURE 1. Terminal connections - top views.

Device type 04

Cases A, B and D



Case C

FIGURE 1. Terminal connections - top view - Continued.

Device type 01

INPUT				OUTPUT				
A ₁	B ₁	A ₂	B ₂	When C ₀ =L			When C ₀ =H	
				Σ ₁	Σ ₂	C ₂	Σ ₁	Σ ₂
L	L	L	L	L	L	L	H	L
H	L	L	L	H	L	L	L	H
L	H	L	L	H	L	L	L	H
H	H	L	L	L	H	L	H	L
L	L	H	L	L	H	L	H	H
H	L	H	L	H	H	L	L	H
L	H	H	L	L	H	L	H	L
H	H	H	L	H	H	L	H	H
L	L	L	H	L	H	H	L	H
H	L	L	H	H	L	L	H	L
L	H	H	H	L	H	L	L	H
H	H	H	H	L	H	H	H	H

Device type 02

INPUT				OUTPUT					
				When C ₀ =L			When C ₀ =H		
A ₁	B ₁	A ₂	B ₂	Σ ₁	Σ ₂	C ₂	Σ ₁	Σ ₂	C ₂
A ₃	B ₃	A ₄	B ₄	Σ ₃	Σ ₄	C ₄	Σ ₃	Σ ₄	C ₄
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	H	
L	H	H	L	H	H	L	L	H	
H	H	H	L	L	H	H	L	H	
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	H	
L	H	L	H	H	H	L	L	H	
H	H	L	H	L	L	H	L	H	
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A₁, A₂, B₁, B₂, and C₀ are used to determine outputs Σ₁ and Σ₂, and the value of the internal carry C₂. The values at C₂, A₃, B₃, A₄, and B₄, are then used to determine outputs Σ₃, Σ₄, and C₄.

FIGURE 2. Truth tables.

Device type 03

Adder 2							
Inputs					Outputs		
\bar{C}_2	B ₂	A ₂	\bar{B}_2	\bar{A}_2	C _{O2}	Σ_2	$\bar{\Sigma}_2$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	L	H	H	L	H
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	H	L	L	H	H	L
L	H	H	L	H	H	L	H
L	H	H	H	L	H	H	L
L	H	H	H	H	H	L	H
L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L
H	L	L	L	H	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	H	L	H
H	L	L	H	H	L	H	L
H	L	H	L	L	H	L	H
H	L	H	L	H	L	H	L
H	L	H	L	H	H	L	H
H	L	H	H	L	H	L	H
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	L	H	H	L	H
H	H	H	L	H	L	H	H
H	H	H	H	H	L	H	H

Adder 1							
Inputs				Outputs			
C ₁	B ₁	A ₁		\bar{C}_{O1}	$\bar{\Sigma}_1$	Σ_1	
L	L	L		H	H	L	
L	L	H		H	L	H	
L	H	L		H	L	H	
L	H	H		L	H	L	
H	L	L		H	L	H	
H	H	L		L	H	L	
H	H	H		L	H	L	
H	H	H		L	H	H	

Device type 04

Inputs			Outputs		
C _n	B	A	\bar{C}_{n+1}	$\bar{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

NOTES:

1. $A = \bar{A}_C + \bar{A}^* + A_1 \cdot A_2$, $B = \bar{B}_C + \bar{B}^* + B_1 \cdot B_2$.
2. When A^* is used as an input, A_1 or A_2 must be low.
When B^* is used as an input, B_1 or B_2 must be low.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* , respectively, must be open or used to perform dot-AND logic.

FIGURE 2. Truth tables - Continued.

Device type 01, Circuit A

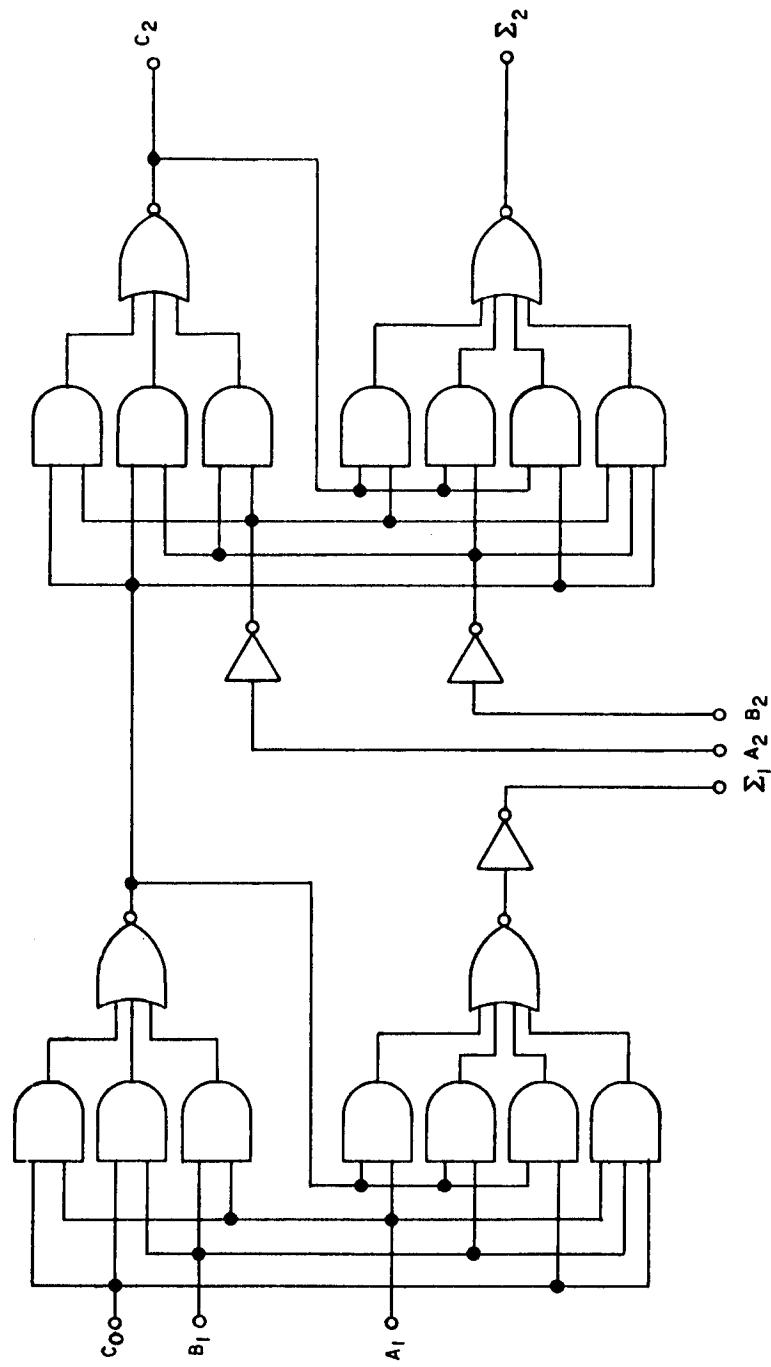


FIGURE 3. Logic diagrams.

Device type 01, Circuit B

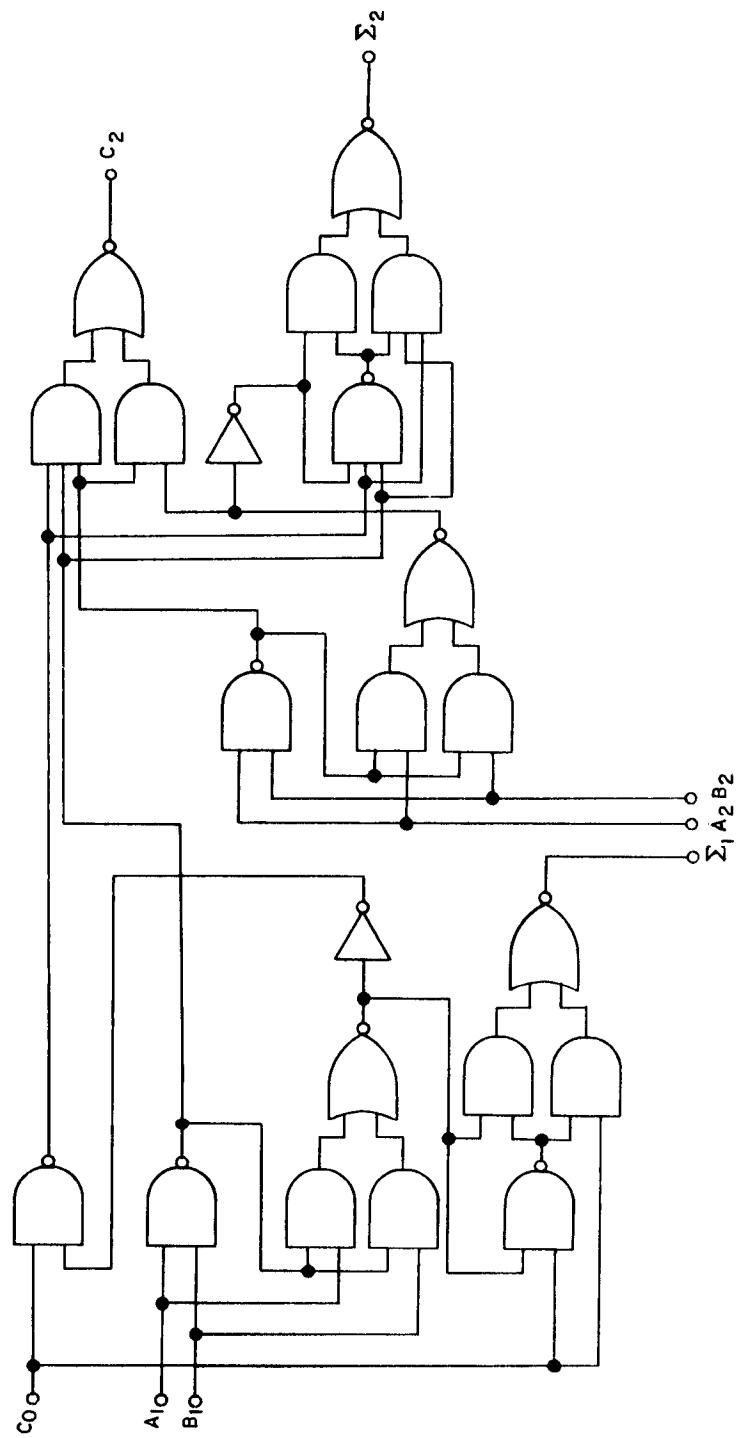


FIGURE 3. Logic diagrams - Continued.

Device type 02, Circuit C, E, G and H

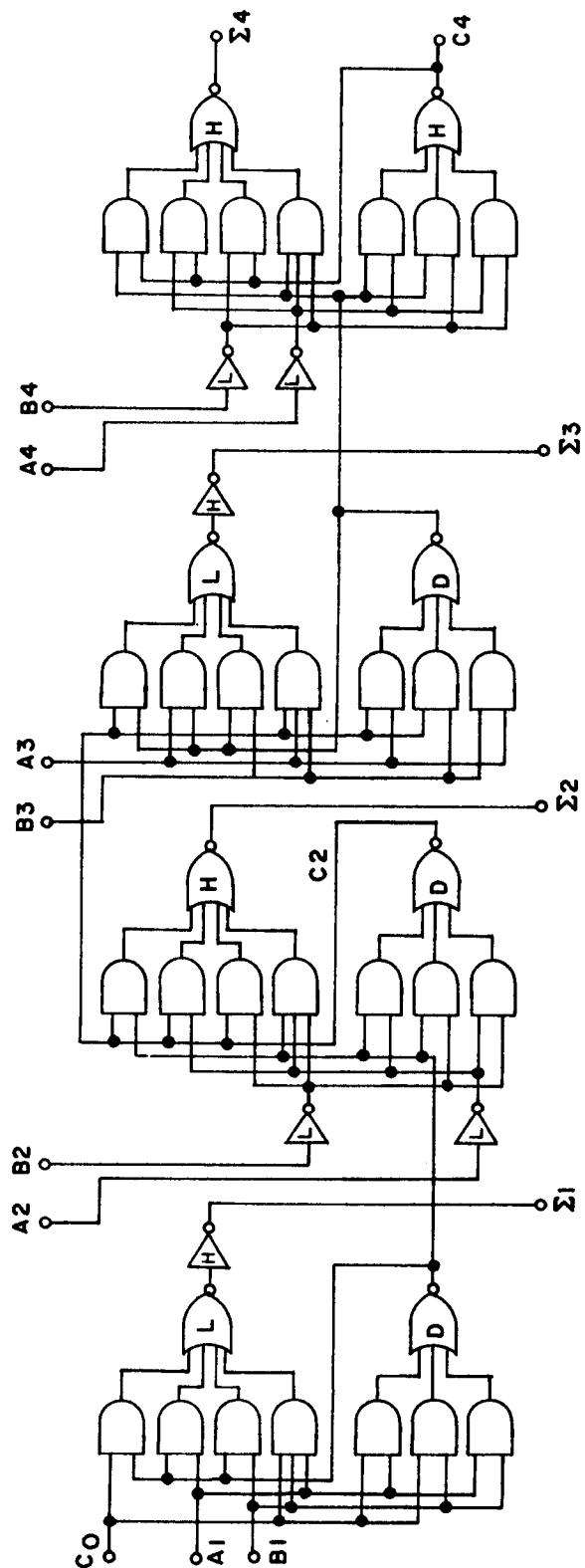


FIGURE 3. Logic diagrams - Continued.

Device type 02, Circuit D

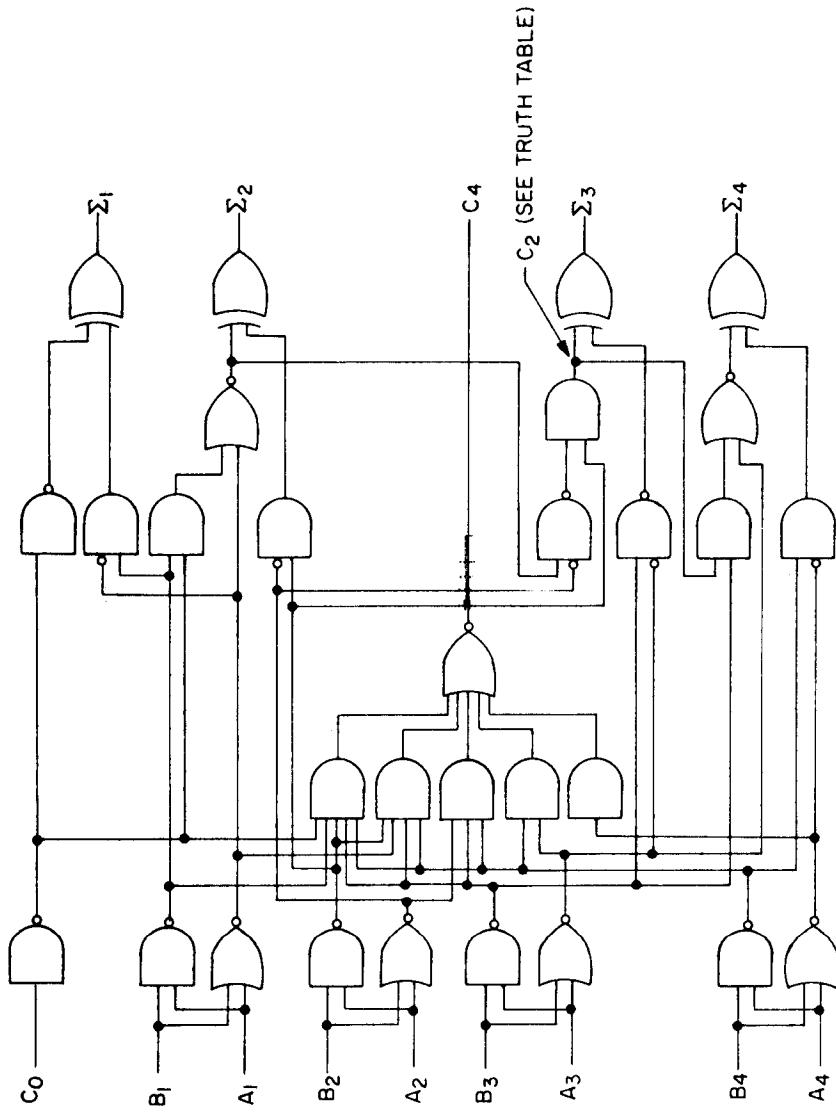


FIGURE 3. Logic diagrams - Continued.

Device type 02, Circuit F

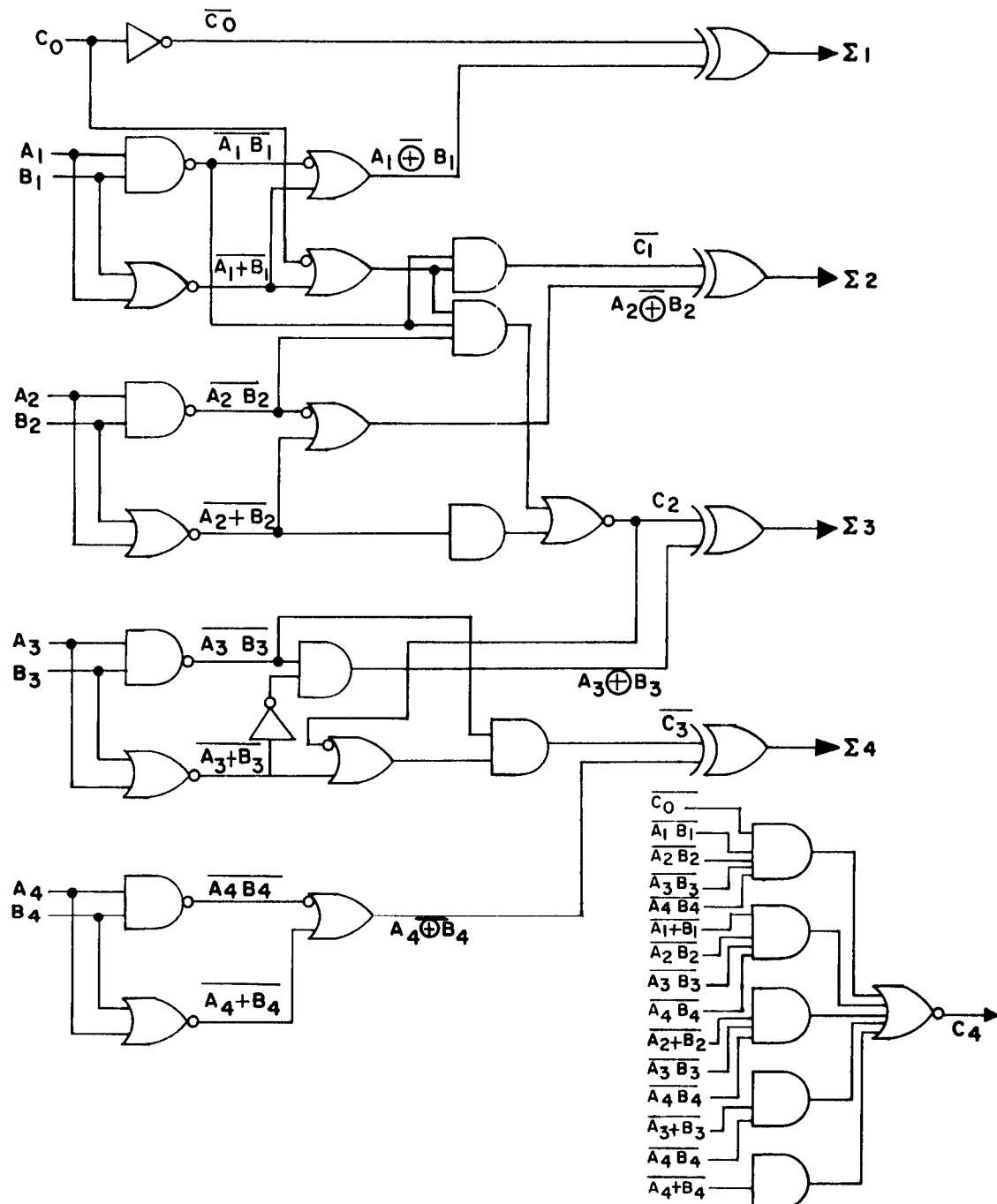


FIGURE 3. Logic diagrams - Continued.

*Device type 03, circuit J.

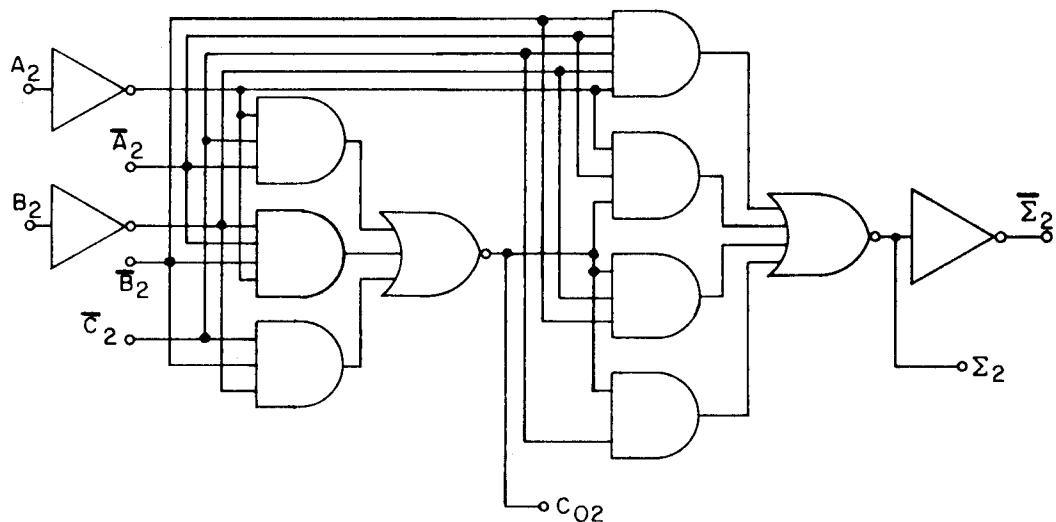
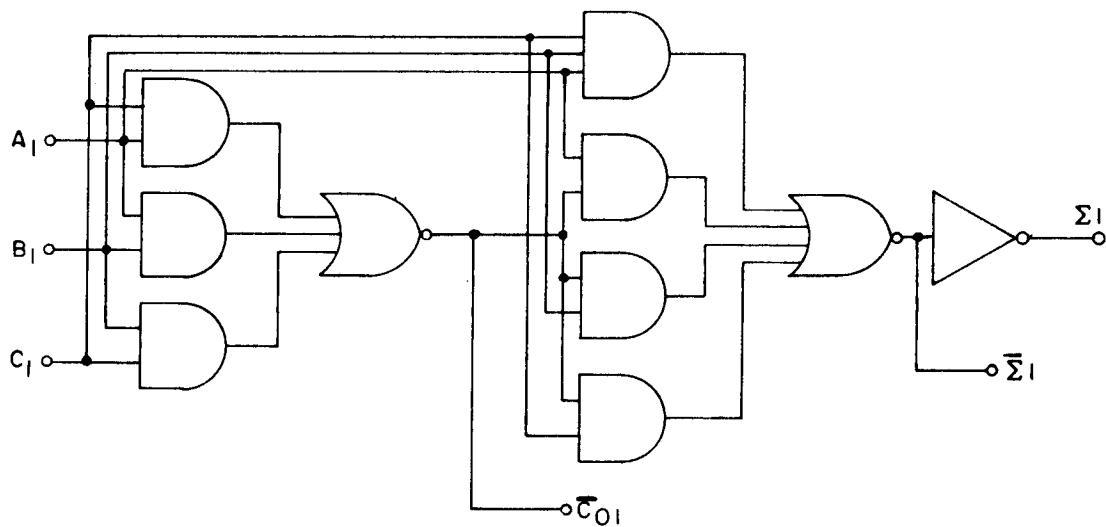


FIGURE 3. Logic diagrams - Continued.

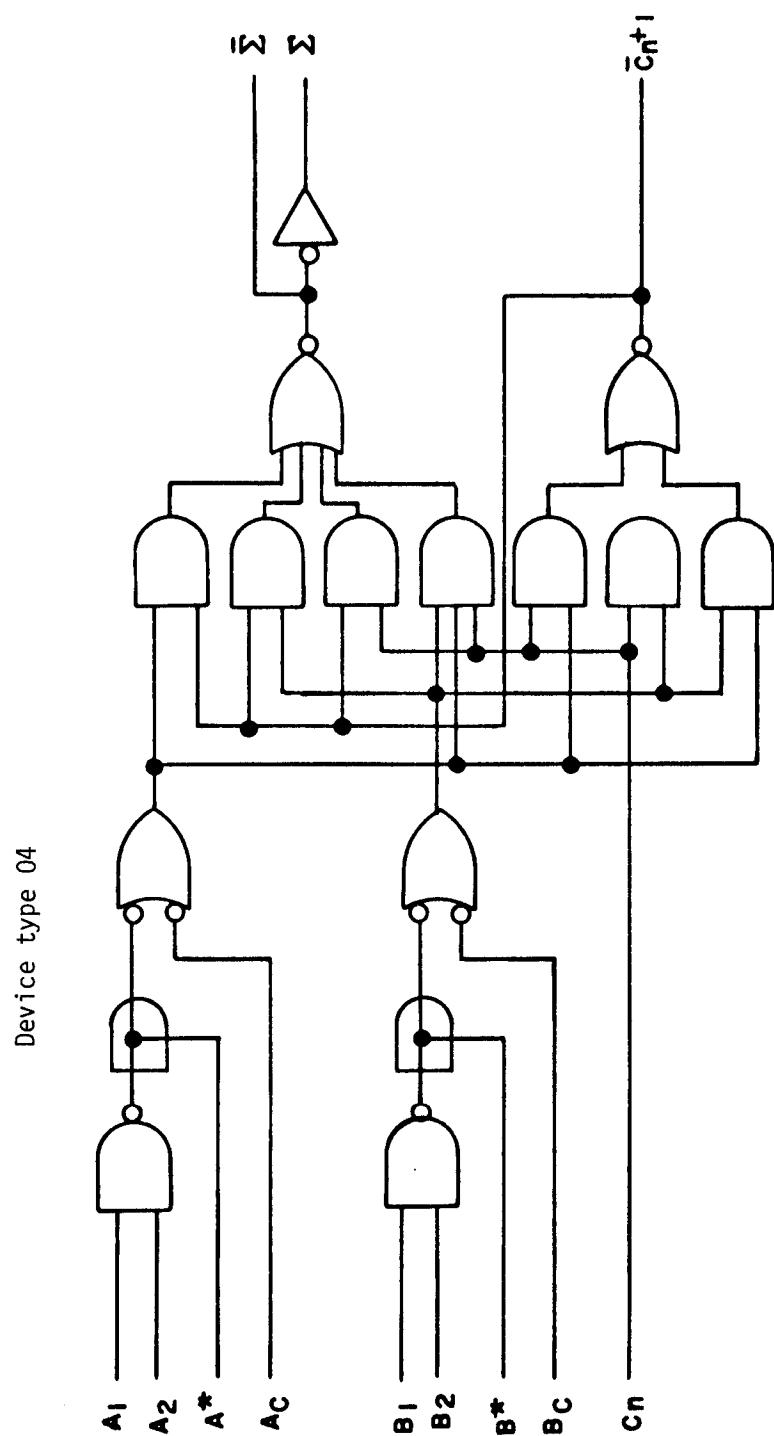
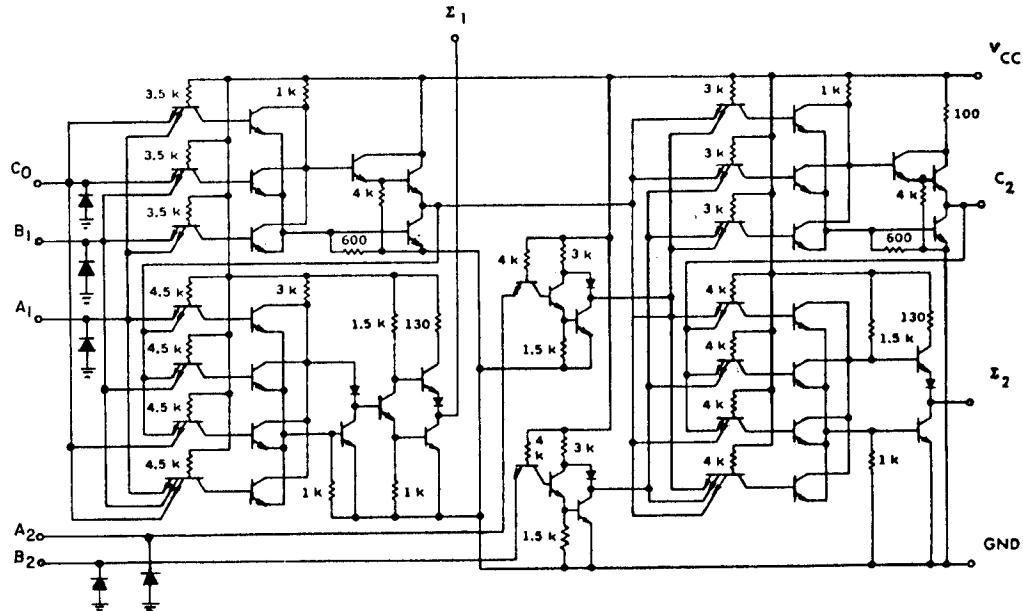


FIGURE 3. Logic diagrams - Continued.

Device type 01, Circuit A



NOTES:

1. Circuits A and B correspond to logic diagrams A and B respectively. These are the only acceptable circuits and logic diagrams for device type 01.
2. Circuits C, G, and H correspond to logic diagram C and circuits D, E, and F correspond to logic diagrams D, E, and F, respectively. These are the only acceptable circuits and logic diagrams for type 02.
3. Circuit J corresponds to logic diagram J. This is the only acceptable circuit and logic diagram for type 03.
4. Component values shown are nominal and resistor values are in ohms.

FIGURE 4. Schematic circuits.

Device type 01, Circuit B

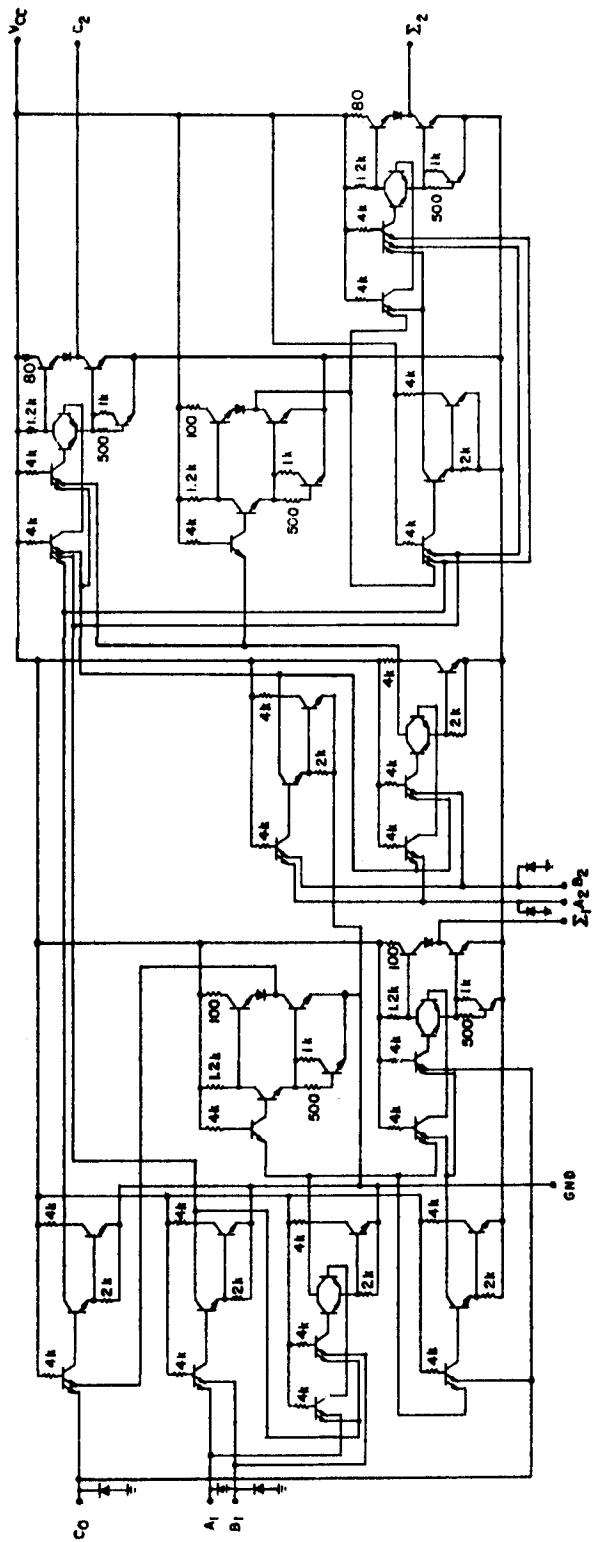
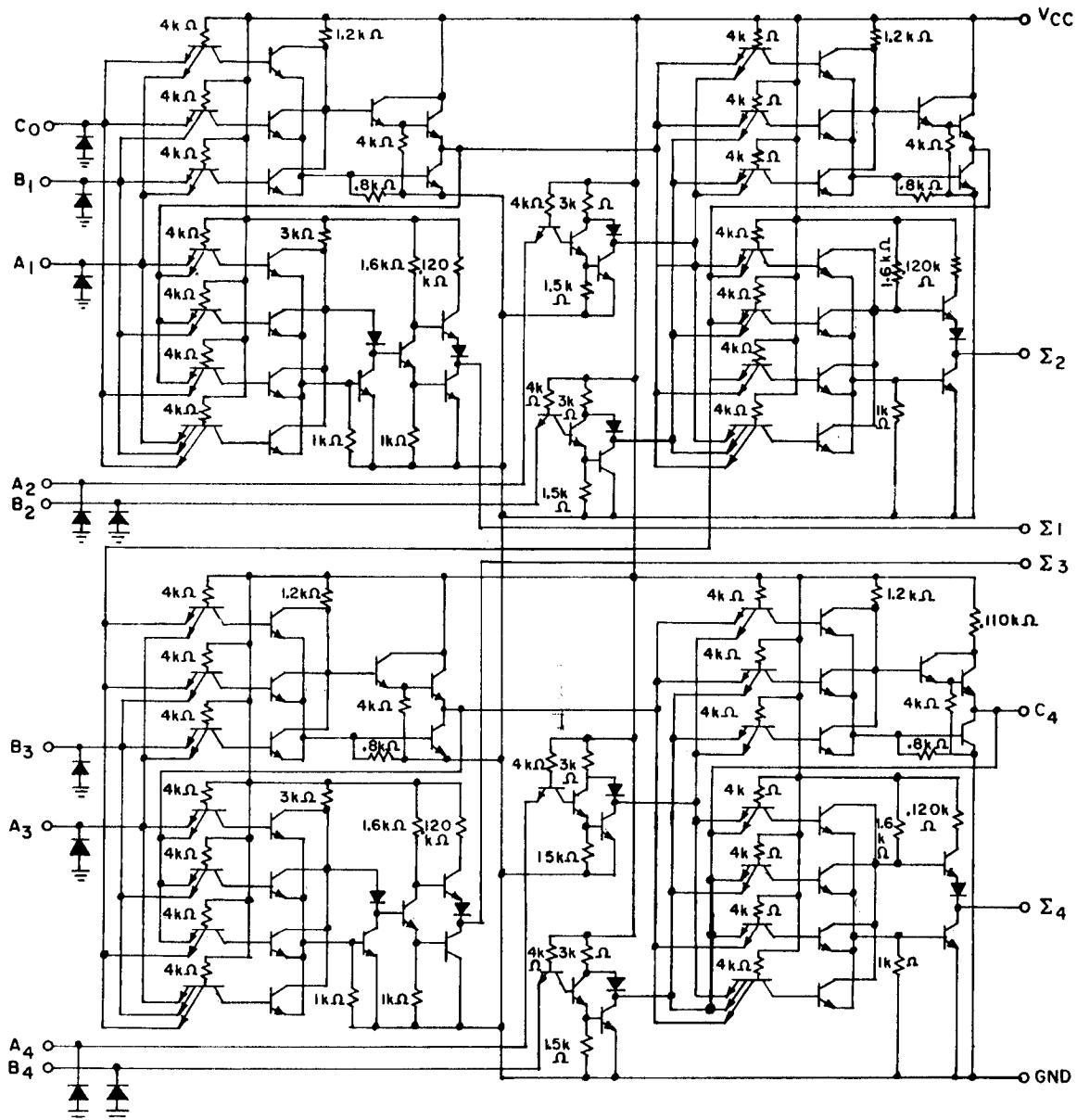


FIGURE 4. Schematic circuits - Continued.

Device type 02, Circuit C

FIGURE 4. Schematic circuits - Continued.

Device type 02, Circuit D

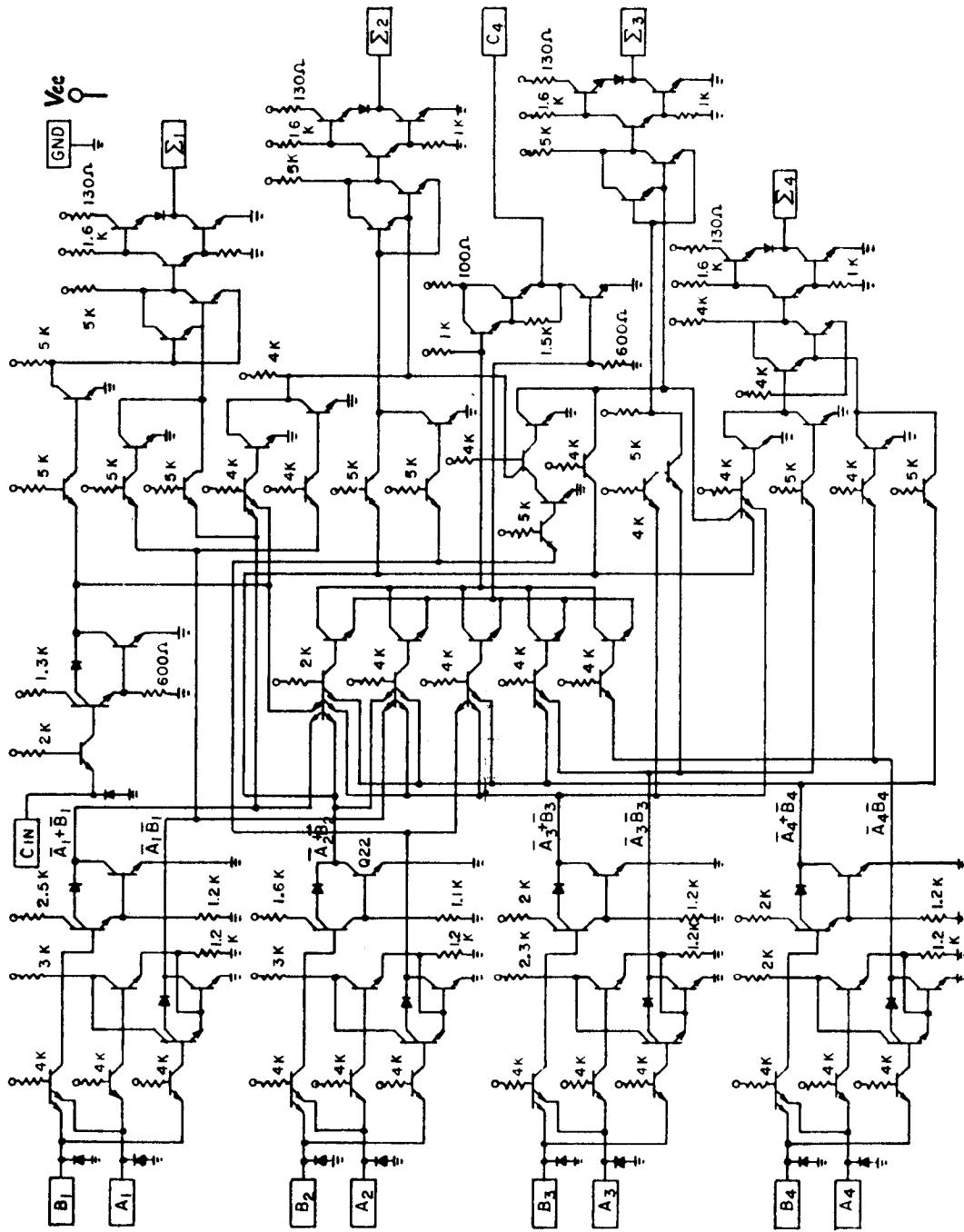


FIGURE 4. Schematic circuits - Continued.

Device type 02, Circuit E.

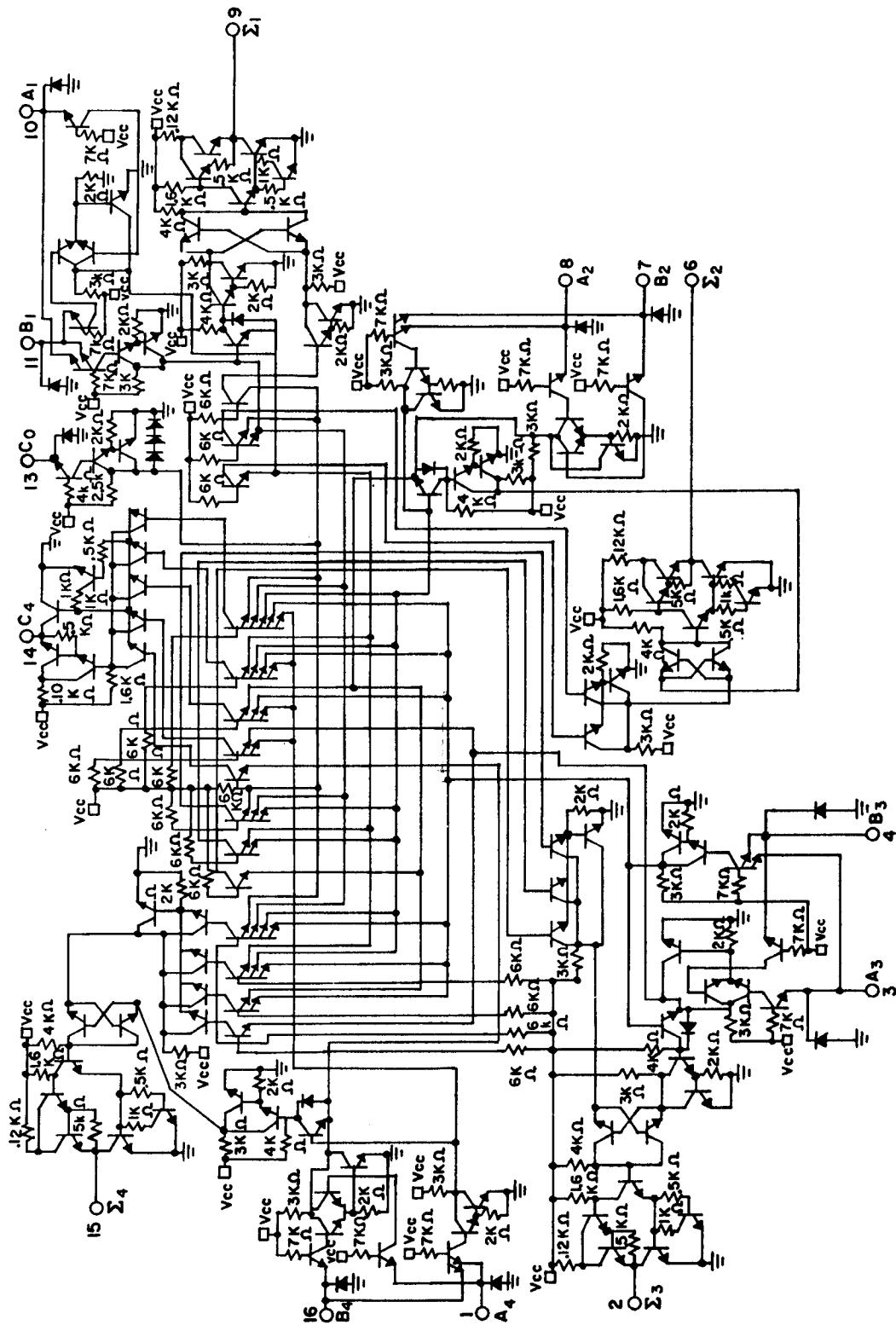
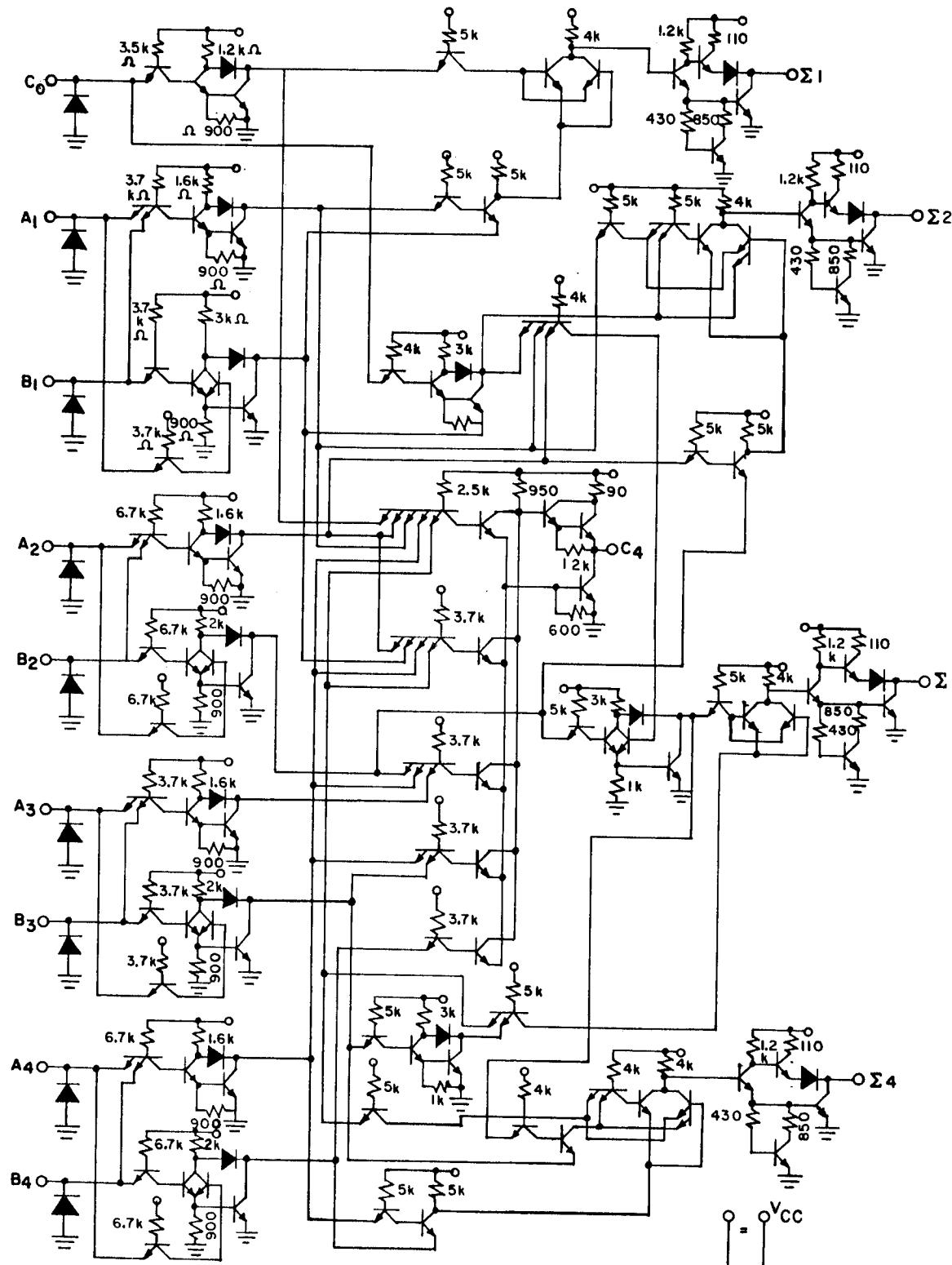


FIGURE 4. Schematic circuits - Continued.

Device type 02, Circuit F

FIGURE 4. Schematic circuits - Continued.

Device type 02, Circuit G

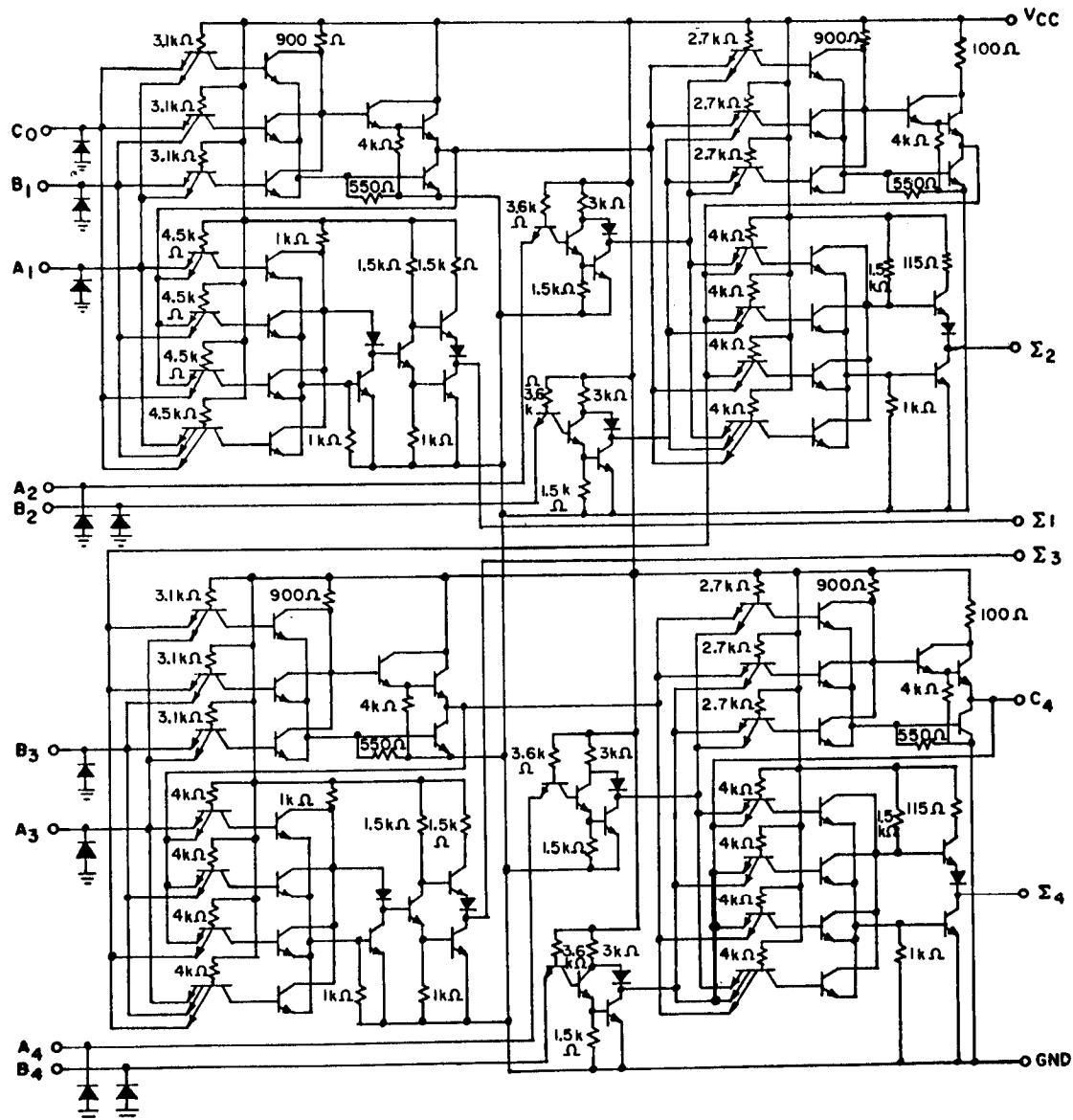


FIGURE 4. Schematic circuits - Continued.

Device type 02, circuit H

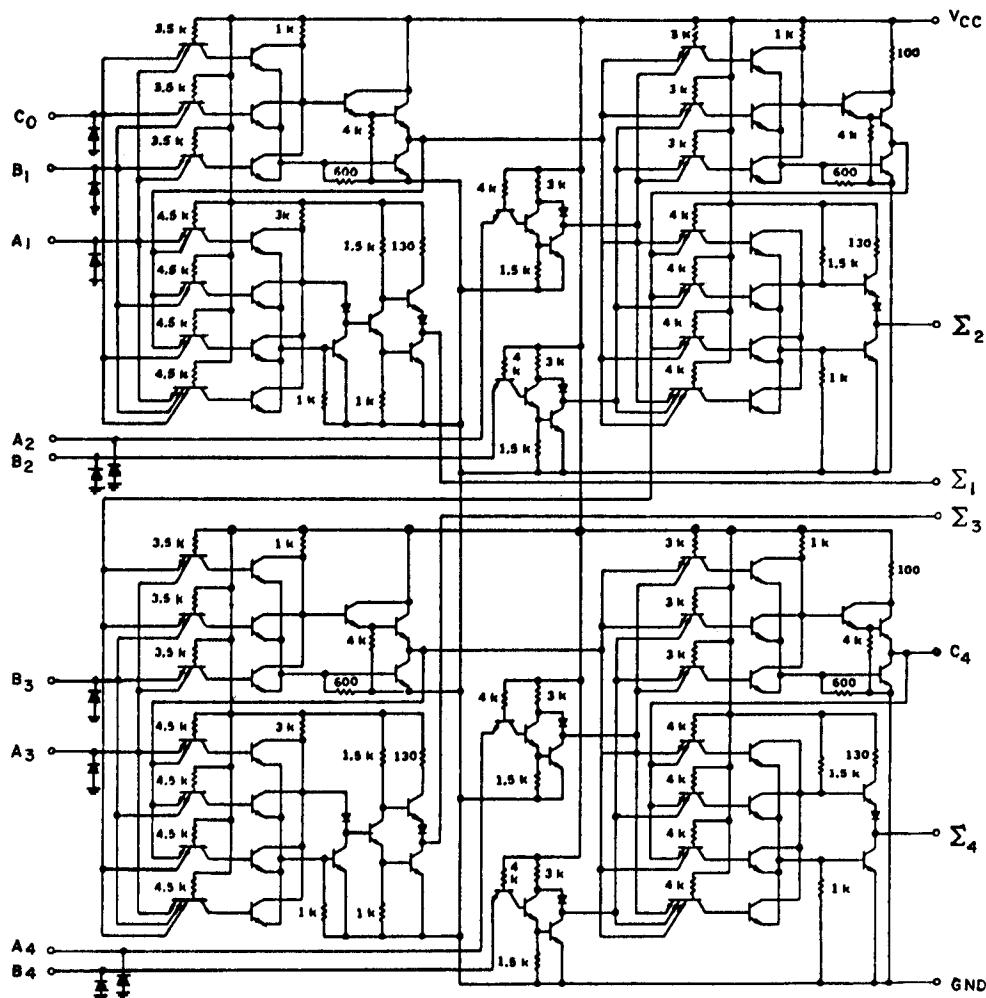


FIGURE 4. Schematic circuits - Continued.

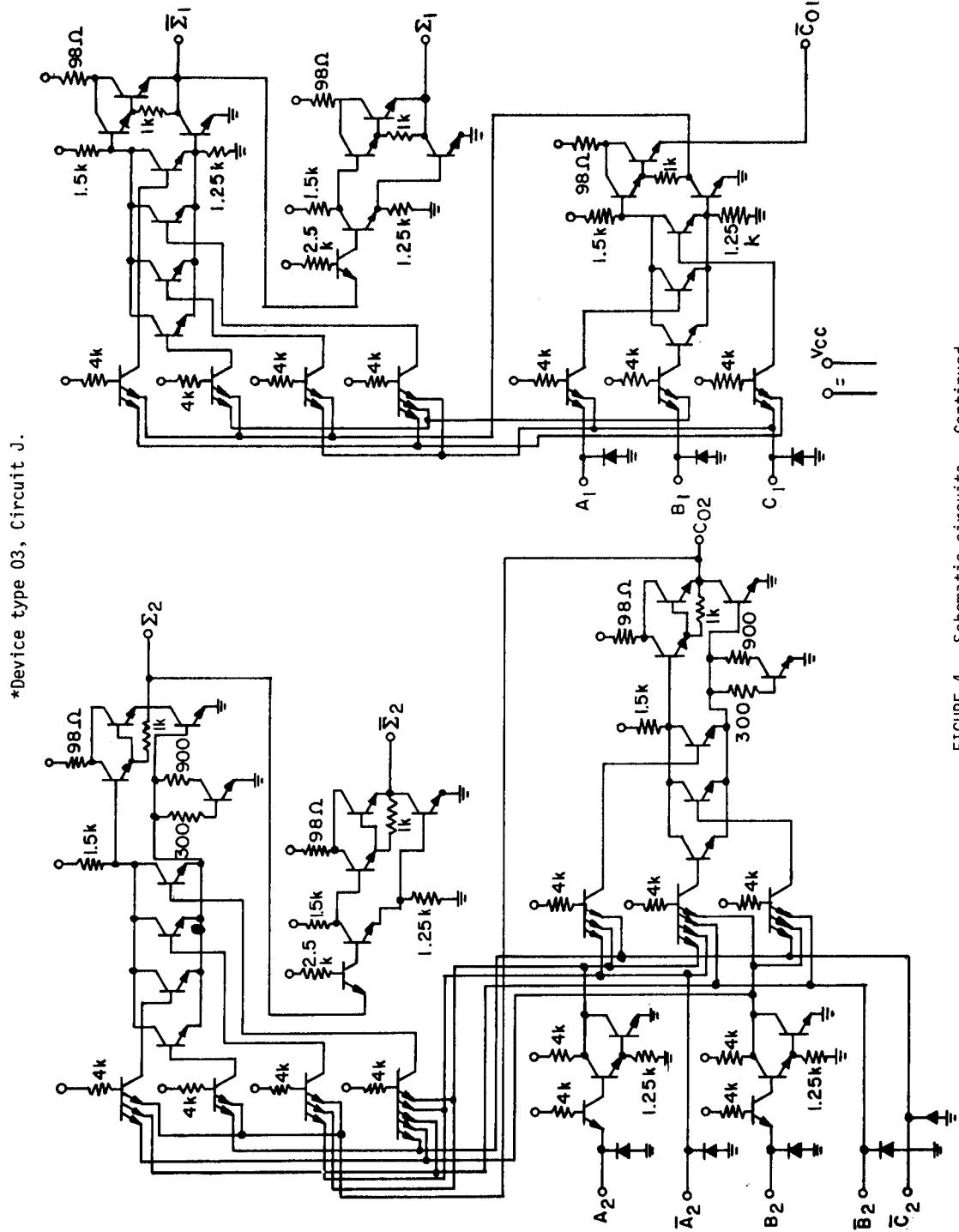


FIGURE 4. Schematic Circuits - Continued.

*Device type 03, Circuit K.

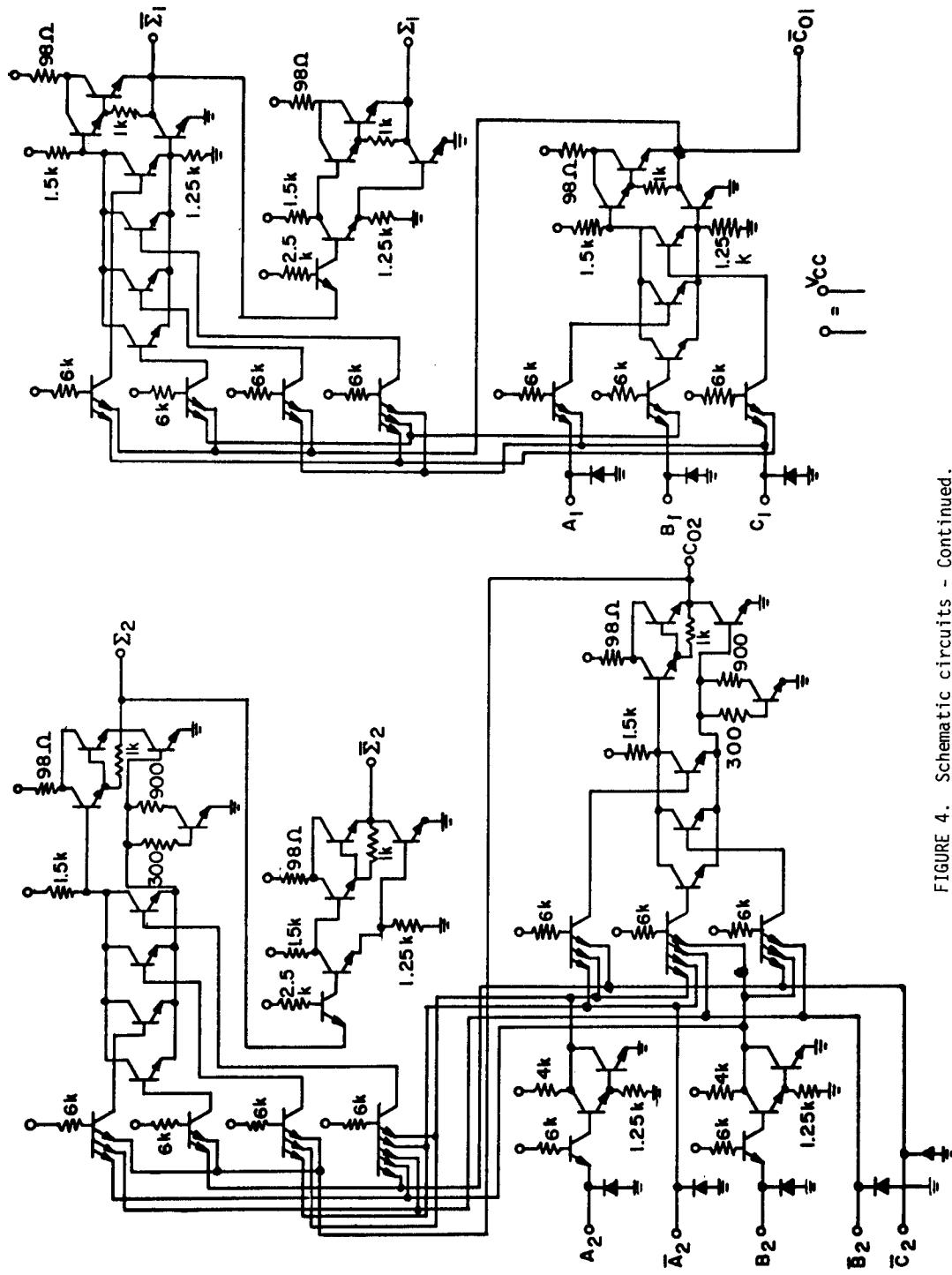


FIGURE 4. Schematic circuits - Continued.

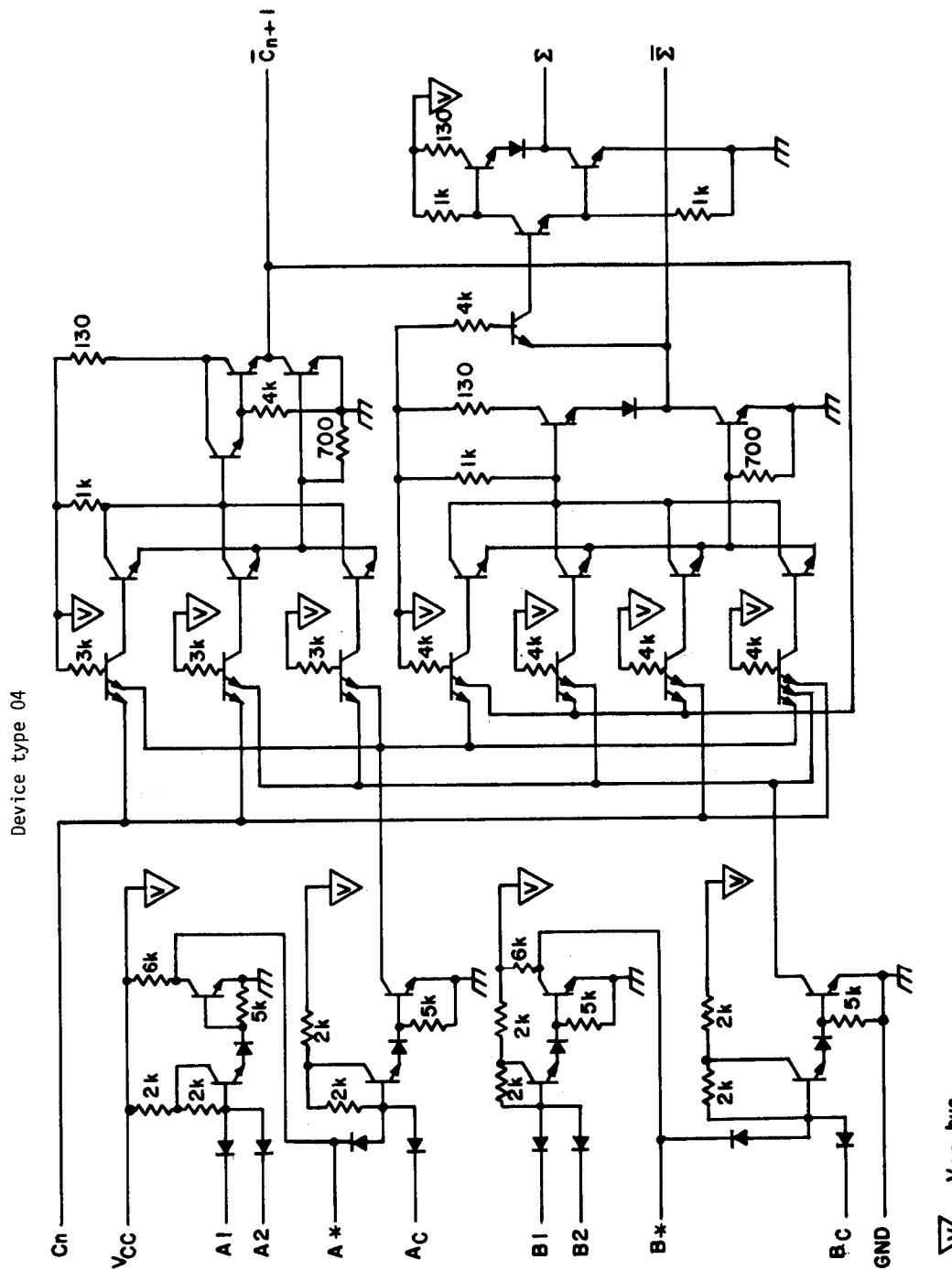
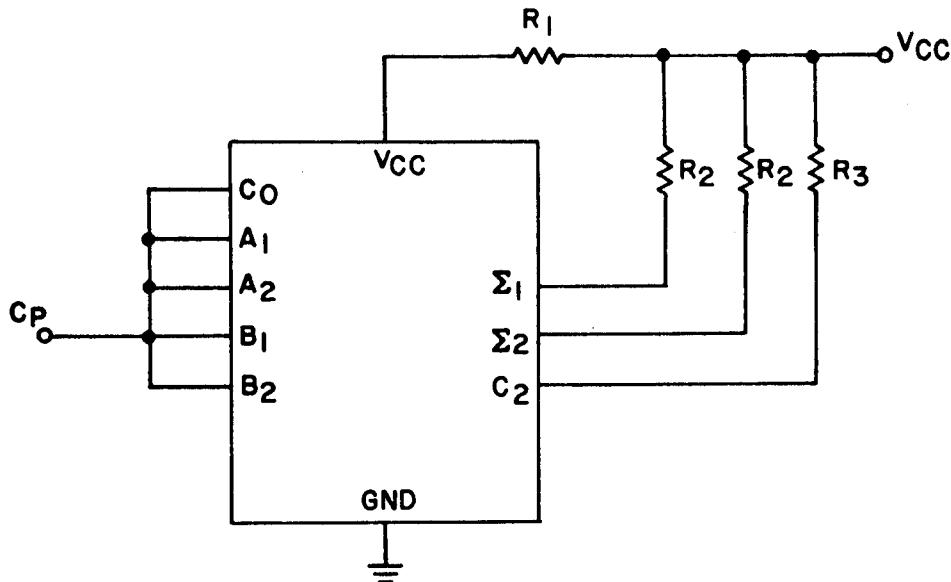


FIGURE 4. Schematic circuits - Continued.

Device type 01

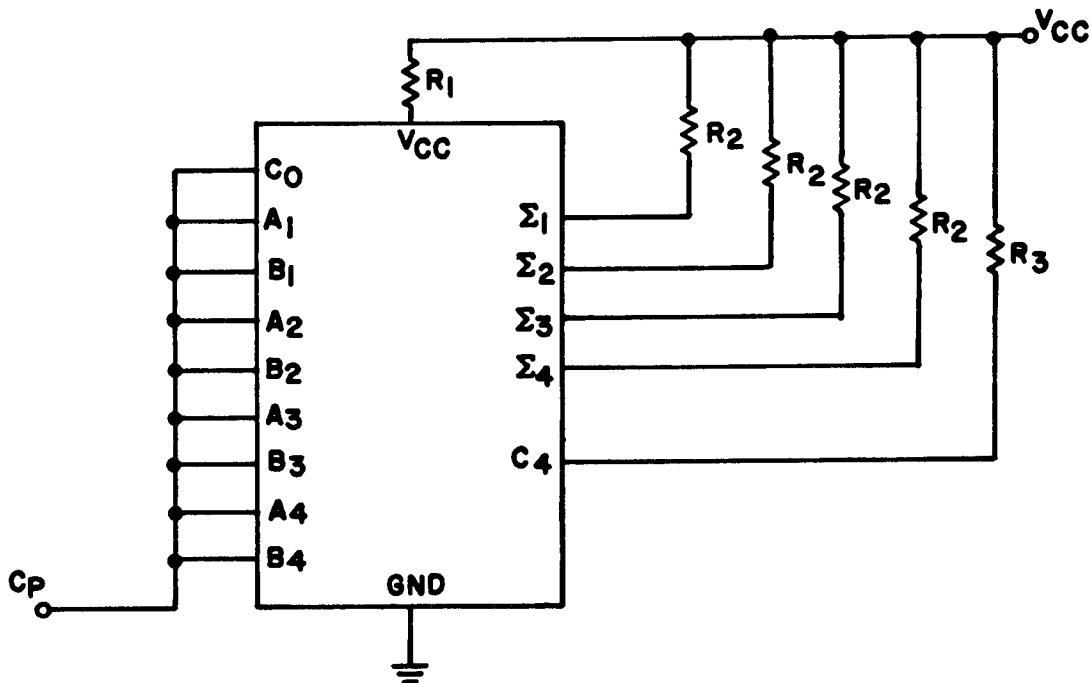


NOTES:

- 1. V_{CC} and R_1 are such that the minimum voltage at the device terminal is 5.0 volts.
- 2. $R_2 = 270\Omega \pm 5\%$.
- 3. $R_3 = 560\Omega \pm 5\%$.
- 4. $CP = 100 \text{ kHz} \pm 50\%$ square wave; duty cycle = $50 \pm 15\%$; $V_{IL} = -0.5 \text{ V to } 0.7 \text{ V}$;
 $V_{IH} = 2.0 \text{ V to } 5.5 \text{ V}$.

FIGURE 5. Burn-in and life test circuits.

Device type 02

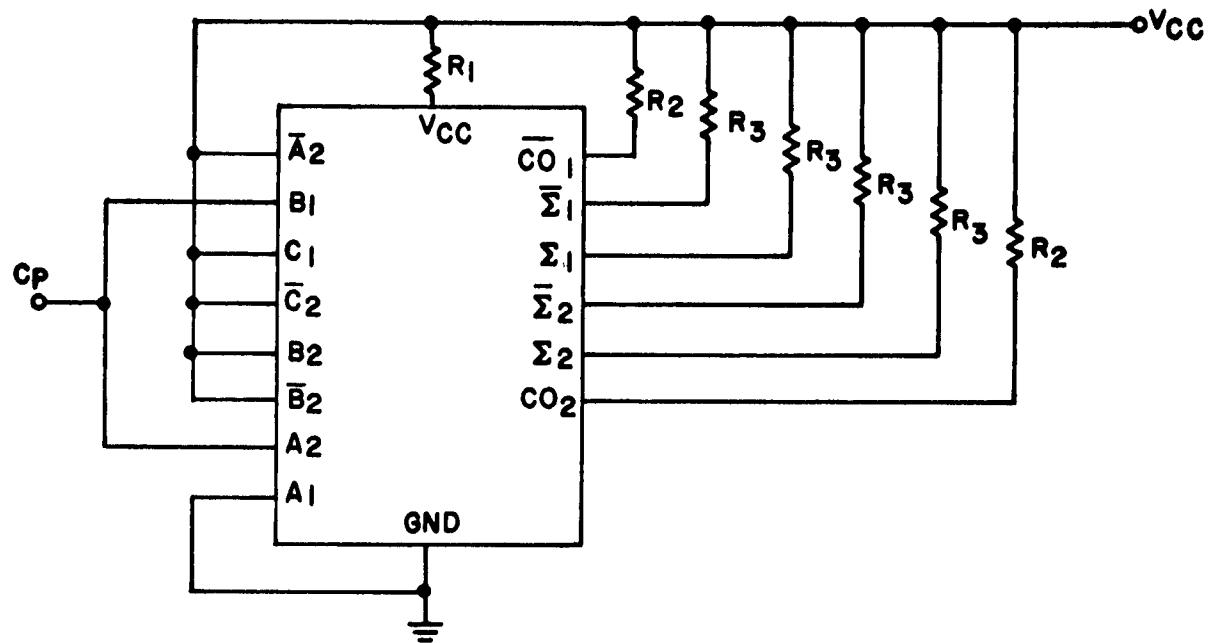


NOTES:

1. V_{CC} and R_1 are such that the minimum voltage at the device terminal is 5.0 volts.
2. $R_2 = 270\Omega \pm 5\%$.
3. $R_3 = 560\Omega \pm 5\%$.
4. $CP = 100 \text{ kHz} \pm 50\%$ square wave; duty cycle = $50 \pm 15\%$; $V_{IL} = -0.5 \text{ V}$ to 0.7 V ;
 $V_{IH} = 2.0 \text{ V}$ to 5.5 V .

FIGURE 5. Burn-in and life test circuits - Continued.

Device type 03

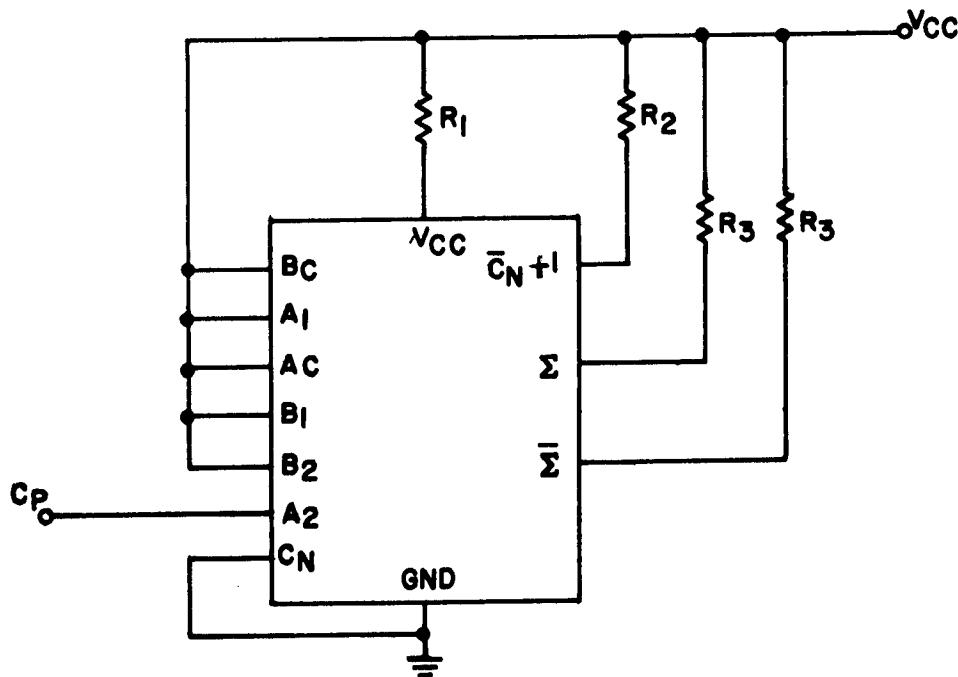


NOTES:

1. V_{CC} and R_1 are such that the minimum voltage at the device terminal is 5.0 volts.
2. $R_2 = 390\Omega \pm 5\%$.
3. $R_3 = 270\Omega \pm 5\%$.
4. $CP = 100$ kHz $\pm 50\%$ square wave; duty cycle = $50 \pm 15\%$; $V_{IL} = -0.5$ V to 0.7 V; $V_{IH} = 2.0$ V to 5.5 V.

FIGURE 5. Burn-in and life test circuits - Continued.

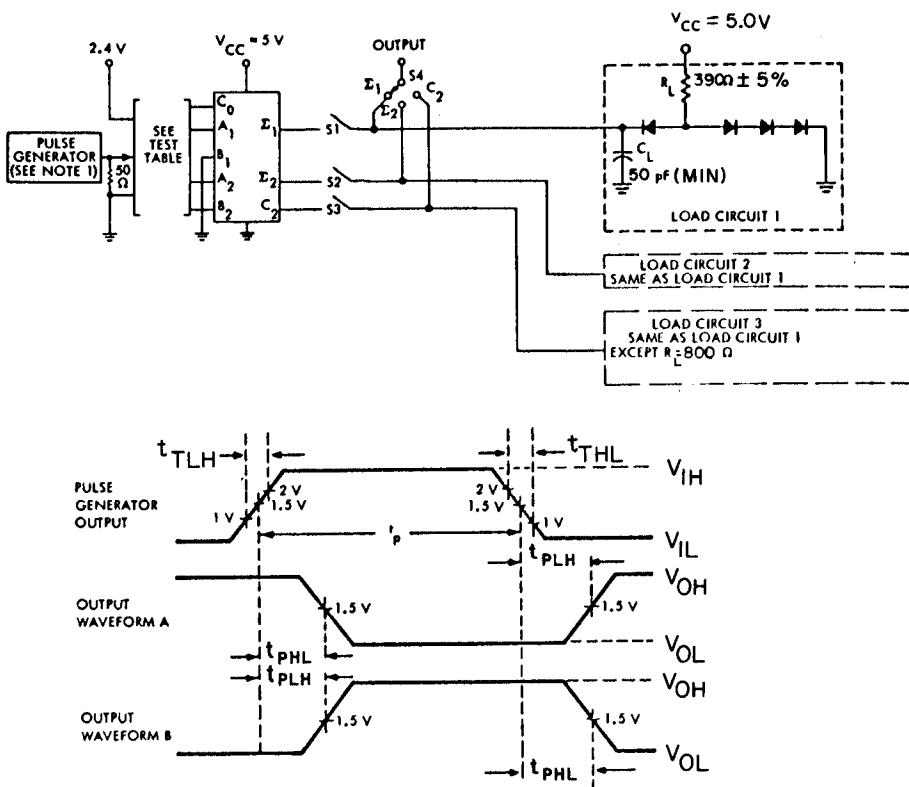
Device type 04



NOTES:

1. R_1 and V_{CC} are such that the minimum voltage at the device terminal is 5.0 volts.
2. $R_2 = 560\Omega \pm 5\%$.
3. $R_3 = 270\Omega \pm 5\%$.
4. $CP = 100 \text{ kHz} \pm 50\%$ square wave; duty cycle = $50 \pm 15\%$; $V_{IL} = -0.5 \text{ V}$ to 0.7 V ; $V_{IH} = 2.0 \text{ V}$ to 5.5 V .

FIGURE 5. Burn-in and life test circuits - Continued.



SWITCHING TIMES TEST TABLE (SEE NOTE 7)							
PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S_4)	APPLY 2.4 V TO	APPLY GND TO	S_1	S_2	S_3
t_{PLH_1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
t_{PHL_1}		Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
t_{PLH_2}	B_2	Σ_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
t_{PHL_2}		Σ_1 (WAVEFORM A)	B_1, B_2	A_1, A_2	OPEN	OPEN	CLOSED
t_{PLH_3}	C_0	Σ_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
t_{PHL_3}		Σ_1 (WAVEFORM A)	B_1, B_2	A_1, A_2	CLOSED	CLOSED	CLOSED
t_{PLH_4}	C_0	Σ_1 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
t_{PHL_4}		Σ_2 (WAVEFORM B)	B_1, B_2	A_1, A_2	CLOSED	CLOSED	CLOSED

NOTES:

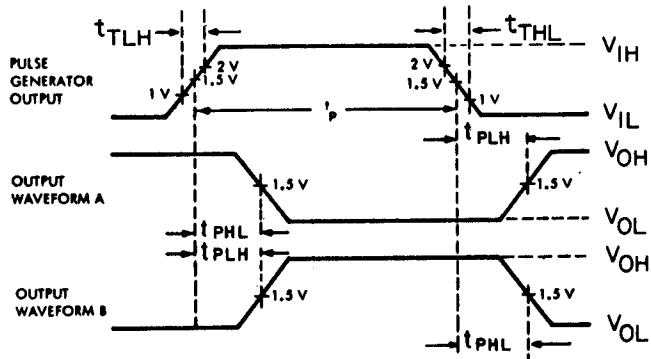
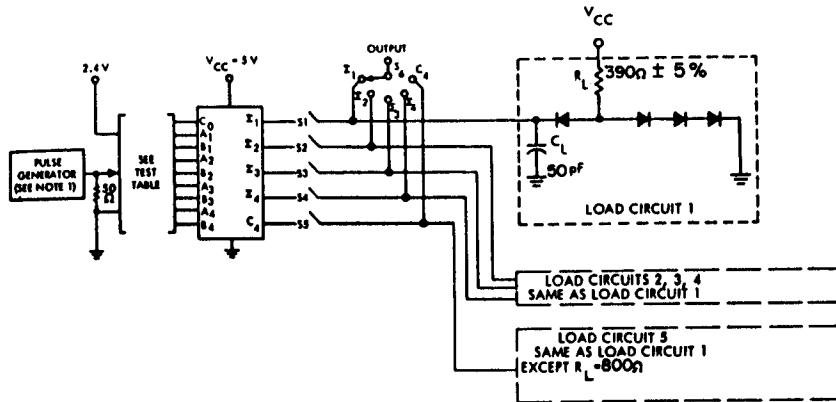
- The generator has the following characteristics: $V_{IH} \geq 2.4V$, $V_{IL} \leq 0.4V$, $t_{TLH} = 8$ to 15 ns, $t_{THL} = 3$ to 5 ns, $PRR = 1$ mHz, $t_p = 200$ ns, and $Z_{out} \approx 50\Omega$.
- Perform test in accordance with test table.
- Each output is tested separately.
- Voltage values are with respect to network ground terminal.
- C_L includes probe and jig capacitance.
- All diodes are 1N3064, or equivalent.
- Inputs and outputs not specified are open.

FIGURE 6. Switching time test circuit - device type 01.

TEST TABLE

PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
t_{PLH_1}	C_0	Σ_1 (WAVEFORM A)	A_1	$B_1, A_2,$ and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
t_{PHL_1}									
t_{PLH_2}	B_2	Σ_2 (WAVEFORM B)	None	$A_1, B_1,$ $A_2,$ and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{PHL_2}									
t_{PLH_3}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{PHL_3}									
t_{PLH_4}	C_0	Σ_3 (WAVEFORM A)	$A_1, A_2,$ and A_3	$B_1, B_2,$ and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
t_{PHL_4}									
t_{PLH_5}	C_0	Σ_4 (WAVEFORM A)	$A_1, A_2,$ A_3 and A_4	$B_1, B_2,$ B_3 , and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
t_{PHL_5}									
t_{PLH_6}	C_0	Σ_4 (WAVEFORM B)	$A_1, A_2,$ A_3 , and A_4	$B_1, B_2,$ B_3 , and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
t_{PHL_6}									
t_{PLH_7}	A_2	Σ_2 (WAVEFORM B)	None	$A_1, B_1,$ $B_2,$ and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{PHL_7}									
t_{PLH_8}	A_4	Σ_4 (WAVEFORM B)	None	$A_3, B_3,$ and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
t_{PHL_8}									
t_{PLH_9}	B_4	Σ_4 (WAVEFORM B)	None	$A_3, B_3,$ and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
t_{PHL_9}									

FIGURE 7. Switching time test circuit - device type 02.



NOTES:

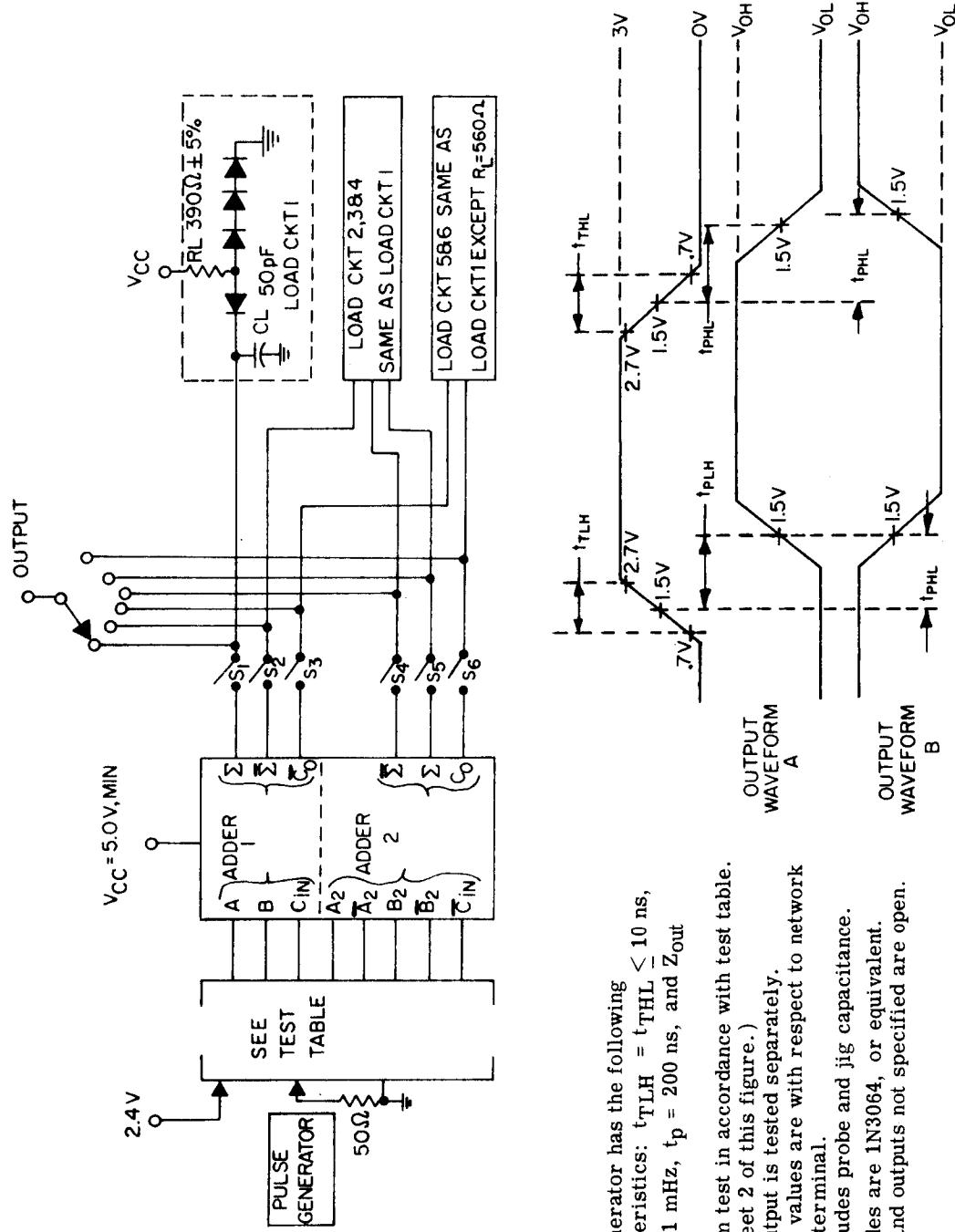
1. The generator has the following characteristics: $V_{IH} \geq 2.4V$, $V_{IL} \leq 0.4V$, $t_{TLH} = 8$ to 15 ns , $t_{THL} = 3$ to 5 ns , $PRR = 1\text{ mHz}$, $t_p = 200\text{ ns}$, and $Z_{out} \approx 50\Omega$.
2. Perform test in accordance with test table. (See sheet 2 of this figure).
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064, or equivalent.
7. Inputs and outputs not specified are open.

FIGURE 7. Switching time test circuit - device type 02 - Continued.

Switching time set up

Para-meter	Apply pulse generator output to	Output under test	Apply 2.4 V to	Apply GND to	S1	S2	S3	S4	S5	S6
tPLH1	C1	(Adder 1) Σ_1 (Wave form) B	A1	B1	Closed	Closed	Closed	Open	Open	Open
tPHL1		(Adder 1) Σ_1 (Wave form) A			Closed	Closed	Closed	Open	Open	Open
tPLH2	C1	(Adder 1) Σ_1 (Wave form) B	A1	B1	Closed	Closed	Closed	Open	Open	Open
tPHL2		(Adder 1) Σ_1 (Wave form) A			Closed	Closed	Closed	Open	Open	Open
tPLH3	C1	(Adder 1) C_{O1} (Wave form) B	A1	B1	Closed	Closed	Closed	Open	Open	Open
tPHL3		(Adder 1) C_{O1} (Wave form) A			Closed	Closed	Closed	Open	Open	Open
tPLH4	A2	(Adder 2) Σ_2 (Wave form) A	C_2 \bar{A}_2, \bar{C}_{IN2}	B_2, \bar{B}_2	Open	Open	Open	Closed	Closed	Closed
tPHL4		(Adder 2) Σ_2 (Wave form) A			Open	Open	Open	Closed	Closed	Closed
tPLH5	A2	(Adder 2) Σ_2 (Wave form) B	C_2 \bar{A}_2, \bar{C}_{IN2}	B_2, \bar{B}_2	Open	Open	Open	Closed	Closed	Closed
tPHL5		(Adder 2) Σ_2 (Wave form) B			Open	Open	Open	Closed	Closed	Closed
tPLH6	A2	(Adder 2) C_{O2} (Wave form) A	C_2 \bar{A}_2, \bar{C}_{IN2}	B_2, \bar{B}_2	Open	Open	Open	Closed	Closed	Closed
tPHL6		(Adder 2) C_{O2} (Wave form) A			Open	Open	Open	Closed	Closed	Closed

*FIGURE 8. Switching time test circuit - device type 03.



*FIGURE 8. Switching time test circuit - device type 03 - Continued.

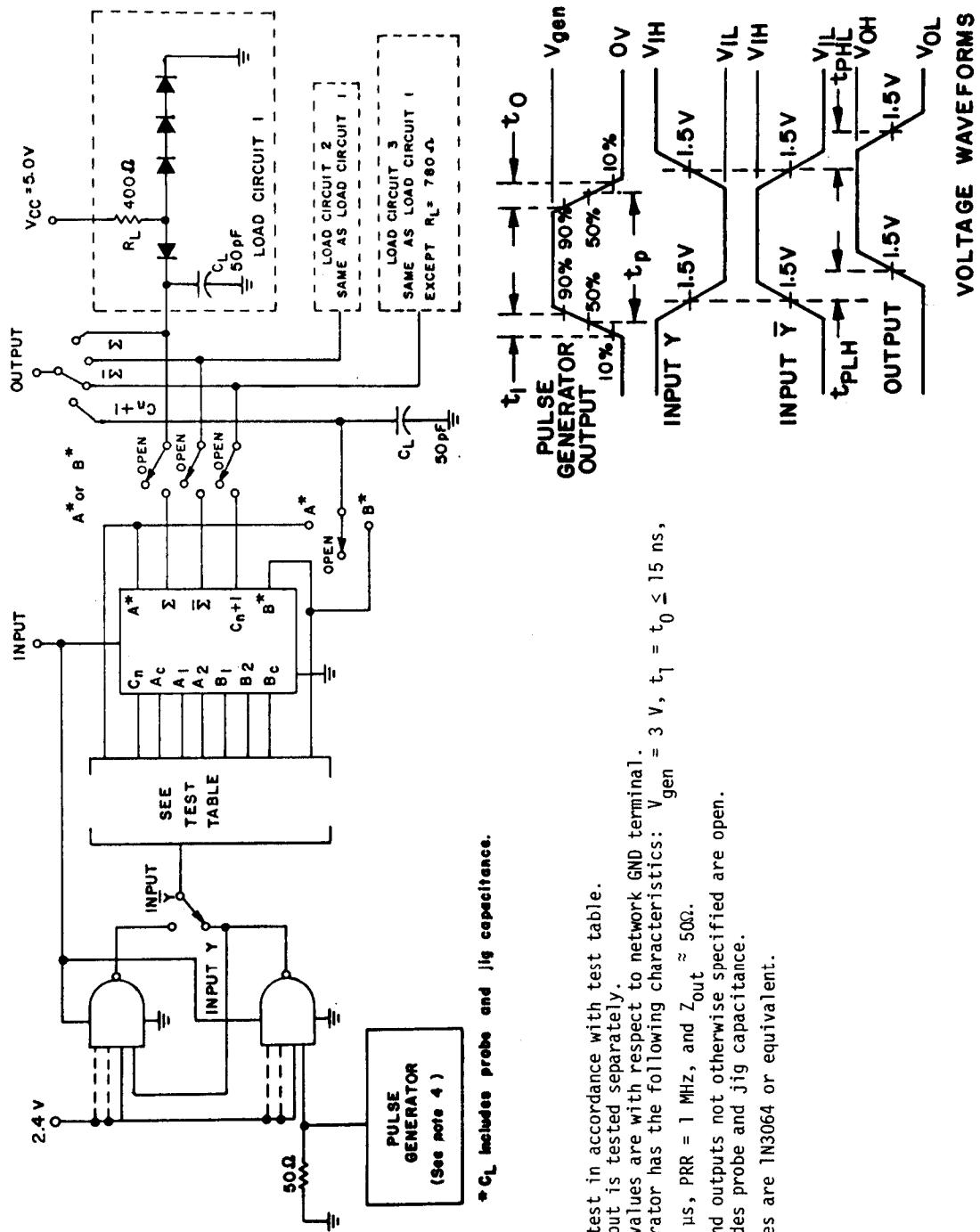


FIGURE 9. Switching time test circuit - device type 04.

TEST TABLE (SEE NOTE 5)

TEST NO.	SYMBOL	OUTPUT UNDER TEST	APPLY INPUT TO Y	APPLY INPUT Y TO	APPLY +2.4V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
64,76	t_{PHL1}	$C_n + I$	NONE	C_n	NONE	B_1	$C_n + I$ (Load circuit 3)
65,77	t_{PLH1}	$C_n + I$	NONE	C_n	NONE	B_1	$C_n + I$ (Load circuit 3)
66,78	t_{PHL2}	$C_n + I$	B_c	NONE	C_n	A_1, B_1	$C_n + I$ (Load circuit 3)
67,79	t_{PLH2}	$C_n + I$	B_c	NONE	C_n	A_1, B_1	$C_n + I$ (Load circuit 3)
							Σ (Load circuit 2)
68,80	t_{PHL3}	Σ	A_c	NONE	C_n	A_1, B_1	Σ (Load circuit 1)
							$C_n + I$ (Load circuit 3)
69,81	t_{PLH3}	Σ	A_c	NONE	C_n	A_1, B_1	Σ (Load circuit 1)
							Σ (Load circuit 2)
							$C_n + I$ (Load circuit 3)
70,82	t_{PHL4}	$\bar{\Sigma}$	B_c	NONE	C_n	B_1	Σ (Load circuit 2)
71,83	t_{PLH4}	$\bar{\Sigma}$	B_c	NONE	C_n	B_1	Σ (Load circuit 2)
72,84	t_{PHL5}	A^*	NONE	A_1	A_2	NONE	$A^* \quad C_L = 50 \text{ pF}$
73,85	t_{PLH5}	A^*	NONE	A_1	A_2	NONE	$A^* \quad C_L = 50 \text{ pF}$
74,86	t_{PHL6}	B^*	NONE	B_1	B_2	NONE	$B^* \quad C_L = 50 \text{ pF}$
75,87	t_{PLH6}	B^*	NONE	B_1	B_2	NONE	$B^* \quad C_L = 50 \text{ pF}$

FIGURE 9. Switching time test circuit - device type 04 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be H > 2.0 V; L < 0.8 V; or open)

See footnotes at end of device type 02.

Some tests terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ\text{C}$ and VIC tests are omitted.

some tests terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ\text{C}$ and V_{IC} tests are omitted.

TABLE III. Group A inspection for device type 01 - Continued.
 Terminal conditions (bins not designated may be H > 2.0 V; L < 0.8 V; or open)

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notes at end of device time 02

See footnotes at end of device type U2.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be H \geq 2.0 V; L \leq 0.8 V; or open)

Subgroup	Symbol	ML- STD-883 method	Case E, F												Test limits								
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Min	Max	Unit	
$T_A = 25^\circ C$	V_{OH}	3006	1	2.0 v		A3	B3	VCC	$\Sigma 2$	B2	A2	$\Sigma 1$	A1	B1	GND	C0	C4	$\Sigma 4$	B4	2.0 v	2.4	--	v
	V_{OL}	3007	2	-0.4mA															$\Sigma 2$	$\Sigma 3$	2.4	--	0.4
			3																$\Sigma 1$	$\Sigma 2$	2.4	--	0.4
			4																$\Sigma 3$	$\Sigma 4$	2.4	--	0.4
			5																$\Sigma 1$	$\Sigma 2$	2.4	--	0.4
			6	0.8 v	2.0 v			4.5 v		2.0 v	2.0 v		-0.4mA						0.8 v	0.8 v	0.8 v	0.8 v	0.8 v
			7	16 mA																-0.2mA	-0.4mA	-0.4mA	-0.4mA
			8																				
			9																				
			10																				
$T_A = 125^\circ C$	V_{IC}	11	-12 mA																				
		12																					
		13																					
		14																					
		15																					
		16																					
		17																					
		18																					
		19																					
		20																					
$T_A = 150^\circ C$	I_{IH1}	3010	21																				
		22																					
		23																					
		24																					
		25																					
		26																					
		27																					
		28																					
		29																					
		30																					
$T_A = 175^\circ C$	I_{IH2}	3010	31																				
		32																					
		33																					
		34																					
		35																					
		36																					
		37																					
		38																					
		39																					
		40																					

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V; L \leq 0.8 V; or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas.	Test limits	
			Test No.	A4	S3	A3	B3	VCC	S2	B2	A2	S1	A1	B1	GND	C0	C4	S4	B4	terminal	Min	Max	Unit
1	I _{H1}	3009	38 CKT C,G,H		0.4 v	0.8 v	5.5 v		5.5 v					GND					A3	-2.3	-6.4	mA	
			38 CKT D		0.4 v	5.5 v													A3	-1.4	-3.2		
			38 CKT E		0.4 v	5.5 v													A3	-0.8	-2.6		
			38 CKT F		0.4 v	5.5 v													A3	-1.4	-3.2		
			39 CKT D		0.8 v	0.4 v													B3	-2.3	-6.4		
			39 CKT E		5.5 v	0.4 v													B3	-1.4	-3.2		
			39 CKT F		5.5 v	0.4 v													B3	-0.8	-2.6		
			40 CKT C,G,H		5.5 v	0.4 v													A1	-1.4	-3.2		
			40 CKT D																A1	-0.8	-2.6		
			40 CKT E																A1	-1.4	-3.2		
			40 CKT F																B1	-2.3	-6.4		
			41 CKT C,G,H																B1	-1.4	-3.2		
			41 CKT D																B1	-0.8	-2.6		
			41 CKT E																B1	-1.4	-3.2		
			41 CKT F																C0	-2.1	-6.4		
			42 CKT C																C0	-0.7	-1.6		
			42 CKT D																C0	-1.4	-3.2		
			42 CKT E																C0	-0.7	-1.6		
			42 CKT F																C0	-1.4	-3.2		
			42 CKT G, H																C0	-2.1	-4.8		
	I _{H2}		43 CKT C,G,H	0.4 v															c	5.5 v	A4	-0.7	-1.6
			43 CKT D	0.4 v															A4	-1.4	-3.2		
			43 CKT E	0.4 v															A4	-0.8	-2.6		
			43 CKT F	0.4 v															B2	-0.7	-1.6		
			44 CKT C,G,H																B2	-1.4	-3.2		
			44 CKT D																B2	-0.8	-2.6		
			44 CKT E																B2	-0.8	-2.6		
			44 CKT F																B2	-0.8	-2.6		
			45 CKT C,G,H																A2	-0.7	-1.6		
			45 CKT D																A2	-1.4	-3.2		
			45 CKT E																A2	-0.8	-2.6		
			45 CKT F																A2	-0.7	-1.6		
			46 CKT C,G,H	5.5 v															B4	-1.4	-3.2		
			46 CKT D	5.5 v															B4	-0.8	-2.6		
			46 CKT E																B4	-0.8	-2.6		
			46 CKT F																B4	-0.8	-2.6		
	I _{OS1}	3011	47	4.5 v	4.5 v	GND	4.5 v	4.5 v											4.5 v	Z3	-20	-35	
			48																Z22				
			49																Z21				
			50																Z24				
			51																C4	-20	-70		
	I _{OS2}																						
	IC _C	3005	52 CKTC, E, G, H	4.5 v	4.5 v	GND	4.5 v	4.5 v											GND	VCC	---	100	
			52 CKTD, F	4.5 v	4.5 v	GND	4.5 v	4.5 v										GND	VCC	---	80		

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 -Continued.

		Terminal conditions (pins not designated may be H \geq 2.0 V; L \leq 0.8 V, or open)												Test limits																																																					
Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	C4	B4	Σ4	C0	C4	B1	B2	A2	B3	A3	Σ3	A4	Test No.	Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	C4	B4	Σ4	C0	C4	B1	B2	A2	B3	A3	Σ3	A4	Test No.
2			Same tests, terminal conditions and limits as for subgroup 1, except TA = -55°C and VIC tests are omitted.																																																																
3			Same tests, terminal conditions and limits as for subgroup 1, except TA = -55°C and VIC tests are omitted.																																																																
$T_A = 25^\circ\text{C}$			53	L 1/	0.8v3/	0.8v3/	4.5 v	L 1/	0.8v3/	0.8v3/	L 1/	0.8v3/	GND	0.8v3/	0.8v3/	L 1/	0.8v3/	All outputs	H or L as shown 1/																																																
			54	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			55	L	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			56	L	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			57	L	0.8 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			58	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			59	H	0.8 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			60	H	2.0 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			61	0.8 v	L	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			62	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			63	H	0.8 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			64	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			65	H	0.8 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			66	L	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			67	L	0.8 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			68	H	2.0 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			69	0.8 v	L	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			70	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			71	H	0.8 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			72	L	2.0 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			73	2.0 v	L	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			74	L	0.8 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			75	H	0.8 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			76	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			77	0.8 v	L	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			78	L	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			79	L	0.8 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			80	H	2.0 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			81	2.0 v	L	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			82	L	0.8 v	0.8 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			83	L	2.0 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				
			84	H	2.0 v	2.0 v	H	L	H	2.0 v	H	2.0 v	H	2.0 v	2.0 v	H	2.0 v	L	L	L	L	L	L	L	L	L	L	L	L	L	L																																				

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See footnotes at end of device type 02.

Same tests, terminal conditions and limits as for subgroup 7, except $T_A = 125$ and -55°C .

TABLE III. Group A inspection for device type 02 - Continued.
 Final conditions (pins not designated may be $H \geq 2.0\text{ V}$; $L \leq 0.8\text{ V}$; or open)

Subgroup	Symbol	ML-STD-883 method	Test No.	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas.			Test limits		
																					terminal	Min	Max	Unit		
$T_A = 25^\circ C$	tPHL1	3003	85																		C0 to $\Sigma 1$	3	37	ns		
	tPLH1		86																		C0 to $\Sigma 1$	44	44			
	tPHL2		87																		B2 to $\Sigma 2$	41	41			
	tPLH2		88																		B2 to $\Sigma 2$	36	36			
	tPHL3		89																		C0 to $\Sigma 2$	42	42			
	tPLH3		90																		C0 to $\Sigma 2$	47	47			
	tPHL4		91																		C0 to $\Sigma 3$	55	55			
	tPLH4		92																		C0 to $\Sigma 3$	66	66			
	tPHL5		93																		C0 to $\Sigma 4$	61	61			
$T_A = 125^\circ C$	tPHL6		94																		C0 to $\Sigma 4$	54	54			
	tPLH6		95																		A2 to $\Sigma 2$	40	40			
	tPHL7		96																		A2 to $\Sigma 2$	41	41			
	tPLH7		97																		A2 to $\Sigma 2$	36	36			
	tPHL8		98																		A4 to $\Sigma 4$	41	41			
	tPLH8		99																		A4 to $\Sigma 4$	36	36			
	tPHL9		100																		B4 to $\Sigma 4$	41	41			
	tPLH9		101																		B4 to $\Sigma 4$	36	36			
	tPHL9		102																		C0 to $\Sigma 1$	3	39			
$T_A = 125^\circ C$	tPHL1		103																		B2 to $\Sigma 1$	51	51			
	tPLH1		104																		B2 to $\Sigma 2$	45	45			
	tPHL2		105																		B2 to $\Sigma 2$	40	40			
	tPLH2		106																		C0 to $\Sigma 2$	51	51			
	tPHL3		107																		C0 to $\Sigma 2$	54	54			
	tPLH3		108																		C0 to $\Sigma 3$	62	62			
	tPHL4		109																		C0 to $\Sigma 3$	77	77			
	tPLH4		110																		C0 to $\Sigma 4$	72	72			
	tPHL5		111																		C0 to $\Sigma 4$	71	71			
$T_A = 125^\circ C$	tPLH6		112																		C0 to $\Sigma 4$	63	63			
	tPHL6		113																		C0 to $\Sigma 4$	55	55			
	tPLH6		114																		A2 to $\Sigma 2$	45	45			
	tPHL7		115																		A2 to $\Sigma 2$	40	40			
	tPLH7		116																		A4 to $\Sigma 4$	45	45			
	tPHL7		117																		A4 to $\Sigma 4$	40	40			
	tPLH8		118																		E4 to $\Sigma 4$	45	45			
	tPHL8		119																		E4 to $\Sigma 4$	40	40			
	tPLH9		120																		C0 to $\Sigma 4$	40	40			

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1/ Output voltages shall be either: (a) $H = 2.4$ V, minimum and $L = 0.4$ V, maximum when using a high speed checker double comparator; or (b) $H \geq 1.5$ V and $L < 1.5$ V when using a high speed shadow timer comparator.

2/ Only a summary of attributes data is required to speed the checker single comparator.

Only a summary of attributes data is required.

Input voltages shown are the maximum for V_L and Circuit B limits for I_{os} shall be -70 mA max.

5/ "GND" when testing for circuit D, E, F, G and H.

6/ Substitute "Open" for circuit F

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TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated may be H \geq 2.0 V; L \leq 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 Test No.	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits
				A2	A1	B1	C1	$\bar{C}01$	$\Sigma 1$	GND	$\bar{\Sigma}2$	$\Sigma 2$	C02	$\bar{C}2$	B2	A2	$\bar{B}2$	VCC	Meas. terminal	Min
TA = 25°C	VOH	3006	1	2.0 v	0.8 v	0.8 v	-560 μ A			GND							4.5 v	$\bar{C}01$	2.4	v
			2	2.0 v	0.8 v	0.8 v	-560 μ A										0.8 v	$\Sigma 1$		
			3	2.0 v	2.0 v		-800 μ A										0.8 v	$\bar{C}02$		
			4	0.8 v	2.0 v												0.8 v	$\Sigma 2$		
			5	2.0 v													0.8 v	$\bar{\Sigma}2$		
			6	2.0 v													0.8 v	$\Sigma 2$		
	VOL	3007	7	0.8 v	2.0 v	2.0 v	8 mA	16 mA	16 mA								0.8 v	$\bar{C}01$	---	0.4
			8	2.0 v	0.8 v	0.8 v	0.8 v										0.8 v	$\Sigma 1$		
			9	0.8 v	0.8 v												0.8 v	$\bar{C}02$		
			10	2.0 v													0.8 v	$\Sigma 2$		
III.1			11	2.0 v													0.8 v	$\bar{\Sigma}2$		
			12	0.8 v													0.8 v	$\Sigma 2$		
	III.1	3009	13														0.4 v	$\bar{C}01$	5.5 v	
III.2			14														0.4 v	$\bar{C}02$	-0.4	-1.3 mA
			15 CKT J		0.4 v	4.5 v	4.5 v										0.4 v	$\bar{A}2$	-0.4	
			15 CKT K		0.4 v	4.5 v	4.5 v										0.4 v	$\bar{A}1$	-1.2	-5.6
			16 CKT J		4.5 v	0.4 v	4.5 v										0.4 v	$\bar{B}1$		-3.9
			16 CKT K		4.5 v	0.4 v	4.5 v										0.4 v	$\bar{B}1$		-5.6
			17 CKT J		4.5 v	0.4 v	4.5 v										0.4 v	$\bar{C}1$		-3.9
			17 CKT K		4.5 v	0.4 v	4.5 v										0.4 v	$\bar{C}1$		-3.9
III.3			18 CKT J	0.4 v													4.5 v	\bar{GND}	4.5 v	
			18 CKT K	0.4 v													4.5 v	$\bar{A}2$	-2.4	
			19 CKT J	4.5 v													0.4 v	$\bar{A}2$	-1.2	
			19 CKT K	4.5 v													0.4 v	$\bar{C}2$	-2.4	
III.4			20 CKT J	4.5 v													0.4 v	$\bar{C}2$	-1.2	
			20 CKT K	4.5 v													0.4 v	$\bar{B}2$	-1.2	
			21	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	2.4 v	\bar{GND}	4.5 v		
HH1	HH1	3010	22	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	2.4 v	\bar{GND}	4.5 v		
			23	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	\bar{GND}	4.5 v		
HH3			24	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	2.4 v	\bar{GND}	4.5 v		
			25	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	2.4 v	\bar{GND}	4.5 v		
			26	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	2.4 v	\bar{GND}	4.5 v		
HH4			27	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	2.4 v	\bar{GND}	4.5 v		
			28	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	GND	2.4 v	2.4 v	\bar{GND}	4.5 v		
			29	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v		
IC6			30	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v		
			31	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			32	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
IC8			33	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			34	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			35	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
IC9			36	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			37	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			38	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
IC10			39	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			40	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			
			41	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	GND	5.5 v	\bar{GND}	4.5 v			

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits
		Test No.	$\bar{A}2$	A1	B1	C1	$\bar{C}01$	$\bar{E}1$	GND	$\bar{E}2$	C02	$\bar{C}2$	B2	A2	$\bar{E}2$	VCC	Meas. terminal	Max	Unit	
1	VIC		41	-12 mA												4.5 v	$\bar{A}2$	A1	-1.5	v
		TA = 25°C	42		-12 mA												B1			
			43			-12 mA											C1			
			44				-12 mA										C2			
			45					-12 mA									B2			
			46						-12 mA								A2			
			47							-12 mA							$\bar{B}2$			
			48								-12 mA									
	ICC		3005	49																
2			Same tests, terminal conditions and limits as for subgroup 1, except TA = 125°C and VIC tests are omitted.																	
3			Same tests, terminal conditions and limits as for subgroup 1, except TA = -55°C and VIC tests are omitted.																	
			$\bar{A}2$ = 7 1/2/25°C																	
			50	0.8 v	0.8 v	0.8 v	0.8 v	H	H	L	H	L	H	H	0.8 v	0.8 v	0.8 v	0.8 v	All outputs as shown	
			51	2.0 v	2.0 v	0.8 v	0.8 v	H	L	H	L	H	L	H	2.0 v	2.0 v	2.0 v	2.0 v		
			52	0.8 v	0.8 v	2.0 v	0.8 v	H	L	H	L	H	L	H	2.0 v	2.0 v	2.0 v	2.0 v		
			53	2.0 v	2.0 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			54	0.8 v	0.8 v	0.8 v	2.0 v	H	L	H	L	H	L	H	2.0 v	2.0 v	2.0 v	2.0 v		
			55	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			56	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			57	2.0 v	2.0 v	2.0 v	2.0 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			58	0.8 v	0.8 v	2.0 v	2.0 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			59	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			60	0.8 v	0.8 v	2.0 v	2.0 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			61	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			62	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			63	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			64	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			65	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			66	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			67	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			68	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			69	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			70	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			71	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			72	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			73	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			74	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			75	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			76	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			77	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			78	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			79	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			80	0.8 v	0.8 v	2.0 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		
			81	2.0 v	2.0 v	0.8 v	0.8 v	L	H	L	H	L	H	H	2.0 v	2.0 v	2.0 v	2.0 v		

8 1/2/ Same tests, terminal conditions and limits as for subgroup 7, except TA = 125 and -55°C.

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be $H \geq 2.0$ V; $L \leq 0.8$ V; or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		A2	A1	B1	C1	$\bar{C}01$	$\Sigma 1$	GND	$\bar{\Sigma}2$	C02	$\bar{C}2$	B2	A2	$\bar{B}2$	VCC	Test limits			
			1	2															Meas. terminal	Min	Max	Unit
9 $T_A = 25^\circ C$	tPHL1 tPHL2 tPHL3 tPHL4 tPHL4 tPHL5 tPHL6 tPHL6	3003	82	83														C1 to $\Sigma 1$	9	45	ns	
				84														C1 to $\bar{\Sigma}1$	9	48		
				85														C1 to $\Sigma 1$	6	31		
				86														C1 to $\bar{\Sigma}1$	6	31		
				87														C1 to $\bar{C}01$	3	14		
				88														C1 to $\bar{C}01$	3	17		
				89														A2 to $\Sigma 2$	11	52		
				90														A2 to $\bar{\Sigma}2$	11	55		
				91														A2 to $\Sigma 2$	8	38		
				92														A2 to $\bar{\Sigma}2$	8	38		
				93														A2 to $\bar{C}02$	5	21		
																		A2 to $\bar{C}02$	5	21		
																			A2 to $\bar{C}02$	5	24	
10 $T_A = 125^\circ C$	tPHL1 tPHL2 tPHL3 tPHL4 tPHL4 tPHL5 tPHL6 tPHL6		94	95														C1 to $\Sigma 1$	9	60		
				96														C1 to $\bar{\Sigma}1$	9	59		
				97														C1 to $\Sigma 1$	6	39		
				98														C1 to $\bar{C}01$	3	21		
				99														C1 to $\bar{C}01$	3	21		
				100														A2 to $\Sigma 2$	11	69		
				101														A2 to $\bar{\Sigma}2$	11	67		
				102														A2 to $\Sigma 2$	8	49		
				103														A2 to $\bar{\Sigma}2$	8	48		
				104														A2 to $\bar{C}02$	5	29		
				105														A2 to $\bar{C}02$	5	28		
11																						

49 Same tests, terminal conditions and limits as for subgroup 10, except $T_A = -55^\circ C$.1/ Output voltages shall be either: (a) $H = 2.4$ V, minimum and $L = 0.4$ V, maximum when using a high speed checker double comparator; or (b) $H \geq 1.5$ V and $L \leq 1.5$ V when using a high speed checker single comparator.2/ Input voltages shown are the maximum for V_{IL} and the minimum for V_{IH} .

TABLE III. Group A inspection for device type 04. Terminal conditions (pins not designated may be $H \geq 2.0$ V; $L \leq 0.8$ V; or open)

Same tests, terminal conditions and limits as for subgroup I, except $T_A = 125^\circ\text{C}$ and VIC tests are omitted.

maximum $A = -33$ C and VIC tests are conducted as for sample 1, same tests, same conditions and units as for sample 1, except $A = -33$ C and VIC tests are omitted.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V; L < 0.8 V; or open)

$$\overline{A} = z.0 \text{ V and } B = 0.8 \text{ V.}$$

Output voltages shall be either: (a) $H = 2.4\text{ V}$, minimum and $L = 0.4\text{ V}$, maximum when using a high speed checker double comparator; or (b) $H \geq 1.5\text{ V}$ and $L < 1.5\text{ V}$ when using a high speed checker single comparator.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.3 Ordering data. Procurement documents should specify the following:

- (a) Complete part number (see 1.2).
- (b) Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- (c) Requirement for certificate of compliance, if applicable.
- (d) Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
- (e) Requirements for packaging and packing.
- (f) Requirements for failure analysis (including required test condition of Method 5003), corrective action and reporting of results, if applicable.
- (g) Requirements for product assurance options.
- (h) Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, and as follows:

GND	- - - - -	Electrical ground (common terminal)
V _{IN}	- - - - -	Voltage level at an input terminal
V _{IC}	- - - - -	Input clamp voltage
I _{IN}	- - - - -	Current flowing into an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. Microcircuits covered by this specification are substitutable for the following commercial device types:

<u>Device type</u>	<u>Commercial type</u>
01	5482, 7482, 9382
02	5483, 7483, 9383
03	9304
04	5480, 7480, 9380

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army - EL
Navy - EC
Air Force - 17

Preparing activity:

Air Force - 17

Review activities:

Army - EL, MI, MU
Air Force - 11, 19, 99
DSA - ES

Agent:

DSA - ES

(Project 5962-0128)

User activities:

Army - SM
Navy - CG, MC, AS, OS, SH