

| INCH-POUND |

MIL-M-38510/655
AMENDMENT 2
27 March 1998
SUPERSEDING
MIL-M-38510/655
AMENDMENT 1
29 January 1988

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS,
BUS TRANSCEIVERS WITH THREE-STATE OUTPUTS,
MONOLITHIC SILICON

Inactive for new design after 9 August 1996

This amendment forms a part of MIL-M-38510/655, dated 30 September 1986,
and is approved for use by all Departments and Agencies of the Department of Defense

PAGE 1

1.2.3, add new case outlines as follows:

"D	F-2 (14-lead, 1/4" x 3/8"), flat package"
"K	F-6 (24-lead, 3/8" x 5/8"), flat package"
"S	F-9 (20-lead, 1/4" x 1/2"), flat package"

The attached insertable replacement pages listed below are replacements for stipulated pages. When the new pages have been entered in the document, insert the amendment as the cover sheet to the specification.

<u>Replacement page</u>	<u>Page replaced</u>
23	Reprinted without change
24	24
25	25
26	Reprinted without change
29	29
30	30
39	39
40	40
71	71
72	72

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PAGE 2

1.3, delete and substitute:

"1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	-0.5 V dc +7.0 V dc
DC input voltage (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	± 20 mA
DC output current per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND current per pin (I_{OC})	± 70 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	300 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):		
Cases C, D, L, K, R, S, 2 and 3	(See MIL-M-38510, appendix C)
Junction temperature (T_J)	+175°C"

PAGE 3

3.2.2: Delete "and logic equations".

3.6.1: Delete "and 4.5.4 herein".

PAGE 4

4.3, second sentence, delete and substitute the following: "Inspections to be performed shall be those specified in 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4)."

PAGE 5

4.4, second sentence, delete and substitute the following: "Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4)."

4.4.1b, and 4.4.1c, delete and substitute:

"b. Subgroups 5 and 6 table I of method 5005 of MIL-STD-883 shall be omitted."

"c. Subgroup 4 ($C_{I/O}$ and C_C) shall be measured only for initial qualification and after process or design changes which may effect capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 Mhz."

PAGE 8

TABLE I, Control capacitance test, max limits column: delete "10" and substitute "15".

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PAGE 8

*TABLE I, ICCΔ symbol, conditions column, delete and substitute the following:

Additional supply current quiescent per input pin (one unit load)	ICCΔ g/	V _{IL} = 0.4 V, V _{IH} = 2.4 V, Test pin(s) at V _{IN} = 2.4 V, Control pin(s) at V _{IN} = 0.4 V, other pin(s) at V _{CC} or GND, I _O = 0 V (see table III)	53	5.5 V		3.0	mA
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PAGE 11

TABLE IA, title: Delete "figures" and substitute "values".

PAGE 12

TABLE II, line 10, columns "Table III subgroups": Add "g/".

Bottom of page, add the following new footnote:

"g/ Subgroups 7 and 8 do not apply to device types 02, 03, and 53."

PAGE 13

FIGURE 1: Delete "Case C" and substitute "Cases C, D".

PAGE 14

FIGURE 4, title, delete and substitute:

"FIGURE 1. Logic diagrams and terminal connections (top view) - Continued."

PAGES 15 AND 16

FIGURE 1: Delete "Case R" and substitute "Cases R and S".

PAGE 18

FIGURE 1: Delete "Case L" and substitute "Cases L and K".

PAGES 19 AND 20

FIGURE 1, NOTE: Delete "case L" and substitute "cases L and K".

PAGES 31 THROUGH 38

TABLE III, heading: Delete "Case C" and substitute "Cases C, D".

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PAGES 33 AND 34

TABLE III, t_{PZH1} and t_{PHZ1} : Delete "10".

TABLE III, t_{PZL1} and t_{PLZ1} : Delete "9".

PAGES 37 AND 38

TABLE III, t_{PZH1} and t_{PHZ1} : Delete "10".

TABLE III, t_{PZL1} and t_{PLZ1} : Delete "9".

PAGES 41 THROUGH 54

TABLE III, heading: Delete "Cases 2, R" and substitute "Cases 2, R, S".

PAGES 41 THROUGH 44

TABLE III: Renumber tests 90 through 308 to 91 through 309.

PAGE 41

TABLE III, test numbers 123 through 138, subgroup 1, max limits column: Delete ".1" and substitute ".2".

PAGE 42

TABLE III, test numbers 139 through 154, subgroup 1, max limits column: Delete "-.1" and substitute "-.2".

TABLE III, test numbers 175 and 176, subgroup 1, max limits column: Delete "10" and substitute "15".

PAGE 44

TABLE III, test numbers 286 through 293, pin 1 column: Delete "6 V" and substitute "4.5 V".

TABLE III, t_{PZH1} and t_{PHZ1} : Delete "10".

TABLE III, t_{PZL1} and t_{PLZ1} : Delete "9".

PAGE 49

TABLE III, t_{PHZ2} and t_{PZH2} : Delete "10".

TABLE III, t_{PLZ2} and t_{PZL2} : Delete "9".

PAGE 54

TABLE III, t_{PHZ2} and t_{PZH2} : Delete "10".

TABLE III, t_{PLZ2} and t_{PZL2} : Delete "9".

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PAGES 55 THROUGH 70

TABLE III, heading: Delete "Case L" and substitute "Cases L, K".

PAGE 61

TABLE III, t_{PZH2} and t_{PHZ2} : Delete "10".

TABLE III, t_{PZL2} and t_{PLZ3} : Delete "9".

PAGES 73 THROUGH 76

TABLE III, heading: Delete "Cases 2, R" and substitute "Cases 2, R, S".

TABLE III: Renumber tests 94 through 312 to 95 through 313.

PAGE 73

TABLE III, test numbers 127 through 141, subgroup 1, max limits column: Delete ".1" and substitute ".2".

PAGE 74

TABLE III, test numbers 143 through 157, subgroup 1, max limits column: Delete "-.1" and substitute "-.2".

TABLE III, test numbers 179 and 180, subgroup 1, max limits column: Delete "10" and substitute "15".

PAGE 76

TABLE III, t_{PZH1} and t_{PHZ1} : Delete "10".

TABLE III, t_{PZL1} and t_{PLZ1} : Delete "9".

TABLE III, test numbers 290 through 297, pin 1 column: Delete "6 V" and substitute "4.5 V".

Footnote 2/, delete and substitute as follows:

"2/ Three-state output conditions are required. For I_{OZL} , set output to high state. For I_{OZH} , set output to low state. Set input pins to $V_{IL} = V_{IL}(\text{max})$ or to $V_{IH} = V_{IH}(\text{min})$ as required for each test."

Add new footnote 8/ as follows:

"8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half the input frequency. The f_{MAX} requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits columns."

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4.4.5 and 4.5.4: Delete in their entirety. PAGE 77

PAGE 78
TABLE V and TABLE VI: Delete in their entirety.

PAGE 79
FIGURE 5: Delete in its entirety.

PAGE 80
TABLE VII: Delete in its entirety.

NOTE: The margins of this amendment are marked with an asterisk to indicate where changes (additions, modifications, corrections, deletions) from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force - 17
NASA - NA

Preparing activity:
DLA - CC

Review activities:
Army - AR, MI, SM
Air Force - 11, 19, 85, 99
Navy - AS, CG, MC, OS, SH, TD

(Project 5962-1815)

Civil Agency Coordinating Activity:
NASA - NA

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Device type 08

Inputs						Data I/O*		Operation of function
G	DIR	CAB	CAB	SAB	SBA	A1 thru A8	B1 thru B8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X			X	X			Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Store B and A data
L	H	X	X	L	X	Input	Output	Real time B data to A bus
L	H	H or L	X	H	X			Store A and B data
X	X	↑	X	X	X	Input	Not specified	Store A, B undefined
X	X	X	↑	X	X	Not specified	Input	Store B, A undefined

H = High level L = Low level X = Irrelevant ↑ = Low-to-high level transition

* = The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Device type 09

Inputs						Data I/O*		Operation of function
G	DIR	CAB	CAB	SAB	SBA	A1 thru A8	B1 thru B8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X			X	X			Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Store B and A data
L	H	X	X	L	X	Input	Output	Real time B data to A bus
L	H	H or L	X	H	X			Store A and B data
X	X	↑	X	X	X	Input	Not specified	Store A, B undefined
X	X	X	↑	X	X	Not specified	Input	Store B, A undefined

H = High level L = Low level X = Irrelevant ↑ = Low-to-high level transition

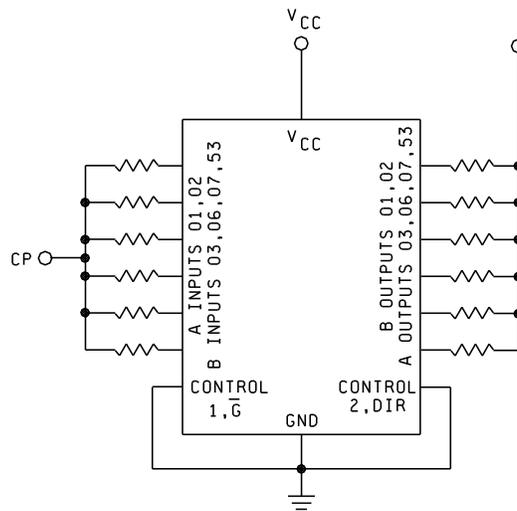
* = The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

FIGURE 2. Truth tables - Continued.

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DEVICE TYPES
01, 02, 03, 06, 07, AND 53



NOTES:

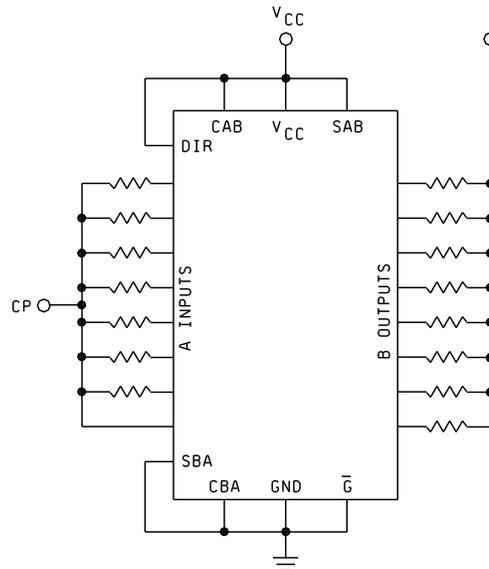
1. For static burn-in I, all inputs shall be connected to GND. Outputs shall be open or connected to $V_{CC}/2$. Resistors are optional on outputs if open. Resistors are required on inputs, and required on outputs connected to $V_{CC}/2$. $R = 470 \Omega$ to $47 \text{ k}\Omega$.
2. For static burn-in II, all inputs shall be connected through the resistors to V_{CC} . Outputs shall be open or connected to $V_{CC}/2$. Resistors are optional on outputs if open. Resistors are required on inputs, and required on outputs connected to $V_{CC}/2$. $R = 470 \Omega$ to $47 \text{ k}\Omega$.
3. For dynamic burn-in, all inputs shall be connected through the resistors in parallel to a common CP. Outputs shall be connected to $V_{CC}/2 \pm 0.5 \text{ V}$ through the resistors. $R = 680 \Omega$ for outputs, 470Ω to $47 \text{ k}\Omega$ for inputs.
4. CP = 25 kHz to 1 MHz square wave; duty cycle = 50 percent ± 15 percent; $V_{IH} = 4.5 \text{ V}$ to V_{CC} ; $V_{IL} = 0 \pm 0.5 \text{ V}$, transitions time $< 0.5 \mu\text{s}$.
5. $V_{CC} = 6.0 \text{ V} + 0.0 \text{ V}, -0.5 \text{ V}$. $V_{CC} = 5.5 \text{ V} + 0.0 \text{ V}, -0.5 \text{ V}$ for device 53.

FIGURE 3. Burn-in and life test circuits.

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DEVICE TYPES 08 AND 09



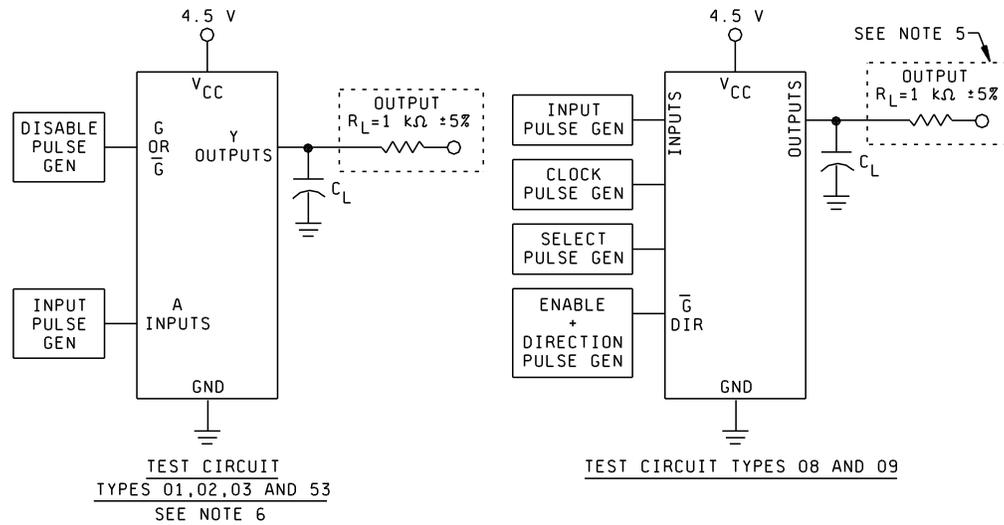
NOTES:

1. For static burn-in I, all inputs shall be connected to GND. Outputs shall be open or connected to $V_{CC}/2$. Resistors are optional on outputs if open. Resistors are required on inputs, and required on outputs connected to $V_{CC}/2$. $R = 470 \Omega$ to $47 \text{ k}\Omega$.
2. For static burn-in II, all inputs shall be connected through the resistors to V_{CC} . Outputs shall be open or connected to $V_{CC}/2$. Resistors are optional on outputs if open. Resistors are required on inputs, and required on outputs connected to $V_{CC}/2$. $R = 470 \Omega$ to $47 \text{ k}\Omega$.
3. For dynamic burn-in, all inputs shall be connected through the resistors in parallel to a common CP. Outputs shall be connected to $V_{CC}/2 \pm 0.5 \text{ V}$ through the resistors. $R = 680 \Omega$ for outputs, 470Ω to $47 \text{ k}\Omega$ for inputs.
4. CP = 25 kHz to 1 MHz square wave; duty cycle = 50 percent ± 15 percent; $V_{IH} = 4.5 \text{ V}$ to V_{CC} ; $V_{IL} = 0 \pm 0.5 \text{ V}$, transitions time $< 0.5 \mu\text{s}$.
- * 5. $V_{CC} = 6.0 \text{ V} + 0.0 \text{ V}, -0.5 \text{ V}$. $V_{CC} = 5.5 \text{ V} + 0.0 \text{ V}, -0.5 \text{ V}$ for device 53.

FIGURE 3. Burn-in and life test circuits - Continued.

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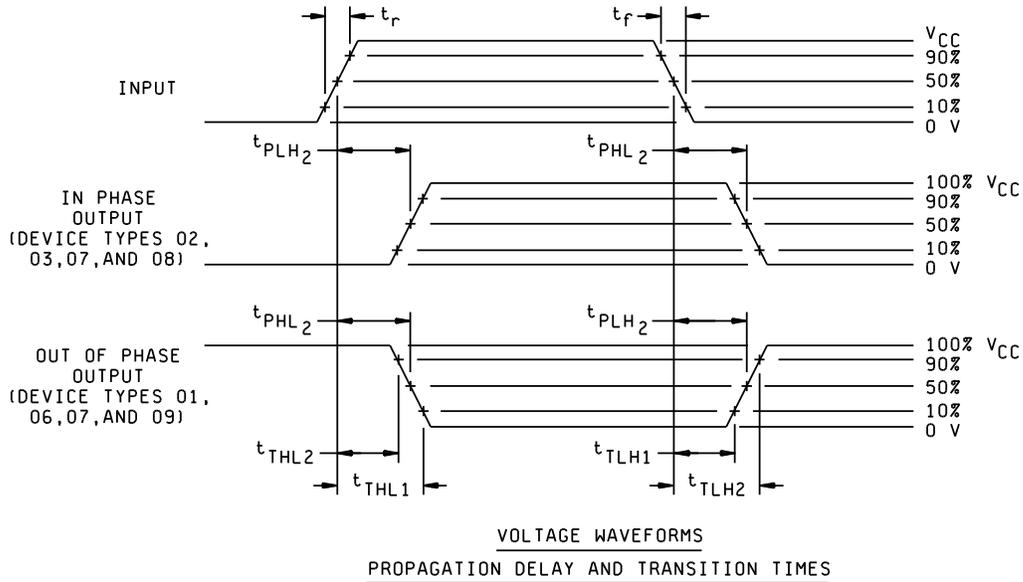
NOTES:

1. $R_L = 1 \text{ k}\Omega \pm 5\%$.
2. $C_L = 50 \text{ pF} \pm 10\%$ including probe and jig capacitance.
3. The pulse generators have the following characteristics:
 $V_{gen} = 4.5 \text{ V}$, $PRR \leq 1 \text{ MHz}$, $t_{TLH} \leq 6 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $Z_{OUT} = 50 \Omega$.
4. Clock pulse characteristics: $t_p(\text{CLK}) = 18 \text{ ns}$, $t_{setup} = 20 \text{ ns}$, $t_{hold} = 5 \text{ ns}$.
5. Output connected to V_{CC} for t_{PLZ} and t_{PZL} ; and to GND for t_{PHZ} and t_{PZH} , see figure 4.
6. The input signal for the 53 device type (HCT) will be 0-3 volts; however, the 50% V_{CC} measure point is 1.3 volts for input and output signals. The 10% V_{CC} and 90% points are, 3 V and 2.7 V, respectively.

FIGURE 4. Switching time test circuit and waveforms.

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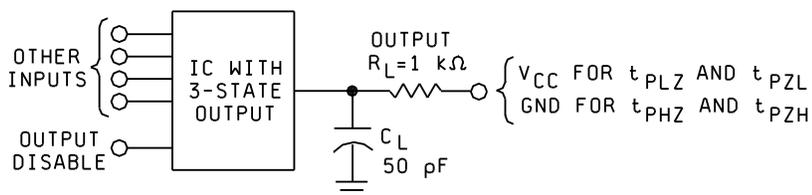
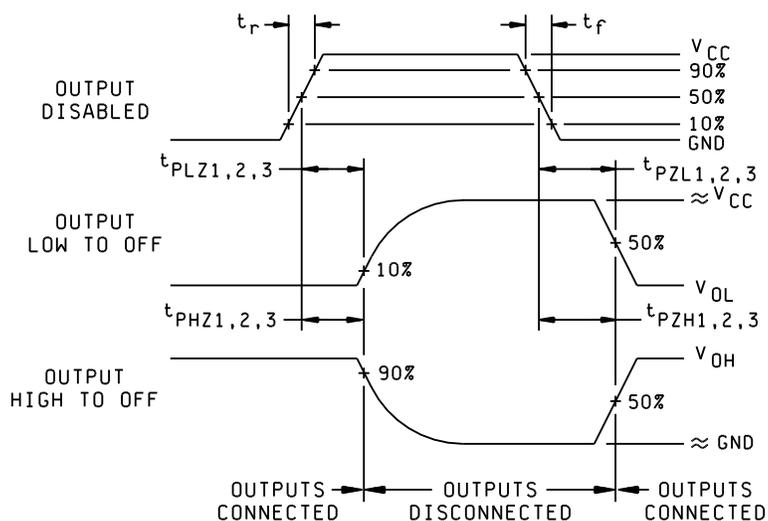
NOTES:

1. Inputs pulse shall have the following characteristics: $t_r = t_f \leq 6$ ns; $PRR \leq 1$ MHz; duty cycle = 50 percent.
2. For unused pin conditions, see table III, footnote 1/.
3. $t_{THL1} - t_{THL2} = t_{THL}$; $t_{TLH2} - t_{TLH1} = t_{TLH}$.

FIGURE 4. Switching time test circuit and waveforms - Continued.

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NOTE:
 $t_r = t_f \leq 6 \text{ ns}$.

Enable and disable times, three-state outputs, all device types.

FIGURE 4. Switching time test circuit and waveforms - Continued.

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