

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS,
DATA SELECTORS/MULTIPLEXERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, high speed, CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	Eight-input data selector/multiplexer, with enable
02	Dual, four-input data selector/multiplexer, with enable
03 and 04	Quad, two-input data selector/multiplexer, with enable
05	Eight-input data selector/multiplexer, three-state outputs, with enable
06	Dual, four-input data selector/multiplexer, three-state outputs, with enable
07	Quad, two-input data selector/multiplexer, three-state outputs with enable
08 and 09	To be included later

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
X	C-1 (16-terminal, .308" x .308" x .100"), square chip carrier package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center AFSC, RADC/RBE-2, Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	- - - - -	-0.5 V dc to +7.0 V dc
DC input voltage (V_{IN})	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage (V_{OUT})	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current (I_{IK}, I_{OK})	- - - - -	± 20 mA
DC output current per pin (I_{OUT}):		
Device types 01 through 04	- - - - -	± 25 mA
Device types 05 through 07	- - - - -	± 35 mA
DC V_{CC} or GND current per pin (I_{CC}):		
Device types 01 through 04	- - - - -	± 50 mA
Device types 05 through 07	- - - - -	± 70 mA
Storage temperature range (T_{STG})	- - - - -	-65°C to $+150^{\circ}\text{C}$
Maximum power dissipation (P_D)	- - - - -	300 mW
Lead temperature (soldering, 10 seconds)	- - - - -	$+300^{\circ}\text{C}$
Thermal resistance junction-to-case (θ_{JC}):		
Cases E, F, R, S, X, and 2	- - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J)	- - - - -	$+175^{\circ}\text{C}$

1.4 Recommended operating conditions.

Input low (V_{IL}) maximum voltage:		
$V_{CC} = 2$ V	- - - - -	0.3 V
$V_{CC} = 4.5$ V	- - - - -	0.9 V
$V_{CC} = 6$ V	- - - - -	1.2 V
Input high (V_{IH}) minimum voltage:		
$V_{CC} = 2$ V	- - - - -	1.5 V
$V_{CC} = 4.5$ V	- - - - -	3.15 V
$V_{CC} = 6$ V	- - - - -	4.2 V
Case operating temperature range (T_C)	- - - - -	-55°C to $+125^{\circ}\text{C}$
Input rise and fall times (t_r, t_f) maximum:		
$V_{CC} = 2$ V	- - - - -	1,000 ns
$V_{CC} = 4.5$ V	- - - - -	500 ns
$V_{CC} = 6$ V	- - - - -	400 ns

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Other publication. The following document forms a part of this specification to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted shall be those listed in the issue of the DODISS specified in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS shall be the issue of the non-Government documents which is current on the date of the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 7-A - Standard for Description of 54/74HCXXX and 54/74HCTXXX High Speed CMOS Devices.

(Application for copies should be addressed to the Electronic Industries Association, Engineering Department, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations which prepare or which distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.1.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.1.2 Truth tables. The truth tables shall be as specified on figure 2.

3.1.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the case operating temperature range specified. A pin for pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity.

3.3 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I. Any additional detailed information of electrical test requirements not covered in table I (i.e., pin for pin conditions and testing sequence) shall be maintained and available upon request from the qualifying activity.

3.4 Correctness of indexing and marking. All devices shall be subjected to the final electrical tests specified in table II after part number marking to verify that they are correctly indexed and identified by part number. Optionally, an approved electrical test may be devised especially for this requirement.

3.5 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 39 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2b or 4.2c as applicable, or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequences specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 of table II herein.

b. Static burn-in test condition A, method 1015 of MIL-STD-883.

(1) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$. Resistor R1 is optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. $R1 = 470\Omega$ to 47 k Ω .

(2) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC} . Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. $R1 = 470\Omega$ to 47 k Ω .

(3) $V_{CC} = 6.0$ V ± 0.5 V.

c. Dynamic burn-in test condition D, method 1015 of MIL-STD-883.

(1) Input resistors = 470Ω to 47 k Ω $\pm 20\%$.

(2) Output resistors = 1 k Ω for device types 01 through 04 and 670Ω for device types 05 through 07.

(3) $V_{CC} = 6.0$ V ± 0.5 V.

(4) $V_{CC}/2 = V_{CC}/2 \pm 0.5$ V.

(5) All data and select inputs shall be connected through the resistors in parallel to a CP. Outputs shall be connected to $V_{CC}/2$ through the resistors. Strobe (output enable) input to GND.

(6) CP = 25 MHz to 1 MHz square wave; duty cycle = 50 $\pm 15\%$; $V_{IH} = 4.5$ V to V_{CC} , $V_{IL} = 0$ V ± 0.5 V; $t_r, t_f \leq 500$ ns.

d. Interim and final electrical parameters shall be as specified in table II herein.

e. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B devices shall be in accordance with MIL-M-38510 for static burn-in. Dynamic burn-in is not required.

TABLE I. Electrical performance characteristics and test requirements.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55°C and +25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
High level output voltage	V _{OH1} 27	V _{IH} = 1.5 V V _{IL} = 0.3 V I _{OH} = -20 μA	A11	2.0 V	1, 2, 3 (3006)	1.95		1.95		V
	V _{OH2} 27	V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OH} = -20 μA	A11	4.5 V		4.45		4.45		
	V _{OH3}	V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OH} = -20 μA	A11	6.0 V		5.95		5.95		
	V _{OH4} 27	V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OH} = -4.0 mA	01,02, 03,04	4.5 V		3.98		3.7		
		V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OH} = -6.0 mA	05,06, 07			3.98		3.7		
	V _{OH5}	V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OH} = -5.2 mA	01,02, 03,04	6.0 V		5.48		5.2		
		V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OH} = -7.8 mA	05,06, 07			5.48		5.2		
	Low level output voltage	V _{OL1} 27	V _{IH} = 1.5 V V _{IL} = 0.3 V I _{OL} = 20 μA	A11		2.0 V	1, 2, 3 (3007)		0.5	
V _{OL2} 27		V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OL} = 20 μA	A11	4.5 V		0.5			0.5	
V _{OL3}		V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OL} = 20 μA	A11	6.0 V		0.5			0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55°C and +25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Low level output voltage	V _{OL4} 2/	V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OL} = 4.0 mA	01,02, 03,04	4.5 V	1, 2, 3 (3007)		0.26		0.4	V
		V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OL} = 6.0 mA	05,06, 07			0.26		0.4		
	V _{OL5}	V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OL} = 5.2 mA	01,02, 03,04	6.0 V			0.26		0.4	
		V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OL} = 7.8 mA	05,06, 07				0.26		0.4	
Positive input clamp voltage	V _{IC+}	V _{CC} = GND I _{IN} = 1 mA T _C = +25°C	A11		1 (3022)	3/	1.5			V
Negative input clamp voltage	V _{IC-}	V _{CC} = open I _{IN} = -1 mA T _C = +25°C	A11				-1.5			V
Input current low	I _{IL} 4/	V _{IN} = GND	A11	6.0 V	1, 2 (3009)		-0.05		-0.1	μA
Input current high	I _{IH} 4/	V _{IN} = 6.0 V	A11					.05		
Supply current quiescent	I _{CC} 4/	V _{IN} = V _{CC} or GND	01,02, 03,04	6.0 V	1, 2 (3005)		0.1		10	μA
			05,06, 07				0.2		20	
Supply current quiescent three-state	I _{CCZ} 4/	V _{IN} = V _{CC}	05,06, 07				0.1		10	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics and test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55°C and +25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Short circuit output current 5/	I _{OS1} 2/	V _O = GND V _I = GND or V _{CC} V _{I(enable)} = GND for (05,06,07)	01,02, 03,04	2.0 V	1, 2, 3 (3011)	-2	-50	-2	-50	mA
			05,06, 07			-2	-60	-2	-60	
	I _{OS2} 2/		01,02, 03,04	4.5 V		-15	-150	-15	-150	
			05,06, 07			-15	-165	-15	-165	
I _{OS3} 2/	01,02, 03,04	6.0 V		-25	-180	-25	-180			
	05,06, 07			-25	-210	-25	-210			
I _{OS4} 2/	01,02, 03,04	4.0 V		-10	-120	-10	-120			
	05,06, 07			-10	-135	-10	-135			
Three-state output (low) leakage current	I _{OZL} 4/	V _I = 4.2 V 6/ V _{IN} , V _{OUT} = GND V _{I(enable)} = 6.0 V	05,06, 07	6.0 V	1, 2 (3020)		-.2		-2.0	μA
Three-state output (high) leakage current	I _{OZH} 4/	V _{I(select)} = 4.2 V V _{I(enable)} = 6.0 V V _{OUT} = 6.0 V 6/	05,06, 07		1, 2 (3021)		.2		2.0	
Capacitance input	C _i	See 4.4.1c T _C = +25°C V _{I(enable)} = 6.0 V	A11		4 (3012)		10			pF
Capacitance control	C _c		A11				15			
Capacitance output	C _o		05,06, 07	6.0 V			20			
Power dissipation capacitance	C _{PD}	See 4.4.1c T _C = +25°C 7/	01,05 02,06 03 04 07		4		110 90 63 40 45			pF
Truth table test	8/	V _{IL} = 0.4 V V _{IH} = 3.7 V verify output V _O	A11	4.5 V	7, 8 (3014)	L	H	L	H	V
		V _{I(enable)} = GND	05,06, 07							

See footnotes at end of table.

TABLE I. Electrical performance characteristics and test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55°C and +25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Propagation delay data to Y	t _{PLH1} t _{PHL1}	C _L = 50 pF ±10% See figure 3 9/ 10/	01,05	4.5 V	9, 10, 11 (3003)	7	37	7	49	ns
			02			6	26	6	35	
			03			3	22	3	29	
			04			3	25	3	33	
			06			6	31	6	41	
			07			3	26	3	35	
Propagation delay data to W	t _{PLH2} t _{PHL2}		01,05			7	37	7	49	
Propagation delay strobe to Y	t _{PLH3} t _{PHL3}		01			5	27	5	36	
			02,03,04			3	28	3	37	
Propagation delay strobe to W	t _{PLH4} t _{PHL4}		01			5	27	5	36	
Propagation delay select to Y	t _{PLH5} t _{PHL5}		01			8	44	8	59	
			02			7	34	7	46	
			03,04			3	28	3	37	
			05			8	42	8	56	
			06			5	31	5	41	
			07			3	31	3	41	
Propagation delay select to W	t _{PLH6} t _{PHL6}		01			8	44	8	59	
			05			8	42	8	56	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55°C and +25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Enable time strobe to Y	t _{PZH1} t _{PZL1}	C _L = 50 pF ±10% R _L = 1 kΩ ±10% See figure 3	05	4.5 V	9, 10, 11 (3003)	5	26	5	35	ns
Enable time strobe to W	t _{PZH2} t _{PZL2}	9/ 10/	05			5	26	5	35	
Enable time control to Y	t _{PZH3} t _{PZL3}		06,07			4	26	4	35	
Disable time strobe to Y	t _{PHZ1} t _{PLZ1}		05			7	39	7	52	
Disable time strobe to W	t _{PHZ2} t _{PLZ2}		05			7	39	7	52	
Disable time control to Y	t _{PHZ3} t _{PLZ3}		06 07			5 4	26 26	5 4	35 35	
Transition delay	t _{TLH1} t _{THL1}	C _L = 50 pF ±10% V _T = GND or V _{CC} See figure 3 9/ 10/	01,02, 03,04, 05,06, 07	4.5 V	9, 10, 11 (3004)	3 2	15 12	3 2	20 16	ns

1/ For a power supply of 5 V ±10 percent, the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. The V_{IH} value at 5.5 V is 3.85 V. The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

- a. V_{IC} (pos) tests, the GND terminal shall be open.
- b. V_{IC} (neg) tests, the V_{CC} terminal shall be open.
- c. I_{CC} tests, the output terminal shall be open.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DESC-EQM) upon request. See 3.2.

2/ Guaranteed but not tested.

3/ For equipment that does not allow "GND" pin to be open during testing, a minimum limit of 0.4 V applies.

4/ Not tested at -55°C.

- 5/ Maximum limits in table I are for device testing only. Minimum limits are guaranteed for design. Only one output shall be shorted at a time.
- 6/ Three-state output conditions are required for I_{OZL} , set output to high state. For I_{OZL} , set output to low state. Set input pins to $V_{IL} = V_{IL}$ (maximum) and $V_{IH} = V_{IH}$ (minimum), as required.
- 7/ Power dissipation capacitance (C_{PD}) per package (device enabled). Power dissipation capacitance (C_{PD}), guaranteed but not tested, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$. (See JEDEC Standard No. 7-A, appendix E.)
- 8/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Correct voltage outputs are ≥ 2.5 V for high logic levels and < 2.5 V for low logic levels. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 2.5$ V, $L < 2.5$ V; high inputs = 3.7 V and low inputs = 0.4 V.
- 9/ For class B devices tested at $V_{CC} = 4.5$ V at $+125^\circ\text{C}$ for sample testing and at $V_{CC} = 4.5$ V at $+25^\circ\text{C}$ for screening guaranteed at other V_{CC} voltages and temperatures, see table IA as appropriate and 4.4.1d. Setup and hold times shall be as specified in the recommended operating conditions (see 1.4) and are referenced to the 50 percent points.
- 10/ See the formula for determining switching times shown in table IA.

TABLE IA. Calculated dynamic figures at -55 and +25 case temperature ($^\circ\text{C}$).

V_{CC}	$T_C = (^\circ\text{C})$ 1/	
	+125	-55 and +25
2.0 V 2/	5	5 x 0.75
4.5 V	1	0.75
6.0 V 2/	0.85	0.85 x 0.75

1/ Normalized numbers (+125 $^\circ\text{C}$ equals 1).

2/ The 2.0 V and 6.0 V numbers are derived from their 4.5 V integer value (rounding off according 5/4).

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S devices ^{1/}			Class B devices ^{1/}		
		Reference paragraph	Table I subgroups ^{2/}	Table III delta limits ^{3/}	Reference paragraph	Table I subgroups ^{2/}	Table III delta limits ^{3/}
1	Interim electrical parameters (method 5004)	1				1	
2	Static burn-in I (method 1015)	4.2b 4.5.2	Required			Not required	
3	Same as line 1		1	Δ			
4	Static burn-in II (method 1015)	4.2b 4.5.2	Required		4.2b 4.5.2	^{4/} Required	
5	Same as line 1	4.2d	1*	Δ	4.2d	1*	Δ
6	Dynamic burn-in (method 1015)	4.2b 4.5.2	Required			Not required	
7	Same as line 1	4.2d	1	Δ			
8	Final electrical parameters (method 5004)		1*,2,3,7,8,9			1*,2,7,9 ^{4/}	
9	Group A test requirements (method 5005)	4.4.1	1,2,3,4,7,8,9,10,11		4.4.1	1,2,3,4,7,8,9,10,11	
10	Group B end-point electrical parameters (method 5005)	4.4.2	1,2,3,9,10,11 ^{5/}	Δ		1 ^{5/}	
11	Group C end-point electrical parameters (method 5005)				4.4.3	1,2	Δ
12	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3		4.4.4	1,2	

^{1/} Blank spaces indicate tests are not applicable.

^{2/} * indicates PDA applies to subgroup 1 (see 4.2.1).

^{3/} Δ indicates delta limit shall be required only on table III, subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

^{4/} The device manufacturer may as an option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

^{5/} Subgroup 1 also applies to electrostatic discharge sensitivity tests.

Device type	Pin name					
	01, 05		02, 06		03, 04, 07	
Case	E, F, X	2	E, F, X	2	E, F, X	2
Pin number						
1	D3	NC	$\overline{1G}$	NC	$\overline{A/B}$	NC
2	D2	D3	B	$\overline{1G}$	1A	$\overline{A/B}$
3	D1	D2	1C3	B	1B	1A
4	D0	D1	1C2	1C3	1Y	1B
5	Y	D0	1C1	1C2	2A	1Y
6	\overline{W}	NC	1C0	NC	2B	NC
7	\overline{G}	Y	1Y	1C1	2Y	2A
8	GND	\overline{W}	GND	1C0	GND	2B
9	C	\overline{G}	2Y	1Y	3Y	2Y
10	B	GND	2C0	GND	3B	GND
11	A	NC	2C1	NC	3A	NC
12	D7	C	2C2	2Y	4Y	3Y
13	D6	B	2C3	2C0	4B	3B
14	D5	A	\overline{A}	2C1	4A	3A
15	D4	D7	$\overline{2G}$	2C2	\overline{G}	4Y
16	VCC	NC	VCC	NC	VCC	NC
17		D6		2C3		4B
18		D5		\overline{A}		4A
19		D4		$\overline{2G}$		\overline{G}
20		VCC		VCC		VCC

FIGURE 1. Terminal connections.

Device type 01

Inputs				Outputs	
Select			Strobe G	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
 D0, D1 . . . D7 = the level of the D respective input

Device type 02

Select inputs		Data inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

FIGURE 2. Truth tables.

Device type 03

Inputs			Output Y	
Strobe \bar{G}	Select \bar{A}/B	Data		
		A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Device type 04

Inputs			Output Y	
Strobe \bar{G}	Select \bar{A}/B	Data		
		A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

FIGURE 2. Truth tables - Continued.

Device type 05

Inputs				Outputs	
Select			Strobe \bar{G}	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

H = high level, L = low level, X = irrelevant
 D0, D1 . . . D7 = the level of the D respective input

Device type 06

Select inputs		Data inputs				Output control	Output
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

FIGURE 2. Truth tables - Continued.

Device type 07

Inputs			Output Y	
Output control G	Select A/B	Data		
		A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

FIGURE 2. Truth tables - Continued.

Device types 01, 02, 03, and 04

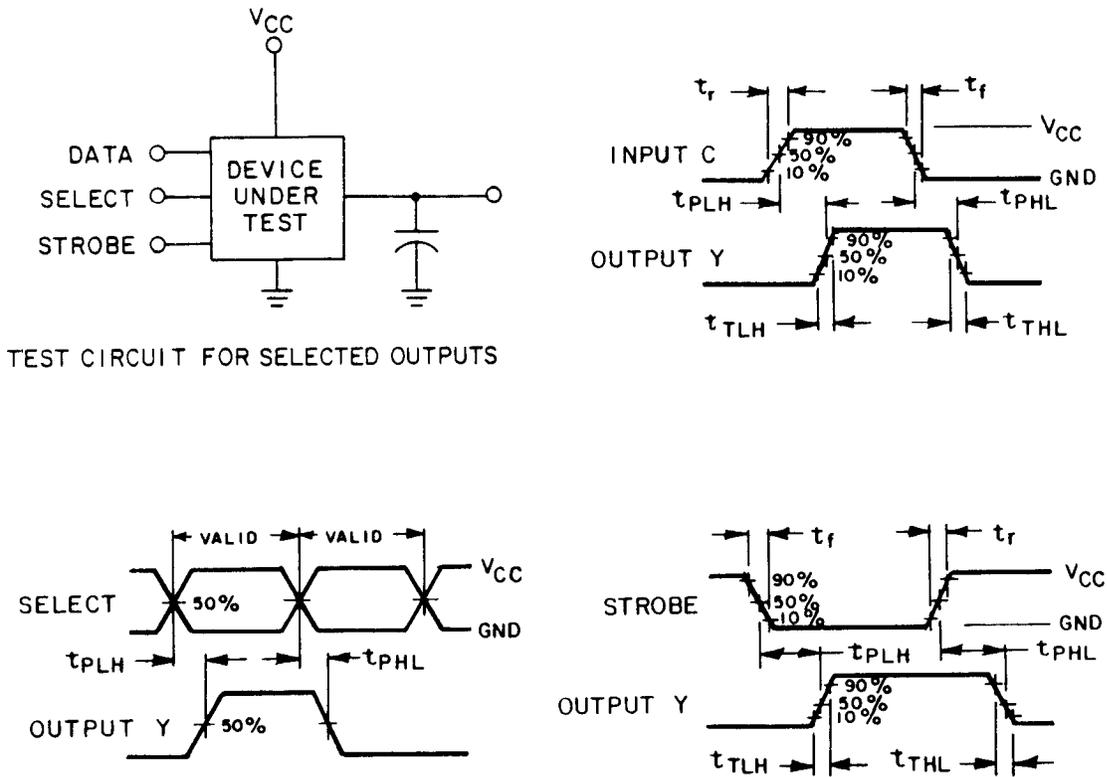
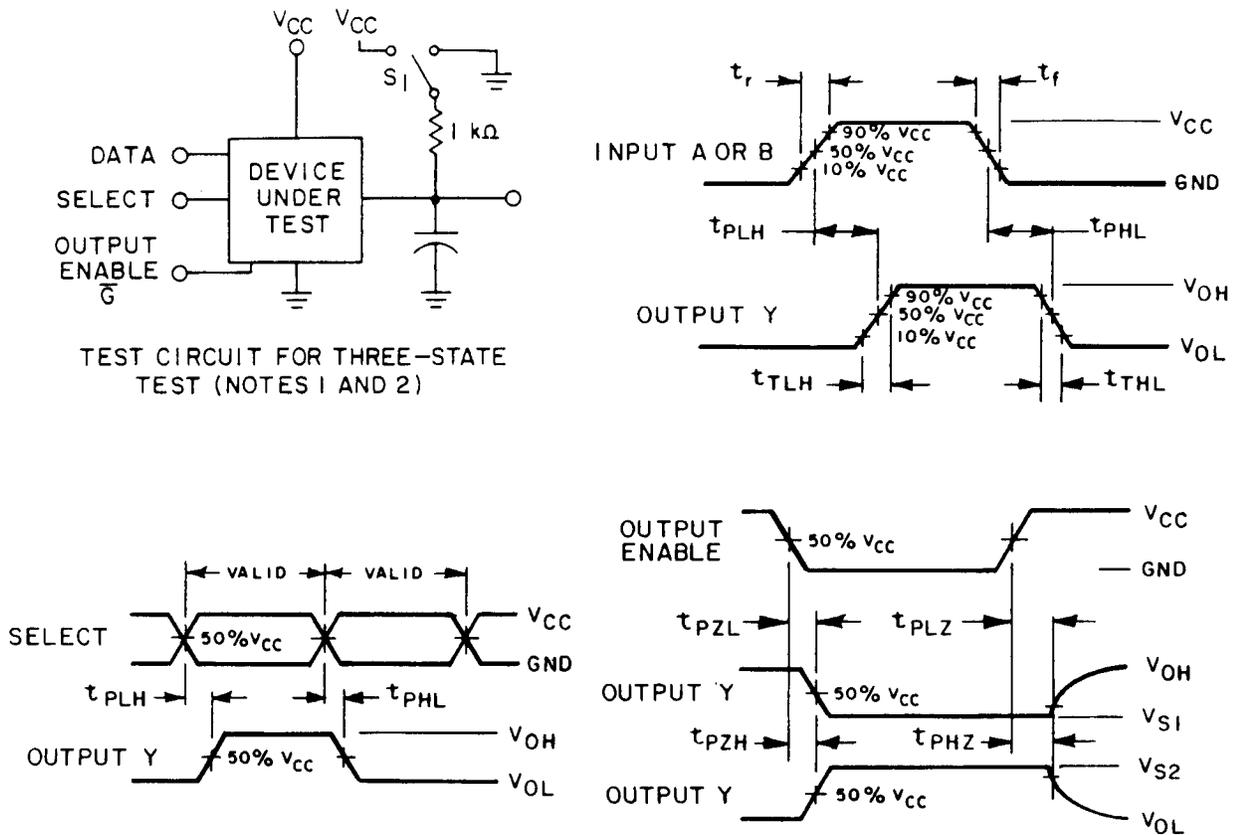


FIGURE 3. Switching time test circuits and waveforms.

Device types 05, 06, and 07



NOTES:

1. C_L includes load and test jig capacitance.
2. $S1 = V_{CC}$ for t_{PZL} , and t_{PLZ} measurements.
 $S1 = GND$ for t_{PZH} , and t_{PHZ} measurements.
3. $C_L = 50$ pF and $R_L = 1000$ ohms.
 Input pulse characteristics: $t_r = t_f \leq 6$ ns.
4. Voltage measurements are to be made with respect to network ground terminal.
5. For t_{PHZ} and t_{PZH} , a 1 k Ω resistor is connected between the output and GND terminal. For t_{PZL} and t_{PLZ} , a 1 k Ω resistor is connected between the output and V_{CC} terminal. $V_{S1} = V_{OL} + 0.1$ V ($V_{OH} - V_{OL}$).
 $V_{S2} = V_{OH} - 0.1$ V ($V_{OH} - V_{OL}$).

FIGURE 3. Switching time test circuits and waveforms - Continued.

- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table III, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D, inspections (see 4.4.1 through 4.4.5).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be performed in accordance with table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_i , C_c , and C_o measurements) shall be measured only for initial qualification and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz.
- d. Subgroups 9 and 11 shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.
- e. Subgroups 7 and 8 tests sufficient to verify truth table, except three-state output conditions need not be verified.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Class S steady-state life (accelerated) shall be conducted using test condition D and the circuit described in 4.2c herein, or equivalent as approved by the qualifying activity.
- b. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using method 3015 modified as follows:
 - (1) Table I pin combinations 4 and 5 shall be deleted.
 - (2) The test sequence specified in method 3015 of MIL-STD-883 shall be repeated an additional four times rather than the two specified.
 - (3) Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.
- c. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection and shall consist of tests specified in table III herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) shall be conducted using test condition D and as specified in 4.5.2 herein using a circuit as described in 4.2c herein, or equivalent, as approved by the qualifying activity.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to within 10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

4.5.3 Quiescent supply current (I_{CC} test). When performing quiescent supply current measurements (I_{CC}), the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the contract or purchase order, a copy of the following data, as applicable, shall be supplied:

- a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and steady-state life tests (see 3.5).
- b. A copy of each radiograph.
- c. The quality conformance inspection data (see 4.4).
- d. Parameter distribution data on parameters evaluated during burn-in (see 3.5).
- e. Final electrical parameters data (see 4.2c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.

- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.
- h. Requirements for "JAN" marking.

TABLE III. Delta limits at +25°C.

Parameter ^{1/}	Device types	
	ATT	
I _{CC}		*30 nA

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C _i - - - - -	Input terminal-to-GND capacitance
GND - - - - -	Ground zero voltage potential
I _{CC} - - - - -	Quiescent supply current
T _A - - - - -	Free air temperature
V _{CC} - - - - -	Positive supply voltage
C _{pD} - - - - -	Power dissipation capacitance

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54HC151, 54HC151B
02	54HC153, 54HC153B
03	54HC157, 54HC157B
04	54HC158, 54HC158B
05	54HC251B
06	54HC253B
07	54HC257

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Do not handle devices by the leads.
- d. Avoid use of plastic, rubber, or silk in MOS areas.
- e. Maintain relative humidity above 50 percent, if practical.

CONCLUDING MATERIAL

Custodians:

Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:

Army - AR, MI
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC, OS, SH

Preparing activity:

Air Force - 17

Agent:

DLA - ES

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