INCH-POUND

MIL-M-38510/702
29 September 1989

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, REGULATING PULSE-WIDTH, MODULATORS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, regulating, pulse-width modulator microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Classification.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit
01	Current-mode pulse-width modulator controller
02	Current-mode pulse-width modulator controller

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum rating.

Supply voltage	+40 V dc
Collector supply voltage	+40 V dc
Output current, source, or sink	500 mA dc
Analog inputs	-0.3 V to $+V_{IN}$
Reference output current	-30 mA dc
Sync output current	-5 mA
Error amplifier output current	-5 mA
Soft start sink current	50 mA
Oscillator charging current	5 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.4 Recommended operating conditions.

Supply voltage range - - - - - - - - - - - - - - - -	+8.0 to +35.0 V dc
Collector supply voltage range - - - - - - - - - - -	+4.5 to +35.0 V dc
Continuous output current source or sink - - - - -	0 to ±200 mA dc
Reference output current - - - - - - - - - - - - - -	0 to -10 mA dc
Sync output current - - - - - - - - - - - - - - - -	0 to -1.3 mA dc
Oscillator charging current - - - - - - - - - - - -	-50 μA to -2 mA dc
Current sense amplifier input common mode range -	0 V to (V_{IN} - 3 V)
Shutdown terminal input voltage - - - - - - - - - -	0 V to V_{IN}
Error amplifier differential input voltage range -	$\pm V_{REF}$
Case operating temperature range (T_C) - - - - - -	-55°C to +125°C

1.5 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
16-lead dual-in-line	E	250 mW at T_A = +125°C	60°C/W	100°C/W
20-terminal square chip carrier	2	277 mW at T_A = +125°C	30°C/W	90°C/W

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Schematic circuits. The schematic circuit shall be submitted to the preparing activity prior to inclusion of a manufacturing's device in this specification and shall be submitted to the qualifying activity (DESC-EQM) as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained by the agent activity (DESC-ECS) and will be available upon request.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3 herein.

3.2.5 Package and sealing material. Package and sealing material shall be in accordance with MIL-M-38510.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. The following electrical performance characteristics apply over the full case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.6.1 Serialization. All class S devices shall be serialized in accordance with MIL-M-38510.

3.6.2 Correctness of indexing and marking. All devices shall be subjected to the final electrical test specified in table II after part marking to verify that they are correctly indexed and identified by part number. Optionally, an approved electrical test may be devised especially for this requirement.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group 52 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ figure 3, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Limits Min	Limits Max	Unit
Cold start/PWM latch	L_{RESET}	T_J = -55°C, R_T = 10 kΩ C_T = 4700 pF, sync I_{OUT} = -1 mA	2/		kHz
REFERENCE SECTION					
Output voltage	V_{REF}	I_O = -1 mA	5.05	5.15	V
Line regulation	V_{RLINE}	8 V ≤ V_{IN} ≤ 40 V	-20	20	mV
Load regulation	V_{RLOAD}	1 mA ≤ I_L ≤ 10 mA	-15	15	mV
Output voltage (total variation)	V_{TVO}	Line, load, and temperature	5.00	5.20	V
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{REF}}$	1 V_{RMS}, f = 2400 Hz	55		dB
Output noise voltage	N_O	T_C = +25°C, (see figure 4)		200	μV_{RMS}
Short circuit output	I_{OS}	V_{REF} = 0 V	-10		mA
OSCILLATOR SECTION					
Initial accuracy	f_{OSC1}	R_T = 10 kΩ, C_T = 4700 pF; T_C = +25°C	39	47	kHz
Oscillator frequency	f_{OSC2}	R_T = 10 kΩ, C_T = 4700 pF; T_C = -55°C and +125°C	38	48	
Frequency change with voltage (voltage stability)	$\frac{\Delta f_{OSC}}{\Delta V_{IN}}$	8 V ≤ V_{IN} ≤ 40 V		2.0	%
Sync output voltage High level	V_{SOH}	I_L = -1.3 mA	3.9		V
Low level	V_{SOL}			2.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ figure 3, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Limits Min	Limits Max	Unit
OSCILLATOR SECTION (continued)					
Sync input voltage High level	V_{SIH}	C_T = 0 V	3.9		V
Low level	V_{SIL}			2.5	
Sync input current	I_{SYNC}	Sync voltage = 5.25 V; C_T = 0 V		1.5	mA
ERROR AMPLIFIER SECTION					
Input offset voltage	V_{IO1}		-5.0	5.0	mV
Input bias current	$\pm I_{IB1}$		-1.0		μA
Input offset current	I_{IO1}		-250	250	nA
Open loop voltage gain	A_{VS}	ΔV_O = 1.2 V to 3 V; V_{CM} = 2 V	80		dB
Unity gain bandwidth	G_{BW}	T_C = +25°C	0.7		H z
Common mode rejection ratio	CMRR1	0 V ≤ V_{CM} ≤ 38 V; V_{IN} = 40 V	75		dB
Power supply rejection ratio	PSRR1	8 V ≤ V_{IN} ≤ 40 V; V_{CM} = 2 V	80		dB
Output sink current (COMPENSATION pin)	I_{SINK}	-15 mV ≤ V_{ID} ≤ -5 V; $V_{COMP\ pin}$ = 1.2 V	2.0		mA
Output source current (COMPENSATION pin)	I_{SOURCE}	15 mV ≤ V_{ID} ≤ 5 V; $V_{COMP\ pin}$ = 2.5 V	-0.4		mA
High level output voltage	V_{OH1}	R_L = (COMP) 15 kΩ	4.3		V
Low level output voltage	V_{OL1}	R_L = (COMP) 15 kΩ		1.0	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ figure 3, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Limits		Unit
			Min	Max	
CURRENT SENSE AMPLIFIER SECTION					
Amplifier gain	A_V	$V_{(-CUR, SENSE pin)}$ = 0 V $V_{(CUR, LIM/SS pin)}$ open 3/ 4/	2.5	3.15	V
Maximum differential signal (positive and negative current sense pin voltages)	V_{DIFF}	$V_{(CUR LIM/SS pin)}$ open 3/ (COMP pin) = 15 k	1.1		V
Input offset voltage	V_{IO2}	$V_{(CUR LIM/SS pin)}$ = 0.5 V COMP pin open 3/	-25	25	mV
Common mode rejection ratio	CMRR2	1 V ≤ V_{CM} ≤ 12 V	60		dB
Power supply rejection ratio	PSRR2	8 V ≤ V_{IN} ≤ 40 V	60		dB
Input bias current	I_{IB2}	$V_{(CUR LIM/SS pin)}$ = 0.5 V COMP pin open 3/	-10		μA
Input offset current	I_{IO2}	$V_{(CUR LIM/SS pin)}$ = 0.5 V COMP pin open 3/	-1.0	1.0	μA
Time delay to outputs	t_{D1}	T_C = +25°C		500	ns
CURRENT LIMIT ADJUST SECTION					
Current limit offset voltage	V_{CLO}	$V_{(-CUR SENSE pin)}$ = 0 V $V_{(+CUR SENSE pin)}$ = 0 V COMP pin open 3/	0.40	0.55	V
Input bias current voltage	I_{IB3}	$V_{(+ERROR AMP pin)}$ = V_{REF} $V_{(-ERROR AMP pin)}$ = 0 V	-30		μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ figure 3, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Limits		Unit
			Min	Max	
SHUTDOWN TERMINAL SECTION					
Threshold voltage	V_{TH}		250	400	mV
Latching voltage	V_{LATCH}	Current into CUR LIM/SS pin = 3.0 mA 5/		2.0	V
Nonlatching voltage	V_{NLATCH}	Current into CUR LIM/SS pin = 0.8 mA 6/	5.0		V
Time delay to outputs	t_{D2}	T_C = +25°C		600	ns
OUTPUT SECTION					
Collector-emitter voltage	V_{CE}		40		V
Collector leakage current	I_C	V_C = 40 V 7/		200	μA
Low level output voltage	V_{OL2}	I_{SINK} = 20 mA I_{SINK} = 100 mA		0.4 2.1	V
High level output voltage	V_{OH2}	I_{SOURCE} = -20 mA I_{SOURCE} = -100 mA	13 12		V
Rise time	t_r	C_L = 1,000 pF		130	ns
Fall time	t_f	C_L = 1,000 pF		130	ns
UNDER-VOLTAGE LOCKOUT SECTION					
Start-up threshold voltage	V_{SU}			8.0	V
Shutdown threshold voltage	V_{SD}		6.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ figure 3, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Limits		Unit
			Min	Max	
TOTAL STANDBY CURRENT					
Supply current	I_{IN}	CURR LIM/SS pin = 0.7 V		21	mA

1/ Standard test conditions (unless otherwise specified): $+V_{IN}$ = 15 V dc, timing resistance = 10 kΩ; timing capacitance = 4,700 pF.

2/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWM LATCH SET command. To minimize the effects of self heating, the test must be completed within the first 50 ms of applied power. The minimum limit shall be equal to 0.49 times the oscillator frequency.

3/ Parameter measured at trip point of latch with $V_{+ERROR\ AMP} = V_{REF}$; $V_{-ERROR\ AMP}$ = 0 V.

4/ Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP\ pin}}{\Delta V_{+CURRENT\ SENSE\ pin}}; \quad \Delta V_{+CURRENT\ SENSE\ pin} = 0 \text{ to } 10 \text{ V}$$

5/ Current into CUR LIM/SS pin guaranteed to latch circuit in shutdown state.

6/ Current into CUR LIM/SS pin guaranteed not to latch circuit in shutdown state.

7/ This parameter only applies to device type 01.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883):

(1) For class S devices: Test condition D using the circuit shown on figure 5, and reverse bias burn-in (method 1015 of MIL-STD-883) using the circuit shown on figure 6; test duration shall be for 240 hours minimum.

(2) For class B devices: Test condition D using the circuit shown on figure 5; test duration shall be for 160 hours minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) for class S and class B devices shall be as specified in MIL-M-38510, based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883 and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004) 1/	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 9, 10, 11	1, 2, 3, 4, 5 6, 7, 9
Group C end-point and group B class S, electrical parameters (method 5005)	1, 2, 3, and table IV delta limits	1 and table IV delta limits
Additional electrical subgroup for group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters (method 5005)	1, 2, 3	1

1/ PDA applies to subgroup 1 (see 4.2c).

Device types	01 and 02	
Case outlines	E	2
Terminal number	Terminal symbol	
1	Cur. limit/ Softstart	NC
2	V_{REF}	Cur. limit/ Softstart
3	-Cur. sense	V_{REF}
4	+Cur. sense	NC
5	+Error amp	-Cur. sense
6	-Error amp	+Cur. sense
7	Compensation	+Error amp
8	C_T	-Error amp
9	R_T	Compensation
10	Sync	C_T
11	Output A	NC
12	GND	R_T
13	V_C	Sync
14	Output B	Output A
15	V_{IN}	GND
16	Shutdown	V_C
17	---	Output B
18	---	NC
19	---	V_{IN}
20	---	Shutdown

NOTE: NC = no connection.

FIGURE 1. Terminal connections.

Device types 01 and 02

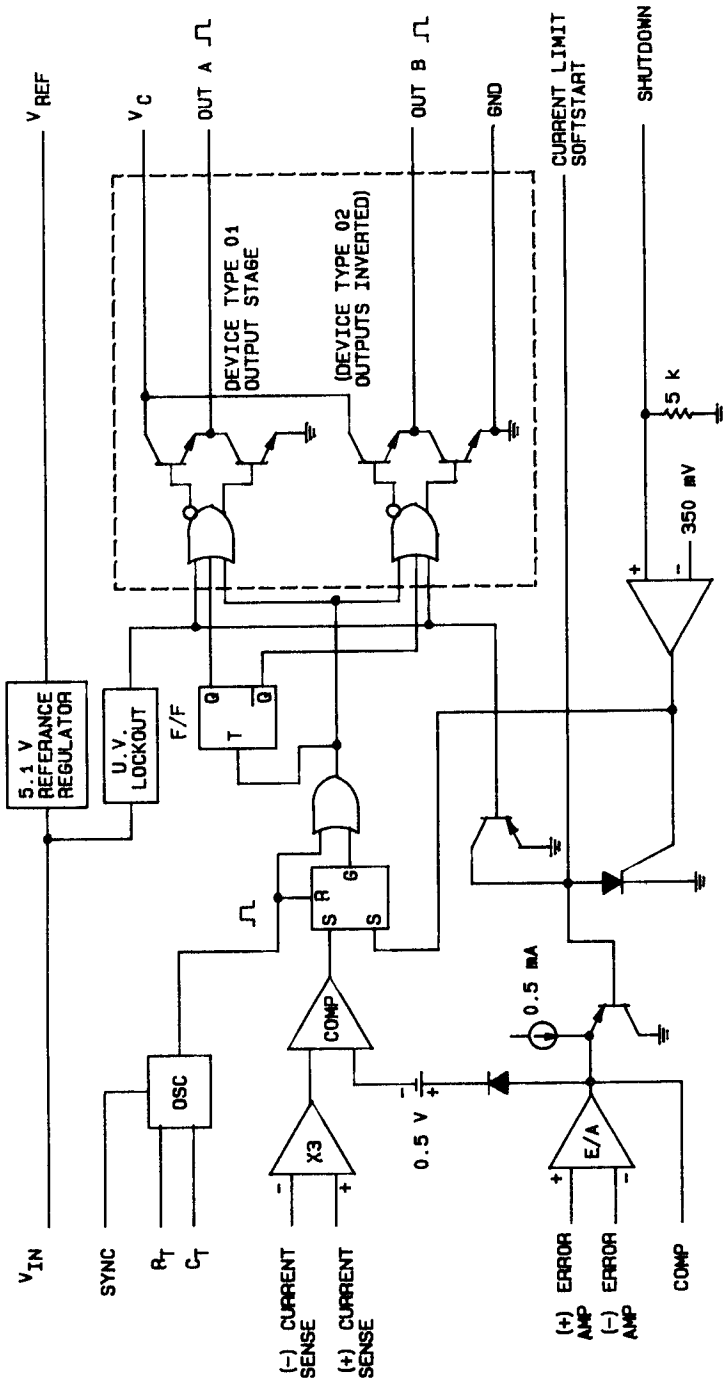


FIGURE 2. Block diagram.

Device types 01 and 02

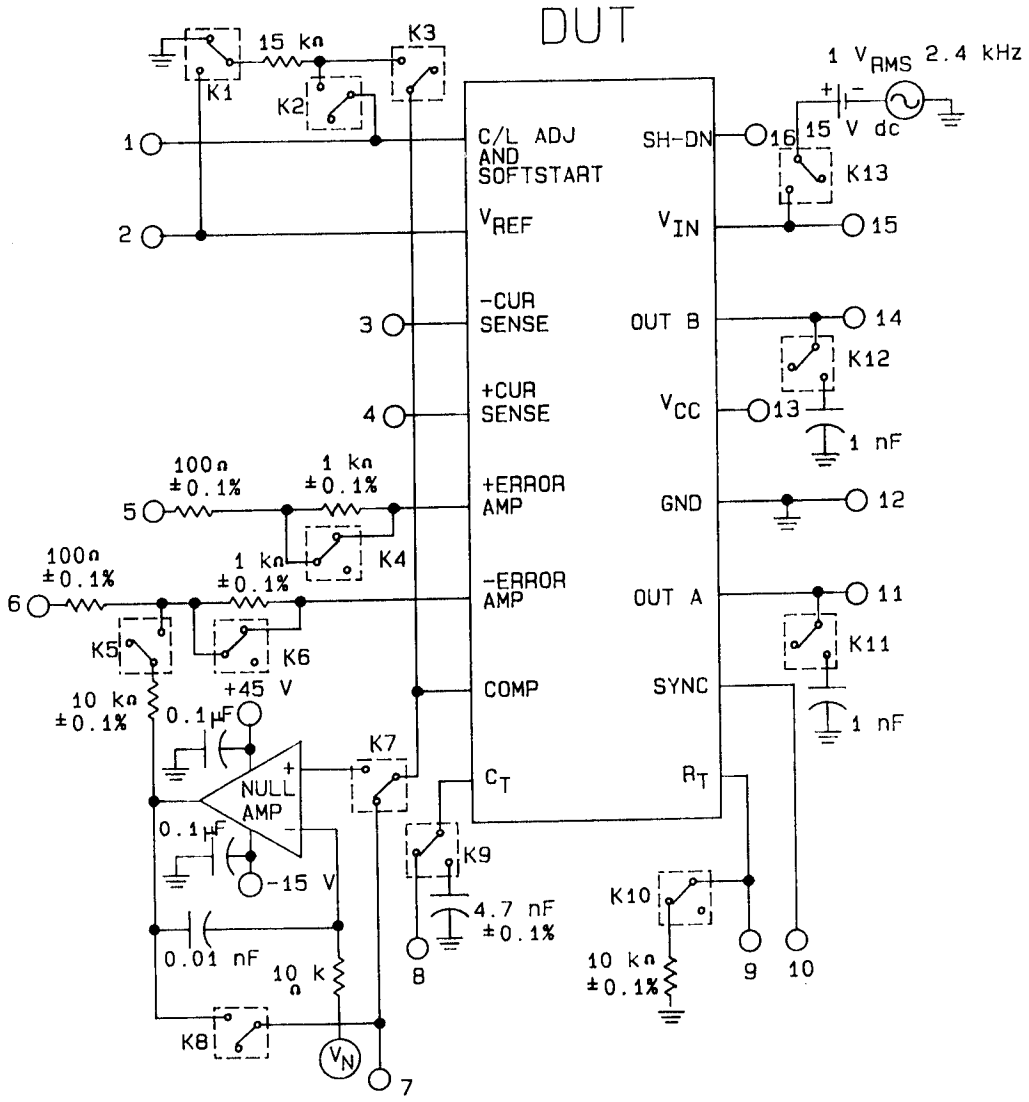
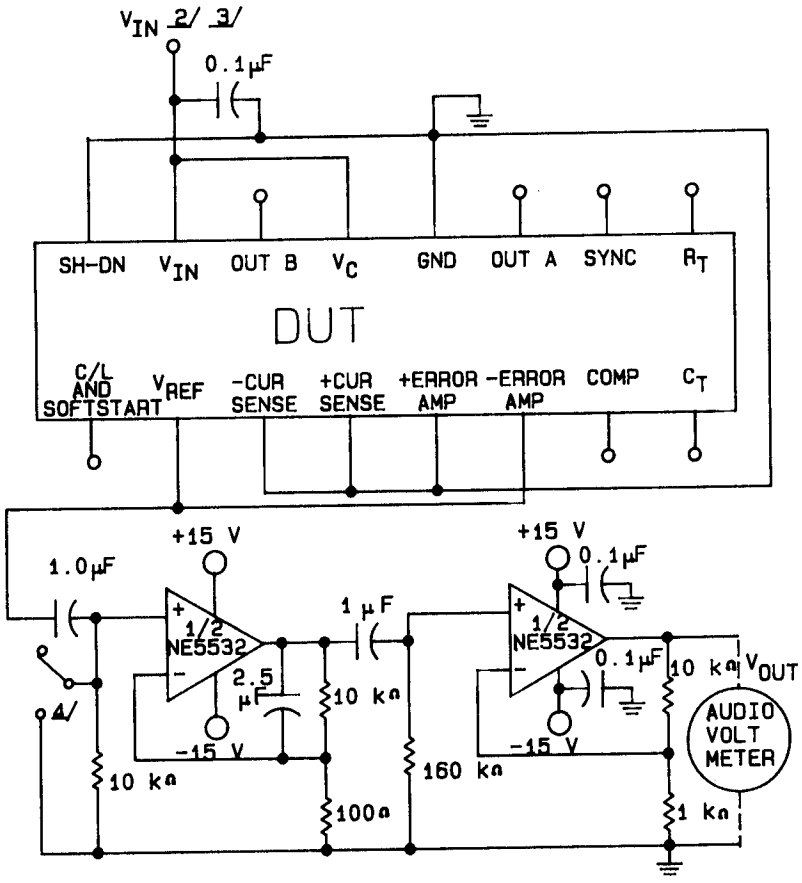


FIGURE 3. Test circuit for static and dynamic tests.

Device types 01 and 02

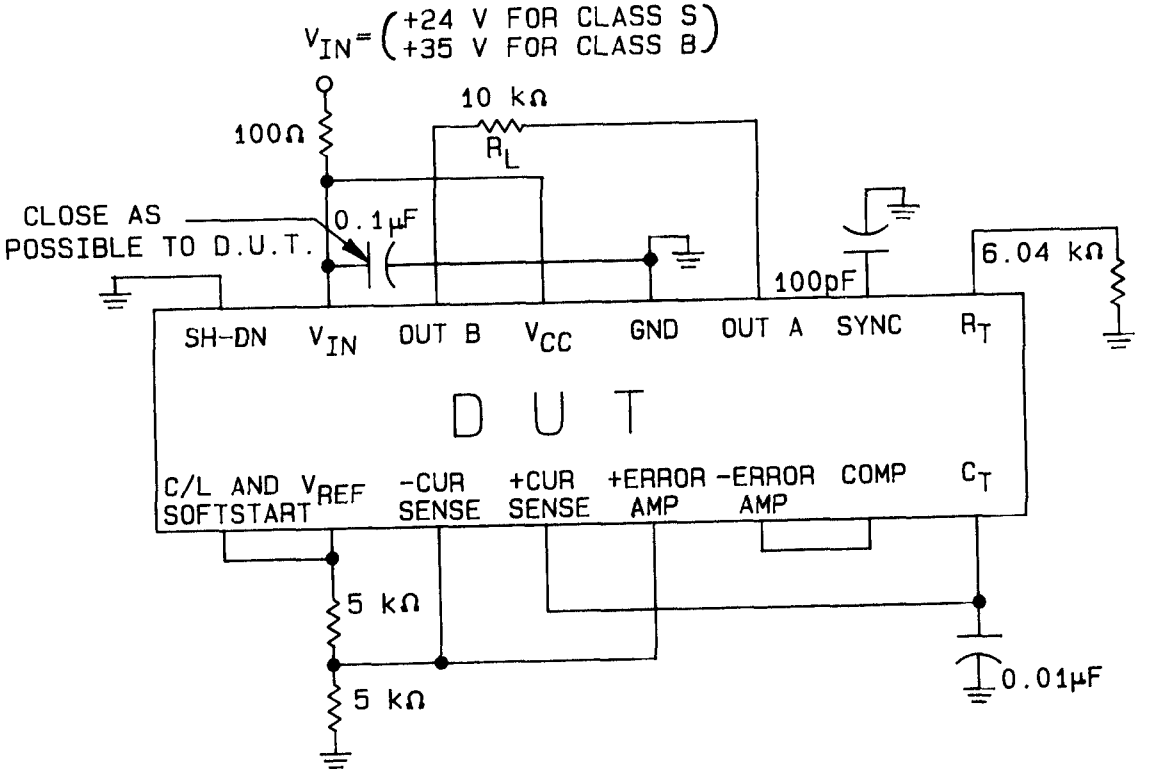


NOTES:
1. All resistors are ±1%, all capacitors are ±5%.
2. V_{IN} = 15 V for V_{REF} output noise voltage test.
3. V_{IN} = 15 V + 1 V_{RMS} 2.4 kHz for V_{REF} ripple rejection test.
4. V_{REF} output noise voltage is measured by determining both the measurement system noise (V_{OUT} with input grounded) and the noise with V_{REF} output connected and then applying the following formula.

$$N_O = \frac{\sqrt{(\text{Measurement})^2 - (\text{Measurement System Noise})^2}}{\text{GAIN } (= 1{,}111)}$$

FIGURE 4. Output noise voltage and ripple rejection test circuit.

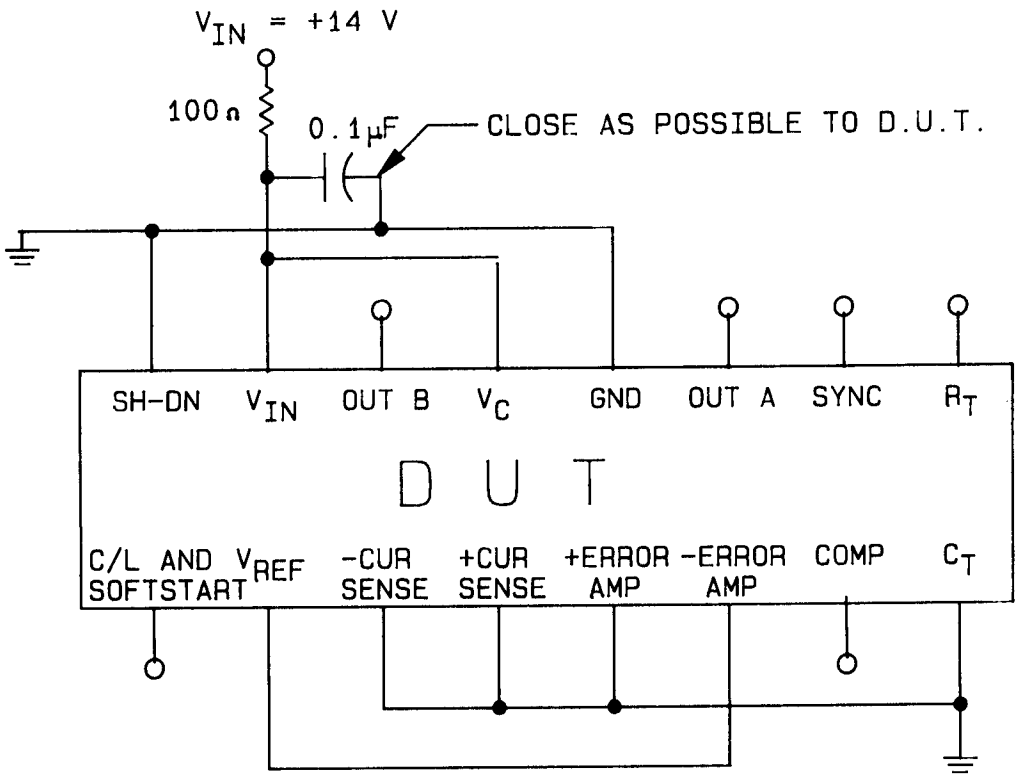
Device types 01 and 02



NOTES:
1. All resistors are ±5 percent, all capacitors are ±20 percent.
2. Bypass capacitors and compensation capacitors are allowed as needed to prevent oscillations.
3. V_{IN} = +35 V for class B, V_{IN} = +24 V for class S.

FIGURE 5. Test circuit, burn-in and operating life test.

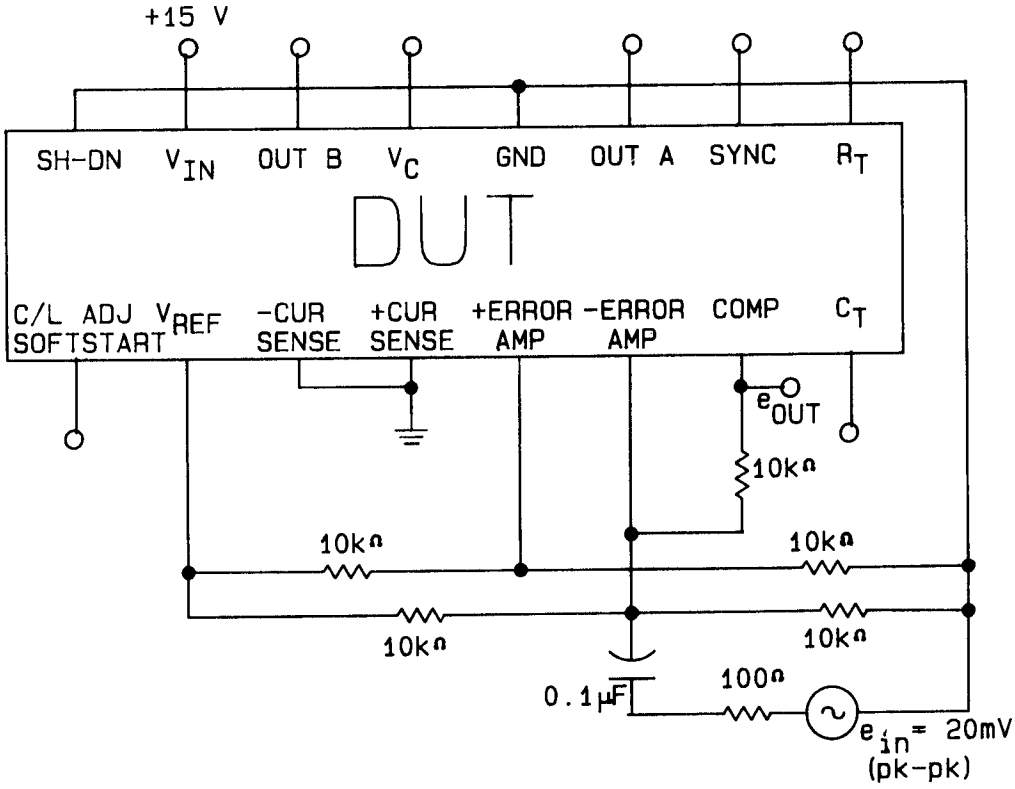
Device types 01 and 02



NOTES: All resistors are ±5 percent, all capacitors are ±20 percent.

FIGURE 6. Test circuit, burn-in (steady state reverse bias and steady state life test.

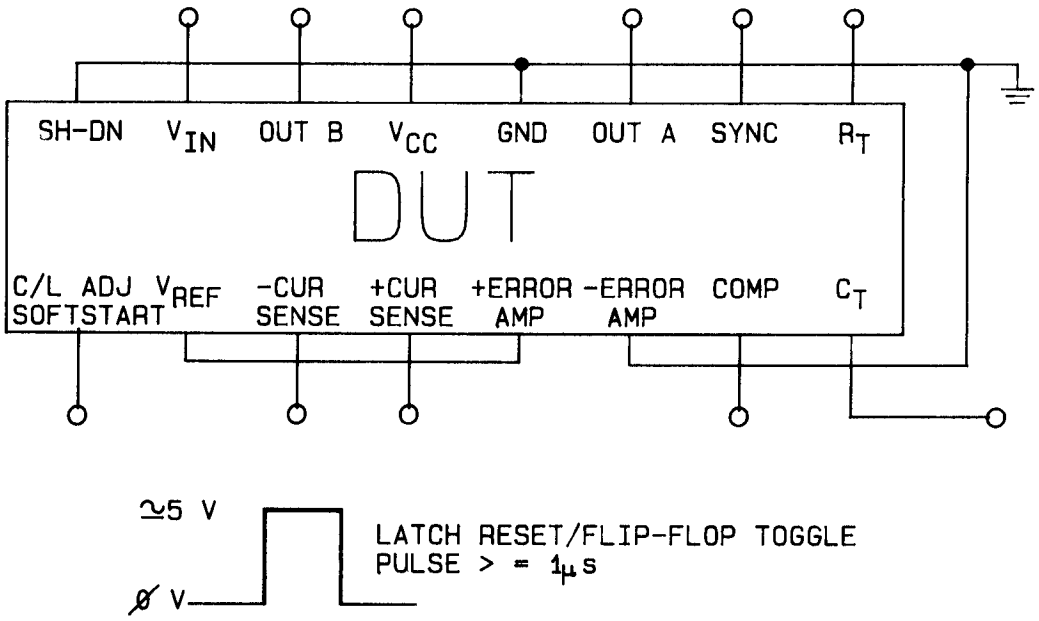
Devices types 01 and 02



NOTES:
1. G_{BW} is measured by increasing signal frequency (starting at 100 kHz) until $e_{OUT} = e_{in}$. The frequency at which this occurs is G_{BW}.
2. Alternate method: Set frequency to 700 kHz. If $e_{OUT} \geq e_{in}$ then $G_{BW} \geq$ 700 kHz.
3. All resistors are ±1%, all capacitors are ±5%.

FIGURE 7. Error amplifier unity gain bandwidth test circuit.

Device types 01 and 02



NOTE: Refer to table III for conditions of pins 1, 3, 4, 7, and 15.

FIGURE 8. Latch reset and flip-flop toggle test circuit.

Device types 01 and 02

a. CURRENT SENSE AMPLIFIER DELAY TO OUTPUTS

b. SHUTDOWN TERMINAL DELAY TO OUTPUTS

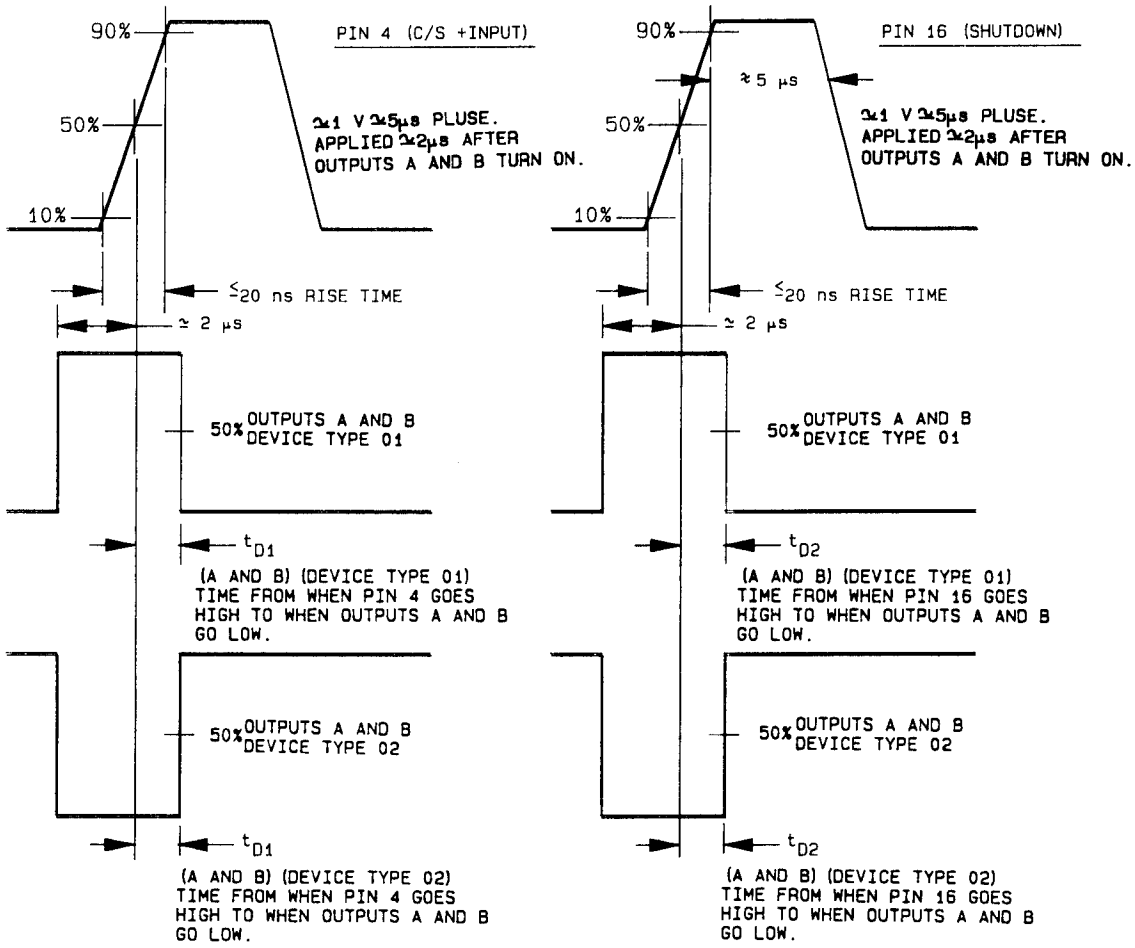


FIGURE 9. Test waveforms.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Subgroup 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

b. Electrical test requirements shall be as specified in table II herein.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test for class S devices shall be in accordance with table IIa of method 5005 of MIL-STD-883, using the circuit shown on figure 6.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table IV herein. Delta limits shall apply only to subgroup 1 of group C inspection for class B devices.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions, or equivalent:

(1) Test condition C, using the circuit shown of figure 5; or test condition A, using the circuit shown on figure 6.

(2) T_C = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. Special subgroups shall be added to group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits of subgroups 10 and 11 as specified in table III herein.

TABLE III. Group A inspection for device types 01 and 02.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/ 1 C.L. adj.	2 V_{REF}	3 Cur. Sense -	4 Cur. Sense +	5 Error Amp +	6 Error Amp -	7 Comp.	8 C_T	9 R_T	10 Sync	11 Output A	13 V_C	14 Output B	15 V_{IN}	16 Shut-down	V N	Energ. relays	Measured (pin(s) No.	Val.	Unit	Notes and equations	Limits Min	Max	Unit
1 T_C = +25°C	V_{REF}	1	Open	-1 mA	GND	GND	GND	V_{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	2	E1	V	V_{REF} = E1	5.05	5.15	V
	V_{RLOAD}	2	"	-10 mA	"	"	"	"	"	"	"	"	"	"	"	15 V	"		"	2	E2	V	V_{RLOAD} = E2 - E1	-15	15	mV
	V_{RLINE}	3	"	0 mA	"	"	"	"	"	"	"	"	"	"	"	8 V	"		"	2	E3	V	V_{RLINE} = E4 - E3	-20	20	mV
			"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"		"	2	E4	V				
	V_{TVO}	4																					V_{TVO} = E2	5.00	5.20	V
		5																					V_{TVO} = E1 + V_{RLINE}	5.00	5.20	V
		6																					V_{TVO} = E2 + V_{RLINE}	5.00	5.20	V
	I_{OS}	7	Open	0 V	GND	GND	GND	V_{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	2	I1	mA	I_{OS} = I1 3/	-80		mA
	V_{SOH}	8	"	Pin 6	"	"	"	"	"	V_{REF} (Pin 2)	Open	-1.3 mA	"	"	"	"	"		"	10	E5	V	V_{SOH} = E5	3.9		V
	V_{SOL}	9	"	"	"	"	"	"	"	GND	"	Open	"	"	"	"	"		"	10	E6	V	V_{SOL} = E6		2.5	V
	V_{SIH}	10	"	Pin 5	"	"	V_{REF}	GND	"	0 V 4/	"	3.9 V	"	" 5/	"	"	"		None	11 14	E7 E8	V V	$V_{SIH} \geq$ 3.9 V if both E7 and E8 = limit 4/ 5/	13 (Type 02 only)	0.4 (Type 01 only)	V
	V_{SIL}	11	"	"	"	"	"	"	"	"	"	2.5 V	"	"	"	"	"		"	11 14	E9 E10	V V	$V_{SIL} \geq$ 2.5 V if E9 or E10 = limit 4/ 5/	13 (Type 01 only)	0.4 (Type 02 only)	V
	I_{SYNC}	12	"	Pin 6	"	"	GND	V_{REF}	"	"		5.25 V	"	"	"	"	"		"	10	I2	mA	I_{SYNC} = I2		1.5	mA
	V_{I01}	13	"	Open	"	"	2.6 V	2.6 V	"	Open	Open	Open	"	"	"	"	"	2.6 V	K5,K7 K8	7 to 6	E11	V	V_{I01} = E11/101	-5	5	mV
	$-I_{IB1}$	14	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	K5,K6 K7,K8	"	E12	V	$-I_{IB1} = \frac{(E12 - E11)}{101000}$	-1		µA
	$+I_{IB1}$	15	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	K4,K5 K7,K8	"	E13	V	$+I_{IB1} = \frac{(E11 - E13)}{101000}$	-1		µA

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/ 1 C.L. adj.	2 V_{REF}	3 Cur. Sense −	4 Cur. Sense +	5 Error Amp +	6 Error Amp −	7 Comp.	8 C_T	9 R_T	10 Sync	11 Output A	13 V_C	14 Output B	15 V_{IN}	16 Shut-down	V N	Energ. relays	Measured (pin(s) No.	Val.	Unit	Notes and equations	Limits Min	Max	Unit
1 T_C = +25°C	I_{IO1}	16																					$I_{IO1} = (-I_{IB1}) - (+I_{IB1})$	-250	250	nA
	CMRR1	17	Open	Open	GND	GND	0 V	0 V	Open	Open	Open	Open	Open	15 V	Open	40 V	GND	2.6 V	K5,K7 K8	7 to 6	E14	V	CMRR1 = 20 log 101 x 38 V / |E14-E15|	75		dB
			"	"	"	"	38 V	38 V	"	"	"	"	"	"	"	"	"	"	"	"	E15	"				
	I_{SINK}	18	"	"	"	"	GND	15 mV	2 mA	"	"	"	"	"	"	15 V	"		None	7	E16	V	I_{SINK} > 2 mA if E16 = limit		1.2	V
	I_{SOURCE}	19	"	"	"	"	15 mV	GND	-.4 mA	"	"	"	"	"	"	"	"		"	"	E17	V	I_{SOURCE} < -0.4 mA if E17 = limit	2.5		V
	V_{OH1}	20	"	"	"	"	15 mV	"	15 kΩ to GND	"	"	"	"	"	"	"	"		K3	"	E18	V	V_{OH1} = E18	4.3		V
	V_{OL1}	21	"	"	"	"	GND	15 mV	15 kΩ to V_{REF}	"	"	"	"	"	"	"	"		K1,K3	"	E19	V	V_{OL1} = E19		2.5	V
	A_V	22	"	Pin 5	"	"	V_{REF}	GND	1.5 V 8/	0 V 4/	"	"	"	15 V 5/	"	"	"		None	"	E20	V	$A_V = \frac{(E21 - E20)}{1\ V}$ 4/ 6/ 7/ 8/	2.5	3	
			"	"	"	1 V	"	"	4.5 V 9/	"	"	"	"	"	"	"	"	"	"	"	E21	V				
	V_{DIFF}	23	"	"	"	1 V 8/	"	"	15 kΩ to GND	"	"	"	"	"	"	"	"		K3	4 to 3	E22	V	V_{DIFF} = E22 4/ 6/ 7/ 8/	1.1		V
	V_{IO2}	24	0.5 V	"	"	-40 mV 7/ 8/	"	"	Open	"	"	"	"	"	"	"	"		None	"	E23	mV	V_{IO2} = E23 4/ 6/ 7/ 8/	-25	25	mV
	CMRR2	25	"	"	1 V	"	"	"	"	"	"	"	"	"	"	"	"		"	"	E24	mV	CMRR2 = 20 log 11 V / |E25-E24| 4/ 6/ 7/ 8/	60		dB
			"	"	12 V	"	"	"	"	"	"	"	"	"	"	"	"		"	"	E25	mV				
	$-I_{IB2}$	26	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"		"	3	I3	μA	$-I_{IB2}$ = I3 4/ 6/ 7/ 8/	-10		μA
	$+I_{IB2}$	27	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	4	I4	mA	$+I_{IB2}$ = I4 4/ 6/ 7/ 8/	-10		μA

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/ 1 C.L. adj.	2 V_{REF}	3 Cur. Sense −	4 Cur. Sense +	5 Error Amp +	6 Error Amp −	7 Comp.	8 C_T	9 R_T	10 Sync	11 Output A	13 V_C	14 Output B	15 V_{IN}	16 Shut-down	V_N	Energ. relays	Measured (pin(s) No.	Val.	Unit	Notes and equations	Limits Min	Max	Unit
1 T_C = +25°C	I_{IO2}	28																					I_{IO2} = I4-I3	-1	1	μA
	V_{IO2}	29	0.5 V 9/	Pin 5	GND	GND	V_{REF}	GND	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	1	E26	V	V_{IO2} = E26 4/ 6/ 7/ 9/	0.45	0.55	V
	I_{IB3}	30	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	1	I5	μA	I_{IB3} = I5	-30		μA
	$V_{TH(LO)}$	31	15k ohms to V_{REF} 10/		"	"	"	"	"	"	"	"	"	" 5/	"	"	250 mV		"	11 14	E27 E28	V V	$V_{TH(LO)} \leq$ 250 mV if E27 or E28 = limit 4/ 5/	13 (Type 01 only)	0.4 (Type 02 only)	V
	$V_{TH(HI)}$	32	"	"	"	"	"	"	"	"	"	"	"	"	"	"	400 mV		"	11 14 1	E29 E30 E31	V V V	$V_{TH(HI)} \leq$ 0.4 V if both E29 and E30 = limit 4/ 5/ and E31 = limit	13 (Type 01 only)	0.4 (Type 02 only) 0.45	V V
	V_{NLATCH}	33	0.8 mA	Pin 5	" "	" "	" "	" "	" "	GND "	" "	" "	" "	" "	" "	" "	400 mV 0 V		None	1 "	E32 E33	V V	$V_{NLATCH} \leq$ 0.8 mA if F32 and E33 = limit	4	0.45	V V
	V_{LATCH}	34	3 mA	Pin 5	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	400 mV 0 V		"	" "	E34 E35	V V	$V_{LATCH} \geq$ 3 mA if E34 and E35 = limit		0.45 0.45	V V
	I_C	35	Open	Pin 6	"	"	GND	V_{REF}	"	"	"	"	"	"	"	40 V	0.4 V		"	13	I6	μA	I_C = I6		200	μA
	$V_{OL2A(LO)}$	36	"	Pin 5	"	"	V_{REF}	GND	"	11/	"	"	20 mA	"	"	15 V	GND		"	11	E36	V	$V_{OL2A(LO)}$ = E36		0.4	V
	$V_{OL2A(HI)}$	37	"	"	"	"	"	"	"	"	"	"	100 mA	"	"	"	"		"	"	E37	V	$V_{OL2A(HI)}$ = E37		2.1	V
	$V_{OL2B(LO)}$	38	"	"	"	"	"	"	"	"	"	"	Open	"	20 mA	"	"		"	14	E38	V	$V_{OL2B(LO)}$ = E38		0.4	V
	$V_{OL2B(HI)}$	39	"	"	"	"	"	"	"	"	"	"	"	"	100 mA	"	"		"	"	E39	V	$V_{OL2B(HI)}$ = E39		2.1	V
	$V_{OH2A(LO)}$	40	"	"	"	"	"	"	"	"	"	"	-20 mA	"	Open	"	"		"	11	E40	V	$V_{OH2A(LO)}$ = E40	13		V
	$V_{OH2A(HI)}$	41	"	"	"	"	"	"	"	"	"	"	-100 mA	"	"	"	"		"	"	E41	V	$V_{OH2A(HI)}$ = E41	12		V
	$V_{OH2B(LO)}$	42	"	"	"	"	"	"	"	"	"	"	Open	"	-20 mA	"	"		"	14	E42	V	$V_{OH2B(LO)}$ = E42	13		V
	$V_{OH2B(HI)}$	43	"	"	"	"	"	"	"	"	"	"	"	"	-100 mA	"	"		"	"	E43	V	$V_{OH2B(HI)}$ = E43	12		V

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/ 1 C.L. adj.	2 V_{REF}	3 Cur. Sense −	4 Cur. Sense +	5 Error Amp +	6 Error Amp −	7 Comp.	8 C_T	9 R_T	10 Sync	11 Output A	13 V_C	14 Output B	15 V_{IN}	16 Shut-down	V N	Energ. relays	Measured (pin(s) No.	Val.	Unit	Notes and equations	Limits Min	Max	Unit
1 T_C = +25°C	V_{SU}	44	15k ohms to V_{REF} 10/		GND	GND	V_{REF}	GND	Open	4/	Open	Open	Open	5/	Open	Raise from < 6 V to 8 V	GND		K1,K2	11 14	E44 E45	V V	V_{SU} < 8 V if E44 or E45 = limit and E46 = limit 4/ 5/	13 (Type 01)	0.4 (Type 02)	V
																				1	E46	V		4		V
	V_{SD}	45	"	"	"	"	"	"	"	"	"	"	"	"	"	Lower from > 8 V to 6 V	"		"	11 14	E47 E48	V V	V_{SD} > 6.0 V if both E47 and E48 = limit and E49 = limit 4/ 5/	13 (Type 02)	0.4 (Type 01)	V
																				1	E49	V			0.45	V
	I_{IN}	46	0.7 V	Pin 5	"	"	"	"	"	Open	"	"	"	15 V	"	15 V	GND		None	15	I7	mA	I_{IN} = I7 4/		22	mA
2 T_C = +125°C	V_{TVO}	47	Open	-1 mA	"	"	GND	V_{REF}	"	"	"	"	"	"	"	"	"		"	2	E50	V	V_{TVO} = E50	5.00	5.20	V
		48 through 92	All test parameters, test conditions, and test limits remaining are identical with tests 2-46 specified in table III, subgroup 1, T_C = +25°C.																							
3 T_C = -55°C		93 through 138	All test parameters, test conditions, and test limits remaining are identical with those specified in table III, subgroup 2, T_C = +125°C.																							
3 T_J = -55°C	L_{RESET}		Open		GND	GND	GND	GND	Open	4.7 nF to GND	10 kΩ to GND	-1 mA		15 V		15 V	GND		K9,K10	11 and 14				2/		
4 T_J = +25°C	$\frac{\Delta V_{IN}}{\Delta V_{REF}}$	139	"	Pin 6	"	"	"	V_{REF}	"	Open	Open	Open	Open	"	Open	15 V + 1 V RMS at 2.4 KHz	"		K13	2	E152	mV rms	$\Delta V_{IN}/\Delta V_{REF}$ = 20 log (1 V/E152) (See figure 4)	55		dB
	f_{OSC1}	140	"	"	"	"	"	"	"	4.7 nF to GND	10 kΩ to GND	"	"	"	"	15 V	"		K9,K10	11	F1	KHz	f_{OSC1} = 2 x F1	39	47	KHz
	$\frac{\Delta f_{OSC}}{\Delta V_{IN}}$	141	"	"	"	"	"	"	"	"	"	"	"	"	"	8 V	"		"	"	F2	KHz	$\Delta f_{OSC}/\Delta V_{IN}$ = 100(F3 - F2)/F2	-2	2	%
			"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"			"	F3	KHz				
	A_{VS}	142	"	Open	"	"	2 V	2 V	"	Open	Open	"	"	"	"	15 V	"	1.2 V	K5,K7 K8	7 to 6	E153	V	$A_{VS} = 20 \log \frac{101 \times 1.8\ V}{\lvert E154-E153 \rvert}$	80		dB
			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	3 V	"	"	E154	V				
	PSRR1	143	"	"	"	"	"	"	"	"	"	"	"	"	"	8 V	"	2 V	"	"	E155	V	$PSRR1 = 20 \log \frac{101 \times 32\ V}{\lvert E156-E155 \rvert}$	80		dB
			"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"	"	"	"	E156	V				

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/ 1 C.L. adj.	2 V_{REF}	3 Cur. Sense -	4 Cur. Sense +	5 Error Amp +	6 Error Amp -	7 Comp.	8 C_T	9 R_T	10 Sync	11 Output A	13 V_C	14 Output B	15 V_{IN}	16 Shut-down	V N	Energ. relays	Measured (pin(s) No.	Val.	Unit	Notes and equations	Limits Min	Max	Unit
4 T_C = +25°C	PSRR2	144	0.5 V	Pin 5	40 mV 8/	GND	V_{REF}	GND	Open	4/	Open	Open	Open	15 V 5/	Open	8 V	GND		None	3	E157	mV	PSRR2 = 20 log 32 V / |E158-E157| 4/ 6/ 8/	60		dB
			"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"		"	"	E158	mV				
5 T_C = +125°C		145, 147 through 150	(With the exception of f_{OSC2} (see test 146), all test parameters, test conditions, equations, notes and test limits are identical with those specified in table III, subgroup 4, T_C = +25°C.)																							
	f_{OSC2}	146	(Test parameters and conditions are identical with those specified in table III, subgroup 4, test 140.)																	11	F4	KHz	f_{OSC2} = 2 x F4	38	48	KHz
6 T_C = -55°C		151, through 156	(All test parameters, test conditions, equations, notes, and test limits are identical with those specified in table III, subgroup 5, T_C = +125°C.)																							
7 T_C = +25°C	N_O	157	Open	See figure 4	GND	GND	GND	V_{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	See figure 4	E175	V RMS	See figure 4 for N_O test figure and equation		200	µV RMS
	G_{BW}	158	"	See figure 7	"	"	See figure 7			"	"	"	"	"	"	"	"		"	7	F7	MHz	G_{BW} = F7 (See figure 7)	0.7		MHz
9 T_C = +25°C	t_{D1A}	159	0.7 V	Pin 5	"	See figure 9	V_{REF}	GND	Open	4.7 nF to GND	10 kΩ to GND	Open	See figure 9	15 V	See figure 9	"	"		K9,K10	11	t1	ns	t_{D1A} = t1 See figure 9		500	µV RMS
	t_{D1B}	160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t2	ns	t_{D1B} = t2 See figure 9		500	ns
	t_{D2A}	161	15 kΩ to V_{REF}	10/		GND	"	"	"	"	"	"	"	"	"	"	See figure 9		K1,K2, K9,K10	11	t3	ns	t_{D2A} = t3 See figure 9 10/		600	ns
	t_{D2B}	162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t4	ns	t_{D2B} = t4 See figure 9 10/		600	ns
	t_{rA}	163	Open	Pin 5	"	"	"	"	"	"	"	"	1 nF to GND	"	1 nF to GND	"	GND		K11,K12	11	t5	ns	t_{rA} = t5 12/		130	ns
	t_{rB}	164	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t6	ns	t_{rB} = t6 12/		130	ns
	t_{fA}	165	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	11	t7	ns	t_{fA} = t7 12/		130	ns
	t_{fB}	166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t8	ns	t_{fB} = t8 12/		130	ns

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/																Energ. relays	Measured (pin(s)			Notes and equations	Limits		Unit
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V_N						Min	Max	
			C.L. adj.	V_{REF}	Cur. Sense		Error Amp		Comp.	C_T	R_T	Sync	Output A	V_C	Output B	V_{IN}	Shut-down			No.	Val.	Unit				
					−	+	+	−																		
10 T_C = +125°C	t_{rA}	167	Open	Pin 5	GND	GND	V_{REF}	GND	Open	4.7 nF to GND	10 kΩ to GND	Open	1 nF to GND	15 V	1 nF to GND	15 V	GND		K11,K12	11	t9	ns	t_{rA} = t9 12/		130	ns
	t_{rB}	168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t10	ns	t_{rB} = t10 12/		130	ns
	t_{fA}	169	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	11	t11	ns	t_{fA} = t11 12/		130	ns
	t_{fB}	170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t12	ns	t_{fB} = t12 12/		130	ns
11 T_C = -55°C		171 through 174	All test parameters, test conditions, equations, notes, and test limits are identical with those specified in table III, subgroup 10, (T_C = +125°C.)																							

1/ Pin 12 = ground.
2/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWM LATCH SET command. To minimize the effects of self heating, the test must be completed within the first 50 ms of applied power. The minimum limit shall be equal to 0.49 times the oscillator frequency.
3/ t < 100 ms, continuous I_{OS} will be less that indicated limits.
4/ Test may need to be preceeded by a PWN LATCH RESET pulse. To reset latch, see figure 8.
5/ Digital logic methods may be used to determine the "on" or "off" status of the outputs (pins 11, 14). The voltage applied to the V_C pin (13) and the (min, max) limits may then be changed to accommodate the appropriate logic levels.
6/ Measured at trip point of latch.
7/ Voltage on pin 4 measured and or applied with respect to voltage at pin 3.
8/ Raise voltage on designated pin until both outputs are in the off state. (0.4 V maximum for type 01, 13 V minimum for type 02.) See note 5.
9/ Lower voltage on designated pin until both outputs are in the off state. (0.4 V maximum for type 01, 13 V minimum for type 02.) See note 5.
10/ To enable testing of the intended shutdown path, pin 1 must be pulled up by a minimum of 250 μA (at pin 1 = 0.5 V).
11/ For type 01 V_{OL} and type 02 V_{OH}, pin 8 = 5 V. For type 02 V_{OL} and type 01 V_{OH}, see note 13.
12/ Measured from 1 V to 11 V at device pins 11 and 14, to 12 (not at adapter pins), see table I, note 8.
13/ Toggle flip flop to turn on desired output (see figure 8).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

TABLE IV. Group C end-point electrical parameters. T_C = +25°C.

Table III test number	Device types	Test	Limit		Unit	Delta		
			Min	Max		Min	Max	
13	01, 02	V_{IO1}	-5.0	+5.0	mV	-0.7	+0.7	mV
14	01, 02	$\pm I_{IB}$	-1.0		μA	-0.1	+0.1	μA
1	01, 02	V_{REF}	+5.00	+5.10	V	-20	+20	mV

1/ Delta limits apply to the measured value (see MIL-M-38510).

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables. Electrical test circuits as prescribed herein or in the referenced test methods of MIL-STD-883 shall be acceptable. Other test circuits shall require the approval of the qualifying activity.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Current values are given for conventional current and are positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cooldown procedures. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, they shall be cooled to within 10°C of their power stable condition at room temperature prior to the removal of the bias.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. Part or Identifying Number (PIN) (see 1.2).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirements for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

h. Requirements for product assurance options.

i. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number.

j. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

L_{RESET}	-	Cold start/PWM latch.
V_{TVO}	-	Total variation of output voltage.
V_{SOL} and V_{SOH}	-	Sync output voltage (high and low levels) of the oscillator section.
V_{SIL} and V_{SIH}	-	Sync input voltage (high and low levels) of the oscillator section.
I_{SYNC}	-	Sync input current.
I_{SINK}	-	Output sync current (compensation pin) of the error amplifier.
I_{SOURCE}	-	Output source current (compensation pin) of the error amplifier.
V_{DIFF}	-	Maximum differential input signal (negative and positive current) sense pin voltages.
V_{CLO}	-	Current limit offset voltage.
V_{TH}	-	Threshold voltage of the shutdown section.
V_{LATCH}	-	Latching voltage of the shutdown terminal.
V_{NLATCH}	-	Nonlatching voltage of the shutdown terminal.
V_{SU}	-	Start-up threshold voltage.
V_{SD}	-	Shutdown threshold voltage.

6.4 Logistic support. Lead material and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification shall functionally replace the generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	UC1846
02	UC1847

6.6 Part or Identifying Number (PIN). The PIN is created as specified in MIL-M-38510.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - MI
Air Force - 11, 19, 85, 99
Navy OS, SH
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1175)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1. DOCUMENT NUMBER	2. DOCUMENT TITLE
MIL-M-38510/702	Microcircuits, Linear, Regulating Pulse-Width, Modulators, Monolithic Silicon

3a. NAME OF SUBMITTING ORGANIZATION	4. TYPE OF ORGANIZATION *(Mark one)*
	☐ VENDOR
b. ADDRESS *(Street, City, State, ZIP Code)*	☐ USER
	☐ MANUFACTURER
	☐ OTHER *(Specify)*: _____

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

6. REMARKS

7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional	b. WORK TELEPHONE NUMBER *(Include Area Code)* – Optional
c. MAILING ADDRESS *(Street, City, State, ZIP Code)* – Optional	8. DATE OF SUBMISSION *(YYMMDD)*

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