

MILITARY SPECIFICATION

Inactive for new design as of 23 August 1996

MICROCIRCUITS, DIGITAL, BIPOLAR, SCHOTTKY TTL,  
FLIP-FLOPS, CASCADABLE, MONOLITHIC SILICON

This amendment forms a part of MIL-M-38510/71C, dated  
23 July 1984, and is approved for use by all  
Departments and Agencies of the Department of Defense.

PAGE 1

Title: Delete and substitute as printed above.

1.2.3, add the following new case outlines:

- "2 C-2 (20-terminal, .350" x .350"), square chip carrier package
- "X C-2A (20-terminal, .350" x .350"), square chip carrier package"

1.3, thermal resistance, junction-to-case (Q<sub>JC</sub>), delete and substitute the following:

\*Thermal resistance, junction-to-case (Q<sub>JC</sub>):  
Cases A, B, C, D, E, F, 2, and X ----- (See appendix C of MIL-M-38510)\*

PAGE 2

1.4, delete "(See figure 5 for individual device type input-setup time and input-hold times.)" and substitute "(See figures 5 through 16 for individual device type input-setup time and input-hold time.)"

3.2.4, delete in its entirety and substitute the following:

"3.2.4 Schematic circuits. Schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in the specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS) as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained by the agent activity and will be available upon request."

The attached insertable replacement pages listed below are replacements for stipulated pages. When the new pages have been entered in the document, insert the amendment as the cover sheet to the specification.

<u>Replacement page</u>	<u>Page replaced</u>
11	11
12	Reprinted without change
19	19
20	20

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PAGE 3

\* TABLE I, delete table I and substitute the following: (alter change made by previous amendment)

"TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	All	2.5 <u>2/</u>		V
Low-level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA	All		0.5 <u>2/</u>	V
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, T <sub>C</sub> = +25°C	All		-1.2	V
Low-level input current at D input	I <sub>IL1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	01		-2.0	mA
Low-level input current at clear input	I <sub>IL2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	01		-6.0	mA
Low-level input current at preset input	I <sub>IL3</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	01		-4.0	mA
Low-level input current at clock input	I <sub>IL4</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	01		-4.0	mA
			02, 03			
Low-level input current at J or K input	I <sub>IL1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	02, 03 04		-1.6	mA
Low-level input current at clear input	I <sub>IL2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	02		-7.0	mA
Low-level input current at clear input	I <sub>IL2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	04		-14.0	mA
Low-level input current at preset input	I <sub>IL3</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	02, 03 04		-6.0	mA
Low-level input current at clock input	I <sub>IL4</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	04		-8.0	mA
Low-level input current, all inputs	I <sub>IL1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	05, 06		-2.0	mA
High-level input current at J, K, or D inputs	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	01, 02 03, 04		50	μA
High-level input current at clear input	I <sub>IH2</sub>		01		150	μA

See footnotes at end of table."

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PAGE 4

TABLE I, propagation delay time, low-to-high level, clock to Q or  $\bar{Q}$ , maximum limits column: Delete "13.0" and substitute "16.0".

PAGE 7

TABLE I, footnote 2/, delete and substitute:

"2/ At  $T_C = +125^\circ\text{C}$ ,  $V_{IL} = 0.7\text{ V}$ ,  $V_{OL}$  maximum = 0.45 V."

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TABLE II, interim electrical parameters test requirements: Delete "(pre burn-in)".

TABLE II, group A test requirements, class B devices: Add "10, 11".

TABLE II, additional electrical subgroups for group C periodic inspections: Delete in its entirety.

4.2a(1), delete and substitute as follows: (alter change made by previous amendment)

"(1) Test condition D or E, using the circuit shown on figure 4, or equivalent. Test condition A and the applicable test circuit shall be allowed with the approval of the qualifying activity."

4.2b., delete and substitute the following:

"b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical test parameters prior to burn-in is optional at the discretion of the manufacturer."

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FIGURE 4, resistor connected to  $V_{CC}$  terminal: Delete "R" and substitute "R<sub>1</sub>".

FIGURE 4, resistor connected to K2 terminal: Delete "R<sub>1</sub>" and substitute "R<sub>2</sub>".

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FIGURE 4, resistors connected to pins 4 and 14: Delete "R<sub>13</sub>" and substitute "R<sub>11</sub>".

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FIGURE 5, note 3: After  $t_A = 10\text{ ns}$ , add " $\pm 20\%$ "; after  $t_B = 10\text{ ns}$ , add " $\pm 20\%$ ".

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FIGURE 11, note 1: After 80 MHz, add "50% duty cycle"; after 60 MHz, add "50% duty cycle".

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TABLE III, pin designations, delete and substitute the following:

Cases														
X,2 11/	2	3	4	6	8	9	10	12	13	14	16	18	19	20
A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	CLR1	D1	CLK1	PRE1	Q1	$\bar{Q}1$	GND	$\bar{Q}2$	Q2	PRE2	CLK2	D2	CLR2	$V_{CC}$

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TABLE III, test numbers 25 and 26, minimum limits column: Delete "-1" and substitute "-0.5" (two places).

TABLE III, test numbers 27 and 28, minimum limits column: Delete "-3" and substitute "-1.5" (two places).

TABLE III, test numbers 29 and 30, minimum limits column: Delete "-2" and substitute "-1.0" (two places).

TABLE III, test numbers 31 and 32, minimum limits column: Delete "-2" and substitute "-1.0" (two places).

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TABLE III, subgroup 2: Delete " $V_{IL} = 0.8 V$ " (as substituted in previous amendment) and substitute " $V_{IL} = 0.7 V$ ".

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TABLE III, test numbers 96 through 99, maximum limits column: Delete "10" and substitute "11.5".

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Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs:  $A = 2.4 V$ ,  $B = 0.4 V$ ."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/ Outputs:  $H \geq 1.5 V$ ,  $L \leq 1.5 V$ ."

Footnote 6/: Delete "Q" and substitute " $\bar{Q}$ ".

Following footnote 10/, add footnote 11/ as follows:

"11/ Cases 2 and X pins not designated are NC."

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TABLE III, pin designations, delete and substitute as follows:

Cases																
2,X <u>10</u> /	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20
E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	CLK1	K1	J1	PRE1	Q1	$\bar{Q}1$	$\bar{Q}2$	GND	Q2	PRE2	J2	K2	CLK2	CLR2	CLR1	V <sub>CC</sub>

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TABLE III,  $I_{IL2}$ , test numbers 31 and 32, maximum limits column: Delete "-6.0" and substitute "-7.0".

TABLE III, test number 33, maximum limits column: delete "." and substitute "-6.0".

TABLE III, device type 02,  $I_{IL4}$ , test numbers 35 and 36, minimum limits column: Add "11".

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TABLE III, subgroup 2: Delete " $V_{IL} = 0.8 V$ " (as substituted in previous amendment) and substitute " $V_{IL} = 0.7 V$ ".

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TABLE III, test numbers 108 through 111, maximum limits column: Delete "." and substitute "9.75".

TABLE III, test number 112, maximum limits column: Delete "." and substitute "9.0".

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Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs: A = 2.4 V, B = 0.4 V."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/  $H \geq 1.5 \text{ V}$ ,  $L \leq 1.5 \text{ V}$ ."

Following footnote 9/, add footnote 10/ as follows:

"10/ Cases 2 and X pins not designated are NC."

TABLE III, at end of the table, add footnote 11/ as follows:

"11/ For circuit B,  $I_{IL4}(\text{min})$  is -0.7 mA."

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TABLE III, pin designations, delete and substitute as follows:

Cases														
X,2 <u>11</u> /	2	3	4	6	8	9	10	12	13	14	16	18	19	20
A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	CLK1	K1	J1	PRE1	Q1	$\overline{\text{Q}}1$	GND	$\overline{\text{Q}}2$	Q2	PRE2	J2	K2	CLK2	V <sub>cc</sub>

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TABLE III, device type 03,  $I_{IL4}$ , test numbers 27 and 28, minimum limits column: Add "12".

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TABLE III, test number 51, maximum limits column: Delete "150" and substitute "250".

TABLE III, subgroup 2: Delete " $V_{IL} = 0.8 \text{ V}$ " (as substituted in previous amendment) and substitute " $V_{IL} = 0.7 \text{ V}$ ".

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TABLE III, test number 110, J1 and J2 columns : Delete "GND" and substitute "2.7" (two places).

PAGE 43

Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs: A = 2.4 V, B = 0.4 V."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/ Outputs:  $H \geq 1.5 \text{ V}$ ,  $L \leq 1.5 \text{ V}$ ."

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Following footnote 10/, add footnote 11/ as follows:

"11/ Cases 2 and X pins not designated are NC."

TABLE III, at end of the table, add footnote 12/ as follows:

"12/ For circuit B,  $I_{IL4}(\text{min})$  is -0.7 mA."

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Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs: A = 2.4 V, B = 0.4 V."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/ Outputs:  $H \geq 1.5$  V,  $L \leq 1.5$  V."

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TABLE III, pin designations, delete and substitute as follows:

Cases																
2,X g/	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20
E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	CLR	Q1	D1	D2	Q2	D3	Q3	GND	CLK	Q4	D4	Q5	D5	D6	Q6	V <sub>CC</sub>

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TABLE III,  $I_{OS}$ : Add "7". Test numbers 46 through 50, maximum limits column: Delete "7" and substitute "-100" (five places).

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TABLE III,  $I_{CEX}$ , CLK pin, test numbers 52 through 57: Delete "C" and substitute "D" (six places).

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Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs: A = 2.4 V, B = 0.4 V."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/ Outputs:  $H \geq 1.5$  V,  $L \leq 1.5$  V."

Footnote 7/: Delete and substitute: "7/ At the manufacturers' option,  $I_{OS}$  tests 45 through 50, the following alternate procedure may be used: Apply 2.75 V at test 45 Q1, test 46 Q2, test 47 Q3, test 48 Q4, test 49 Q5, and test 50 Q6, using min/max limits of -20/-50 mA."

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TABLE III,  $I_{OS}$ , V<sub>CC</sub> pin, test numbers 49 through 65: Delete "4.5 V" and substitute "5.5 V".

TABLE III,  $I_{CEX}$ , CLK pin, test numbers 58 through 65: Delete "C" and substitute "D".

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Footnote 2/: Delete in its entirety and substitute as follows:

"2/ Inputs: A = 2.4 V, B = 0.4 V."

Footnote 3/: Delete in its entirety and substitute as follows:

"3/ Outputs: H  $\geq$  1.5 V, L  $\leq$  1.5 V."

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4.4.3b, delete in its entirety.

4.4.3c(1), delete and substitute as follows: (alter change made by previous amendment)

"(1) Test condition D or E, using the circuit shown on figure 4, or equivalent. Test condition A and the applicable test circuit shall be allowed with the approval of the qualifying activity."

The margins of this amendment are marked with asterisks to indicate where changes (additions, modifications, corrections, deletions) from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

CONCLUDING MATERIAL

Custodians:

Army - ER  
Navy - EC  
Air Force - 17

Preparing activity:  
DLA - CC

Review activities:

Army - AR, MI, SM  
Navy - AS, CG, MC, OS, SH, TD  
Air Force - 19, 85, 99

(Project 5962-1794)

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Pin number			Pin name									
Cases			Device type 01		Device type 02		Device type 03		Device type 04	Device type 05		Device type 06
2 and X	E and F	A,B,C, and D	2 and X	A,B,C, and D	2 and X	E and F	2 and X	A,B,C, and D	A,B,C, and D	2 and X	E and F	E and F
1	1	1	NC	CLR1	NC	CLK1	NC	CLK1	CLR	NC	CLR	CLR
2	2	2	CLR1	D1	CLK1	K1	CLK1	K1	K1	CLR	Q1	Q1
3	3	3	D1	CLK1	K1	J1	K1	J1	J1	Q1	D1	Q1
4	4	4	CLK1	PRE1	J1	PRE1	J1	PRE1	PRE1	D1	D2	D1
5	5	5	NC	Q1	PRE1	Q1	NC	Q1	Q1	D2	Q2	D2
6	6	6	PRE1	Q1	NC	Q1	PRE1	Q1	Q1	NC	D3	Q2
7	7	7	NC	GND	Q1	Q2	NC	GND	GND	Q2	Q3	Q2
8	8	8	Q1	Q2	Q1	GND	Q1	Q2	Q2	D3	GND	GND
9	9	9	Q1	Q2	Q2	Q2	Q1	Q2	Q2	Q3	CLK	CLK
10	10	10	GND	PRE2	GND	PRE2	GND	PRE2	PRE2	GND	Q4	Q3
11	11	11	NC	CLK2	NC	J2	NC	J2	J2	NC	D4	Q3
12	12	12	Q2	D2	Q2	K2	Q2	K2	K2	CLK	Q5	D3
13	13	13	Q2	CLR2	PRE2	CLK2	Q2	CLK2	CLK	Q4	D5	D4
14	14	14	PRE2	V <sub>cc</sub>	J2	CLR2	PRE2	V <sub>cc</sub>	V <sub>cc</sub>	D4	D6	Q4
15	15		NC		K2	CLR1	NC			Q5	Q6	Q4
16	16		CLK2		NC	V <sub>cc</sub>	J2			NC	V <sub>cc</sub>	V <sub>cc</sub>
17			NC		CLK2		NC			D5		
18			D2		CLR2		K2			D6		
19			CLR2		CLR1		CLK2			Q6		
20			V <sub>cc</sub>		V <sub>cc</sub>		V <sub>cc</sub>			V <sub>cc</sub>		

FIGURE 2. Terminal connections.

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Device type 01

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

Device type 02

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

Device type 03

Inputs				Outputs	
Preset	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

Device type 04

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

H = High level (steady state).

L = Low level (steady state).

X = Irrelevant.

↑ = Transition from low to high level.

↓ = Transition from high to low level.

Q<sub>0</sub> = The level of Q before the indicated input conditions were established.

Toggle: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

\*This configuration is unstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Device types 05 and 06  
(each flip-flop)

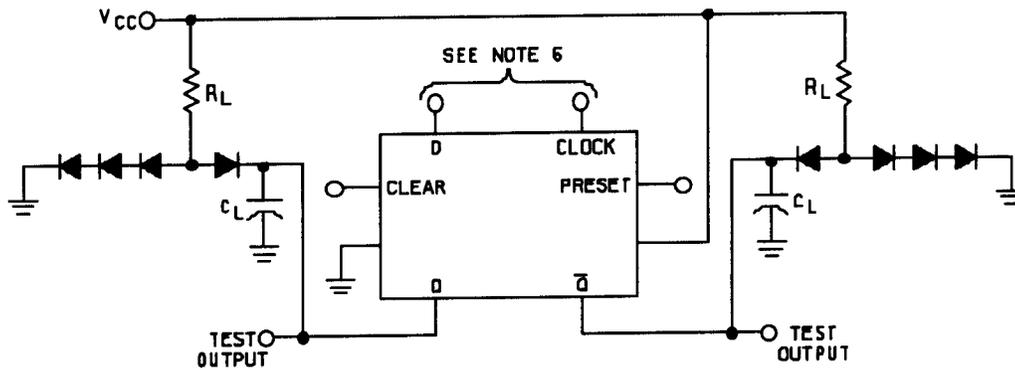
Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}^\dagger$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

† = device type 06 only.

FIGURE 3. Truth tables.

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NOTES:

1.  $t_r = t_f \leq 2.5$  ns,  $t_{(SETUP)} L = 5$  ns,  $t_{(HOLD)} L = 3$  ns,  
 $t_{(SETUP)} H = 5$  ns,  $t_{(HOLD)} H = 3$  ns,  $PRR \leq 1$  MHz,  $t_d = 10$  ns.
2. When testing  $F_{MAX}$  for subgroup 9, IN(D)  $PRR = 75$  MHz with  $t_d = 6$  ns  
and for subgroups 10 and 11, IN(D)  $PRR = 55$  MHz with  $t_d = 8$  ns.
3.  $C_L = 50$  pF  $\pm 10$  percent, including jig and probe capacitance.
4.  $R_L = 280\Omega \pm 5$  percent.
5. All diodes are 1N3064, or equivalent.
6. See table III for input conditions.
7. Setup and hold time functionality may be verified by separate test  
from propagation delay tests, by monitoring the output at specified  
setup hold conditions.

FIGURE 6. Synchronous waveforms and test circuit type 01.

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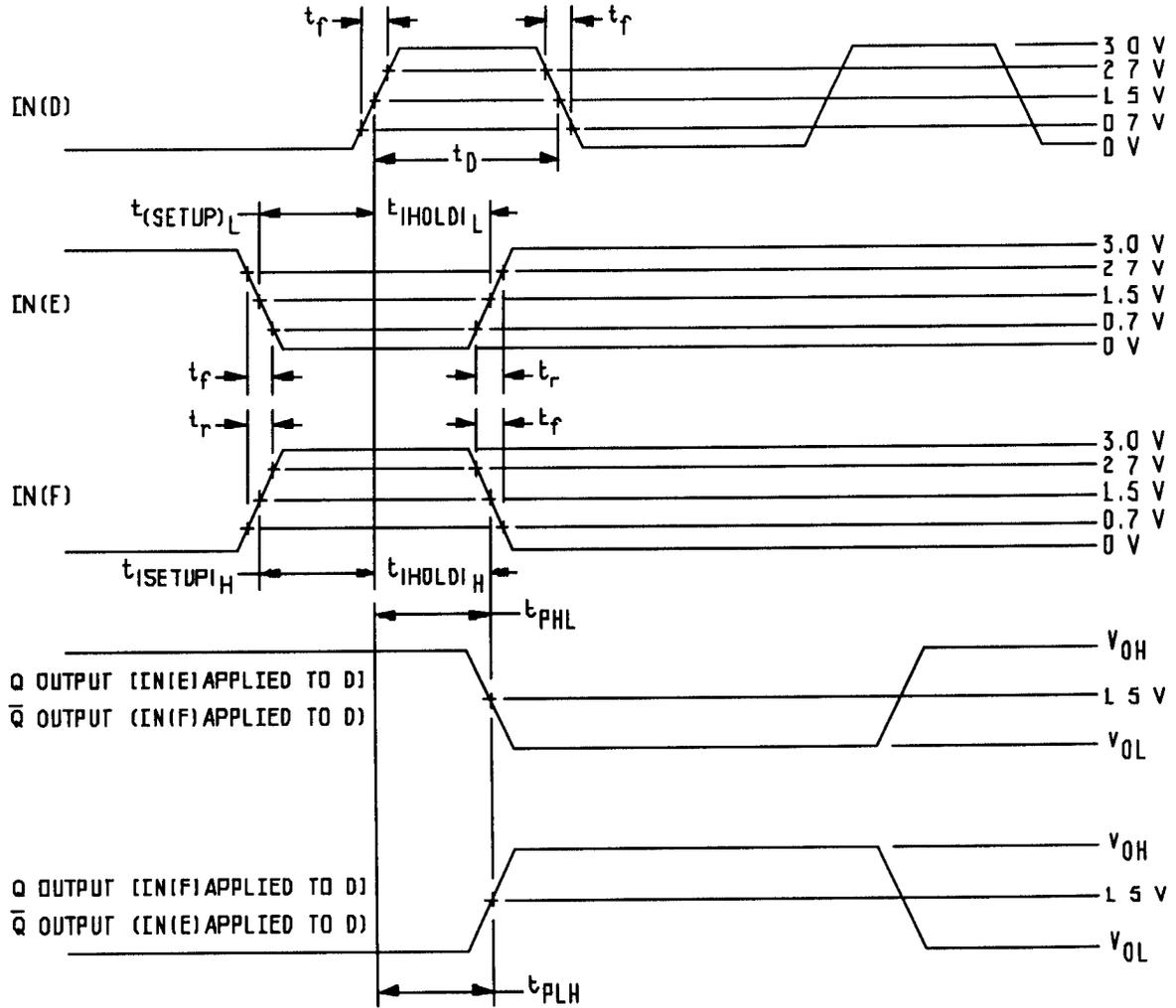


FIGURE 6. Synchronous waveforms and test circuit type 01 - Continued.

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