

Qualification requirements have been removed for device type 02. See scope.

MIL-M-38510/76B
4 December 1985
SUPERSEDING
MIL-M-38510/76A
7 November 1983

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR SCHOTTKY TTL, CASCADABLE, SHIFT REGISTERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, Schottky TTL, shift register microcircuits. Qualification requirements are removed for device type 02. This device type is inactive for new design after the date of this revision. For the remaining device type 01, two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, with the exception that the "JAN" or "J" certification mark shall not be used for device type 02.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	4 bit cascadable bidirectional shift register
02 <u>2/</u>	4 bit cascadable parallel-access shift register

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.

Supply voltage range- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range - - - - -	-1.2 V dc at -18 mA to +5.5 V dc
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P _D) <u>1/</u>	
Device type 01- - - - -	700 mW dc
Device type 02 <u>2/</u> - - - - -	700 mW dc
Lead temperature (soldering, 10 seconds)- -	+300°C
Thermal resistance, junction-to-case (θ _{JC}):	
Cases E and F - - - - -	(See MIL-M-38510, appendix C)
Junction temperature (T _J) <u>3/</u> - - - - -	+175°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2/ Qualification requirements are removed for this device.

3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) -	2.0 V dc
Maximum low-level input voltage (V_{IL}) ^{4/}	0.8 V dc
Case operating temperature range (T_C) - -	-55°C to +125°C

Fan out

Device type 01

High logic level - - - - -	20
Low logic level - - - - -	10

Device type 02 ^{5/}

High logic level - - - - -	20
Low logic level - - - - -	10

Device type 01

Width of clock input pulse - - - - -	10 ns minimum
Width of clear input pulse - - - - -	12 ns minimum
t_p (data) - - - - -	8 ns minimum
Data input setup time - - - - -	5 ns minimum
Hold time at any input - - - - -	3 ns minimum
Mode control setup time - - - - -	11 ns minimum

Device type 02 ^{5/}

Width of clock input pulse - - - - -	10 ns minimum
Width of clear input pulse - - - - -	12 ns minimum
t_p (data) - - - - -	8 ns minimum
Shift load input setup time - - - - -	11 ns minimum
Data input setup time - - - - -	5 ns minimum
Clear input setup time - - - - -	9 ns minimum
Shift load release time - - - - -	6 ns minimum
Data hold time - - - - -	3 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

^{4/} $V_{IL} = 0.7$ V at 125°C.

^{5/} Qualification requirements removed for this device type.

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table and timing diagrams. The truth tables and timing diagrams shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Schematic circuits. Schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS) as a prerequisite for qualification. All qualified manufacturer's schematics shall be maintained by the agent activity and will be available upon request.

3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used for device type 02.

3.7 Microcircuit group assignment. The microcircuit devices covered by this specification shall be in microcircuit group number 12 (see MIL-M-38510, appendix E).

3.8 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line. Not necessarily the line producing the device type described herein. This shall apply only for device type 02.

3.9 Certification. Certification in accordance with MIL-M-38510 is not required for device type 02.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Units
				Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2.0 \text{ V}$; $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1 \text{ mA}$	01, 02 <u>3/</u>	2.5		V
		@ $T_C = +125^{\circ}\text{C}$, $V_{IL} = 0.7 \text{ V}$	02 <u>3/</u>			
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2.0 \text{ V}$; $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$	01, 02 <u>3/</u>		0.5	V
		@ $T_C = +125^{\circ}\text{C}$, $V_{IL} = 0.7 \text{ V}$	01, 02 <u>3/</u>		0.45	
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$, $T_C = 25^{\circ}\text{C}$	01, 02 <u>3/</u>		-1.2	V
High level input current, all inputs	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$	01, 02 <u>3/</u>		50	μA
High level input current, all inputs	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	01, 02 <u>3/</u>		1	mA
Low level input current, all inputs	I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$	01, 02 <u>3/</u>	-0.5	-2	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}$ <u>1/</u>	01, 02 <u>3/</u>	-40	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$ <u>2/</u>	01, 02 <u>3/</u>		130	mA
Collector cut-off current	I_{CEX}	$V_{CC} = 5.5 \text{ V}$, $V_{IH} = 5.5 \text{ V}$ $V_{OH} = 5.5 \text{ V}$	01, 02 <u>3/</u>		250	μA
Maximum clock frequency	f_{MAX}	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF}$	01	70		MHz
Propagation delay time, high-to-low level output from clear	t_{pHL1}	$R_L = 280\Omega$ (See figure 5)	01	4	28	ns
Propagation delay time, low-to-high level output from clock	t_{pLH2}		01	4	19	ns
Propagation delay time, high-to-low level output from clock	t_{pHL2}		01	4	25	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Units
				Min	Max	
Maximum clock frequency	f_{MAX}	$V_{\text{CC}} = 5.0 \text{ V}$ $C_L = 50 \text{ pF}$	02 <u>3/</u>	70		MHz
Propagation delay time, high-to-low level output from clear	t_{pHL1}	$R_L = 280\Omega$ (See figure 6)		4	28	ns
Propagation delay time, low-to-high level output from clear	t_{pLH2}			4	19	ns
Propagation delay time, high-to-low level output from clock	t_{pHL2}			4	25	ns

1/ Not more than one output should be shorted at a time.

2/ Device type:

01 - With all outputs open, inputs A thru D grounded, 5.5 V applied to S_0 , S_1 , clear, and the serial inputs, I_{CC} is tested by applying clock pulse.

02 - With the outputs open, clear at 4.5 V, shift load, J, K, and data inputs grounded, I_{CC} is measured by applying clock pulse.

3/ Qualification requirements are removed from device type 02.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices <u>1/</u>	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004)	1*,2,3,7,9,10,11	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,7,8,9,10,11	1,2,3,7,9,10,11
Group B test requirements (method 5005) subgroup 5 <u>2/</u>	1,2,3,7,8,9,10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3
Additional electrical subgroups for group C periodic inspections	N/A	None
Group D end-point electrical parameters (method 5005)	1,2,3	1,2,3

*PDA applies to subgroup 1 (see 4.2c).

1/ Class S product assurance class is not applicable for device type 02.

2/ Group B test requirements shall not apply to device type 02.

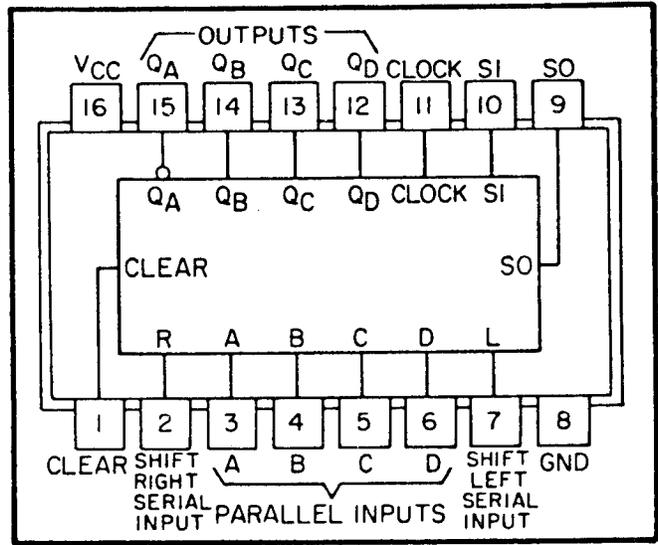
4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

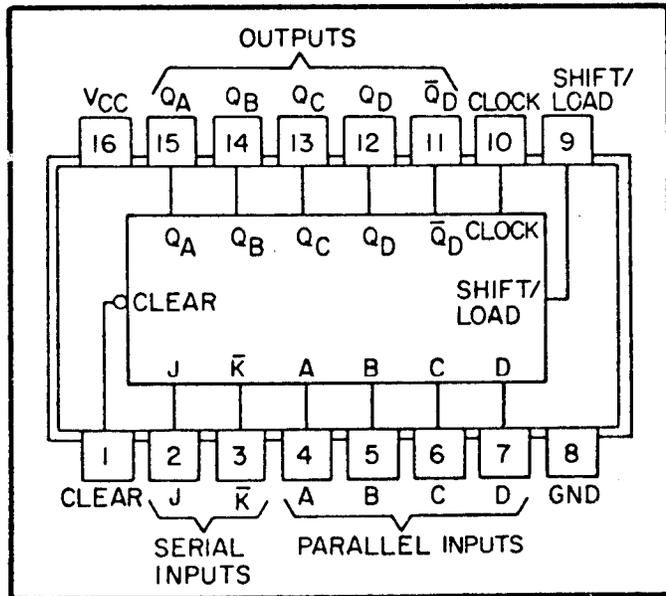
4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on device type 01 prior to qualification and quality conformance inspection, and on device type 02 prior to qualification conformance inspection. The following additional criteria shall apply:

- a. Burn-in (method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

Device type 01
Cases E and F



Device type 02
Cases E and F



NOTE: Qualification requirements removed for this device type.

FIGURE 1. Terminal connections.

Device type 01

The register has four modes of operation:

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

		INPUTS								OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

- H = high level (steady state)
- L = low level (steady state)
- X = irrelevant (any input, including transitions)
- ↑ = transition from low to high level
- a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
- $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the indicated steady state input conditions were established.
- $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ respectively, before the most-recent ↑ transition of the clock.

FIGURE 2. Truth tables and timing diagrams

Device type 01

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

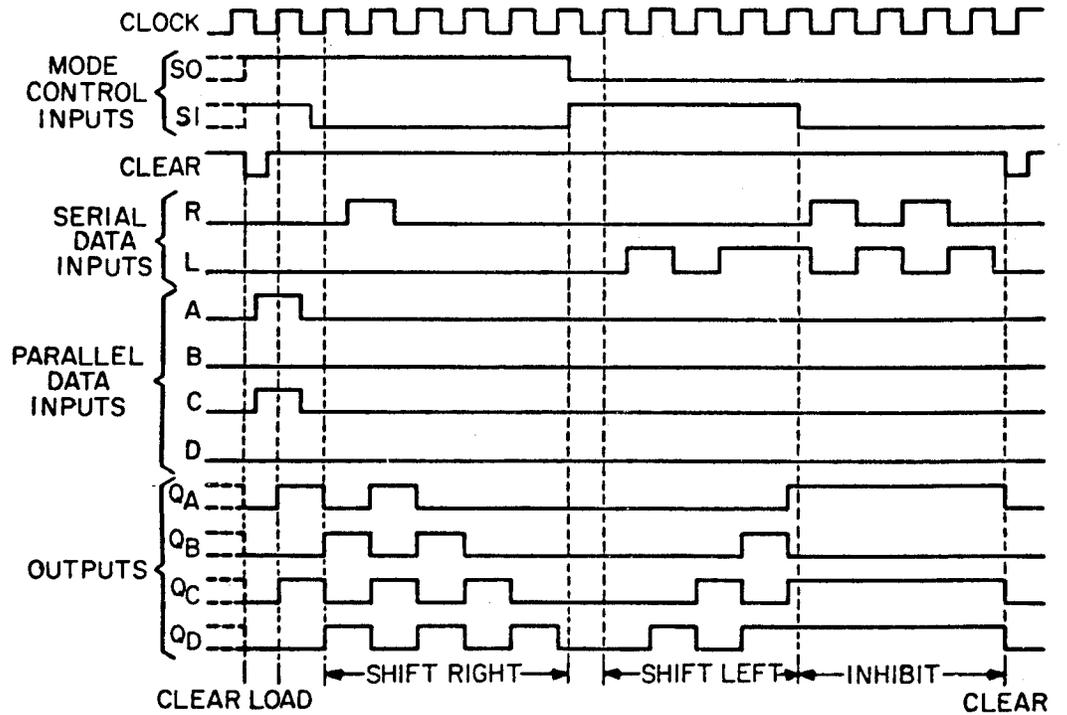


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 02

The register has two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D, or T-type flip-flop as shown in the truth table.

INPUTS					OUTPUTS								
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
			J	\bar{K}	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	\bar{d}
H	H	L	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	\bar{Q}_{DO}
H	H	↑	L	H	X	X	X	X	Q_{AO}	Q_{AO}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	H	L	X	X	X	X	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady state input at A, B, C, or D, respectively.

Q_{AO} , Q_{BO} , Q_{CO} , Q_{DO} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady state input conditions were established.

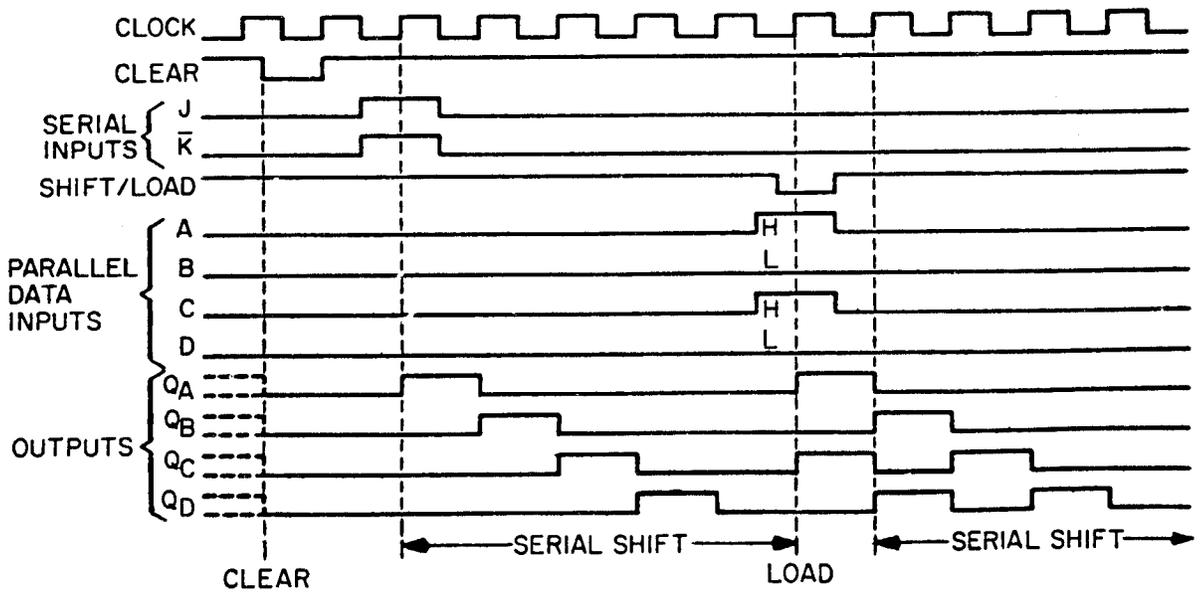
Q_{An} , Q_{Bn} , Q_{Cn} = the level of Q_A , Q_B , or Q_C , respectively, before the most-recent transition of the clock.

NOTE: Qualification requirements removed for this device type.

FIGURE 2. Truth tables and timing diagrams - Continued

Device type 02

typical clear, shift, and load sequences



NOTE: Qualification requirements removed for this device type.

FIGURE 2. Truth tables and timing diagrams - Continued

Device type 01

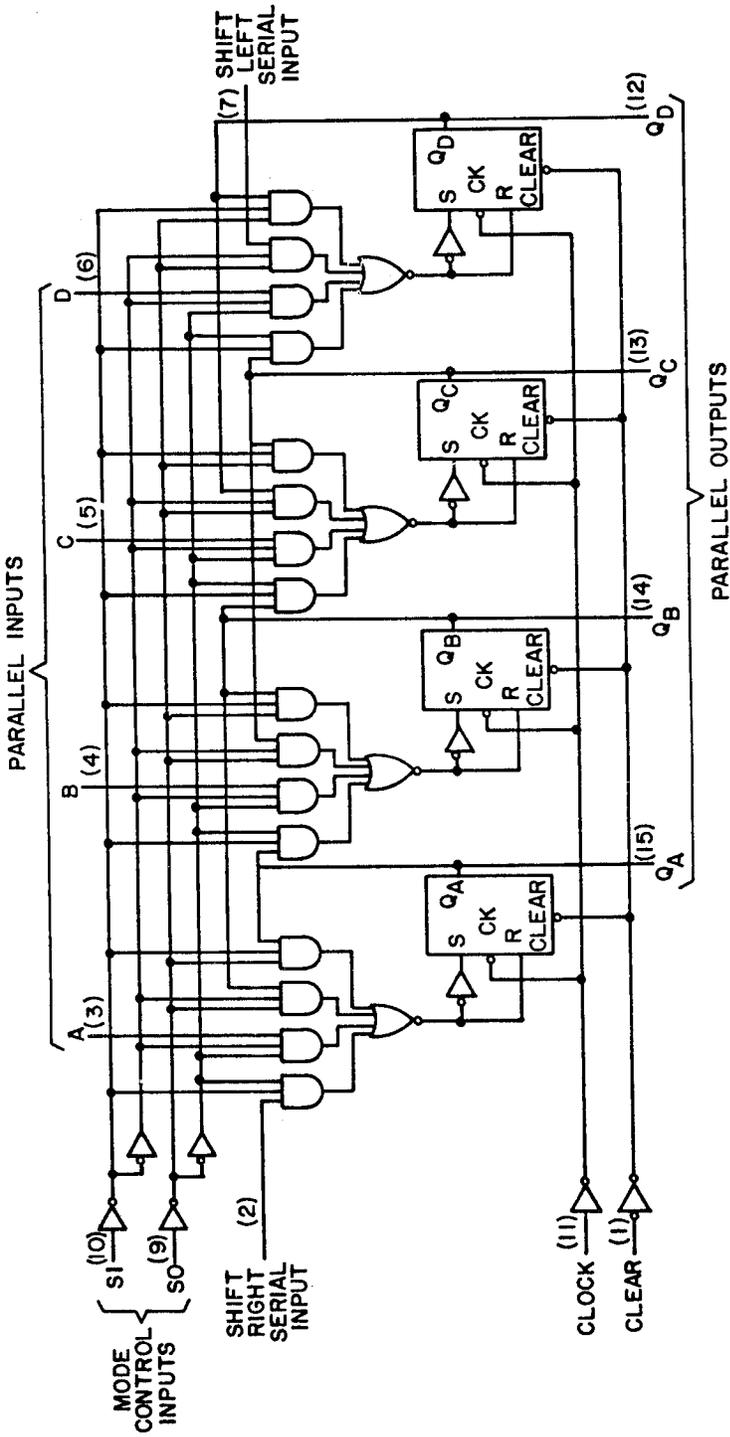
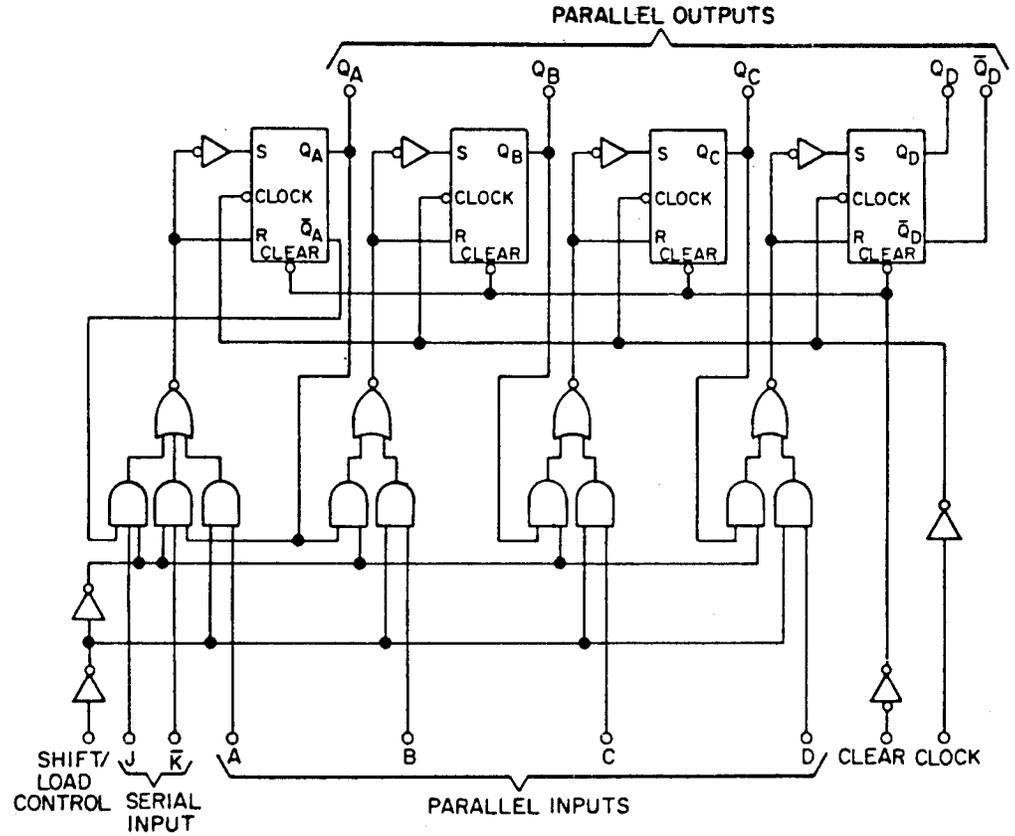


FIGURE 3. Logic diagrams.

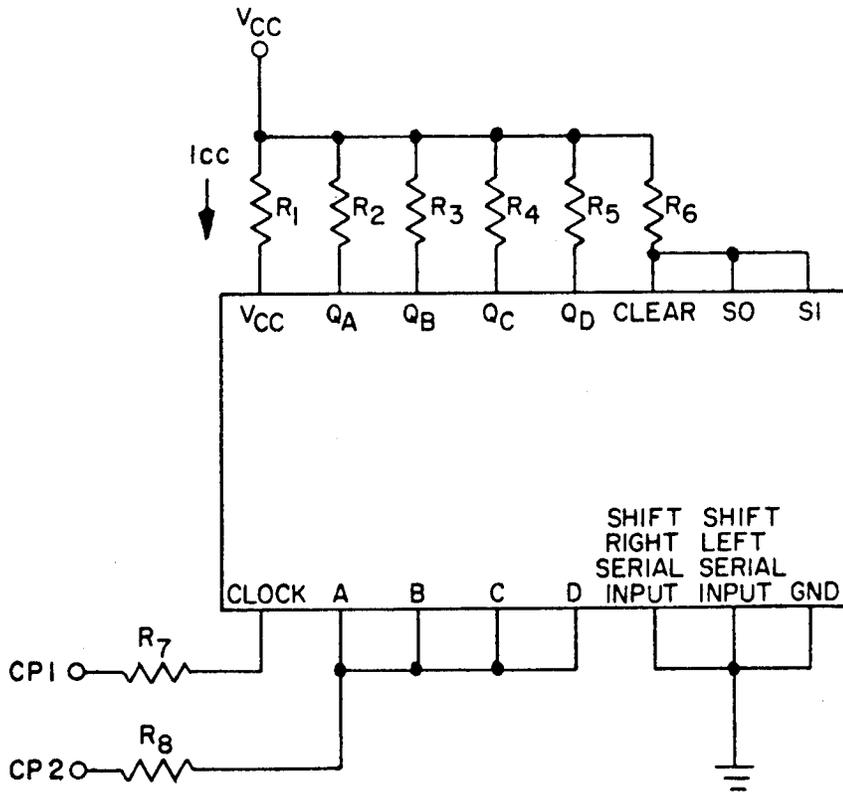
Device type 02



NOTE: Qualification requirements removed for this device type.

FIGURE 3. Logic diagrams - Continued

Device type 01

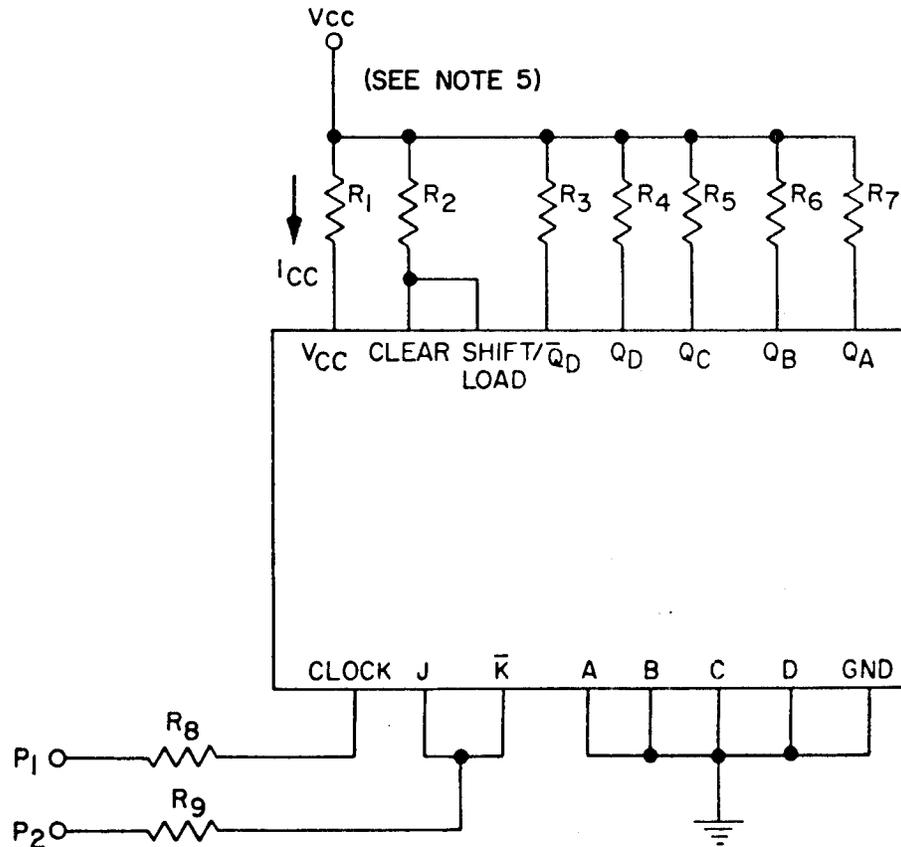


NOTES:

1. $R_2 - R_6 = 220\Omega \pm 5\%$.
 $R_7 - R_8 = 27\Omega \pm 5\%$.
2. V_{CC} and R_1 shall be chosen to insure a 5.0 V minimum at device V_{CC} terminal.
3. CP1 = 100 kHz $\pm 50\%$ square wave; duty cycle = 50 $\pm 15\%$; $V_{IL} = -0.5$ V minimum to +0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum.
4. CP2 = 50 kHz $\pm 50\%$ square wave synchronized with CP1. All other conditions are the same as CP1.

FIGURE 4. Burn-in and life test circuits.

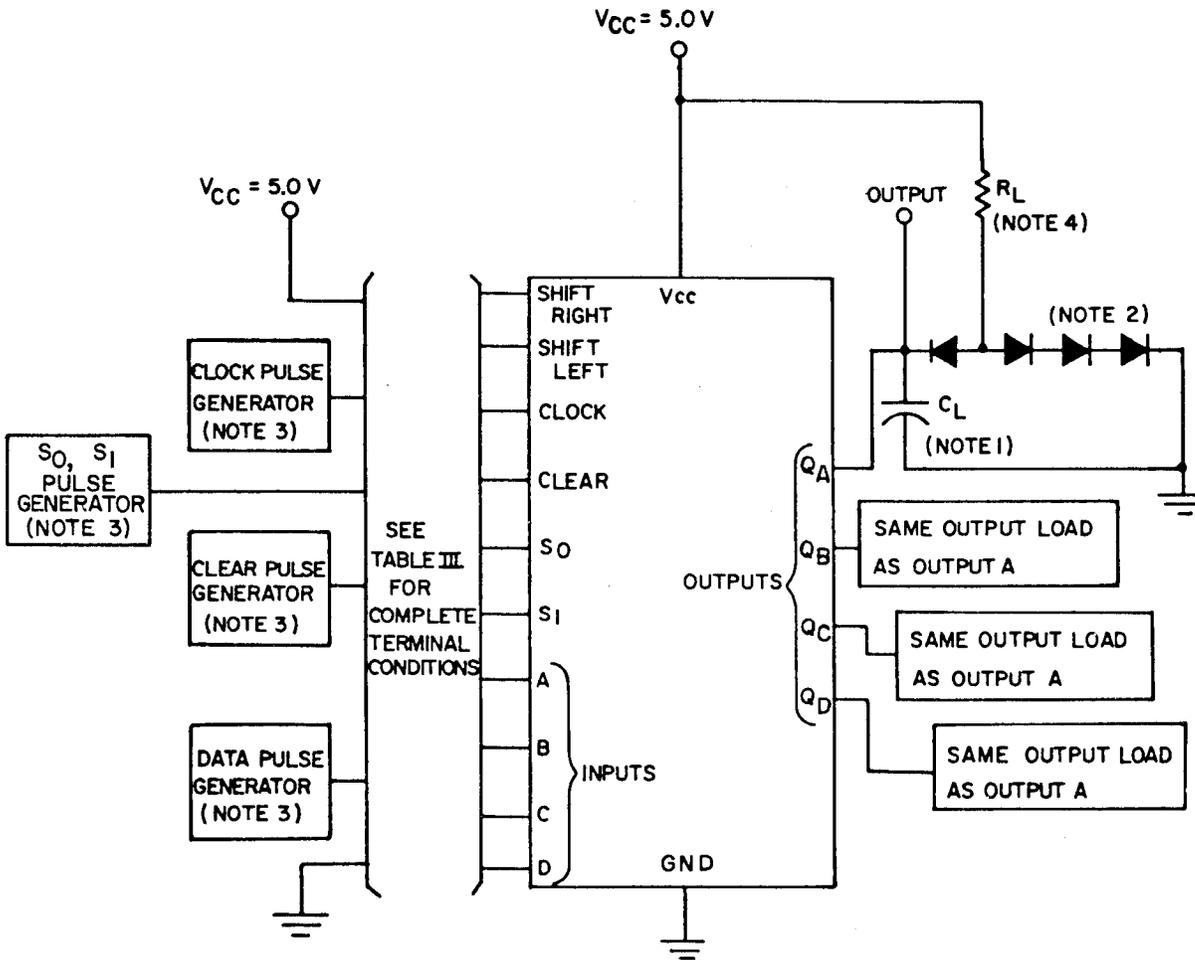
Device type 02



NOTES:

1. $R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = 220\Omega \pm 5\%$.
 $R_8 = R_9 = 27 \pm 5\%$.
2. V_{CC} and R_1 shall be chosen to insure a 5.0 V minimum at device V_{CC} terminal.
3. CP1 = 100 kHz $\pm 50\%$ square wave; duty cycle = 50 $\pm 15\%$; $V_{IL} = -0.5$ V minimum to +0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum.
4. CP2 = 50 kHz $\pm 50\%$ square wave synchronized with CP1. All other conditions are the same as CP1.
5. Qualification requirements removed for this device type.

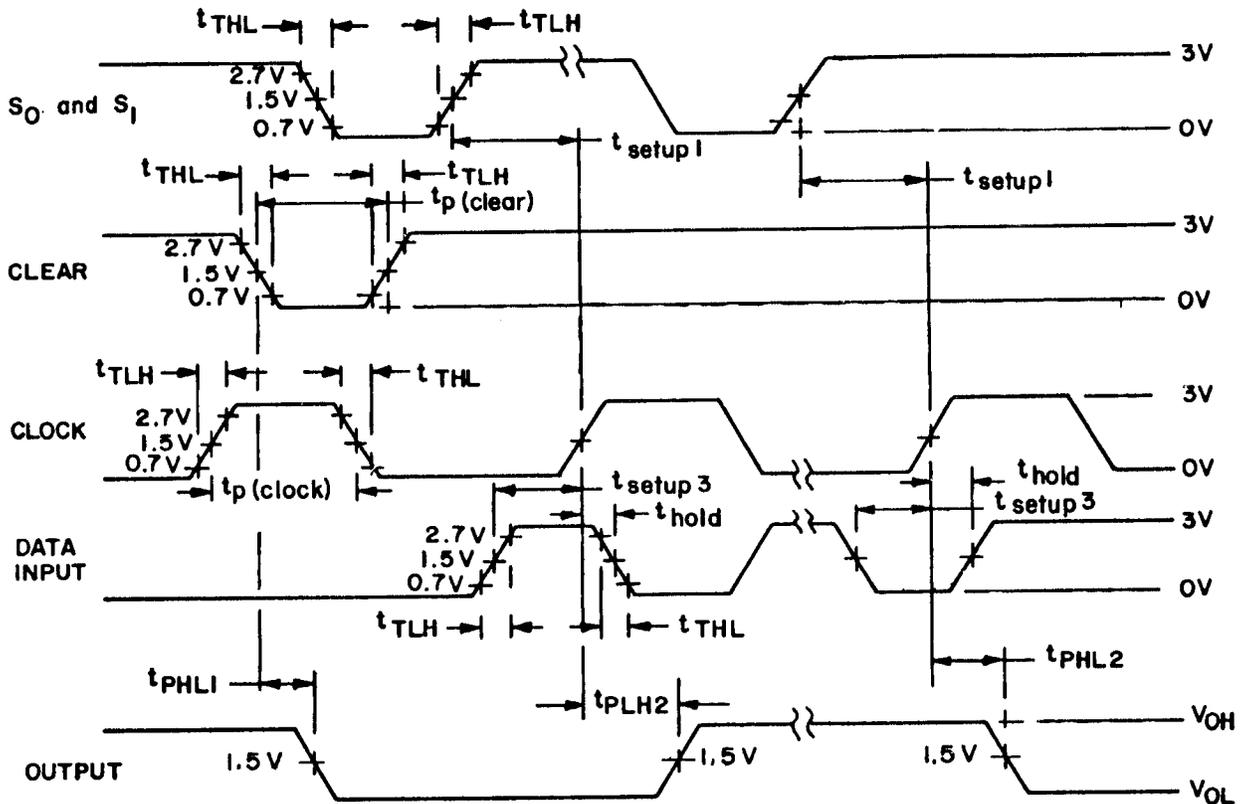
FIGURE 4. Burn-in and life test circuits - Continued.



NOTES:

1. $C_L = 50 \text{ pF} \pm 10\%$; including scope probe, wiring and stray capacitance without package in test fixture.
2. All diodes are 1N3064, or equivalent.
3. Unless otherwise specified in the notes associated with the individual tests, all pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_{TLH} \leq 2.5 \text{ ns}$.
4. $R_L = 280\Omega \pm 5\%$.

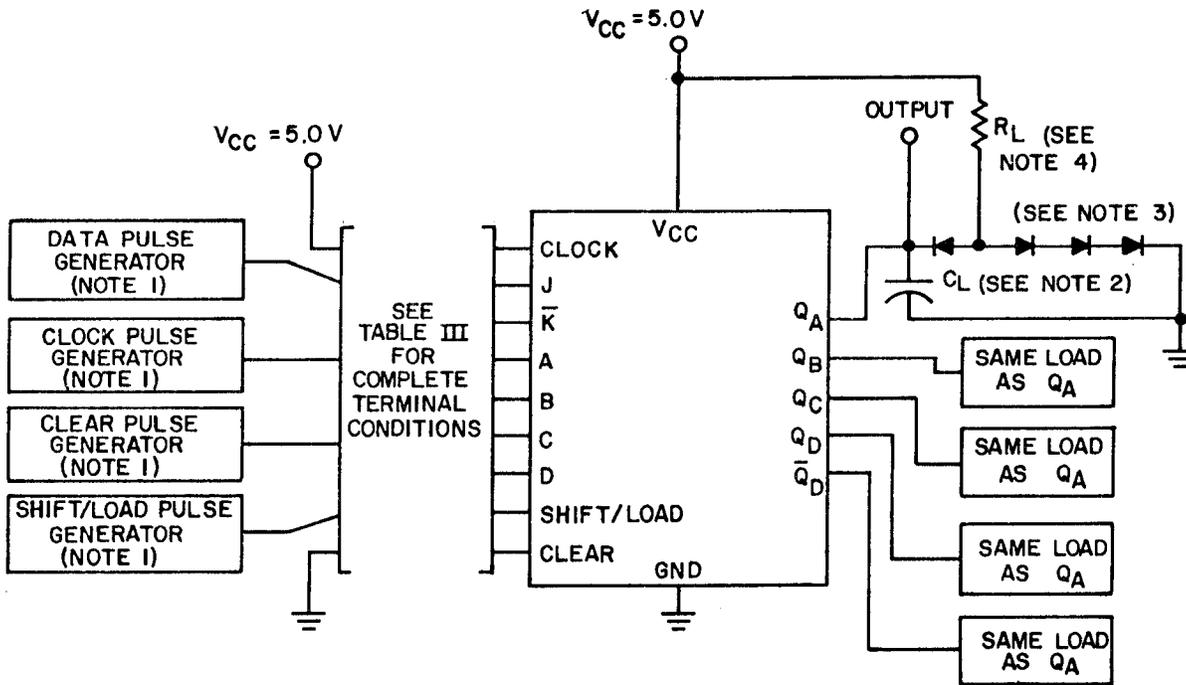
FIGURE 5. Switching test circuit and waveforms for device type 01.



NOTES:

1. S_0 and S_1 , $t_{setup} = 11$ ns.
2. The clear pulse has the following characteristics: t_p (clear) = 12 ns, and $PRR \leq 1$ MHz.
3. The data pulse has the following characteristics: t_p (data) = 8 ns, $t_{setup} = 5$ ns, $t_{hold} = 3$ ns and $PRR \leq 1$ MHz.
4. The clock pulse has the following characteristics: t_p (clock) = 10 ns, and $PRR \leq 1$ MHz for t_{PHL1} measurement and 2 MHz for t_{PLH2} and t_{PHL2} measurements.
5. For each clock-to-output t_{PLH2} and t_{PHL2} measurement the clear input is momentarily grounded then raised to and held at 3 V minimum.
6. For f_{MAX} measurement at -55°C and 125°C the clock input $PRR \leq 56$ MHz and the shift right input $PRR \leq 28$ MHz; at 25°C the clock input $PRR \leq 70$ MHz and the shift right input $PRR \leq 35$ MHz.
7. Load circuits on a given output are only required where the specific test given in table III indicated OUT on that output. Load circuits may otherwise be omitted.

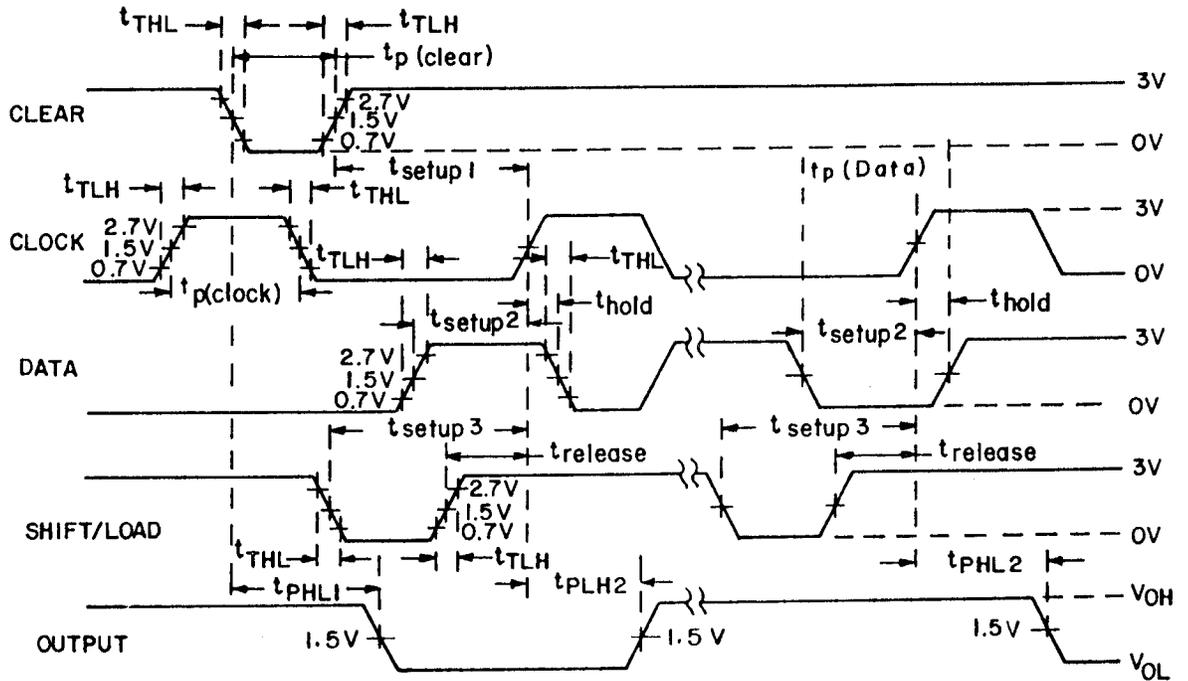
FIGURE 5. Switching test circuit and waveforms for device type 01 - Continued.



NOTES:

1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 2.5$ ns, $t_{THL} \leq 2.5$ ns, $Z_{OUT} \approx 5\Omega$.
2. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance without package in test fixture.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 280\Omega \pm 5\%$.
5. Load circuit on a given output are only required where the specific test given in table III indicates "OUT" on the output. Load circuits may otherwise be omitted.
6. Qualification requirements removed for this device type.

FIGURE 6. Switching test circuit and waveforms for device type 02



NOTES:

1. The shift/load pulse has the following characteristics: t_p (shift/load) = 5 ns minimum, $t_{\text{setup}} = 11$ ns, $t_{\text{release}} = 6$ ns maximum and $\text{PRR} \leq 2$ MHz.
2. The clear pulse has the following characteristics: t_p (clear) = 12 ns, $t_{\text{setup}} = 9$ ns, and $\text{PRR} \leq 1$ MHz.
3. The data pulse has the following characteristics: t_p (data) = 8 ns, $t_{\text{setup}} = 5$ ns, $t_{\text{hold}} = 3$ ns and $\text{PRR} \leq 1$ MHz.
4. The clock pulse has the following characteristics: t_p (clock) = 10 ns, and $\text{PRR} \leq 1$ MHz for t_{PHL1} measurement and 2 MHz for t_{PLH2} and t_{PHL2} measurements.
5. For each clock-to-output t_{PLH2} and t_{PHL2} measurement the clear input is momentarily grounded then raised to and held at 3 V minimum.
6. For f_{MAX} measurement at -55°C and 125°C the clock input $\text{PRR} \leq 56$ MHz; at 25°C the clock input $\text{PRR} \leq 70$ MHz.
7. Qualification requirements removed for this device type.

FIGURE 6. Switching test circuit and waveforms for device type 02 - Continued

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be $H \geq 2.0 V$, $L \leq 0.8 V$ or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E.F. Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit	
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S ₀	S ₁	Clock	Q _D	Q _C	Q _B	Q _A	V _{CC}		Min	Max		
$T_C = 25^\circ C$	V _{OH}	3006	1	2.0 V		2.0 V	2.0 V	2.0 V	2.0 V		GND	2.0 V	2.0 V	D							QA	2.5	V	
			2	"		"	"	"	"	"		"	"	"	"							QB	"	"
			3	"		"	"	"	"	"		"	"	"	"							QC	"	"
			4	"		"	"	"	"	"		"	"	"	"							QD	"	"
	V _{OL}	3007	5	"		0.8 V	0.8 V	0.8 V	0.8 V		"	"	"	"							QA	10.5	"	
			6	"		"	"	"	"	"		"	"	"	"							QB	"	"
			7	"		"	"	"	"	"		"	"	"	"							QC	"	"
			8	"		"	"	"	"	"		"	"	"	"							QD	"	"
	V _{IC}		9	-18 mA		-18 mA	-18 mA	-18 mA	-18 mA		"										Clear	-1.2	"	
			10																			Shift R	"	"
			11																			Input A	"	"
			12																			Input B	"	"
			13																			Input C	"	"
			14																			Input D	"	"
			15																			Shift L	"	"
			16																			S ₀	"	"
			17																			S ₁	"	"
			18																			Clock	"	"
	I _{IHL}	3009	19	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V		"	5.5 V	GND								Clear	-0.5	mA	
			20																			Shift R	"	"
			21																			Input A	"	"
			22																			Input B	"	"
			23																			Input C	"	"
			24																			Input D	"	"
			25																			Shift L	"	"
			26																			S ₀	"	"
			27																			S ₁	"	"
			28																			Clock	"	"
	I _{IHL}	3010	29	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V		"	5.5 V	GND								Clear	50	μA	
			30																		Shift R	"	"	
			31																			Input A	"	"
			32																			Input B	"	"
			33																			Input C	"	"
			34																			Input D	"	"
			35																			Shift L	"	"
			36																			S ₀	"	"
			37																			S ₁	"	"
			38																			Clock	"	"
	I _{IHL}		39	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		"	5.5 V	GND								Clear	1.0	mA	
			40																		Shift R	"	"	
			41																			Input A	"	"
			42																			Input B	"	"
			43																			Input C	"	"
			44																			Input D	"	"
			45																			Shift L	"	"
			46																			S ₀	"	"
47																			S ₁	"	"			
48																			Clock	"	"			

See notes at end of device type 01.

TABLE III. Group A inspection for for device type 01 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit					
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S0	S1	Clock	QD	QC	QB	QA	VCC	Measured terminal	Min		Max				
1 T _C = 25°C	I _{OS}	3011	49	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	D				GND	GND	5.5 V	QA	-40	-100	mA			
			50	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			51	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			52	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
	I _{CC}	3005	53	5.5 V	5.5 V	GND	GND	GND	GND	5.5 V	"	5.5 V	5.5 V	D					"	VCC			130	mA			
	I _{CEX}		54	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V		"	5.5 V	5.5 V	D				5.5 V	5.5 V	5.5 V	QA		250	μA			
			55	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			56	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			57	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = 125°C, V _{IC} tests are omitted, V _{IL} = 0.7 V and V _{OL} (max) = 0.45 V.																										
3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55°C, V _{IC} tests are omitted.																										
7 T _C = 25°C	Truth table test	3014	58	B	B	A	B	A	B	B	GND	A	A	A	L	L	L	L	L	5.0 V							
			59	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			60	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			61	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			62	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			64	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			65	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			66	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			69	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			73	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			77	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
81	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
85	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
86	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
87	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
88	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
89	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
90	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
91	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
92	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
93	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
94	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V, L < 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit		
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	GND	GND	S0	S1	Clock	Qd	Qc	Qb	Qa	Vcc		Measured terminal	Min
10	f _{MAX}	E	138	F	IN	GND	GND	GND	GND	GND	GND	5.0 V	GND	IN	OUT				5.0 V	Qd	28.0		MHz	
TC = 125°C	t _{PHL1}	3003	139	IN	15.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	IN		OUT		OUT		Clear/QA	4	28	ns	
			140	"	"	"	"	"	"	"	"	"	"	"	"						Clear/Qb	"	"	"
			141	"	"	"	"	"	"	"	"	"	"	"	"		OUT				Clear/Qc	"	"	"
			142	"	"	"	"	"	"	"	"	"	"							Clear/Qd	"	"	"	
TC = 125°C	t _{PLH2}	"	143	F	IN	IN	IN	IN	IN	IN	IN	G	G	"				OUT		Clock/QA	"	19	"	
			144	"	"	"	"	"	"	"	"	"	"	"	"						Clock/Qb	"	"	"
			145	"	"	"	"	"	"	"	"	"	"	"	"		OUT				Clock/Qc	"	"	"
			146	"	"	"	"	"	"	"	"	"	"						Clock/Qd	"	"	"		
TC = 125°C	t _{PHL2}	"	147	G	IN	IN	IN	IN	IN	IN	IN	"	"	"				OUT		Clock/QA	"	25	"	
			148	"	"	"	"	"	"	"	"	"	"	"	"						Clock/Qb	"	"	"
			149	"	"	"	"	"	"	"	"	"	"	"	"		OUT				Clock/Qc	"	"	"
			150	"	"	"	"	"	"	"	"	"	"						Clock/Qd	"	"	"		

11 Same tests, terminal conditions, and limits as subgroup 10, except Tc = -55°C.

NOTES:

- A. Terminal connected to 2.0 V minimum.
- B. Terminal connected to 0.8 V maximum.
- C. Tests shall be performed in the sequence specified. Output voltages shall be either high "H" or "L" as indicated in the terminal conditions columns. Output voltage test limits over the specified temperature range shall be either: (1) H = 2.5 V minimum and L = 0.5 V maximum when using a high speed checker double comparator, or (2) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
- D. Input is a single clock pulse.
- E. See figure 5 herein for switching test circuit and waveforms.
- F. The clear input is momentarily grounded, then raised to and held at 3.0 V minimum/5.5 V maximum.
- G. 3.0 V minimum, 5.0 V maximum.
- H. I_L = Limits shall be as follows:

Measured terminal	min/max limits (mA) for circuit			
	A	B	C	D
Clear S ₀ , S ₁	-0.7/-1.3	-1/-2	-1/-2	-1/-2
Shift, R L, A, B, C, D, Clock	-1/-2	-1/-2	-1/-2	-1/-2

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits					
				Clear	J	K	Input A	Input B	Input C	Input D	GND	Shift Load	Clock	Q ₀	Q ₀	Q ₀	Q _B	Q _A	V _{CC}	Measured terminal	Min	Max	Unit		
1 T _C = 25°C	V _{OH}	3006	1	2.0 V			2.0 V	2.0 V	2.0 V	2.0 V	GND	0.8 V	D						4.5 V	Q _A	2.5	V			
			2	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _B	"	"		
			3	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _C	"	"		
			4	"			0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	"	"	"	-1 mA	-1 mA	-1 mA	-1 mA	"	Q _D	"	"		
			5	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _D	"	"	
	V _{OL}	3007	6	2.0 V			0.8 V	0.8 V	0.8 V	0.8 V	"	"	"	"	"	"	"	"	"	"	Q _A	0.5	"		
			7	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _B	"	"		
			8	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _C	"	"		
			9	"			2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	"	"	"	20 mA	20 mA	20 mA	20 mA	"	Q _D	"	"		
			10	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q _D	"	"	
	V _{IC}		11	-18 mA																	Clear	-1.2	"		
			12	"																		J	"	"	
			13	"			-18 mA															K	"	"	
			14	"			-18 mA																A	"	"
			15	"																			B	"	"
			16	"																			C	"	"
			17	"																			D	"	"
			18	"																			Shift/Load	"	"
			19	"																			Clock	"	"
	I _{IHL}	3009	20	0.5 V																	Clear	G	"		
			21	GND	0.5 V																	J	"	"	
			22	F	5.5 V	0.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	K	"	"	
			23	"	5.5 V	0.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	"	A	"	"
			24	"	"																		B	"	"
			25	"	"																		C	"	"
			26	"	"																		D	"	"
			27	"	"																		Shift/Load	"	"
28	"	"																		Clock	"	"			
	I _{IHL1}	3010	29	2.7 V																	Clear	G	"		
			30	5.5 V	2.7 V	2.7 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	J	"	"	
			31	GND																		"	"	"	
			32	"																		"	"	"	
			33	"																		"	"	"	
			34	"																		"	"	"	
			35	"																		"	"	"	
36	"																		"	"	"				
37	"																		"	"	"				
	I _{IHL2}		38	5.5 V																	Clear	1	"		
			39	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	J	"	"	
			40	GND																		"	"	"	
			41	"																		"	"	"	
			42	"																		"	"	"	
			43	"																		"	"	"	
			44	"																		"	"	"	
45	"																		"	"	"				
46	"																		"	"	"				
																				Shift/Load	"	"			
																				Clock	"	"			

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits						
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	Shift Load	IClock	$\bar{Q}D$	QD	Qc	QB	QA	VCC	Measured terminal	Min	Max	Unit			
1	I_{OS}	3011	47	5.5 V			5.5 V	5.5 V	5.5 V	15.5 V	GND	GND	D								QA	-40	-100	mA		
			48	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QB	"	"	"	
			49	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QC	"	"	"
			50	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QD	"	"	"
			51	GND			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QD	"	"	"
2	I_{CC}	3005	52	5.5 V	GND	GND	GND	GND	GND	GND	"	"	"	"	"	"	"	"	"	"	VCC		130	mA		
			53	5.5 V			5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	"	QA	5.5 V	250	μ A	
3	I_{CEX}		54	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	QB	"	"	"		
			55	"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QC	"	"	"	
7	Truth table test	3014	58	B	B	B	B	B	B	B	B	A	A	H	L	L	L	L	L	L						
			59	A	A	A	A	A	A	A	A	A	GND	A	A	"	"	"	"	"	"	"				
7	$T_C = 25^\circ C$		60	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"					
			61	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			62	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			64	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			65	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			66	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			69	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			73	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
77	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
81	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
85	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
86	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
87	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
88	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
89	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
90	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
91	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
92	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
93	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
2	Same tests, terminal conditions, and limits as subgroup 1, except $T_C = 125^\circ C$, VIC tests are omitted, $V_{IL} = 0.7 V$ and $V_{OL} (max) = 0.45 V$.																									
3	Same tests, terminal conditions, and limits as subgroup 1, except $T_C = -55^\circ C$ and VIC tests are omitted.																									

See notes at end of device type 02.

TABLE III. Group A inspection for for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
				Clear	J	K	Input A	Input B	Input C	Input D	GND	Shift load	Clock	$\bar{Q}D$	QD	QC	QB	QA	VCC	Measured terminal	Min	Max	Unit
10 Tc = 125°C	tpHL2	"	125	IN			IN	IN			GND	IN	IN				OUT	OUT	"	Clock/QA	4	25	ns
		"	126	"				IN			"	"	"				OUT		"	Clock/QB	"	"	"
		"	127	"					IN		"	"	"		OUT		OUT		"	Clock/QC	"	"	"
		"	128	"						IN	"	"	"						"	Clock/QD	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except Tc = -55°C.																						

NOTES:

- Terminal connected to 2.0 V minimum.
- Terminal connected to 0.8 V maximum.
- Tests shall be performed in the sequence specified. Output voltages shall be either high "H" or "L" as indicated in the terminal conditions columns. Output voltage test limits over the specified temperature range shall be either: (1) H = 2.5 V minimum and L = 0.5 V maximum when using a high speed checker double comparator, or (2) H \geq 1.5 V and L < 1.5 V when using a high speed checker single comparator.
- Input is a single clock pulse.
- See figure 6 herein for switching test circuit and waveforms.
- The clear input is momentarily grounded, then raised to and held at 5.5 V.
- IIL limits shall be as follows:

Measured terminal	min/max Limits (mA) for circuit			
	A	B	C	D
Clear	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5
Shift/load				
J, K, A, B, C, D Clock	-1/-2	-1/-2	-1/-2	-1/-2
Clear	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5
Shift/load				

4.3 Qualification inspection. Qualification inspection is not required, this shall apply only for device type 02. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein. For groups A, B, C, and D inspections, see 4.4.1 through 4.4.4.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data (see 6.6) may be used to satisfy the requirements for groups C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical test requirements for device 01 shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for Government microcircuit applications (original equipment) and logistic purposes. Device type 02 is intended only for use for logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity for device type 02. In addition to that, notification to the qualifying activity for device type 01, if applicable.
- e. For device type J1, requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for packaging and packing, device type 02. Requirement for product assurance options, device type 01.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable, these requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. For device type 01, requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Ground zero voltage potential.
I _{IN}	- - - - -	Current flowing into an input terminal.
V _{IN}	- - - - -	Voltage level at an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Generic test data. This shall apply only for device type 02. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54S194
02 6/	54S195

6/ Qualification requirements removed for this device type.

6.7 Manufacturers' designators. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designations.

Device type	Manufacturer			
	Circuit A	Circuit B	Circuit C	Circuit D
	Texas Instruments	Advanced Micro Devices	Fairchild	National
01	X	X	X	X

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - SH, OS, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

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