[INCH-POUND]

MIL-M-38510/765
25 February 1991

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, ADVANCED CMOS,
SHIFT REGISTERS, MONOLITHIC SILICON, POSITIVE LOGIC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, advanced CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assurance (RHA) are provided and are reflected in the complete Part or Identifying Number (PIN).

1.2 Classification.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit
01	To be included after dating
02	To be included after dating
03	To be included after dating
04	To be included after dating
05	To be included after dating
06	8-bit bidirectional universal shift/storage register with three-state outputs
07	To be included after dating

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20 terminal, .358" x .358" x .100"), square chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441-5700 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±100 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	300 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	+3.0 V dc to +5.5 V dc
Output voltage range	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum low level input voltage (V_{IL})	0.90 V dc at V_{CC} = 3.0 V dc
	1.35 V dc at V_{CC} = 4.5 V dc
	1.65 V dc at V_{CC} = 5.5 V dc
Minimum high level input voltage (V_{IH})	2.10 V dc at V_{CC} = 3.0 V dc
	3.15 V dc at V_{CC} = 4.5 V dc
	3.85 V dc at V_{CC} = 5.5 V dc
Input rise and fall rate (t_r, t_f) maximum:	
V_{CC} = 3.6 V, V_{CC} = 5.5 V	8 ns/V

Minimum setup time, HIGH or LOW, Sn to CLK (t_{s1}): Device type 06

V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	8.5 ns
T_C = +125°C	9.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	6.0 ns
T_C = +125°C	7.0 ns

1/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back up systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq$ 70% of V_{CC}, $V_{IL} \leq$ 30% of V_{CC}, $V_{OH} \geq$ 70% of V_{CC} at -20 µA, $V_{OL} \leq$ 30% of V_{CC} at 20 µA.

	Device type 06
Minimum hold time, HIGH or LOW, Sn to CLK (t_{h1}):	
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	2.0 ns
T_C = +125°C	2.0 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	2.0 ns
T_C = +125°C	2.5 ns
Minimum setup time, HIGH or LOW, I/On to CLK (t_{s2}):	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	5.5 ns
T_C = +125°C	6.0 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	3.5 ns
T_C = +125°C	4.0 ns
Minimum hold time, HIGH or LOW, I/On to CLK (t_{h2}):	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	1.5 ns
T_C = +125°C	1.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	2.0 ns
T_C = +125°C	2.0 ns
Minimum setup time, HIGH or LOW, DS0 or DS7 to to CLK (t_{s3}):	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	6.5 ns
T_C = +125°C	7.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	4.0 ns
T_C = +125°C	5.0 ns
Minimum hold time, HIGH or LOW, DS0 or DS7 to CLK (t_{h3}):	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	1.0 ns
T_C = +125°C	1.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	1.5 ns
T_C = +125°C	1.5 ns
Minimum CLK pulse width (t_{w1}), HIGH or LOW:	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	5.0 ns
T_C = +125°C	5.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	5.0 ns
T_C = +125°C	5.0 ns
Minimum $\overline{MR}$ pulse width (t_{w2}), LOW:	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	5.0 ns
T_C = +125°C	5.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	5.0 ns
T_C = +125°C	5.0 ns
Minimum recovery time (t_{rec}), $\overline{MR}$ to CLK:	Device type 06
V_{CC} = 3.0 V dc; T_C = +25°C, -55°C	2.5 ns
T_C = +125°C	2.5 ns
V_{CC} = 4.5 V dc; T_C = +25°C, -55°C	2.5 ns
T_C = +125°C	2.5 ns

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.1.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.1.2 Truth tables. The truth tables shall be as specified on figure 2.

3.1.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I. Electrical performance characteristics apply over the case operating temperature range specified. Test conditions for these specified characteristics and limits are as specified in table I. A pin-for-pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity, on qualified devices.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I. Radiation hardness assurance level designators M, D, R, and H (see MIL-M-38510) in table I are postirradiation end-point electrical parameters.

3.5 Correctness of indexing and marking. All devices shall be subjected to the final electrical tests specified in table II after PIN marking (marked in accordance with MIL-M-38510) to verify that they are correctly indexed and identified by PIN (see 6.7). Optionally, an approved electrical test may be devised especially for this requirement.

3.5.1 Radiation hardness assurance identifier. The radiation hardness assurance identifier shall be in accordance with MIL-M-38510 and herein (see 3.4).

3.6 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 40 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
High level output voltage	V_{OH1} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10$ V $V_{IL} = 0.90$ V $I_{OL} = -50$ µA		All	3.0 V	1,2,3 (3006)	2.9		2.9		V
	V_{OH2} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15$ V $V_{IL} = 1.35$ V $I_{OH} = -50$ µA		All	4.5 V		4.4		4.4		
	V_{OH3}	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85$ V $V_{IL} = 1.65$ V $I_{OH} = -50$ µA		All	5.5 V		5.4		5.4		
			M			1 (3006) 5/			---		
			D						---		
			R						---		
			H						---		
	V_{OH4} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10$ V $V_{IL} = 0.90$ V $I_{OH} = -4.0$ mA		All	3.0 V	1,2,3 (3006)	2.4		2.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
High level output voltage	V_{OH5}	$V_{IN} = V_{IH}$ or V_{IL} V_{IH} = 3.15 V V_{IL} = 1.35 V I_{OH} = -24 mA		All	4.5 V	1,2,3 (3006)	3.7		3.7		V
			M			1 (3006)			---		
			D			5/			---		
			R						---		
			H						---		
	V_{OH6} 4/	$V_{IN} = V_{IH}$ or V_{IL} V_{IH} = 3.85 V V_{IL} = 1.65 V I_{OH} = -24 mA		All	5.5 V	1,2,3 (3006)	4.7		4.7		
	V_{OH7} 6/	$V_{IN} = V_{IH}$ or V_{IL} V_{IH} = 3.85 V V_{IL} = 1.65 V I_{OH} = -50 mA		All	5.5 V		3.85		3.85		
			M			1 (3006)			---		
			D			5/			---		
			R						---		
			H						---		
Low level output voltage	V_{OL1} 4/	$V_{IN} = V_{IH}$ or V_{IL} V_{IH} = 2.10 V V_{IL} = 0.90 V I_{OL} = 50 µA		All	3.0 V	1,2,3 (3007)		0.1		0.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/	Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Low level output voltage	V_{OL2} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15$ V $V_{IL} = 1.35$ V $I_{OL} = 50$ µA	All	4.5 V	1,2,3 (3007)		0.1		0.1	V
	V_{OL3}	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85$ V $V_{IL} = 1.65$ V $I_{OL} = 50$ µA	All	5.5 V			0.1		0.1	
			M		1 (3007) 5/				---	
			D						---	
			R						---	
			H						---	
	V_{OL4} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10$ V $V_{IL} = 0.90$ V $I_{OL} = 12$ mA	All	3.0 V	1,2,3 (3007)		0.4		0.5	
	V_{OL5}	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15$ V $V_{IL} = 1.35$ V $I_{OL} = 24$ mA	All	4.5 V			0.4		0.5	
			M		1 (3007) 5/				---	
			D						---	
			R						---	
			H						---	

See footnotes at end of table.

the worst case simulation of power pulses ... each final application specific electrical design and layout ...

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Low level output voltage	V_{OL6} 4/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85$ V $V_{IL} = 1.65$ V $I_{OL} = 24$ mA		All	5.5 V	1,2,3 (3007)		0.4		0.5	V
	V_{OL7} 6/	$V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85$ V $V_{IL} = 1.65$ V $I_{OL} = 50$ mA		All	5.5 V			1.65		1.65	
			M			1 (3007) 5/				---	
			D							---	
			R							---	
			H							---	
Positive input clamp voltage	V_{IC+} 7/	$V_{CC} = GND$ $I_{IN} = 1$ mA		All		1 (3022)	0.4	1.5			V
			M			1 (3022) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Negative input clamp voltage	V_{IC} 7/	V_{CC} = open I_{IN} = -1 mA		All		1 (3022)	-0.4	-1.5			V
			M			1 (3022)			---	---	
			D			5/			---	---	
			R						---	---	
			H						---	---	
Input current low (excluding I/O ports)	I_{IL} 7/	V_{IN} = GND		All	5.5 V	1,2 (3009)		-0.1		-1.0	µA
			M			1 (3009)				---	
			D			5/				---	
			R							---	
			H							---	
Input current high (excluding I/O ports)	I_{IH} 7/	V_{IN} = V_{CC}		All	5.5 V	1,2 (3009)		0.1		1.0	
			M			1 (3009)				---	
			D			5/				---	
			R							---	
			H							---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Supply current quiescent	I_{CC} 7/	V_{IN} = V_{CC} or GND		ALL	5.5 V	1,2 (3005)		2		10	µA
			M			1 (3005) 5/				---	
			D							---	
			R							---	
			H							---	
Three-state output leakage current low	I_{OZL} 7/	V_{OUT} = GND 8/		ALL	5.5 V	1,2,3 (3005)		-0.6		-11.0	µA
			M			1 (3005) 5/				---	
			D							---	
			R							---	
			H							---	
Three-state output leakage current high	I_{OZH} 7/	V_{OUT} = V_{CC} 8/		ALL	5.5 V	1,2,3 (3005)		+0.6		11.0	µA
			M			1 (3005) 5/				---	
			D							---	
			R							---	
			H							---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/	Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Input/output capacitance	$C_{I/O}$	See 4.4.1c T_C = 25°C 9/	ALL	5.5V	4 (3012)		15			pF
Input capacitance	C_{IN}	See 4.4.1c T_C = 25°C	ALL	GND	4 (3012)		10			
Power dissipation capacitance	C_{PD}	See 4.4.1c T_C = 25°C 10/	ALL		4		190			
Latch-up input/output overvoltage 11/	I_{CC} (O/V1)	$t_w \geq 100$ µs $t_{cool} \geq t_w$ 5 µs $\leq t_r \leq$ 5 ms 5 µs $\leq t_f \leq$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 10.5 V	ALL	5.5 V	2				200	mA
Latch-up input/output positive overcurrent 11/	I_{CC} (O/I1+)	$t_w \geq 100$ µs $t_{cool} \geq t_w$ 5 µs $\leq t_r \leq$ 5 ms 5 µs $\leq t_f \leq$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = +120 mA	ALL	5.5 V	2				200	mA
Latch-up input/output negative overcurrent 11/	I_{CC} (O/I1-)	$t_w \geq 100$ µs $t_{cool} \geq t_w$ 5 µs $\leq t_r \leq$ 5 ms 5 µs $\leq t_f \leq$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = -120 mA	ALL	5.5 V	2				200	mA
Latch-up input/output overvoltage 11/	I_{CC} (O/V2)	$t_w \geq 100$ µs $t_{cool} \geq t_w$ 5 µs $\leq t_r \leq$ 5 ms 5 µs $\leq t_f \leq$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 9.0 V	ALL	5.5 V	2				100	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Truth table test	12/	V_{IL} = .45 V V_{IH} = 2.5 V Verify output V_O		All	3.0 V	7 (3014) 5/	L	H			
		V_{IL} = .6 V V_{IH} = 3.7 V Verify output V_O		All	4.5 V	7,8 (3014) 5/	L	H	L	H	
Maximum CLK frequency	f_{MAX}	C_L = 50 pF R_L = 500Ω See 4.4.1f		ALL	3.0 V	9,10,11	90		70		MHz
					4.5 V		130		80		
Propagation delay time, CLK to 1/On	t_{PHL1}, t_{PLH1}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	3.0 V	9,10,11 (3003)	1.0	23.0	1.0	26.5	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	
	t_{PHL1}, t_{PLH1}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	4.5 V	9,10,11 (3003)	1.0	16.0	1.0	18.5	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/	Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Propagation delay time, CLK to Q0, CLK to Q7	t_{PHL2}, t_{PLH2}	C_L = 50 pF, R_L = 500Ω, See figure 3 13/ 14/	ALL	3.0 V	9,10,11 (3003)	1.0	21.5	1.0	26.5	ns
			M		9 (3003)			---	---	
			D		5/			---	---	
			R					---	---	
			H					---	---	
	t_{PHL2}, t_{PLH2}	C_L = 50 pF, R_L = 500Ω, See figure 3 13/ 14/	ALL	4.5 V	9,10,11 (3003)	1.0	14.5	1.0	18.0	ns
			M		9 (3003)			---	---	
			D		5/			---	---	
			R					---	---	
			H					---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Propagation delay time, $\overline{MR}$ to Q0, or $\overline{MR}$ to Q7	t_{PHL3}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	3.0 V	9,10,11 (3003)	1.0	22.5	1.0	27.0	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	
	t_{PHL3}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	4.5 V	9,10,11 (3003)	1.0	15.5	1.0	18.5	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Propagation delay time, $\overline{MR}$ to I/On	t_{PHL4}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	3.0 V	9,10,11 (3003)	1.0	21.5	1.0	26.5	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	
	t_{PHL4}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	4.5 V	9,10,11 (3003)	1.0	15.0	1.0	18.0	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Output enable time, $\overline{OEn}$ to I/On	t_{PZH1}, t_{PZL1}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	3.0 V	9,10,11 (3003)	1.0	19.5	1.0	23.5	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	
		C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	4.5 V	9,10,11 (3003)	1.0	13.0	1.0	16.0	ns
			M			9 (3003) 5/			---	---	
			D						---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

ground terminal. Numerals given are conventional and may be changed as long

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Output enable time, SO = S1 = H to I/On	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω See figure 3 14/ 15/		ALL	3.0 V	9,10,11 (3003)	1.0	19.5	1.0	23.5	ns
			M			9 (3003)			---	---	
			D			5/			---	---	
			R						---	---	
			H						---	---	
		C_L = 50 pF R_L = 500Ω See figure 3 14/ 15/		ALL	4.5 V	9,10,11 (3003)	1.0	13.0	1.0	16.0	ns
			M			9 (3003)			---	---	
			D			5/			---	---	
			R						---	---	
			H						---	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/		Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits		+125°C limits		Unit
							Min	Max	Min 3/	Max 3/	
Output disable time, $\overline{OE}n$ to I/On	t_{PHZ1}, t_{PLZ1}	C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	3.0 V	9,10,11 (3003)	1.0	19.0	1.0	22.5	ns
			M			9 (3003)			---	---	
			D			5/			---	---	
			R						---	---	
			H						---	---	
		C_L = 50 pF R_L = 500Ω See figure 3 13/ 14/		ALL	4.5 V	9,10,11 (3003)	1.0	14.0	1.0	17.0	ns
			M			9 (3003)			---	---	
			D			5/			---	---	
			R						---	---	
			H						---	---	

TABLE I. Electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued.

Test	Symbol	Test conditions, unless otherwise specified 1/	Device type 2/	V_{CC}	Group A subgroups (test method)	-55°C/+25°C limits Min	-55°C/+25°C limits Max	+125°C limits Min 3/	+125°C limits Max 3/	Unit
Output disable time, SO = S1 = H to I/On	t_{PHZ2}, t_{PLZ2}	C_L = 50 pF R_L = 500Ω See figure 3 14/ 15/	ALL	3.0 V	9,10,11 (3003)	1.0	19.0	1.0	22.5	ns
			M		9 (3003)			---	---	
			D		5/			---	---	
			R					---	---	
			H					---	---	
		C_L = 50 pF R_L = 500Ω See figure 3 14/ 15/	ALL	4.5 V	9,10,11 (3003)	1.0	14.0	1.0	17.0	ns
			M		9 (3003)			---	---	
			D		5/			---	---	
			R					---	---	
			H					---	---	

1/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
c. I_{CC} tests, the output terminal shall be open.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DESC-EQM) upon request.

2/ The word "All" in the device type column, means non-RHA and RHA preirradiation limits for all devices. Where M, D, R, and H in the conditions column are postirradiation limits for those device types specified in the device type column.

3/ When dashes (---) are present, RHA samples do not have to be tested at +125°C prior to irradiation.

4/ This parameter is provided as design information only.

5/ Postirradiation electrical measurements for any RHA level shall be performed at T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum.

7/ Not tested at -55°C.

8/ Three-state output conditions are required. For I_{OZL}, set outputs to high state. For I_{OZH}, set outputs to low state. Set input pins to V_{IL} = $V_{IL(MAX)}$ and V_{IH} = $V_{IH(MIN)}$, as required. I_{OZL} and I_{OZH} shall include I_{IL} and I_{IH} respectively.

9/ Set output enable control pins to V_{CC} or GND, as applicable, to disable the outputs.

10/ Power dissipation capacitance (C_{PD}), is provided as design information only and is guaranteed but not tested. C_{PD} determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$, and the dynamic current consumption, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}$.

11/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over}, are to be accurate within ±5 percent.

12/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L ≤ 2.5 V; high inputs = 3.7 V and low inputs = 0.6 V for V_{CC} = 4.5 V and H ≥ 1.5 V, L ≤ 1.5 V; high inputs = 2.5 V and low inputs = 0.45 V for V_{CC} = 3.0 V. Tests at V_{CC} = 3.0 V are for RHA specified devices only (T_A = +25°C ±5°C).

13/ Devices are tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested, see 4.4.1d.

14/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1 ns and guaranteed by guardbanding V_{CC} = 4.5 V limits to 1.5 ns.

15/ Measured only for initial test and after process or design changes which may affect this parameter.

Device type	06
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	S0
2	$\overline{OE1}$
3	$\overline{OE2}$
4	I/06
5	I/04
6	I/02
7	I/00
8	Q0
9	$\overline{MR}$
10	GND
11	DS0
12	CLK
13	I/01
14	I/03
15	I/05
16	I/07
17	Q7
18	DS7
19	S1
20	V_{CC}

FIGURE 1. Terminal connections.

Device type 06

Asyncronous operations (CP, DS0, DS7 = X, $\overline{OE1}$, $\overline{OE2}$ = L,
S0 and S1 shall not simultaneously = H)

Mode	Inputs			Input/outputs				Outputs	
	$\overline{MR}$	S0	S1	I/O_0	I/O_1	...	I/O_7	Q0	Q7
Reset	L	X	X	L	L	...	L	L	L
Hold	H	L	L	N/C	N/C	...	N/C	N/C	N/C

Syncronous operations (MR = H, $\overline{OE1}$, $\overline{OE2}$ = L)

Mode	Inputs					Input/outputs 1/ 2/				Outputs 2/	
	CP	S0	S1	DS0	DS7	I/O_0	I/O_1	...	I/O_7	Q0	Q7
Load	↑	H	H	X	X	Z	Z	...	Z	D0	D7
Shift right	↑	L	H	L	X	L	D0	...	D6	L	D6
	↑	L	H	H	X	H	D0	...	D6	H	D6
Shift left	↑	H	L	X	L	D1	D2	...	L	D1	L
	↑	H	L	X	H	D1	D2	...	H	D1	H

1/ When S0 = S1 = H simultaneously, outputs I/On are in a high impedance state (Z).
2/ Shown are the state of the outputs after the low-to-high clock transition. D0 to D7 represent the data that was stored in the eight flip-flops, Q0 to Q7, prior to the clock transition.

FIGURE 2. Truth tables.

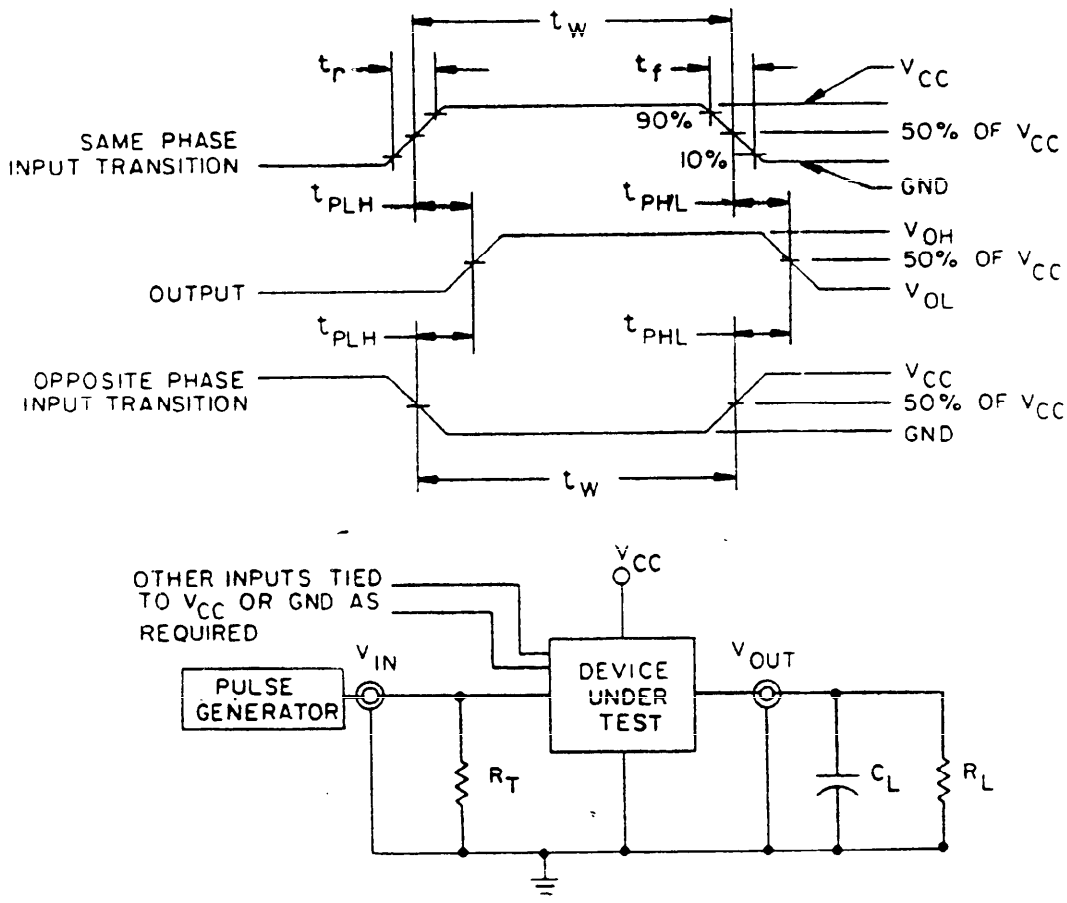
High Z conditions

Mode	Inputs		Input/outputs 1/				Outputs	
	$\overline{OE1}$	$\overline{OE2}$	I/O_0	I/O_1	...	I/O_7	Q0	Q7
High Z	H	X	Z	Z	...	Z	2/	2/
	X	H	Z	Z	...	Z	2/	2/

1/ When S0 = S1 = H simultaneously, outputs I/On are in a high impedance state (Z).
2/ During the High Z condition, shift, hold, load, and reset operations can still occur. Outputs Q0 and Q7 are affected accordingly.

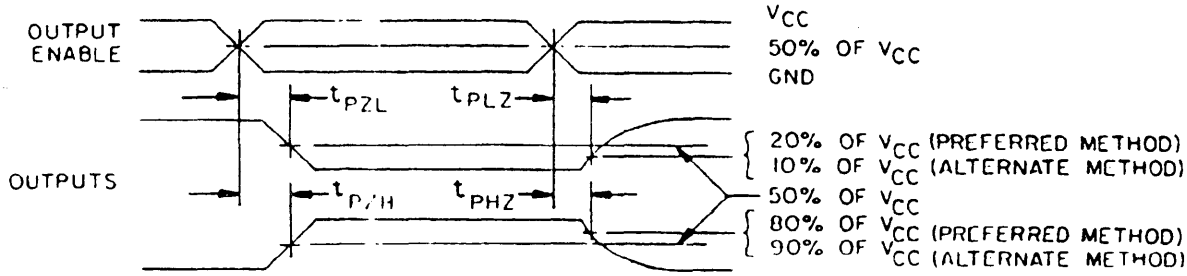
H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
↑ = Low-to-high clock transition
M/C = No change

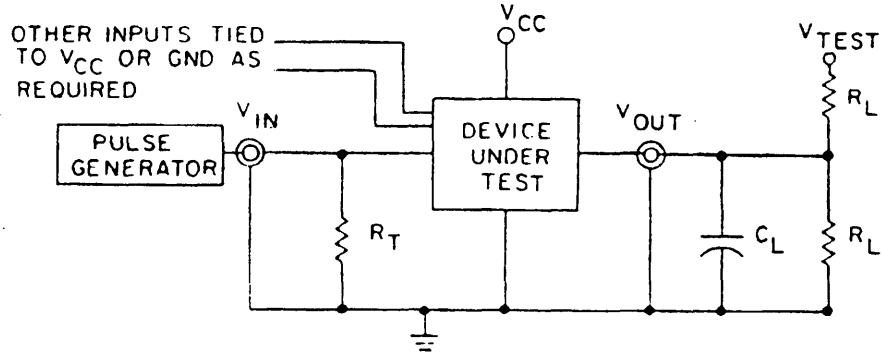
FIGURE 2. Truth tables - Continued.



NOTES:
1. $t_r = t_f \leq 3$ ns; PRR $\leq$ 10 MHz; duty cycle = 50 percent.
2. C_L = 50 pF or equivalent, includes test jig and probe capacitance.
3. R_L = 500Ω or equivalent.
4. R_T = 50Ω or equivalent.

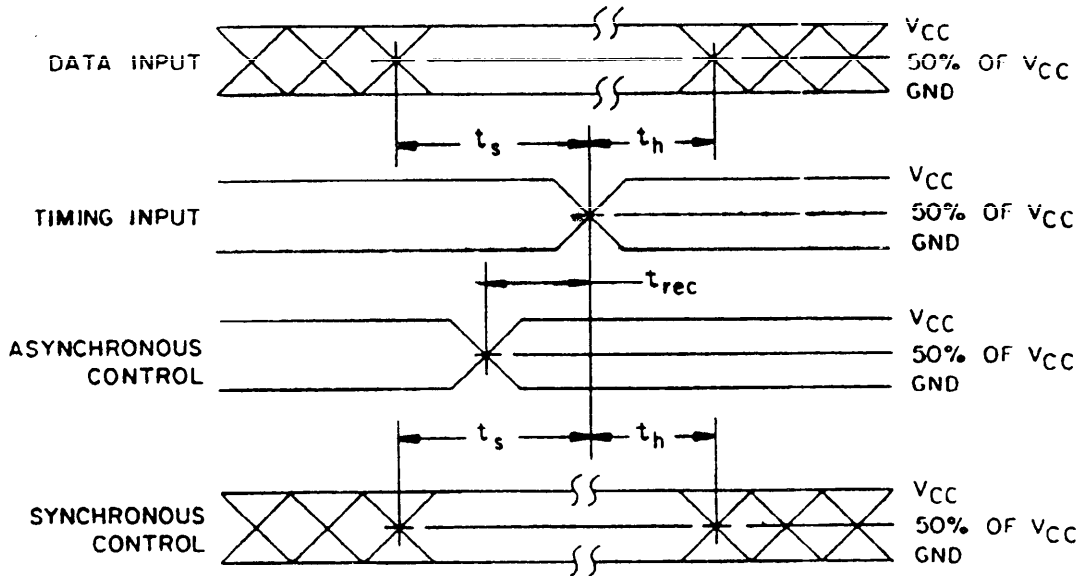
FIGURE 3. Switching time waveforms and test circuits.





NOTES:
1. **Preferred method:**
   When measuring t_{PHZ} or t_{PZH}: V_{TEST} = GND.
   When measuring t_{PLZ} or t_{PZL}: V_{TEST} = 2 (V_{CC}).
2. **Alternate method:**
   When measuring t_{PHZ} or t_{PZH}: V_{TEST} = Open.
   When measuring t_{PLZ} or t_{PZL}: V_{TEST} = 2 (V_{CC}).
3. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
4. R_L = 500Ω or equivalent.
5. R_T = 50Ω or equivalent.
6. V_{IN} = 0 V to V_{CC}.

FIGURE 3. Switching time waveforms and test circuits - Continued.



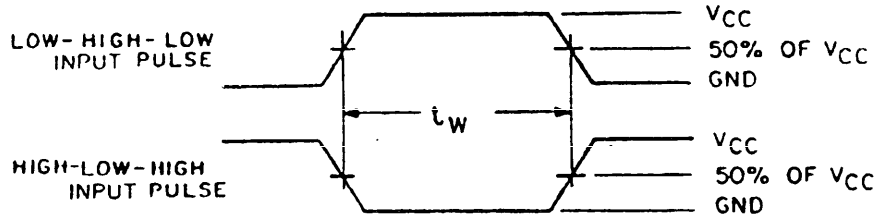


FIGURE 3. Switching time waveforms and test circuits - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2b or 4.2c as applicable, or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 of table II herein.

b. Static burn-in, test condition A, method 1015 of MIL-STD-883. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(1) For static burn-in I, all pins except V_{CC}, Q0 and Q7 shall be connected to GND. Outputs Q0 and Q7 may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are only required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ

(2) For static burn-in II, all pins except GND, Q0 and Q7 shall be connected to V_{CC}. The GND pin shall be connected to GND. Outputs Q0 and Q7 may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are only required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ

(3) $V_{CC} = 5.5$ V ± 0.5 V.

c. Dynamic burn-in, test condition D, method 1015 of MIL-STD-883.

(1) Input resistors = 220Ω to 47 kΩ ± 20%.

(2) Output resistors = 220Ω ± 20%.

(3) $V_{CC} = 5.5$ V ± 0.5 V.

(4) V_{CC} nominal = $V_{CC}/2 \pm 0.5$ V.

(5) The $\overline{OE1}$, $\overline{OE2}$, and S1 inputs shall be connected to the resistors in parallel to GND. The S0, $\overline{MR}$, and DS7 inputs shall be connected to the resistors in parallel to V_{CC}. The I/00 through I/07, Q0 and Q7 outputs shall be connected to the resistors on parallel with V_{CC} nominal. The CP and DS0 inputs shall be connected to CP1 and CP2, respectively.

(6) CP1 = 50 kHz to 150 kHz square wave; CP2 = 25 kHz to 75 kHz square wave; duty cycle = 50 percent ±15 percent; $V_{IH} = 4.5$ V to V_{CC}, $V_{IL} = 0$ V ± 0.5 V; t_r, $t_f \leq 100$ ns.

d. Interim and final electrical parameters shall be as specified in table II herein.

e. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B devices shall be in accordance with MIL-M-38510 for static burn-in. Dynamic burn-in is not required.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100 percent, divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and 4.3.1 herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. Only those device types that pass ESDS testing at 2,000 volts or greater shall be considered as conforming to the requirements of this specification. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be performed in accordance with table II herein.

b. O/V (latch-up) tests shall be measured only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. Test all applicable pins on five devices with zero failures.

c. $C_{I/O}$, C_{IN}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. Subgroups 7 and 8 tests shall be sufficient to verify the truth table.

f. f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with zero failures.

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S device 1/			Class B device 1/		
		Reference paragraphs	Table I subgroups 2/	Table III delta limits 3/	Reference paragraphs	Table I subgroups 2/	Table III delta limits 3/
1	Interim electrical parameters (method 5004)		1			1	
2	Static burn-in I (method 1015)	4.2b 4.5.2	5/ Required			Not required	
3	Same as line 1		1	delta			
4	Static burn-in II (method 1015)	4.2b 4.5.2	5/ Required		4.2b 4.5.2	4/	
5	Same as line 1	4.2d	1*	delta	4.2d	1*	delta
6	Dynamic burn-in (method 1015)	4.2b 4.5.2	5/ Required			Not required	
7	Same as line 1	4.2d	1	delta			
8	Final electrical parameters (method 5004)		1*,2,7,9			1*,2,7,9 4/	
9	Group A test requirements (method 5005)	4.4.1	1,2,3,4,7, 8,9,10, 11		4.4.1	1,2,3,4,7, 8,9,10, 11	
10	Group B end-point electrical parameters (method 5005)	4.4.2	1,2,3,7, 8,9,10, 11	delta			
11	Group C end-point electrical parameters (method 5005)				4.4.3	1,2	delta
12	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3		4.4.4	1,2	
13	Group E end-point electrical parameters (method 5005)	4.4.5	1,7,9		4.4.5	1,7,9	

See footnotes on next page.

1/ Blank spaces indicate tests are not applicable.
2/ *indicates PDA applies to subgroup (see 4.2.1).
3/ Delta indicates the delta limit shall be required only on table I subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).
4/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in tests of line 1.
5/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II, method 5005 of MIL-STD-883 and as follows:

a. Class S steady-state life (accelerated) shall be conducted using test condition D, method 1005 of MIL-STD-883 and the circuit described in 4.2c herein, or equivalent as approved by the qualifying activity.

b. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table III herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III, method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.

b. Steady-state life test (method 1005 of MIL-STD-883) shall be conducted using test condition D and as specified in 4.5.2 herein using a circuit as described in 4.2c herein, or equivalent as approved by the qualifying activity.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV, method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

TABLE III. Delta limits at +25°C.

Parameter 1/	Device types	Limits
I_{cc}	All	±100 nA
I_{cch}	All	±100 nA
I_{ccl}	All	±100 nA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.5 Group E inspection. Group E inspection is required only for device types intended to be marked as radiation hardness assured (see 3.5.2). RHA testing shall be performed in accordance with table V, method 5005 of MIL-STD-883 and electrical tests in table I herein. RHA quality conformance inspection sample tests shall be performed at the level specified in the purchase order.

a. RHA test for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table I herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure.

e. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent of the devices are tested at input high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

(1) Inputs tested high, V_{CC} = 5.5 V dc +5 percent, R_{CC} = 10Ω ±5 percent, V_{IN} = 5.0 V dc +20 percent, R_{IN} = 1 kΩ ±5 percent, and all outputs are open. The output enable control pin(s) shall be connected to R_{IN} in parallel to V_{CC} or GND, as applicable, to enable the outputs.

(2) Inputs tested low, V_{CC} = 5.5 V dc +5 percent, R_{CC} = 10Ω ±5 percent, V_{IN} = 0.0 V dc, and all outputs are open. The output enable control pin(s) shall be connected to R_{IN} in parallel to V_{CC} or GND, as applicable, to enable the outputs.

f. Subgroups 1 and 2 of table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to within +10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

4.5.3 Quiescent supply current. When performing quiescent supply current measurements (I_{CC}), the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, shall be supplied.

a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, RHA tests and steady-state life tests (see 3.4).

b. A copy of each radiograph.

c. The quality conformance inspection data (see 4.4).

d. Parameter distribution data on parameters evaluated during burn-in (see 3.4).

e. Final electrical parameters data (see 4.2d).

f. RHA delta limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory).

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Acquisition requirements. The acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1 and 2.2).

c. Lead material and finish may be specified (see 3.3).

d. Complete PIN (see 6.7).

e. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

f. Requirements for certificate of compliance, if applicable.

g. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

h. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

i. Requirements for product assurance and radiation hardness assurance options.

j. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.

k. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
O/V	Latch-up over-voltage.
O/I	Latch-up over-current.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
$C_{I/O}$	Input/output terminal-to-GND capacitance.
C_{IN}	Input terminal-to-GND capacitance.
C_{PD}	Power dissipation capacitance.
V_{IC}	Positive input clamp voltage.
t_w	Trigger duration (width).

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead finish C (see 3.3). Longer length leads and lead forming shall not affect the PIN.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges, postirradiation performance or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
*01	54AC164
*02	54AC165
*03	54AC166
*04	54AC194
*05	54AC195
06	54AC299
*07	54AC595

* To be included at a later date.

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static build up. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Avoid use of plastic, rubber, or silk in MOS areas.

e. Maintain relative humidity above 50 percent, if practical.

6.7 PIN. The PIN is formulated in accordance with MIL-M-38510.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI
Air Force - 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC, OC, SH

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1228)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8 In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER	2. DOCUMENT DATE (YYMMDD)
3. DOCUMENT TITLE		

4. NATURE OF CHANGE *(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)*

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) AUTOVON (If applicable)	e. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME	b. TELEPHONE (Include Area Code) (1) Commercial	(2) AUTOVON
ROME AIR DEVELOPMENT CENTER	315-330-2945	587-2945
c. ADDRESS (Include Zip Code) RADC/RBR GRIFFISS AFB NY 13441-5700	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340	

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