

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, SCHOTTKY TTL,
 ARITHMETIC LOGIC UNIT/FUNCTION GENERATORS,
 MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, Schottky TTL, arithmetic logic unit/function generators. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	4-bit arithmetic logic unit/function generator
02	Lookahead carry generator

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package
J	D-3 (24-lead, 1/2" x 1-1/4"), dual-in-line package
K	F-6 (24-lead, 3/8" x 5/8"), flat package
Z	F-8 (24-lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings:

Supply voltage range	- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range	- - - - -	-1.2 V dc at -18 mA to +5.5 V dc
Storage temperature range	- - - - -	-65°C to +150°C
Maximum power dissipation (P _D)	1/ - - - - -	
Device type 01	- - - - -	990 mW dc
Device type 02	- - - - -	544 mW dc
Lead temperature (soldering, 10 seconds)	- -	+300°C
Thermal resistance, junction-to-case (θ _{JC}):		
The thermal resistance shall be as specified on figure C-6 in Appendix C of MIL-M-38510.		
Junction temperature (T _J)	2/ - - - - -	+175°C

- 1/ Must withstand the added P_D due to short circuit condition (e.g., I_{OS}) at one output for 5 seconds duration.
- 2/ Maximum junction temperature shall not be exceeded except for the allowable short duration burn-in screening per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions:

Supply voltage range (V_{CC}) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) - - -	2.0 V dc
Maximum low-level input voltage (V_{IL}) <u>2/</u> - -	0.8 V dc
Normalized fanout (each output) <u>3/</u>	
Logical low level - - - - -	10 maximum
Logical high level - - - - -	20 maximum
Case operating temperature range (T_C) - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and pin designations. The terminal connections and pin designations shall be as specified on figure 1.

3.2.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3.

2/ $V_{IL} = 0.7 V @ 125^\circ C.$

3/ A fanout of 20 normalized loads is provided to facilitate connection of unused inputs to used inputs.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; \underline{2}/$ $V_{IN} = 2.0 \text{ V}; I_{OH} = -1 \text{ mA}$	01, 02	2.5		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; \underline{2}/$ $V_{IH} = 2.0 \text{ V}; I_{OL} = 20 \text{ mA}$	01, 02	0.2	0.5	$\underline{3}/$ V
Input diode clamp	V_{IC}	$V_{CC} = 4.5 \text{ V}; I_{IN} = -18 \text{ mA}$ $T_C = +25^{\circ}\text{C}$	01, 02		-1.2	V
Low-level input current at M input	I_{IL1}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	01	-1	-2	mA
Low-level input current at B input	I_{IL2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	01	-3	-6	mA
Low-level input current at S_0 or S_3 input	I_{IL3}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	01	-4	-8	mA
Low-level input current at S_1 or S_2	I_{IL4}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V}; \underline{5}/$ $A_0, A_1, A_2, A_3 = 5.5 \text{ V}$	01	-4	-8	mA
Low-level input current at C_n input	I_{IL5}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{5}/$	01	-5	-10	mA
Low-level input current at A input	I_{IL6}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	01	-2	-4	mA
Low-level input current at \bar{G}_1 input	I_{IL1}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V},$ $C_n = \text{GND} \underline{4}/$	02	-8	-16	mA
Low-level input current at \bar{P}_1 input	I_{IL2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V},$ $C_n = \text{GND} \underline{4}/$	02	-4	-8	mA
Low-level input current at \bar{G}_0 input	I_{IL3}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V},$ $C_n = \text{GND} \underline{4}/$	02	-7	-14	mA
Low-level input current at \bar{P}_0 input	I_{IL4}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	02	-4	-8	mA
Low-level input current at \bar{G}_3 input	I_{IL5}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	02	-4	-8	mA
Low-level input current at \bar{P}_3 input	I_{IL6}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V} \underline{4}/$	02	-2	-4	mA

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Low-level input current at C_n input	I_{IL7}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V}$ <u>4/</u>	02	-1	-2	mA
Low-level input current at \bar{G}_2 input	I_{IL8}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V},$ $C_n = \text{GND}$ <u>4/</u>	02	-7	-14	mA
Low-level input current at P_2 input	I_{IL9}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 0.5 \text{ V}$ <u>4/</u>	02	-3	-6	mA
High-level input current at M input	I_{IH1}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V}$ <u>5/</u>	01		50	μA
High-level input current at \bar{A} or \bar{B} input	I_{IH2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V}$ <u>5/</u>	01		150	μA
High-level input current at S_0 or S_3 input	I_{IH3}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V}$ <u>5/</u>	01		200	μA
High-level input current at S_1 or S_2 input	I_{IH4}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V};$ <u>5/</u> $\bar{B}_0, \bar{B}_1, \bar{B}_2, \bar{B}_3 = 5.5 \text{ V}$	01		200	μA
High-level input current at C_n input	I_{IH5}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V}$ <u>4/</u>	01		250	μA
High-level input current at M input	I_{IH6}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V}$ <u>5/</u>	01		1	mA
High-level input current at \bar{A} or \bar{B} input	I_{IH7}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V}$ <u>5/</u>	01		1	mA
High-level input current at S_0 or S_3 input	I_{IH8}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V}$ <u>5/</u>	01		1	mA
High-level input current at S_1 or S_2 input	I_{IH9}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V};$ <u>5/</u> $\bar{B}_0, \bar{B}_1, \bar{B}_2, \bar{B}_3 = 5.5 \text{ V}$	01		1	mA
High-level input current at C_n input	I_{IH10}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V}$ <u>4/</u>	01		1	mA
High-level input current at \bar{G}_1 input	I_{IH11}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V};$ $C_n = 5.5 \text{ V}$ <u>5/</u>	02		400	μA
High-level input current at P_1 input	I_{IH2}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 2.7 \text{ V}$ $C_n = 5.5 \text{ V}$ <u>5/</u>	02		200	μA

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High-level input current at \bar{G}_0 input	I_{IH3}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		350	μA
High-level input current at \bar{P}_0 input	I_{IH4}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V } \underline{5/}$	02		200	μA
High-level input current at \bar{G}_3 input	I_{IH5}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V } \underline{5/}$	02		200	μA
High-level input current at \bar{P}_3 input	I_{IH6}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V } \underline{5/}$	02		100	μA
High-level input current at C_n input	I_{IH7}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V } \underline{5/}$	02		50	μA
High-level input current at \bar{G}_2 input	I_{IH8}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		350	μA
High-level input current at \bar{P}_2 input	I_{IH9}	$V_{CC} = 5.5\text{ V}; V_{IN} = 2.7\text{ V } \underline{5/}$	02		150	μA
High-level input current at \bar{G}_1 input	I_{IH10}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at \bar{P}_1 input	I_{IH11}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at \bar{G}_0	I_{IH12}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at \bar{P}_0 input	I_{IH13}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at \bar{G}_3 input	I_{IH14}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V};$ $C_n = \text{GND } \underline{5/}$	02		1	mA
High-level input current at \bar{P}_3 input	I_{IH15}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at C_n input	I_{IH16}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V } \underline{5/}$	02		1	mA
High-level input current at \bar{G}_2	I_{IH17}	$V_{CC} = 5.5\text{ V}; V_{IN} = 5.5\text{ V};$ $C_n = 5.5\text{ V } \underline{5/}$	02		1	mA

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
High-level input current at \overline{P}_2 input	I_{IH18}	$V_{CC} = 5.5 \text{ V}; V_{IN} = 5.5 \text{ V } \underline{5/}$	02		1	mA
Short-circuit output current at \overline{G} output	I_{OS1}	$V_{CC} = 5.5 \text{ V}; S_3, \overline{A}_3, \overline{B}_3$ $= 5.5 \text{ V } \underline{5/} \underline{6/}$	01	-40	-100	mA
Short-circuit output current at C_{n+4} output	I_{OS2}	$V_{CC} = 5.5 \text{ V } \underline{5/} \underline{6/}$	01	-40	-100	mA
Short-circuit output current at \overline{P}, F_0 thru F_3 outputs	I_{OS3}	$V_{CC} = 5.5 \text{ V } \underline{4/} \underline{6/}$	01	-40	-100	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}; V_{IL} = \text{GND};$ $V_{IH} = 5.5 \text{ V } \underline{6/}$	02	-40	-100	mA
Collector cutoff current	I_{CEX}	$V_{CC} = 5.5 \text{ V}; V_{OH} = 5.5 \text{ V};$ $V_{IH} = 2.0 \text{ V}; V_{IL} = \text{GND}$	01		1	mA
		$V_{CC} = 5.5 \text{ V}; V_{OH} = 5.5 \text{ V};$ $V_{IH} = 5.5 \text{ V}; V_{IL} = \text{GND}$	02		250	μA
Low-level supply current	I_{CCL}	$V_{CC} = 5.5 \text{ V}; V_{IL} = 0 \text{ V};$ $V_{IH} = 5.5 \text{ V } \underline{7/}$	01		180	mA
	I_{CCL}	$V_{CC} = 5.5 \text{ V}; V_{IL} = 0 \text{ V};$ $V_{IH} = 5.5 \text{ V}$	02		99	mA
High-level supply current	I_{CCH}	$V_{CC} = 5.5 \text{ V}; V_{IL} = 0 \text{ V};$ $V_{IH} = 5.5 \text{ V } \underline{8/}$	01		180	mA
	I_{CCH}	$V_{CC} = 5.5 \text{ V}; V_{IL} = 0 \text{ V};$ $V_{IH} = 5.5 \text{ V}$	02		65	mA
Propagation delay times, high-to-low level output: <u>9/</u>						
\overline{A}_i or \overline{B}_i to any \overline{F} sum mode	t_{PHL1}	$V_{CC} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	23	ns
\overline{A}_i or \overline{B}_i to any \overline{F} diff mode	t_{PHL2}	$V_{CC} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	28	ns
\overline{A}_i or \overline{B}_i to \overline{F} sum mode	t_{PHL3}	$V_{CC} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	16	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Propagation delay times, high-to-low level output: 9/						
\overline{A}_i or \overline{B}_i to \overline{F} diff mode	t_{PHL4}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	20	ns
\overline{A}_i or \overline{B}_i to \overline{G} sum mode	t_{PHL5}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	16	ns
\overline{A}_i or \overline{B}_i to \overline{G} diff mode	t_{PHL6}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	20	ns
C_n to any F_0 sum mode	t_{PHL7}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	16	ns
\overline{A}_i or \overline{B}_i to $A = B$ diff mode	t_{PHL8}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	36	ns
C_n to C_{n+4} sum mode	t_{PHL9}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	14.5	ns
C_n to C_{n+4} diff mode	t_{PHL10}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	14.5	ns
\overline{A}_i or \overline{B}_i to C_{n+4} sum mode	t_{PHL11}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	25	ns
\overline{A}_i or \overline{B}_i to C_{n+4} diff mode	t_{PHL12}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	29	ns
\overline{A}_i or \overline{B}_i to any F logic mode	t_{PHL13}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 logic mode test table	01	2	28	ns
Propagation delay times, low-to-high level output: 9/						
\overline{A}_i or \overline{B}_i to any \overline{F} sum mode	t_{PLH1}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	23	ns
\overline{A}_i or \overline{B}_i to any \overline{F} diff mode	t_{PLH2}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 diff mode test table	01	2	26	ns
\overline{A}_i or \overline{B}_i to \overline{F} sum mode	t_{PLH3}	$V_{\text{CC}} = 5.0 \text{ V}$ See figure 5 sum mode test table	01	2	16	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Propagation delay times, low-to-high level output: <u>9/</u>						
\bar{A}_i or \bar{B}_i to \bar{F} diff mode	t _{PLH4}	$V_{CC} = 5.0\text{ V}$ See figure 5 diff mode test table	01	2	20	ns
\bar{A}_i or \bar{B}_i to \bar{G} sum mode	t _{PLH5}	$V_{CC} = 5.0\text{ V}$ See figure 5 sum mode test table	01	2	16	ns
\bar{A}_i or \bar{B}_i to \bar{G} diff mode	t _{PLH6}	$V_{CC} = 5.0\text{ V}$ See figure 5 diff mode test table	01	2	20	ns
C_n to any \bar{F} sum mode	t _{PLH7}	$V_{CC} = 5.0\text{ V}$ See figure 5 sum mode test table	01	2	16	ns
A_i or B_i to $A = B$ diff mode	t _{PLH8}	$V_{CC} = 5.0\text{ V}$ See figure 5 diff mode test table	01	2	29	ns
C_n to C_{n+4} sum mode	t _{PLH9}	$V_{CC} = 5.0\text{ V}$ See figure 5 sum mode test table	01	2	14.5	ns
C_n to C_{n+4} diff mode	t _{PLH10}	$V_{CC} = 5.0\text{ V}$ See figure 5 diff mode test table	01	2	14.5	ns
\bar{A}_i or \bar{B}_i to C_{n+4} sum mode	t _{PLH11}	$V_{CC} = 5.0\text{ V}$ See figure 5 sum mode test table	01	2	25	ns
\bar{A}_i or \bar{B}_i to C_{n+4} diff mode	t _{PLH12}	$V_{CC} = 5.0\text{ V}$ See figure 5 diff mode test table	01	2	29	ns
\bar{A}_i or \bar{B}_i to any \bar{F} logic mode	t _{PLH13}	$V_{CC} = 5.0\text{ V}$ See figure 5 logic mode test table	01	2	26	ns
Propagation delay times, high-to-low level output: <u>10/</u>						
C_n to $C_{n+X}, C_{n+Y},$ C_{n+Z}	t _{PHL1}	$V_{CC} = 5.0\text{ V}; \bar{F}_0, \bar{F}_1, \bar{F}_2$ $= \text{GND}; \bar{G}_i = 2.7\text{ V}$	02	2	14.5	ns
$\bar{F}_0, \bar{F}_1,$ or $\bar{F}_2,$ to $C_{n+X}, C_{n+Y}, C_{n+Z}$	t _{PHL2}	$V_{CC} = 5.0\text{ V}; \bar{F}_0, \bar{F}_1, \bar{F}_2$ $= \text{GND}; C_n, \bar{G}_i = 2.7\text{ V}$	02	2	11	ns
$\bar{G}_0, \bar{G}_1,$ or \bar{G}_2 to $C_{n+Y}, C_{n+X}, C_{n+Z}$	t _{PHL3}	$V_{CC} = 5.0\text{ V}; C_n, \bar{F}_0, \bar{F}_1,$ $\bar{F}_2 = \text{GND}, \bar{G}_i = 2.7\text{ V}$ <u>11/</u>	02	2	11	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Propagation delay times, high-to-low level output: <u>10/</u>						
$\bar{P}_1, \bar{P}_2, \text{ or } \bar{P}_3 \text{ to } \bar{G}$	t_{PHL4}	$V_{CC} = 5.0 \text{ V}; \bar{P}_i = \text{GND}; \underline{11/}$ $C_n, \bar{G}_1, \bar{G}_2, \bar{G}_3 = 2.7 \text{ V}$	02	2	14.5	ns
$\bar{G}_0, \bar{G}_1, \bar{G}_2, \text{ or } \bar{G}_3$ to \bar{G}	t_{PHL5}	$V_{CC} = 5.0 \text{ V}; \bar{G}_i = 2.7 \text{ V}; \underline{11/}$ $\bar{P}_1, \bar{P}_2, \bar{P}_3 = \text{GND}$	02	2	14.5	ns
$\bar{P}_0, \bar{P}_1, \bar{P}_2, \text{ or } \bar{P}_3$ to \bar{P}	t_{PHL6}	$\bar{P}_i = \text{GND} \underline{11/}, V_{CC} = 5.0 \text{ V};$ $C_n, \bar{G}_i = 2.7 \text{ V}$	02	2	14	ns
Propagation delay times, low-to-high level output: <u>10/</u>						
$C_n \text{ to } C_{n+X}, C_{n+Y},$ C_{n+Z}	t_{PLH1}	$V_{CC} = 5.0 \text{ V}; \bar{P}_0, \bar{P}_1, \bar{P}_2$ $= \text{GND}; \bar{G}_i = 2.7 \text{ V}$	02	2	14	ns
$\bar{P}_0, \bar{P}_1, \text{ or } \bar{P}_2 \text{ to}$ $C_{n+X}, C_{n+Y}, C_{n+Z}$	t_{PLH2}	$V_{CC} = 5.0 \text{ V}; C_n, \bar{G}_i = 2.7$ $\text{V}; \bar{P}_0, \bar{P}_1, \bar{P}_2 = \text{GND} \underline{11/}$	02	2	11	ns
$\bar{G}_0, \bar{G}_1, \text{ or } \bar{G}_2 \text{ to}$ $C_{n+X}, C_{n+Y}, C_{n+Z}$	t_{PLH3}	$V_{CC} = 5.0 \text{ V}; C_n, \bar{P}_0, \bar{P}_1,$ $\bar{P}_2 = \text{GND}; \bar{G}_i = 2.7 \text{ V} \underline{11/}$	02	2	11	ns
$\bar{P}_1, \bar{P}_2, \text{ or } \bar{P}_3, \text{ to } \bar{G}$	t_{PLH4}	$V_{CC} = 5.0 \text{ V}; C_n, \bar{G}_1, \bar{G}_2,$ $\bar{G}_3 = 2.7 \text{ V}; \bar{P}_i = \text{GND} \underline{11/}$	02	2	11.5	ns
$\bar{G}_0, \bar{G}_1, \bar{G}_2, \text{ or } \bar{G}_3$ to \bar{G}	t_{PLH5}	$V_{CC} = 5.0 \text{ V}; \bar{P}_1, \bar{P}_2, \bar{P}_3$ $= \text{GND}; \bar{G}_i = 2.7 \text{ V} \underline{11/}$	02	2	11.5	ns
$\bar{P}_0, \bar{P}_1, \bar{P}_2, \text{ or } \bar{P}_3$ to \bar{P}	t_{PLH6}	$V_{CC} = 5.0 \text{ V}; \bar{P}_i = \text{GND} \underline{11/}$ $C_n, \bar{G}_i = 2.7 \text{ V}$	02	2	10	ns

1/ Condition of inputs specified in table III.

2/ $V_{IL} = 0.7 \text{ V}$ dc at 125°C .

3/ $V_{OL(max)} = 0.45 \text{ V}$ dc at 125°C .

4/ All unspecified inputs at 5.5 V .

5/ All unspecified inputs at 0 V .

6/ Not more than one output should be shorted at a time.

7/ S_i, M, \bar{A}_i at 4.5 V ; all other inputs grounded; outputs open.

8/ S_i, M at 4.5 V ; all other inputs grounded; outputs open.

9/ In \bar{A}_i and $\bar{B}_i, i = 0, 1, 2, \text{ or } 3$.

10/ In \bar{G}_i and $\bar{P}_i, i = 0, 1, 2, \text{ or } 3$.

11/ If not under test.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 11 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9, 10, 11
Group B test requirements (method 5005) subgroup 5	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3
Additional electrical subgroups for group C periodic inspections	N/A	None
Group D end-point electrical parameters (method 5005)	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1 (see 4.3c.).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

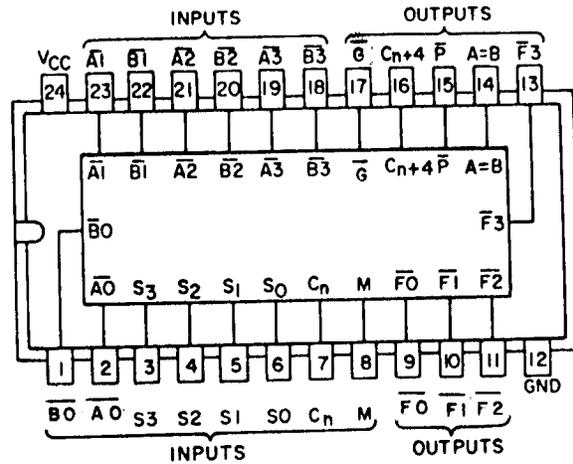
a. Burn-in (method 1015 of MIL-STD-883).

- (1) Test condition D, using the circuit shown on figure 4, or equivalent.
- (2) $T_A = +125^\circ\text{C}$, minimum.

Pin designations

Designation	Pin nos.	Function
$\bar{A}3, \bar{A}2, \bar{A}1, \bar{A}0$	19, 21, 23, 2	Word A inputs
$\bar{B}3, \bar{B}2, \bar{B}1, \bar{B}0$	18, 20, 22, 1	Word B inputs
$S3, S2, S1, S0$	3, 4, 5, 6	Function-select inputs
C_n	7	Inv. carry input
M	8	Mode control input
$\bar{F}3, \bar{F}2, \bar{F}1, \bar{F}0$	13, 11, 10, 9	Function outputs
$A = B$	14	Comparator output
\bar{P}	15	Carry propagate output
C_{n+4}	16	Inv. carry output
\bar{G}	17	Carry generate output
V_{CC}	24	Supply voltage
GND	12	Ground

Cases J, K, and Z

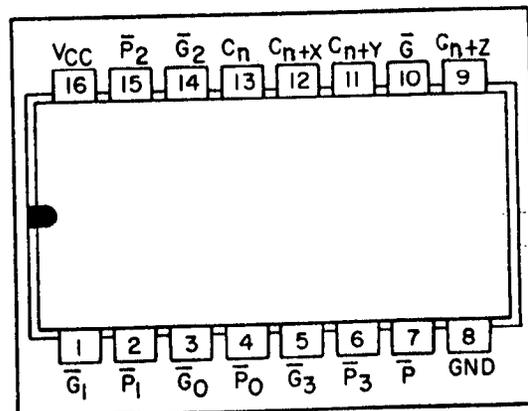


Device type 01

Pin designations

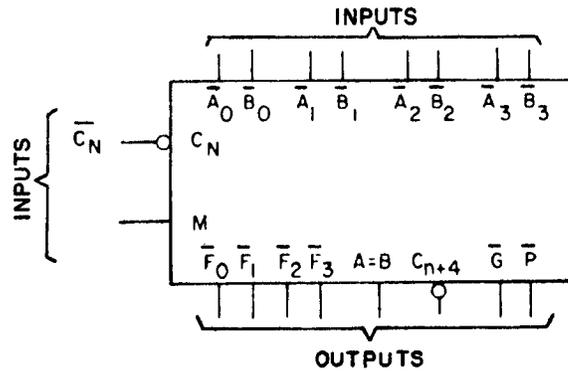
Designation	Pin nos.	Function
C_n	13	Carry input
$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	3, 1, 14, 5	Carry generate input
$\bar{P}0, \bar{P}1, \bar{P}2, \bar{P}3$	4, 2, 15, 6	Carry propagate input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry output
\bar{G}	10	Carry generate output
\bar{P}	7	Carry propagate output

Cases E and F



Device type 02

FIGURE 1. Terminal connections and pin designations.



Selection S ₃ S ₂ S ₁ S ₀	Active high data ^{3/}		
	M = H Logic functions	M = L; Arithmetic operations	
		C _n = 0 C _n = 1 = H	C _n = 1 C _n = 0 = L
0	L L L L	F = \bar{A}	F = A plus 1
1	L L L H	F = $\overline{A + B}$	F = (A + B) plus 1
2	L L H L	F = $\bar{A}B$	F = (A + \bar{B}) plus 1
3	L L H H	F = 0	F = zero
4	L H L L	F = $\bar{A}\bar{B}$	F = A plus $\bar{A}\bar{B}$
5	L H L H	F = \bar{B}	F = (A + B) plus $\bar{A}\bar{B}$
^{2/} 6	L H H L	F = $A \oplus B$	F = A minus B
7	L H H H	F = $A\bar{B}$	F = $\bar{A}\bar{B}$
8	H L L L	F = $\bar{A} + B$	F = A plus AB plus 1
9	H L L H	F = $\overline{A \oplus B}$	F = A, plus B plus 1
10	H L H L	F = B	F = (A + \bar{B}) plus AB plus 1
11	H L H H	F = AB	F = AB
12	H H L L	F = 1	F = A plus A ^{1/}
13	H H L H	F = A + \bar{B}	F = (A + B) plus A plus 1
14	H H H L	F = A + B	F = (A + \bar{B}) plus A plus 1
15	H H H H	F = A	F = A

^{1/} Each bit is shifted to the next more significant position.

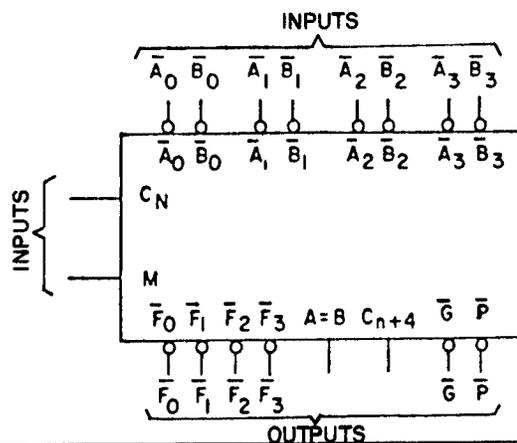
^{2/} This device (ALU) can be used as a comparator when placed in the subtract mode (i. e., S₃S₂S₁S₀ are at logical levels LHHH respectively) and the following expressions are valid:

Active high data

- When C_n is high and C_{n+4} is high, then A ≤ B
- When C_n is low and C_{n+4} is high, then A < B
- When C_n is high and C_{n+4} is low, then A > B
- When C_n is low and C_{n+4} is low, then A ≥ B

^{3/} The table shown applies for positive logic. If negative logic is used, active high data becomes active low data.

FIGURE 2. Truth tables and logic equations for device type 01.



Selection $S_3S_2S_1S_0$	Active low data ^{5/}			
	M = H Logic functions	M = L; Arithmetic operations		
		$C_n = 0 = L$	$C_n = 1 = H$	
0	L L L L	$F = \bar{A}$	F = A minus 1	F = A
1	L L L H	$F = \overline{AB}$	F = AB minus 1	F = AB
2	L L H L	$F = \bar{A} + B$	F = $A\bar{B}$ minus 1	F = $A\bar{B}$
3	L L H H	F = 1	F = minus 1 (2's compl)	F = zero
4	L H L L	$F = \overline{A + B}$	F = A plus (A + \bar{B})	F = A plus (A + \bar{B}) plus 1
5	L H L H	$F = \bar{B}$	F = AB plus (A + \bar{B})	F = AB plus (A + \bar{B}) plus 1
^{4/} 6	L H H L	$F = \overline{A \oplus B}$	F = A minus B minus 1	F = A minus B
7	L H H H	$F = A + \bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) plus 1
8	H L L L	$F = \bar{A}B$	F = A plus (A + B)	F = A plus (A + B) plus 1
9	H L L H	$F = A \oplus B$	F = A plus B	F = A plus B plus 1
10	H L H L	F = B	F = $A\bar{B}$ plus (A + B)	F = $A\bar{B}$ plus (A + B) plus 1
11	H L H H	F = A + B	F = A + B	F = (A + B) plus 1
12	H H L L	F = 0	F = A plus A _{1/}	F = A plus A plus 1
13	H H L H	$F = A\bar{B}$	F = AB plus A	F = AB plus A plus 1
14	H H H L	F = AB	F = $A\bar{B}$ plus A	F = $A\bar{B}$ plus A plus 1
15	H H H H	F = A	F = A	F = A plus 1

^{4/} This device (ALU) can be used as a comparator when placed in the subtract mode (i.e., $S_3S_2S_1S_0$ are at logical levels LHHH respectively) and the following expressions are valid:

Active low data

- When C_n is low and C_{n+4} is low, then $A \leq B$
- When C_n is high and C_{n+4} is low, then $A < B$
- When C_n is low and C_{n+4} is high, then $A > B$
- When C_n is high and C_{n+4} is high, then $A \geq B$

^{5/} The table shown applies for negative logic. If positive logic is used, active low data becomes active high data.

FIGURE 2. Truth tables and logic equations for device type 01 - Continued.

Inputs									Outputs				
C _n	\bar{G}_0	\bar{P}_0	\bar{G}_1	\bar{P}_1	\bar{G}_2	\bar{P}_2	\bar{G}_3	\bar{P}_3	C _{n+x}	C _{n+y}	C _{n+z}	\bar{G}	\bar{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X	H	X				L	
X	H	H	H	X	H	X	H	X				L	
L	H	X	H	X	H	X						L	
X	X	X	X	X	L	X	L	X				L	
X	X	X	L	X	X	L	X	L				L	
X	L	X	X	L	X	L	X	L				L	
H	X	L	X	L	X	L	X	L				L	
		X	X	X	X	H	H						H
		X	X	H	H	H	X						H
		X	H	X	H	X	H	X					H
		X	X	X	X	L	X						H
		X	X	X	L	X	X	L					H
		X	L	X	X	L	X	L					H
		L	X	L	X	L	X	L					L
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = High voltage level
 L = Low voltage level
 X = Don't care

FIGURE 2. Truth tables and logic equations for device type 02 - Continued.

DEVICE TYPE 01

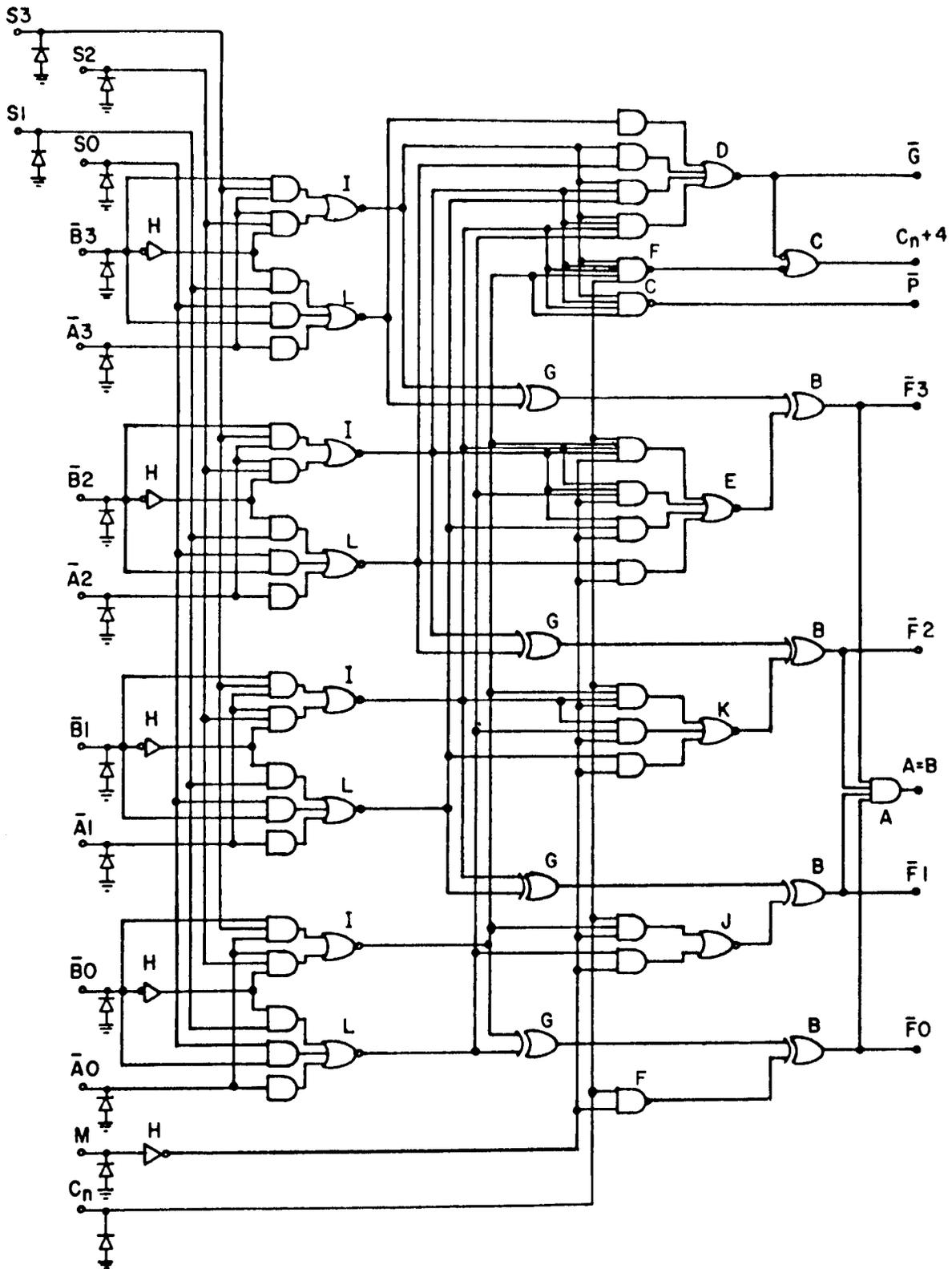


FIGURE 3. Logic diagrams.

DEVICE TYPE 02

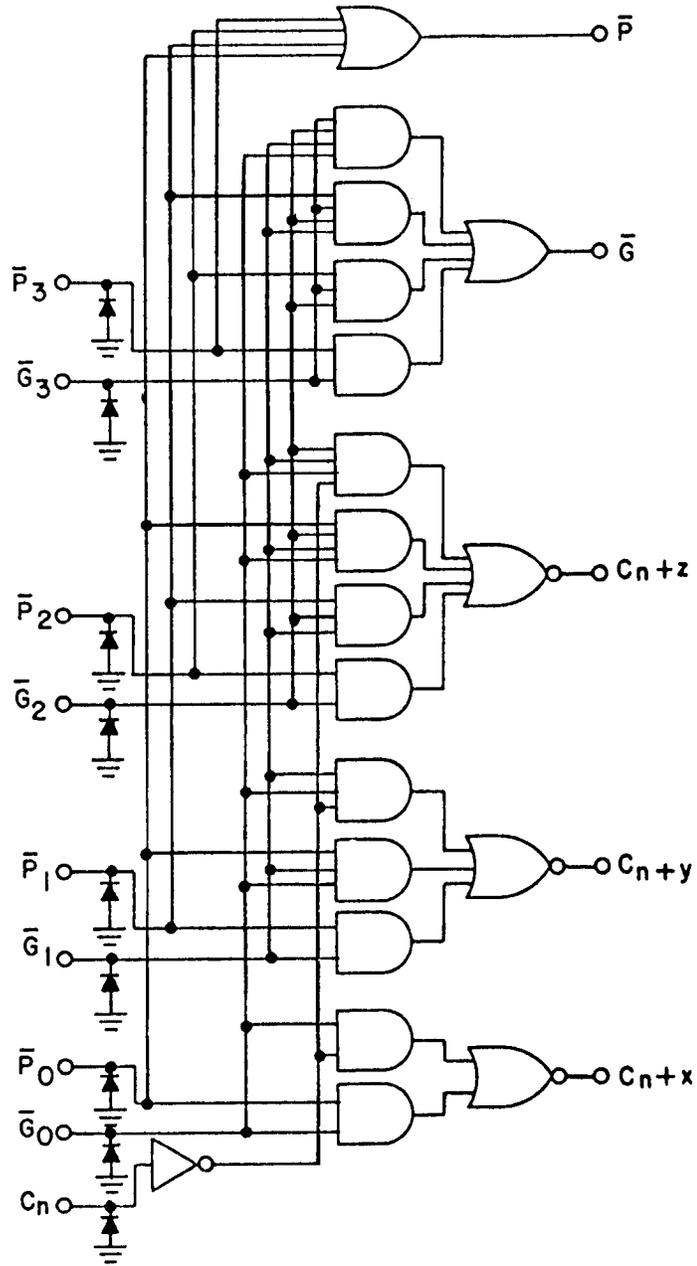
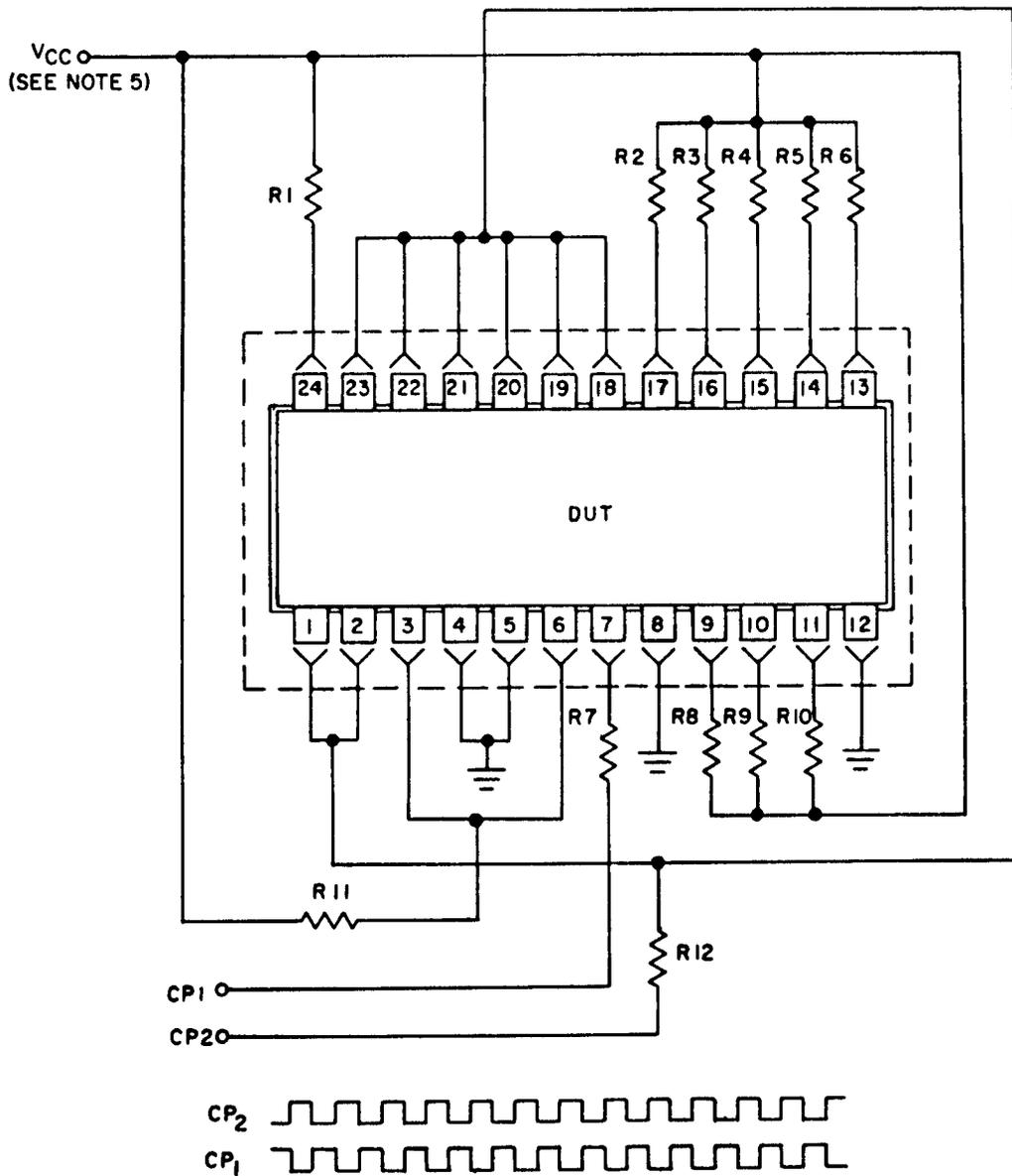


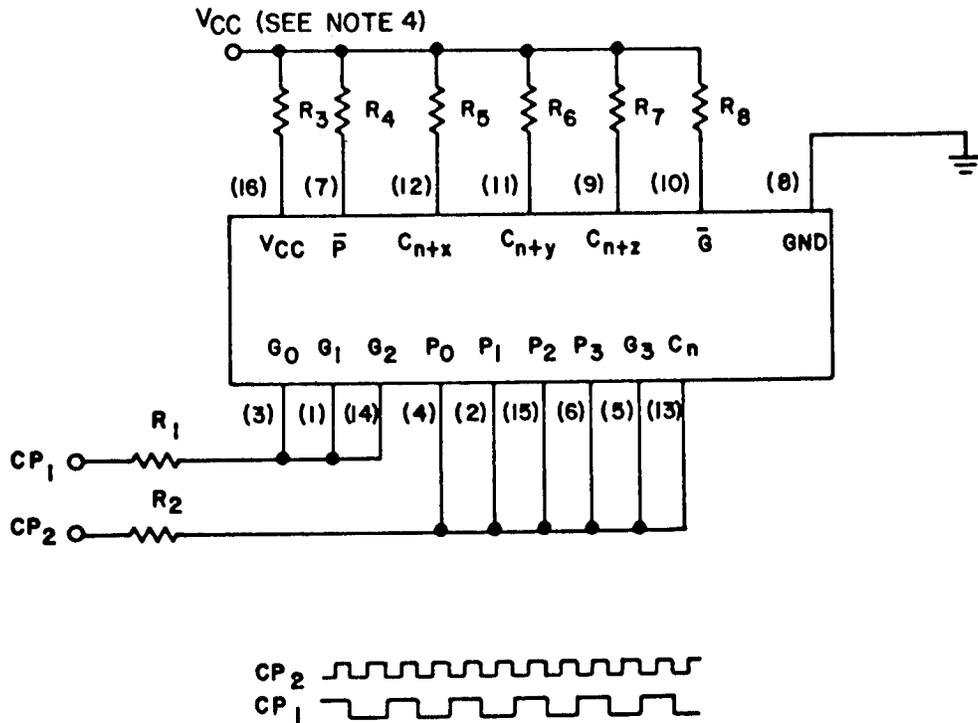
FIGURE 3. Logic diagrams - Continued.



NOTES:

1. $R_1 = 5 \text{ ohms} \pm 5\%$.
2. $R_7 = 27 \text{ ohms} \pm 5\%$.
3. $R_2 \text{ thru } R_6 = R_8 \text{ thru } R_{11} = 100 \text{ ohms} \pm 5\%$.
4. $R_{12} = 82 \text{ ohms} \pm 5\%$.
5. VCC shall be high enough to insure 5 V minimum at device terminals.
6. CP1 = 100 kHz $\pm 10\%$, duty cycle = 50% $\pm 10\%$, 3 V minimum at device terminals.
7. CP2 = 100 kHz $\pm 10\%$, duty cycle = 50% $\pm 10\%$, 3 V minimum at device terminals.

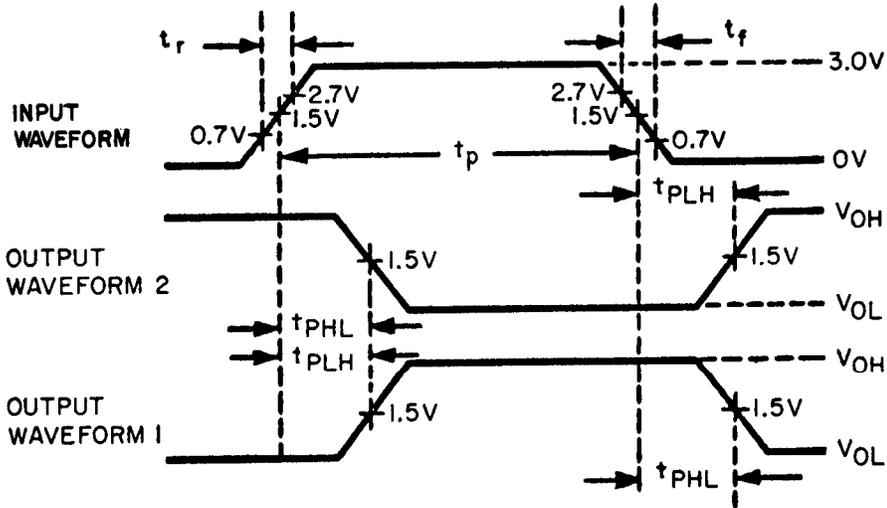
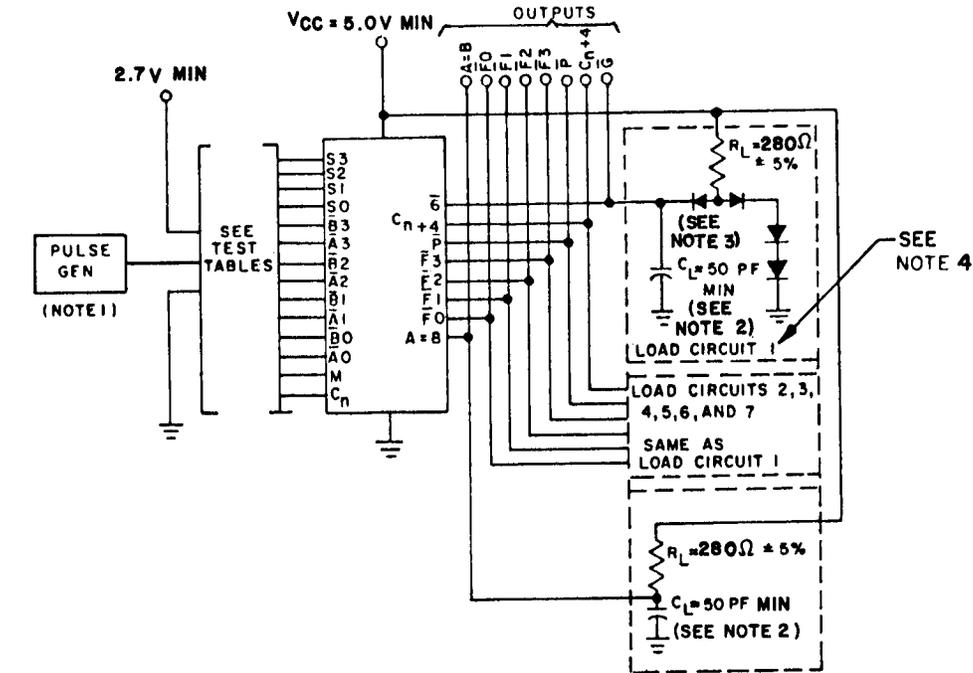
FIGURE 4. Test circuit for burn-in and life test for device type 01.



NOTES:

1. $R_1 = R_2 = 10\Omega \pm 5\%$.
2. $R_3 = 4.7\Omega \pm 5\%$.
3. R_4 thru $R_8 = 180\Omega \pm 5\%$.
4. V_{CC} shall be high enough to insure 5 V minimum at device terminals.
5. $CP_1 = 100 \text{ kHz} \pm 10\%$, duty cycle, 50% $\pm 10\%$, 3 V minimum at device terminals.
6. $CP_2 = 50 \text{ kHz} \pm 10\%$, duty cycle, 50% $\pm 10\%$, 3 V minimum at device terminals.

FIGURE 4. Test circuit for burn-in and life test for device type 02 - Continued.



NOTES:

1. The input pulse has the following characteristics: $PRR \leq 1\text{ MHz}$, $t_r = t_f < 2.5\text{ ns}$, $Z_{OUT} \approx 50\Omega$.
2. C_L Includes probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. Load circuit is required on a given output only where table III indicates "OUT" on that output. Load circuits may otherwise be omitted.

FIGURE 5. Waveforms for propagation delay time and test circuit for device type 01.

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 2.7 \text{ V}$, $S_1 = S_2 = M = 0 \text{ V}$

TEST	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 2.7 V	APPLY GND	APPLY 2.7 V	APPLY GND		
t_{PLH1}	\bar{A}_i ^{1/}	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	Any \bar{F}_i	1
t_{PHL1}							
t_{PLH1}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	Any \bar{F}_i	1
t_{PHL1}							
t_{PLH3}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	1
t_{PHL3}							
t_{PLH3}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	1
t_{PHL3}							
t_{PLH5}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	1
t_{PHL5}							
t_{PLH5}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	1
t_{PHL5}							
t_{PLH7}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F}_i	1
t_{PHL7}							
t_{PLH9}	C_n	None	None	All \bar{A}	All \bar{B}	C_{n+4}	1
t_{PHL9}							
t_{PLH11}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} and C_n	C_{n+4}	2
t_{PHL11}							
t_{PLH11}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} and C_n	C_{n+4}	2
t_{PHL11}							

^{1/} In \bar{A}_i , \bar{B}_i and \bar{F}_i , $i = 0, 1, 2, \text{ or } 3$.

FIGURE 5. Waveforms for propagation delay time and test circuit for device type 01 - Continued.

DIFF MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 2.7 V, S0 = S3 = M = 0 V

TEST	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 2.7 V	APPLY GND	APPLY 2.7 V	APPLY GND		
t_{PLH2}	\bar{A}_i 1/	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	Any \bar{F}_i	1
t_{PHL2}							
t_{PLH2}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	Any \bar{F}_i	2
t_{PHL2}							
t_{PLH4}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	1
t_{PHL4}							
t_{PLH4}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	2
t_{PHL4}							
t_{PLH6}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	1
t_{PHL6}							
t_{PLH6}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	2
t_{PHL6}							
t_{PLH8}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	1
t_{PHL8}							
t_{PLH8}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	2
t_{PHL8}							
t_{PLH10}	C_n	None	None	All \bar{A} and \bar{B}	None	C_{n+4}	1
t_{PHL10}							
t_{PLH12}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}	2
t_{PHL12}							
t_{PLH12}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}	1
t_{PHL12}							

1/ In \bar{A}_i, \bar{B}_i and $\bar{F}_i, i = 0, 1, 2, \text{ or } 3.$

FIGURE 5. Waveforms for propagation delay time and test circuit for device type 01 - Continued.

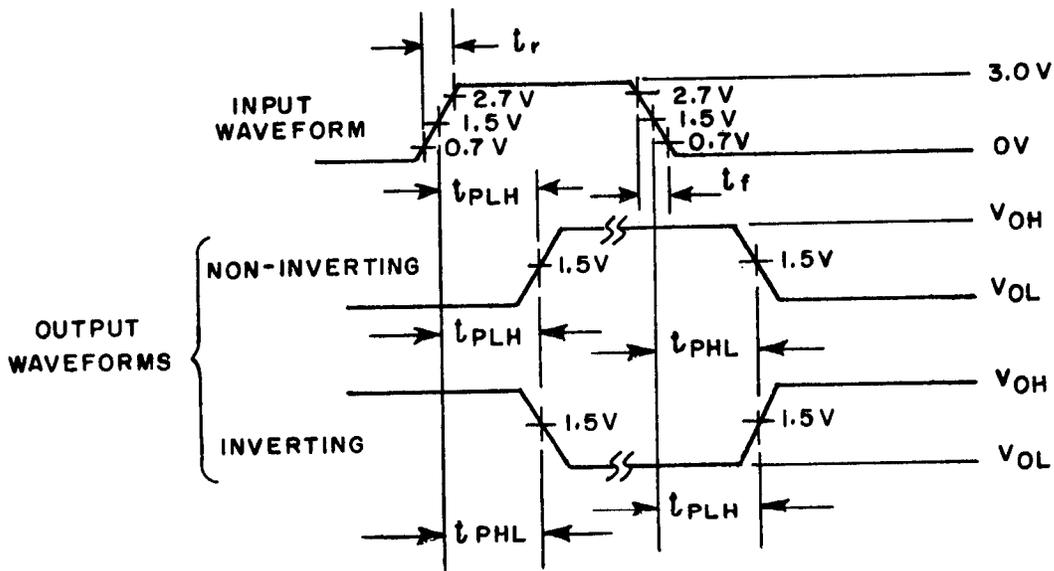
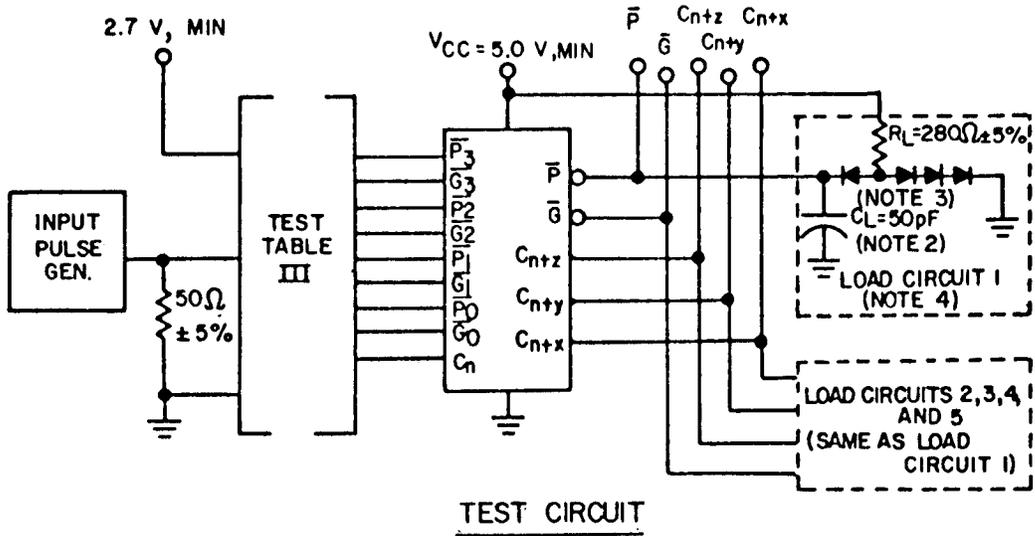
LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 2.7 V, S0 = S3 = 0 V

TEST	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 2.7 V	APPLY GND	APPLY 2.7 V	APPLY GND		
t_{PLH13}	\bar{A}_i 1/	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	Any \bar{F}_i	1
t_{PHL13}							
t_{PLH13}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	Any \bar{F}_i	1
t_{PHL13}							

1 In \bar{A}_i , \bar{B}_i and \bar{F}_i , $i = 0, 1, 2$, or 3 .

FIGURE 5. Waveforms for propagation delay time and test circuit for device type 01 - Continued.



NOTES:

1. The input pulse has the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f \leq 2.5 \text{ ns}$, $Z_{OUT} \approx 50 \Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. Load circuit is required on a given output only where table III indicates "OUT" on that output. Load circuits may otherwise be omitted.

FIGURE 5. Waveforms for propagation delay time and test circuit for device type U2 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883-method	CERES U.K.2	Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open)																								Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Mfn	
I1H1	VOH	3006	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	C _{IN} +4 F ₀ F ₁ F ₂ F ₃	2,5	V	
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				24
I1H2	VOL	3007	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	C _{IN} +4 F ₀ F ₁ F ₂ F ₃ A = B	0,2	0,5	V							
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
				9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
I1H3	I1L1	3009	16	17	18	19	20	21	22	23	24	M	-1	-2	mA															
				17	18	19	20	21	22	23	24																			
				17	18	19	20	21	22	23	24																			
				17	18	19	20	21	22	23	24																			
				17	18	19	20	21	22	23	24																			
				17	18	19	20	21	22	23	24																			
				17	18	19	20	21	22	23	24																			
I1H4	I1L2	3009	17	18	19	20	21	22	23	24	M	-3	-6	V																
				18	19	20	21	22	23	24																				
				18	19	20	21	22	23	24																				
				18	19	20	21	22	23	24																				
				18	19	20	21	22	23	24																				
				18	19	20	21	22	23	24																				
				18	19	20	21	22	23	24																				
I1H5	I1L3	3009	21	22	23	24	M	-4	-8	V																				
				22	23	24																								
				22	23	24																								
				22	23	24																								
				22	23	24																								
				22	23	24																								
				22	23	24																								
I1H6	I1L4	3009	23	24	25	26	27	28	29	30	M	-5	-10	V																
				24	25	26	27	28	29	30																				
				24	25	26	27	28	29	30																				
				24	25	26	27	28	29	30																				
				24	25	26	27	28	29	30																				
				24	25	26	27	28	29	30																				
				24	25	26	27	28	29	30																				
I1H7	I1L5	3009	25	26	27	28	29	30	M	-2	-4	V																		
				26	27	28	29	30																						
				26	27	28	29	30																						
				26	27	28	29	30																						
				26	27	28	29	30																						
				26	27	28	29	30																						
				26	27	28	29	30																						
I1H8	I1L6	3009	26	27	28	29	30	M	-2	-4	V																			
				27	28	29	30																							
				27	28	29	30																							
				27	28	29	30																							
				27	28	29	30																							
				27	28	29	30																							
				27	28	29	30																							
I1H9	I1L7	3009	31	32	33	34	35	36	37	38	M	50	µA																	
				32	33	34	35	36	37	38																				
				32	33	34	35	36	37	38																				
				32	33	34	35	36	37	38																				
				32	33	34	35	36	37	38																				
				32	33	34	35	36	37	38																				
				32	33	34	35	36	37	38																				

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (THIS NOT DESIGNATED MAY BE $\geq 2.0V$, $I \leq 0.8V$, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24	Measured terminal	Test limits		Unit	
					Min	Max		
$T_c = 25^\circ C$	tPH1	3003 (Fig. 5)	1	B_0	2.7 V	2.7 V	20	ns
			2	X_0	IN	2.7 V		
			3	S_3	2.7 V	2.7 V		
			4	S_2	GND	2.7 V	2.7 V	
			5	S_1	GND	2.7 V	2.7 V	
			6	Y_0	2.7 V	2.7 V	2.7 V	
			7	C_n	GND	2.7 V	2.7 V	
			8	M	GND	2.7 V	2.7 V	
			9	F_0	OUT	2.7 V	2.7 V	
			10	F_1	OUT	2.7 V	2.7 V	
			11	F_2	OUT	2.7 V	2.7 V	
			12	F_3	OUT	2.7 V	2.7 V	
			13	F_4	OUT	2.7 V	2.7 V	
	tPH2		139	GND	2.7 V	2.7 V	25	ns
			140	IN	2.7 V	2.7 V		
			141	IN	2.7 V	2.7 V		
			142	IN	2.7 V	2.7 V		
			143	IN	2.7 V	2.7 V		
			144	GND	2.7 V	2.7 V		
			145	GND	2.7 V	2.7 V		
			146	GND	2.7 V	2.7 V		
			147	IN	2.7 V	2.7 V		
			148	IN	2.7 V	2.7 V		
			149	IN	2.7 V	2.7 V		
			150	IN	2.7 V	2.7 V		
			151	IN	2.7 V	2.7 V		
152	GND	2.7 V	2.7 V					
153	GND	2.7 V	2.7 V					
154	GND	2.7 V	2.7 V					
	tPH3		155	2.7 V	2.7 V	23	ns	
			156	GND	2.7 V	2.7 V		
			157	IN	2.7 V	2.7 V		
			158	IN	2.7 V	2.7 V		
			159	IN	2.7 V	2.7 V		
			160	GND	2.7 V	2.7 V		
			161	GND	2.7 V	2.7 V		
			162	GND	2.7 V	2.7 V		
			163	2.7 V	2.7 V	2.7 V		
			164	GND	2.7 V	2.7 V		
			165	GND	2.7 V	2.7 V		
			166	IN	2.7 V	2.7 V		
			167	IN	2.7 V	2.7 V		
168	GND	2.7 V	2.7 V					
169	GND	2.7 V	2.7 V					
170	GND	2.7 V	2.7 V					
	tPH4		171	IN	2.7 V	18	ns	
			172	GND	2.7 V	2.7 V		
			173	GND	2.7 V	2.7 V		
			174	IN	2.7 V	2.7 V		
			175	IN	2.7 V	2.7 V		
			176	GND	2.7 V	2.7 V		
			177	GND	2.7 V	2.7 V		
			178	GND	2.7 V	2.7 V		
			179	GND	2.7 V	2.7 V		
			180	GND	2.7 V	2.7 V		
			181	GND	2.7 V	2.7 V		
			182	GND	2.7 V	2.7 V		
			183	GND	2.7 V	2.7 V		

See footnotes at end of device type 01.

TABLE III. Group A Inspection for device type O1 - Continued.
Terminal conditions (pins not designated may be $V \geq 2.0$ V, $I \leq 0.8$ V, or open).

Subgroup	Symbol	MIL-STD-883-method	Case J,K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Test limits		Unit			
																												Min	Max				
10 $T_c = +125^\circ\text{C}$	t _{PHL11}	3003 (Fig. 5)	415	B ₀	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND	2	25	ns														
				F ₀	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₁	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₂	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₃	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				A-8	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				C _{n+4}	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₅	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₂	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
				F ₃	IN	2.7 V	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND																	
11	t _{PHL12}	423	B ₀	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND	29				
			F ₀	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND					
			F ₁	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND					
			F ₂	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₃	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			A-8	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			C _{n+4}	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₅	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₂	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₃	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
12	t _{PHL13}	439	B ₀	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND	28				
			F ₀	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND					
			F ₁	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND					
			F ₂	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₃	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			A-8	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			C _{n+4}	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₅	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₂	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				
			F ₃	IN	2.7 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	OUT	GND	2.7 V	GND	GND	GND	GND	GND	GND				

1/ Same tests, terminal conditions, and limits as subgroup 10, except $T_c = -55^\circ\text{C}$.

2/ Tests shall be performed in sequence.

3/ Inputs:
A = 3.0 V minimum
B = 0.0 V or GND

4/ Outputs:
H > 1.5 V
L < 1.5 V

5/ Only a summary of attributes data is required.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be $H \geq 2.0$ V, $L \leq 0.8$ V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E _F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	\bar{P}	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{P}_2	V_{CC}		Min	Max	
$T_c +25^\circ C$	V _{OH}	3006	1	2.0 V	0.8 V	2.0 V	2.0 V	2.0 V	0.8 V	-1 mA	GND					0.8 V	0.8 V	2.0 V	4.5 V	\bar{P}	2.5		V
		"	2	0.8 V	0.8 V	2.0 V	"					2.0 V	2.0 V	"	"	C_{n+Z}	"		"				
		"	3	0.8 V	0.8 V	2.0 V	"					0.8 V	0.8 V	"	"	\bar{G}	"		"				
		"	4	0.8 V	2.0 V	"					0.8 V	0.8 V	"	"	C_{n+Y}	"		"					
		"	5	0.8 V	2.0 V	0.8 V	2.0 V	2.0 V	2.0 V	2.0 V	"					0.8 V	0.8 V	"	"	C_{n+X}	"		"
V _{OL}		3007	6	0.8 V	20 mA	"					2.0 V	2.0 V	0.8 V	"	\bar{P}	0.2	0.5	"					
		"	7	0.8 V	20 mA	"					2.0 V	2.0 V	2.0 V	"	C_{n+Z}	"	"	"					
		"	8	2.0 V	2.0 V	"					2.0 V	2.0 V	2.0 V	"	\bar{G}	"	"	"					
		"	9	2.0 V	2.0 V	"					2.0 V	2.0 V	2.0 V	"	C_{n+Y}	"	"	"					
		"	10	2.0 V	2.0 V	"					2.0 V	2.0 V	2.0 V	"	C_{n+X}	"	"	"					
V _{IC}			11	-18 mA	-18 mA															\bar{G}_1		-1.2	"
			12			-18 mA														\bar{P}_1		"	"
			13			-18 mA														\bar{G}_0		"	"
			14			-18 mA														\bar{P}_0		"	"
			15			-18 mA														\bar{G}_3		"	"
			16			-18 mA														\bar{P}_3		"	"
			17			-18 mA														C_n		"	"
			18			-18 mA														\bar{G}_2		"	"
			19			-18 mA														\bar{P}_2		"	"
I _{IL1}		3009	20	0.5 V	5.5 V							GND	5.5 V	5.5 V	5.5 V	\bar{G}_1	-8	-16	mA				
		"	21	5.5 V	0.5 V	5.5 V														\bar{P}_1	-4	-8	"
		"	22		5.5 V	0.5 V														\bar{G}_0	-7	-14	"
		"	23			5.5 V	0.5 V										5.5 V			\bar{P}_0	-4	-8	"
		"	24				5.5 V	0.5 V												\bar{G}_3	-4	-8	"
		"	25					5.5 V	0.5 V											\bar{P}_3	-2	-4	"
		"	26						5.5 V								0.5 V			C_n	-1	-2	"
		"	27														GND	0.5 V		\bar{G}_2	-7	-14	"
		"	28														5.5 V	5.5 V	0.5 V	\bar{P}_2	-3	-6	"
I _{IH1}		3010	29	2.7 V	GND	GND	GND	GND	GND								GND	GND		\bar{G}_1	400		μA
		"	30	GND	2.7 V	GND														\bar{P}_1	200		"
		"	31	GND	GND	2.7 V														\bar{G}_0	350		"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	\bar{P}	GND	Cn+Z	\bar{G}	Cn+Y	Cn+X	Cn	\bar{G}_2	\bar{P}_2	V _{CC}		Min	Max	
T _C +25 °C	I _{IH4}	3010	32	GND	GND	GND	2.7 V	GND	GND							GND	GND	GND	5.5 V	P ₀		200	μA
	I _{IH5}	"	33	"	"	"	GND	2.7 V	GND							"	"	"	"	G ₃		200	"
	I _{IH6}	"	34	"	"	"	"	GND	2.7 V							"	"	"	"	P ₃		100	"
	I _{IH7}	"	35	"	"	"	"	"	GND							2.7 V	"	"	"	C _n		50	"
	I _{IH8}	"	36	"	"	"	"	"	"							5.5 V	2.7 V	"	"	G ₂		350	"
	I _{IH9}	"	37	"	"	"	"	"	"							GND	GND	2.7 V	"	P ₂		150	"
	I _{IH10}	"	38	5.5 V	"	"	"	"	"							5.5 V	"	GND	"	G ₁		1	mA
	I _{IH11}	"	39	GND	5.5 V	"	"	"	"							"	"	"	"	P ₁		"	"
	I _{IH12}	"	40	"	GND	5.5 V	"	"	"							"	"	"	"	G ₀		"	"
	I _{IH13}	"	41	"	"	GND	5.5 V	"	"							GND	"	"	"	P ₀		"	"
	I _{IH14}	"	42	"	"	"	"	GND	5.5 V	"						"	"	"	"	G ₃		"	"
	I _{IH15}	"	43	"	"	"	"	"	GND	5.5 V						"	"	"	"	P ₃		"	"
	I _{IH16}	"	44	"	"	"	"	"	"	GND						5.5 V	"	"	"	C _n		"	"
	I _{IH17}	"	45	"	"	"	"	"	"	"						5.5 V	5.5 V	"	"	G ₂		"	"
	I _{IH18}	"	46	"	"	"	"	"	"	"						GND	GND	5.5 V	"	P ₂		"	"
	I _{OS}	47	3011		5.5 V	GND	5.5 V	5.5 V	GND												P		-100
48		"		GND	GND	5.5 V	GND	5.5 V	5.5 V	GND										C _{n+Z}		"	"
49		"		5.5 V	5.5 V	GND	GND	5.5 V	5.5 V	5.5 V										G		"	"
50		"		GND	GND	GND	GND	"	"	"										C _{n+Y}		"	"
51		"		"	"	GND	"	"	"	"										C _{n+Z}		"	"
I _{ICL}	3005	52	5.5 V	"	5.5 V	"	GND	GND											V _{CC}		99	"	
I _{ICCH}	3005	53	GND	"	5.5 V	"	5.5 V	5.5 V											V _{CC}		65	"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E,F Method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{P}_2	V_{CC}	Min		Max					
1	ICEX		54	GND	GND	5.5 V	5.5 V	GND	GND	5.5 V	GND	5.5 V	GND	GND	GND	GND	GND	GND	5.5 V	5.5 V	F		250	μ A		
			55	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	5.5 V	5.5 V	GND	5.5 V	GND	5.5 V	5.5 V	GND	GND	GND	GND	G		"	"	"	
			56	GND	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	C _{n+Y}		"	"	"
			58	GND	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	C _{n+X}		"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _c = +125°C and V _{IC} tests are omitted. V _{IL} = 0.7 V dc and V _{OL(max)} = 0.45 V dc.																									
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _c = -55°C and V _{IC} tests are omitted.																									
7	Functional tests 1/4/		59	B 2/	L 3/	GND	H 3/	H 3/	L 3/	H 3/	H 3/	B 2/	B 2/	B 2/	B 2/	A11 output	H or L as shown 3/									
			60	B	B	A	A	A	H	H	H	GND	H	H	L	H	H	A	A	A	A	"	"			
			61	A	A	B	B	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			62	A	B	A	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			63	B	A	A	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			64	A	B	A	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			65	B	B	A	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
			66	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			69	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
			71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
8 1/4/	Same tests, terminal conditions, and limits as for subgroup 7, except T _c = +125°C and -55°C.																									
9	t _{PLH1}	3003 (Fig 5)	73	2.7 V	GND	2.7 V	GND	2.7 V	2.7 V	GND	GND				OUT	IN	2.7 V	GND	5.0 V	C _n to C _{n+X}	2	12	ns			
			74	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	C _n to C _{n+X}	"	12.5	"		
			75	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	C _n to C _{n+Y}	"	12	"		
			76	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	C _n to C _{n+Y}	"	12.5	"		
			77	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	C _n to C _{n+Z}	"	12	"		
			78	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	C _n to C _{n+Z}	"	12.5	"		
			79	"	"	"	"	"	"	"	"	"	"	"	OUT	2.7 V	"	"	"	"	F ₀ to C _{n+X}	"	9	"		

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883E,F Test method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit	
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	\bar{P}	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{P}_2	V_{CC}	Measured terminal	Min		Max
9 $T_C = +25^\circ C$	tPHL2	3003 (Fig 5)	80	2.7 V	GND	2.7 V	IN	2.7 V	2.7 V		GND	GND			OUT	2.7 V	2.7 V	GND	5.0 V	\bar{P}_0 to C_{n+X}	2	9	ns
	tPLH2	"	81	"	"	"	"	"	"	"	"	"		OUT					"	\bar{P}_0 to C_{n+Y}	"	"	"
	tPHL2	"	82	"	"	"	"	"	"	"	"	"		OUT					"	\bar{P}_0 to C_{n+Y}	"	"	"
	tPLH2	"	83	"	"	"	"	"	"	"	"	OUT							"	\bar{P}_0 to C_{n+Z}	"	"	"
	tPHL2	"	84	"	"	"	"	"	"	"	"	OUT							"	\bar{P}_0 to C_{n+Z}	"	"	"
	tPLH2	"	85	"	IN	"	GND	"	"	"	"	"		OUT					"	\bar{P}_1 to C_{n+Y}	"	"	"
	tPHL2	"	86	"	"	"	"	"	"	"	"	"		OUT					"	\bar{P}_1 to C_{n+Y}	"	"	"
	tPLH2	"	87	"	"	"	"	"	"	"	"	"	OUT						"	\bar{P}_1 to C_{n+Z}	"	"	"
	tPHL2	"	88	"	"	"	"	"	"	"	"	"			OUT				"	\bar{P}_1 to C_{n+Z}	"	"	"
	tPLH2	"	89	"	"	GND	"	"	"	"	"	"						IN	"	\bar{P}_2 to C_{n+Z}	"	"	"
	tPHL2	"	90	"	"	"	"	"	"	"	"	"						IN	"	\bar{P}_2 to C_{n+Z}	"	"	"
	tPLH3	"	91	"	"	IN	"	"	"	"	"	"				OUT	GND	"	GND	\bar{G}_0 to C_{n+X}	"	"	"
	tPHL3	"	92	"	"	"	"	"	"	"	"	"				OUT	"	"	"	\bar{G}_0 to C_{n+X}	"	"	"
	tPLH3	"	93	"	"	"	"	"	"	"	"	"			OUT				"	\bar{G}_0 to C_{n+Y}	"	"	"
tPHL3	"	94	"	"	"	"	"	"	"	"	"			OUT				"	\bar{G}_0 to C_{n+Y}	"	"	"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E,F method	Cases Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit	
				\bar{G}_1	\bar{F}_1	\bar{G}_0	\bar{F}_0	\bar{G}_3	\bar{F}_3	\bar{P}	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{F}_2	V_{CC}		Min	Max		
9 $T_C = +25^\circ C$	t_{pLH3}	3003 (F7g 5)	95	2.7 V	GND	IN	GND	2.7 V	2.7 V		GND	OUT				GND	2.7 V	GND	5.0 V	\bar{G}_0 to C_{n+Z}	2	9	ns	
	t_{pHL3}	"	96	2.7 V	"	IN	"	"	"		"	OUT				"	"	"	"	\bar{G}_0 to C_{n+Z}	"	"	"	
	t_{pLH3}	"	97	IN	"	2.7 V	"	"	"		"		OUT			"	"	"	"	"	\bar{G}_1 to C_{n+Y}	"	"	"
	t_{pHL3}	"	98	"	"	"	"	"	"		"			OUT		"	"	"	"	"	\bar{G}_1 to C_{n+Y}	"	"	"
	t_{pLH3}	"	99	"	"	"	"	"	"		"	OUT				"	"	"	"	"	\bar{G}_1 to C_{n+Z}	"	"	"
	t_{pHL3}	"	100	"	"	"	"	"	"		"		"			"	"	"	"	"	\bar{G}_1 to C_{n+Z}	"	"	"
	t_{pLH3}	"	101	2.7 V	"	"	"	"	"		"		"			"	IN	IN	"	"	\bar{G}_2 to C_{n+Z}	"	"	"
	t_{pHL3}	"	102	"	"	"	"	"	"		"		"			"	IN	IN	"	"	\bar{G}_2 to C_{n+Z}	"	"	"
	t_{pLH4}	"	103	"	IN	GND	"	"	"	GND		"		OUT		2.7 V	2.7 V	"	"	"	\bar{F}_1 to \bar{G}	"	9.5	"
	t_{pHL4}	"	104	"	IN	"	"	"	"	"		"		"		"	"	"	"	"	\bar{P}_1 to \bar{G}	"	12.5	"
	t_{pLH4}	"	105	"	GND	"	"	"	"	"		"		"		"	"	"	IN	"	\bar{P}_2 to \bar{G}	"	9.5	"
	t_{pHL4}	"	106	"	"	"	"	"	"	"		"		"		"	"	"	IN	"	\bar{P}_2 to \bar{G}	"	12.5	"
t_{pLH4}	"	107	"	"	"	"	"	"	IN		"		"		"	"	"	GND	"	\bar{P}_3 to \bar{G}	"	9.5	"	
t_{pHL4}	"	108	"	"	"	"	"	"	IN		"		"		"	"	"	"	"	\bar{P}_3 to \bar{G}	"	12.5	"	
t_{pLH5}	"	109	"	"	"	IN	"	"	GND		"		"		"	"	"	"	"	\bar{G}_0 to \bar{G}	"	9.5	"	
t_{pHL5}	"	110	"	"	IN	"	"	"	"		"		"		"	"	"	"	"	\bar{G}_0 to \bar{G}	"	12.5	"	
t_{pLH5}	"	111	IN	"	"	2.7 V	"	"	"		"		"		"	"	"	"	"	\bar{G}_1 to \bar{G}	"	9.5	"	
t_{pHL5}	"	112	IN	"	"	2.7 V	"	"	"		"		"		"	"	"	"	"	\bar{G}_1 to \bar{G}	"	12.5	"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E,F method	Cases test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit
				\bar{G}_1	\bar{F}_1	\bar{G}_0	\bar{F}_0	\bar{G}_3	\bar{F}_3	\bar{P}	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{F}_2	V_{CC}	Measured terminal	Min	
9 $T_C = +25^\circ C$	t_{pLH5}	3003 (Fig 5)	113	2.7 V	GND	2.7 V	GND	2.7 V	GND		GND		OUT			2.7 V	IN	GND	5.0 V	\bar{G}_2 to \bar{G}	2	9.5 ns
	t_{pHL5}	"	114	"	"	"	"	2.7 V	"	"	"	"	"	"	"	"	IN	"	"	\bar{G}_2 to \bar{G}	"	12.5 "
	t_{pLH5}	"	115	"	"	"	"	IN	"	"	"	"	"	"	"	"	2.7 V	"	"	\bar{G}_3 to \bar{G}	"	9.5 "
	t_{pHL5}	"	116	"	"	"	"	IN	"	"	"	"	"	"	"	"	"	"	"	\bar{G}_3 to \bar{G}	"	12.5 "
	t_{pLH6}	"	117	"	"	"	IN	2.7 V	"	OUT	"	"	"	"	"	"	"	"	"	\bar{F}_0 to \bar{P}	"	8.5 "
	t_{pHL6}	"	118	"	"	"	IN	"	"	"	"	"	"	"	"	"	"	"	"	\bar{F}_0 to \bar{P}	"	12 "
	t_{pLH6}	"	119	"	IN	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	\bar{F}_1 to \bar{P}	"	8.5 "
	t_{pHL6}	"	120	"	IN	"	"	"	"	"	"	"	"	"	"	"	"	"	"	\bar{F}_1 to \bar{P}	"	12 "
	t_{pLH6}	"	121	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	\bar{P}_2 to \bar{P}	"	8.5 "
	t_{pHL6}	"	122	"	"	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	\bar{F}_2 to \bar{P}	"	12 "
	t_{pLH6}	"	123	"	"	"	"	"	"	IN	"	"	"	"	"	"	"	GND	"	\bar{P}_3 to \bar{P}	"	8.5 "
	t_{pHL6}	"	124	"	"	"	"	"	"	IN	"	"	"	"	"	"	"	"	"	\bar{F}_3 to \bar{P}	"	12 "
	10 $T_C = +125^\circ C$	t_{pLH1}	"	125	"	"	"	"	"	2.7 V	"	"	"	"	"	OUT	IN	2.7 V	"	"	C_n to C_{n+X}	"
t_{pHL1}		"	126	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	C_n to C_{n+X}	"	14.5 "
t_{pLH1}		"	127	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	C_n to C_{n+Y}	"	14 "
t_{pHL1}		"	128	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	C_n to C_{n+Y}	"	14.5 "
t_{pLH1}		"	129	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	C_n to C_{n+Z}	"	14 "
t_{pHL1}	"	130	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	C_n to C_{n+Z}	"	14.5 "	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E,F test method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit	
				\bar{C}_1	\bar{P}_1	\bar{C}_0	\bar{P}_0	\bar{C}_3	\bar{F}_3	\bar{P}	GND	\bar{C}_{n+Z}	\bar{C}	\bar{C}_{n+Y}	\bar{C}_{n+X}	\bar{C}_n	\bar{C}_2	\bar{P}_2	VCC	Measured terminal	Min		Max
10 $T_C = +125^\circ\text{C}$	t_{PLH2}	3003 (F19 5)	131	2.7 V	GND	2.7 V	IN	2.7 V	2.7 V						OUT	2.7 V	2.7 V	GND	5.0 V	\bar{P}_0 to \bar{C}_{n+X}	2	11	ns
	t_{PHL2}	"	132	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	\bar{P}_0 to \bar{C}_{n+X}	"	"	"
	t_{PLH2}	"	133	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	\bar{P}_0 to \bar{C}_{n+Y}	"	"	"
	t_{PHL2}	"	134	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	\bar{P}_0 to \bar{C}_{n+Y}	"	"	"
	t_{PLH2}	"	135	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	\bar{P}_0 to \bar{C}_{n+Z}	"	"	"
	t_{PHL2}	"	136	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	\bar{P}_0 to \bar{C}_{n+Z}	"	"	"
	t_{PLH2}	"	137	"	IN	"	GND	"	"	"	"	"	"	"	OUT	"	"	"	"	\bar{P}_1 to \bar{C}_{n+Y}	"	"	"
	t_{PHL2}	"	138	"	"	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	\bar{P}_1 to \bar{C}_{n+Y}	"	"	"
	t_{PLH2}	"	139	"	"	"	"	"	"	"	"	"	OUT	"	"	"	"	"	"	\bar{P}_1 to \bar{C}_{n+Z}	"	"	"
	t_{PHL2}	"	140	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	\bar{P}_1 to \bar{C}_{n+Z}	"	"	"
	t_{PLH2}	"	141	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	\bar{P}_2 to \bar{C}_{n+Z}	"	"	"
	t_{PHL2}	"	142	"	"	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	\bar{P}_2 to \bar{C}_{n+Z}	"	"	"
	t_{PLH3}	"	143	"	"	"	IN	"	"	"	"	"	"	"	"	OUT	GND	"	GND	\bar{C}_0 to \bar{C}_{n+X}	"	"	"
	t_{PHL3}	"	144	"	"	"	IN	"	"	"	"	"	"	"	"	OUT	GND	"	GND	\bar{C}_0 to \bar{C}_{n+X}	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E,F test method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit		
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{P}_2	V_{CC}	Measured terminal	Min	Max			
10 $T_C = +125^\circ C$	t_{PLH3}	3003 (Fig 5)	145	2.7 V	GND	IN	GND	2.7 V	2.7 V	GND	GND			OUT		GND	2.7 V	GND	5.0 V	\bar{G}_0 to C_{n+Y}	2	11	ns	
	t_{PHL3}	"	146	"	"	"	"	"	"	"	"	"	"	OUT		"	"	"	"	\bar{G}_0 to C_{n+Y}	"	"	"	
	t_{PLH3}	"	147	"	"	"	"	"	"	"	"	OUT				"	"	"	"	\bar{G}_0 to C_{n+Z}	"	"	"	
	t_{PHL3}	"	148	"	"	"	"	"	"	"	"	OUT				"	"	"	"	\bar{G}_0 to C_{n+Z}	"	"	"	
	t_{PLH3}	"	149	IN	"	2.7 V	"	"	"	"	"	"	"	OUT		"	"	"	"	"	\bar{G}_1 to C_{n+Y}	"	"	"
	t_{PHL3}	"	150	"	"	"	"	"	"	"	"	"	"	OUT		"	"	"	"	"	\bar{G}_1 to C_{n+Y}	"	"	"
	t_{PLH3}	"	151	"	"	"	"	"	"	"	"	"	OUT			"	"	"	"	"	\bar{G}_1 to C_{n+Z}	"	"	"
	t_{PHL3}	"	152	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	"	\bar{G}_1 to C_{n+Z}	"	"	"
	t_{PLH3}	"	153	2.7 V	"	"	"	"	"	"	"	"	"	"		"	"	IN	"	"	\bar{G}_2 to C_{n+Z}	"	"	"
	t_{PHL3}	"	154	"	"	"	"	"	"	"	"	"	"	"		"	"	IN	"	"	\bar{G}_2 to C_{n+Z}	"	"	"
	t_{PLH4}	"	155	"	IN	"	"	"	"	GND	"	"	"	OUT		"	2.7 V	2.7 V	"	"	\bar{P}_1 to \bar{G}	"	11.5	"
	t_{PHL4}	"	156	"	IN	"	"	"	"	"	"	"	"	"		"	"	"	"	"	\bar{P}_1 to \bar{G}	"	14.5	"
	t_{PLH4}	"	157	"	"	GND	"	"	"	"	"	"	"	"		"	"	"	IN	"	\bar{P}_2 to \bar{G}	"	11.5	"
	t_{PHL4}	"	158	"	"	"	"	"	"	"	"	"	"	"		"	"	"	IN	"	\bar{P}_2 to \bar{G}	"	14.5	"
	t_{PLH4}	"	159	"	"	"	"	"	"	IN	"	"	"	"		"	"	"	GND	"	\bar{P}_3 to \bar{G}	"	11.5	"
	t_{PHL4}	"	160	"	"	"	"	"	"	IN	"	"	"	"		"	"	"	"	"	\bar{P}_3 to \bar{G}	"	14.5	"
t_{PLH5}	"	161	"	"	"	IN	"	"	GND	"	"	"	"		"	"	"	"	"	\bar{G}_0 to \bar{G}	"	11.5	"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H \geq 2.0 V, L \leq 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 E/F test method	Cases no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		Unit		
				\bar{G}_1	\bar{P}_1	\bar{G}_0	\bar{P}_0	\bar{G}_3	\bar{P}_3	\bar{P}	GND	C_{n+Z}	\bar{G}	C_{n+Y}	C_{n+X}	C_n	\bar{G}_2	\bar{P}_2	V_{CC}	Measured terminal	Min		Max	
10 $T_C = +125^\circ C$	t_{PHL5}	3003 (Fig 5)	162	2.7 V	GND	IN	GND	2.7 V	GND	GND	GND		OUT			2.7 V	2.7 V	GND	5.0 V	\bar{G}_0 to \bar{G}	2	14.5	ns	
	t_{PLH5}	"	163	IN	"	2.7 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	\bar{G}_1 to \bar{G}	"	11.5	"
	t_{PHL5}	"	164	IN	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	\bar{G}_1 to \bar{G}	"	14.5	"
	t_{PLH5}	"	165	2.7 V	"	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	"	\bar{G}_2 to \bar{G}	"	11.5	"
	t_{PHL5}	"	166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	"	\bar{G}_2 to \bar{G}	"	14.5	"
	t_{PLH5}	"	167	"	"	"	"	"	IN	"	"	"	"	"	"	"	"	2.7 V	"	"	\bar{G}_3 to \bar{G}	"	11.5	"
	t_{PHL5}	"	168	"	"	"	"	"	IN	"	"	"	"	"	"	"	"	"	"	"	\bar{G}_3 to \bar{G}	"	14.5	"
	t_{PLH6}	"	169	"	"	"	IN	2.7 V	"	"	OUT	"	"	"	"	"	"	"	"	"	\bar{P}_0 to \bar{P}	"	10	"
	t_{PHL6}	"	170	"	"	"	IN	IN	"	"	"	"	"	"	"	"	"	"	"	"	\bar{P}_0 to \bar{P}	"	14	"
	t_{PLH6}	"	171	"	"	IN	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	\bar{P}_1 to \bar{P}	"	10	"
	t_{PHL6}	"	172	"	"	IN	"	"	"	"	"	"	"	"	"	"	"	"	"	"	\bar{P}_1 to \bar{P}	"	14	"
	t_{PLH6}	"	173	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	IN	"	"	\bar{P}_2 to \bar{P}	"	10	"
	t_{PHL6}	"	174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	IN	"	"	\bar{P}_2 to \bar{P}	"	14	"
	t_{PLH6}	"	175	"	"	"	"	"	"	IN	"	"	"	"	"	"	"	"	GND	"	\bar{P}_3 to \bar{P}	"	10	"
	t_{PHL6}	"	176	"	"	"	"	"	"	IN	"	"	"	"	"	"	"	"	GND	"	\bar{P}_3 to \bar{P}	"	14	"

11 Same tests, terminal conditions, and limits as subgroup 10, except $T_C = -55^\circ C$.

1/ Tests shall be performed in sequence.

2/ Inputs:

- A = 3.0 V minimum
- B = 0.0 V or GND

3/ Outputs:

- H > 1.5 V
- L < 1.5 V

4/ Only a summary of attributes data is required.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by Appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.

- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

- GND - - - - - Ground zero voltage potential.
- V_{IN} - - - - - Voltage level at an input terminal.
- I_{IN} - - - - - Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54S181
02	54S182

6.6 Manufacturers' designations. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designations.

Device type	Circuits	
	A	B
	Texas Instruments	Signetics Corp.
01	X	X
02	X	

Custodians:

Army - ER
Navy - EC
Air Force - 17

Preparing activity:

Air Force - 17

(Project 5962-0683)

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Agent:

DLA - ES