

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL TTL,
SHIFT REGISTERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, shift register microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	4 bit right-shift, left-shift register
02	5 bit shift register
03	8 bit parallel-out serial shift register
04	8 bit parallel-load shift register
05	4 bit bidirectional shift register
06	4 bit parallel-access shift register

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline, MIL-M-38510, appendix C</u>
A	F-1 (14-pin, 1/4" x 1/4", flat pack)
B	F-3 (14-pin, 3/16" x 1/4", flat pack)
C	D-1 (14-pin, 1/4" x 3/4", dual-in-line pack)
D	F-2 (14-pin, 1/4" x 3/8", flat pack)
E	D-2 (16-pin, 1/4" x 7/8", dual-in-line pack)
F	F-5 (16-pin, 1/4" x 3/8", flat pack)

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	- - - - -	-0.5 Vdc to 7.0 Vdc
Input voltage range	- - - - -	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range	- - - - -	-65° to 150°C
Maximum power dissipation per register, P_D	1/	
Device type 01	- - - - -	422 mWdc
Device type 02	- - - - -	400 mWdc
Device type 03	- - - - -	322 mWdc
Device type 04	- - - - -	372 mWdc
Device type 05	- - - - -	360 mWdc
Device type 06	- - - - -	372 mWdc

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Lead temperature
 (soldering, 10 seconds) - - - - - 300°C
 Thermal resistance, junction to case - - - - - $\theta_{JC} = \begin{cases} 0.09^\circ\text{C}/\text{mW} & \text{for flat pack} \\ 0.08^\circ\text{C}/\text{mW} & \text{for dual-in-line pack} \end{cases}$
 Junction temperature - - - - - $T_J = 175^\circ\text{C}$

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	- - - - -	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	- - - - -	2.0 Vdc
Maximum low level input voltage	- - - - -	0.8 Vdc
Ambient operating temperature range	- - - - -	-55° to 125°C
Fan out		
Device types 01, 02, 04, 05, and 06		
High logic level	- - - - -	20
Low logic level	- - - - -	10
Device type 03		
High logic level	- - - - -	10
Low logic level	- - - - -	5
Device type 01		
Low level setup time at mode control with respect to clock 1 input	- - - - -	35 ns minimum
High level setup time at mode control with respect to clock 2 input	- - - - -	35 ns minimum
Low level setup time at mode control with respect to clock 2 input	- - - - -	10 ns minimum
High level setup time at mode control with respect to clock 1 input	- - - - -	10 ns minimum
Width of clock pulse	- - - - -	20 ns minimum
Setup time required at serial A, B, C, D inputs	- - - - -	20 ns minimum
Hold time required at serial A, B, C, D inputs	- - - - -	5 ns minimum
Device type 02		
Minimum clock pulse width	- - - - -	35 ns maximum
Minimum clear pulse width	- - - - -	30 ns maximum
Minimum preset pulse width	- - - - -	30 ns maximum
Serial input setup time	- - - - -	30 ns minimum
Serial input hold time	- - - - -	0 ns minimum
Device type 03		
Minimum clock pulse width	- - - - -	30 ns maximum
Minimum clear pulse width	- - - - -	50 ns maximum
Serial setup time	- - - - -	15 ns minimum
Serial hold time	- - - - -	10 ns maximum
Device type 04		
Width of clock input pulse	- - - - -	20 ns minimum
Width of load input pulse	- - - - -	25 ns minimum
Clock enable setup time	- - - - -	30 ns minimum
Parallel input setup time	- - - - -	10 ns minimum
Serial input setup time	- - - - -	35 ns minimum
Shift setup time	- - - - -	45 ns minimum
Hold time at serial input	- - - - -	0 ns maximum
Hold time at parallel input	- - - - -	25 ns maximum
Device type 05		
Width of clock input pulse	- - - - -	20 ns minimum
Width of clear input pulse	- - - - -	20 ns minimum
Data input setup time	- - - - -	20 ns minimum
Clear input setup time	- - - - -	25 ns minimum
Hold time at any input	- - - - -	7 ns minimum
Mode control setup time	- - - - -	30 ns minimum

Device type 06	
Width of clock input pulse	16 ns minimum
Width of clear input pulse	12 ns minimum
Shift load input setup time	27 ns minimum
Data input setup time	20 ns minimum
Clear input setup time	25 ns minimum
Shift load release time	10 ns maximum
Data hold time	0 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables and timing diagrams. The truth tables and timing diagrams shall be as specified on figure 2.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Schematic circuits. The schematic circuits shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range, unless otherwise specified.

MIL-M-38510/9D
TABLE I. Electrical characteristics.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}, V_{IN} = 2.0 \text{ V}$ $I_{OH} = -400 \mu\text{A}$	02,03	2.4		Volts
		$V_{CC} = 4.5 \text{ V}, V_{IN} = 2.0 \text{ V}$ $I_{OH} = -800 \mu\text{A}$	01,04, 05,06	2.4		Volts
'Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, V_{IN} = 0.8 \text{ V}$ $I_{OL} = 16 \text{ mA}$	01,02,04, 05,06		0.4	Volts
		$V_{CC} = 4.5 \text{ V}, V_{IN} = 0.8 \text{ V}$ $I_{OL} = 8 \text{ mA}$	03		0.4	Volts
High level input voltage	V_{IH}	$V_{CC} = 4.5 \text{ V}$	01,02,03, 04,05,06	2.0		Volts
Low level input voltage	V_{IL}	$V_{CC} = 4.5 \text{ V}$	01,02,03, 04,05,06		0.8	Volts
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}, I_{IN} = -12 \text{ mA}$ $T_A = 25^\circ\text{C}$	01,02,03 04,05,06		-1.5	Volts
High level input current at any input except mode control	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	01		40	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	01		100	μA
High level input current at mode control	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	01		80	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	01		200	μA
High level input current at any input except preset	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	02		40	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	02		100	μA
High level input current at preset	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	02		200	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	02		500	μA
High level input current at any input except clear	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	03		40	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	03		100	μA
High level input current at clear	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	03		80	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	03		200	μA
High level input current other than load input	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	04		40	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	04		100	μA
High level input current, load input	I_{IH3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	04		120	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	04		300	μA
High level input current	I_{IH1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 2.4 \text{ V}$	05,06		40	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	05,06		100	μA
Low level input current at any input except mode control	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	01	-0.4	-1.6	mA
Low level input current at mode control	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	01	-0.8	-3.2	mA
Low level input current at any input except preset	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	02	-0.7	-1.6	mA
Low level input current at preset	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	02	-3.0	-8.0	mA
Low level input current at any input except clear	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	03	-0.4	-1.6	mA
Low level input current at clear	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	03	-0.7	-2.6	mA

See footnotes at end of table.

TABLE I. Electrical characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Low level input current, load input	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	04	-1.2	-3.9	mA
Low level input current other than clock and load input	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	04	-0.4	-1.3	mA
Low level input current, clock input	I_{IL3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	04	-0.4	-1.6	mA
Low level input current other than S_0 , S_1 , and clock input	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	05	-0.4	-1.3	mA
Low level input current at S_0 and S_1 input	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	05	-0.4	-1.6	mA
Low level input current at clock input	I_{IL3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	05	-0.7	-1.6	mA
Low level input current at clear input	I_{IL1}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	06	-0.4	-1.3	mA
Low level input current other than clear and clock inputs	I_{IL2}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	06	-0.4	-1.6	mA
Low level input current at clock input	I_{IL3}	$V_{CC} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	06	-0.7	-1.6	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}$ 1/		01	-18	-57 mA
				02,05,06	-20	-57 mA
				03	-10	-27.5 mA
				04	-20	-55 mA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$ 2/		01	72	mA
				02	68	mA
				04,05,06	63	mA
Supply current	I_{CC1}	$V_{CC} = 5.5 \text{ V}, V_{IN(\text{Clock})} = 0.4 \text{ V}$ 2/	03		44	mA
	I_{CC2}	$V_{CC} = 5.5 \text{ V}, V_{IN(\text{Clock})} = 2.4 \text{ V}$ 2/	03		54	mA
Maximum shift frequency	f_{MAX}	$V_{CC} = 5 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 400\Omega \pm 5\%$ (See figure 6)	01	16		MHz
Propagation delay time, low-to-high level from clock 1 or clock 2 to outputs	t_{PLH}			10	42	ns
Propagation delay time, high-to-low level from clock 1 or clock 2 to outputs	t_{PHL}			10	49	ns
Maximum clock frequency	f_{MAX}		02	7		MHz
Propagation delay time, low-to-high level, from clock to output	t_{PLH1}	$V_{CC} = 5 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 400\Omega \pm 5\%$ (See figure 7)	02	12	56	ns
Propagation delay time, high-to-low level, from clock to output	t_{PHL1}			12	56	ns
Propagation delay time, low-to-high level, from preset to output	t_{PLH2}			12	59	ns
Propagation delay time, high-to-low level, from clear to output	t_{PHL3}			12	77	ns

See footnotes at end of table.

TABLE I. Electrical characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Maximum clock frequency	f_{MAX}	$V_{CC} = 5 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 800\Omega \pm 5\%$ (See figure 8)	03	18		MHz
Propagation delay time, high-to-low level, clear input to Q outputs	t_{PHL1}			12	63	ns
Propagation delay time, high-to-low level, clock input to Q outputs	t_{PHL2}			10	52	ns
Propagation delay time, low-to-high level, clock input to Q outputs	t_{PLH2}			10	42	ns
Maximum clock frequency	f_{MAX}	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 400\Omega \pm 5\%$ (See figure 9)	04	14		MHz
Propagation delay time, low-to-high level, load input to any output	t_{PLH1}			10	40	ns
Propagation delay time, high-to-low level, load input to any output	t_{PHL1}			11	60	ns
Propagation delay time, low-to-high level, clock input to any output	t_{PLH2}			6	37	ns
Propagation delay time, high-to-low level, clock input to any output	t_{PHL2}			10	47	ns
Propagation delay time, low-to-high level, H input to Q_H output	t_{PLH3}			5	27	ns
Propagation delay time, high-to-low level, H input to Q_H output	t_{PHL3}			11	54	ns
Propagation delay time, low-to-high level, H input to \bar{Q}_H output	t_{PLH4}			10	41	ns
Propagation delay time, high-to-low level, H input to \bar{Q}_H output	t_{PHL4}			10	41	ns
Maximum clock frequency	f_{MAX}	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 400\Omega \pm 5\%$ (See figure 10)	05	18		MHz
Propagation delay time, high-to-low level output from clear	t_{PHL1}			7	48	ns
Propagation delay time, low-to-high level output from clock	t_{PLH2}			7	36	ns
Propagation delay time, high-to-low level output from clock	t_{PHL2}			7	44	ns

See footnotes at end of table.

TABLE I. Electrical characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Maximum clock frequency	f_{MAX}	$V_{CC} = 5.0 \text{ V}$ $C_L = 50 \text{ pF} \pm 10\%$ $R_L = 400\Omega \pm 5$ (See figure 11)	06	24		MHz
Propagation delay time, high-to-low level output from clear	t_{PHL1}			7	34	ns
Propagation delay time, low-to-high level output from clock	t_{PLH2}			7	28	ns
Propagation delay time, high-to-low level output from clock	t_{PHL2}			7	34	ns

1/ Not more than one output should be shorted at a time.

2/ Device type:

- 01 - With the outputs open, mode control at 4.5 V, clock pulse applied to both clock inputs, I_{CC} is measured immediately after the application of the clock pulse.
- 02 - With the outputs open, presets at 4.5 V, I_{CC} is measured with the clock at ground and again with the clock at 4.5 V.
- 03 - I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V applied to clear.
- 04 - With the outputs open, serial at ground, clock, clock inhibit, and parallel inputs at 4.5 V, I_{CC} is measured by applying momentary ground, then 4.5 V to shift load prior to measurement.
- 05 - With all outputs open, inputs A thru D grounded, 5.5 V applied to S_0 , S_1 , clear, and the serial inputs, I_{CC} is tested by applying clock pulse.
- 06 - With the outputs open, clear at 5.5 V, shift load, J, K, and data inputs grounded, I_{CC} is measured by applying clock pulse.

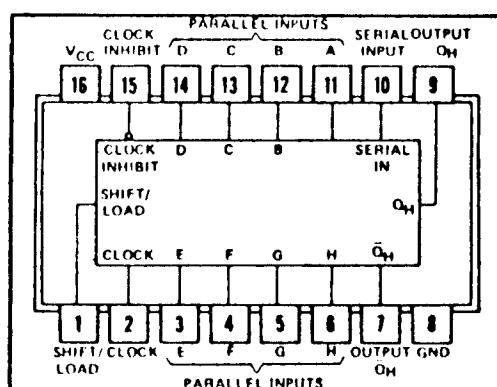
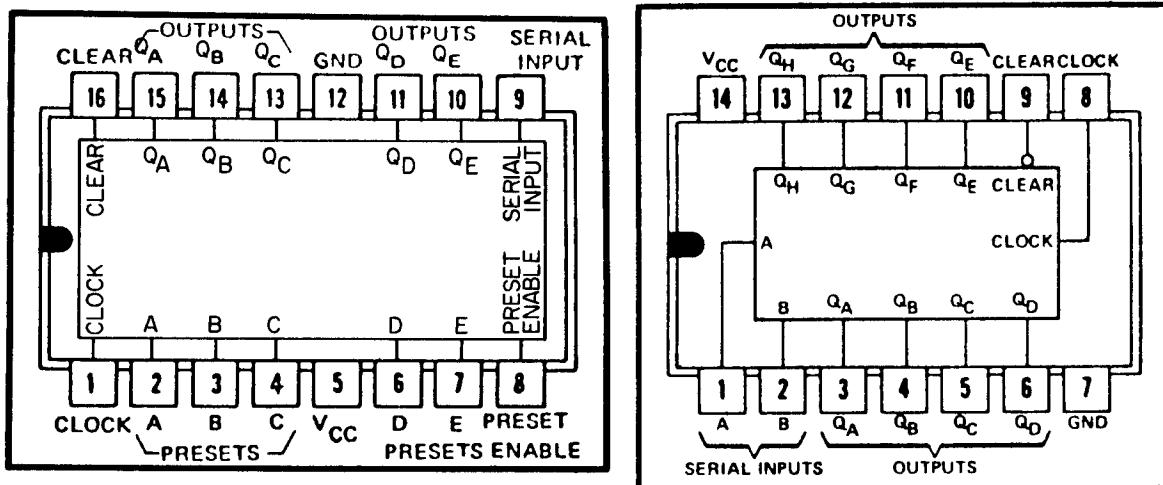
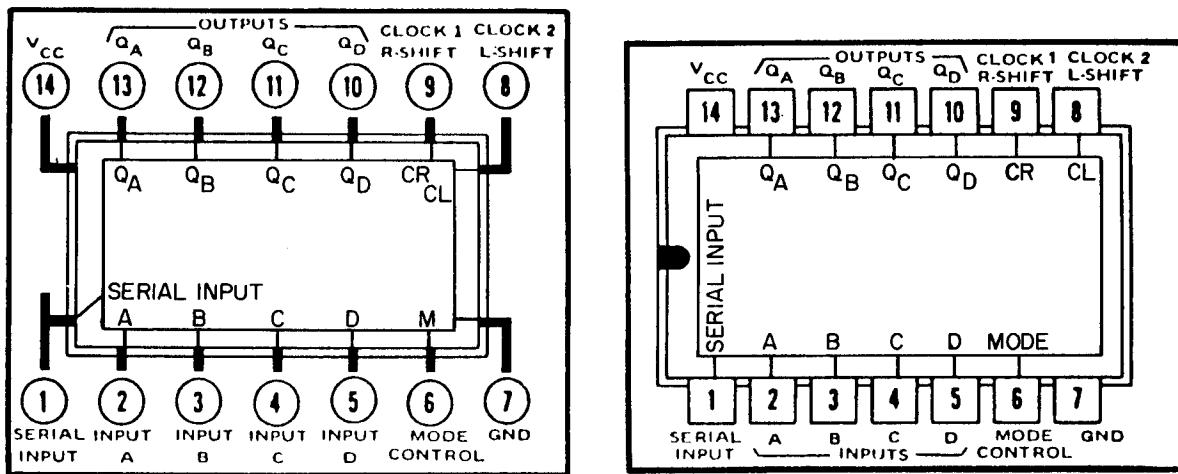
3.5 Electrical test requirements. Electrical test requirements shall be as specified in table II. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification and quality conformance by device class are specified in table II. (Subgroups 7 and 8 testing require only a summary of attributes data).

TABLE II. Electrical test requirements.

Applicable tests and MIL-STD-883 test methods	Subgroups (see table III) 1/		
	Class S device 2/	Class B device 2/	Class C device 2/
Interim electrical parameters (pre burn-in) (method 5004)	1	1	
Final electrical test parameters method 5004	1*,2,3,7, 9,10,11	1*,2,3, 7,9	1,7
Group A test requirements method 5005	1,2,3,7,8, 9,10,11	1,2,3,7, 9,10,11	1,2,3, 7,9
Group C end-point electrical parameters (method 5005)		1,2,3	1
Additional electrical subgroups for group C periodic inspections			10,11
Group D end-point electrical parameters (method 5005)	1,2,3	1,2,3	1

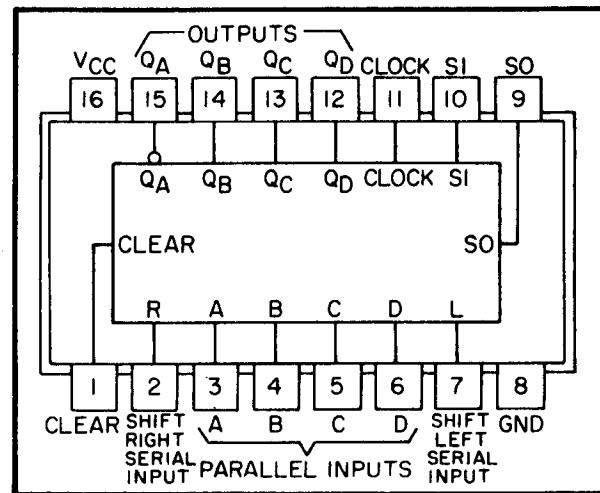
1/ (*) indicates PDA applies to subgroup 1 (see 4.2 c).

2/ Blank spaces indicate tests are not applicable.

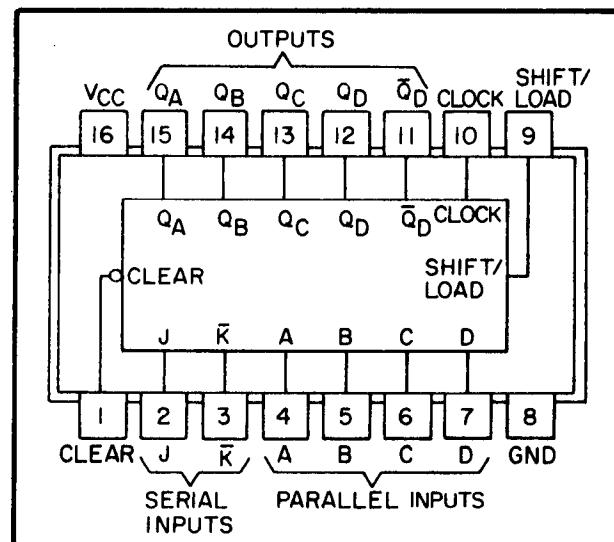


Cases E and F
Device Type 04

FIGURE 1. Terminal connections.



Cases E and F
Device Type 05



Cases E and F
Device Type 06

FIGURE 1. Terminal connections - continued

MIL-M-38510/9D
Device type 01

MODE CONTROL	INPUTS					OUTPUTS			
	CLOCKS		SERIAL	PARALLEL		QA	QB	QC	QD
	2 (L)	1 (R)		A	B	C	D		
H	H	X	X	X	X	X	X	QA0	QB0
H	H	↓	X	X	a	b	c	a	b
H	↓	X	X	QB†	QC†	QD†	d	QBn	QCn
L	L	H	X	X	X	X	X	QA0	QB0
L	X	↓	H	X	X	X	X	H	QA _n
L	X	↓	L	X	X	X	X	L	QA _n
↑	L	L	X	X	X	X	X	QA0	QB0
↓	L	L	X	X	X	X	X	QA0	QB0
↓	L	H	X	X	X	X	X	QA0	QB0
↑	H	L	X	X	X	X	X	QA0	QB0
↑	H	H	X	X	X	X	X	QA0	QB0

^tShifting left required external connection of QB to A, QC to B, and QD to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established.

QA_n, QB_n, QC_n, QD_n = the level of QA, QB, QC, or QD, respectively, before the most-recent ↓ transition of the clock.

Device type 02

CLEAR	INPUTS					OUTPUTS						
	PRESET ENABLE	PRESET				CLOCK	SERIAL	QA	QB	QC	QD	QE
		A	B	C	D							
L	L	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	↑	H	H	QA _n	QB _n	QC _n	QD _n
H	L	X	X	X	X	↑	L	L	QA _n	QB _n	QC _n	QD _n

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

QA0, QB0, etc = the level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.

QA_n, QB_n, etc = the level of QA, QB, etc, respectively before the most-recent ↑ transition of the clock.

Device type 03

CLEAR	INPUTS			OUTPUTS			
	CLOCK	A	B	QA	QB	...	QH
L	X	X	X	L	L	L	
H	L	X	X	QA0	QB0	QH0	
H	↑	H	H	H	QA _n	QG _n	
H	↑	L	X	L	QA _n	QG _n	
H	↑	X	L	L	QA _n	QG _n	

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QA_n, QG_n = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

FIGURE 2. Truth tables and timing diagrams.

MIL-M-38510/9D
Device type 04

INPUTS					INTERNAL		OUTPUT	
SHIFT/ LOAD	CLOCK	CLOCK	SERIAL	PARALLEL	A...H	QA	QB	QH
L	X	X	X	X	a...h	a	b	h
H	L	L	X	X	X	QA0	QB0	QH0
H	L	↑	H	X	X	H	QA _n	QG _n
H	L	↑	L	X	X	L	QA _n	QG _n
H	H	↑	X	X	X	QA0	QB0	QH0

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a...h = the level of steady-state input at inputs A thru H, respectively.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady state input conditions were established.

QA_n, QG_n = the level of QA or QG, respectively, before the most recent ↑ transition of the clock.

Device type 05

CLEAR	INPUTS					OUTPUTS				
	MODE S ₁ S ₀	CLOCK	SERIAL		PARALLEL		QA	QB	QC	QD
			LEFT	RIGHT	A	B				
L	X X	X	X	X	X X X X	X X X X	L	L	L	L
H	X X	L	X	X	X X X X	X X X X	QA0	QB0	QC0	QD0
H	H H	↑	X	X	a b c d	a b c d	a b c d	a b c d	a b c d	a b c d
H	L H	↑	X	H	X X X X	X X X X	H	QA _n	QB _n	QC _n
H	L H	↑	X	L	X X X X	X X X X	L	QA _n	QB _n	QC _n
H	H L	↑	H	X	X X X X	X X X X	QBn	QCn	QDn	H
H	H L	↑	L	X	X X X X	X X X X	QBn	QCn	QDn	L
H	L L	X	X	X	X X X X	X X X X	QA0	QB0	QC0	QD0

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively

QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established

QA_n, QB_n, QC_n, QD_n = the level of QA, QB, QC, or QD, respectively, before the most recent ↑ transition of the clock

Device type 06

CLEAR	INPUTS					OUTPUTS				
	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL		QA	QB	QC	QD
			J	K	A	B				
L	X	X	X X	X X	X X X X	X X X X	L	L	L	L
H	L	↑	X X	a b c d	a b c d	a b c d	a b c d	ād	a b c d	ād
H	H	L	X X	X X X X	X X X X	X X X X	QA0	QB0	QC0	QD0
H	H	↑	L H	X X X X	X X X X	X X X X	QA0	QA0	QBn	QCn
H	H	↑	L L	X X X X	X X X X	X X X X	L	QA _n	QBn	QCn
H	H	↑	H H	X X X X	X X X X	X X X X	H	QA _n	QBn	QCn
H	H	↑	H L	X X X X	X X X X	X X X X	āAn	āAn	QBn	QCn

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively

QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established

QA_n, QB_n, QC_n = the level of QA, QB, or QC, respectively, before the most recent transition of the clock

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 01

Positive logic: Mode control = L for right shift.
 Mode control = H for left shift or parallel load.

Transfer of information to the output pins occurs when the clock input goes from a logical H to a logical L.

Device type 02

Positive logic: Low input of clear sets all outputs to logical L.

Clear input is independent of clock.
 Preset is independent of the clock or clear inputs.

The flip-flops may be independently set to the logical H state by applying a logical H to both the preset input of the specific flip-flop and the common preset input.

Transfer of information to the output pins occurs when the clock input goes from a logical L to a logical H.

The clear input shall be a logical H and the preset input shall be at a logical L when clocking occurs.

The proper information shall appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform.

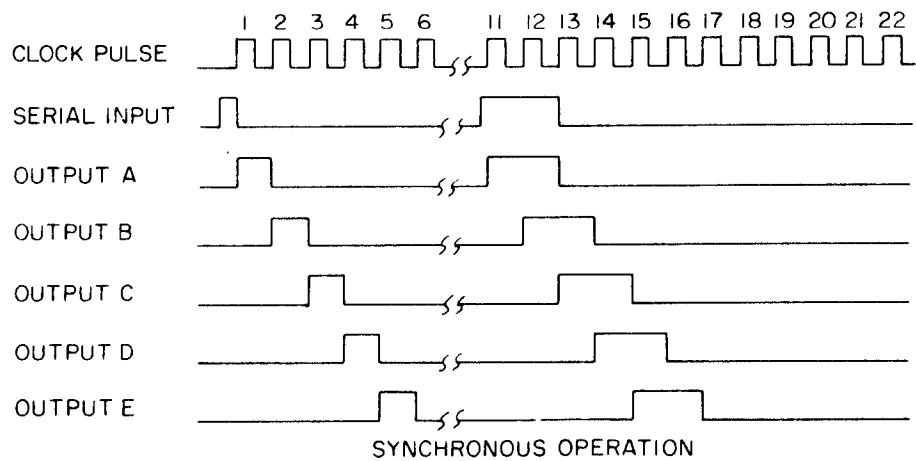
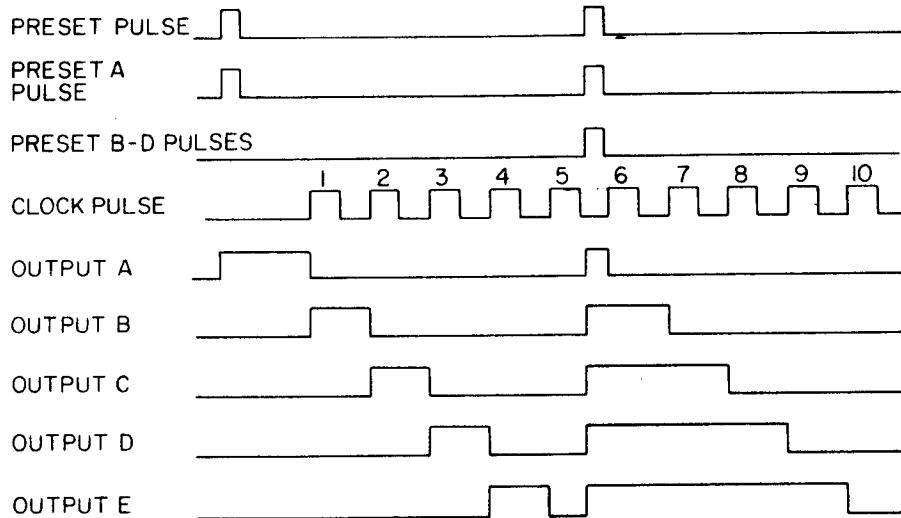


FIGURE 2. Truth tables and timing diagrams - Continued.



ASYNCHRONOUS OPERATION

DEVICE TYPE 02

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

NOTE:

INPUTS NOT SHOWN ARE HELD AT LOGIC LEVEL "L".

Device type 03

SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

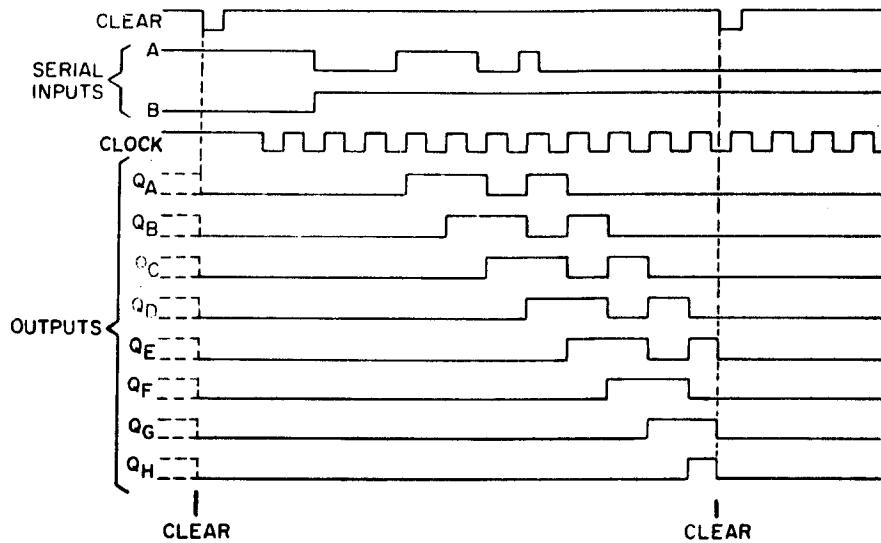
Positive logic: t_n = bit time before clock pulse. t_{n+1} = bit time after clock pulse.

Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

The clear input is asynchronous. Low-level at clear input sets all outputs to logical low.

FIGURE 2. Truth table and timing diagrams - continued.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES



Device Type 04

Positive logic: Transfer of information to the output occurs when the clock input goes from a logical L to a logical H.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES

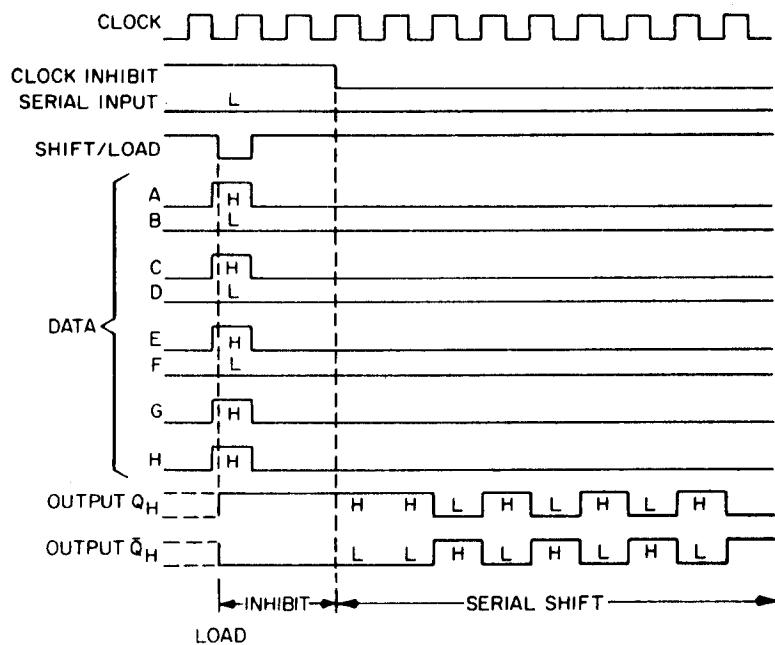


FIGURE 2. Truth tables and timing diagrams - continued.

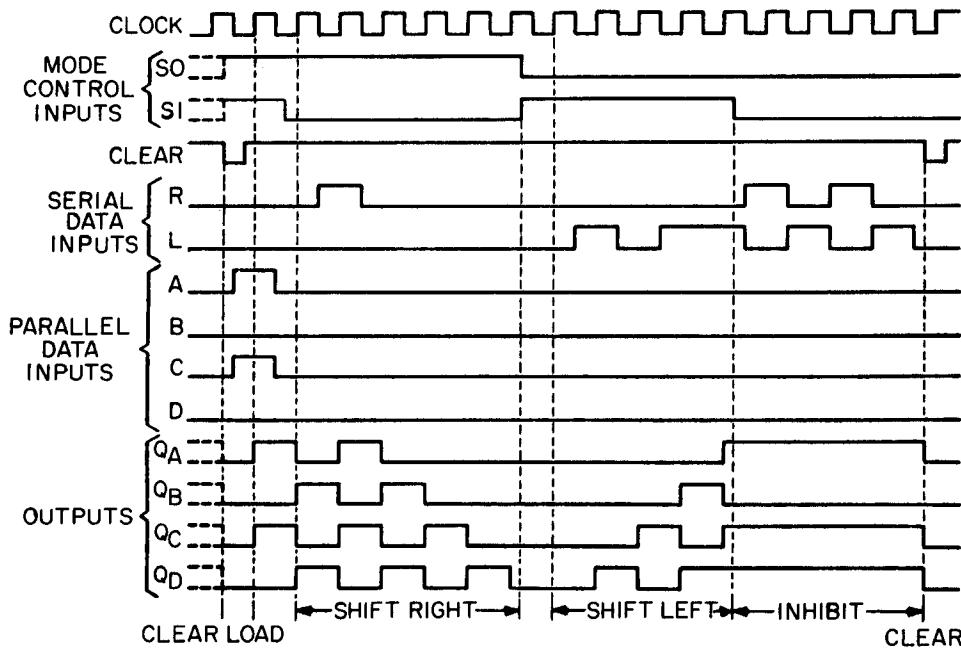
Device Type 05**Positive logic:**

The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	SO
Parallel (Broadside) Load	H	H
Shift Right (in the direction QA toward QD)	L	H
Shift Left (In the direction QD toward QA)	H	L
Inhibit Clock (Do nothing)	L	L

In the parallel-load mode, data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

FIGURE 2. Truth tables and timing diagrams - continued.

Device type 06

Positive logic:

The registers have two modes of operation:

Parallel (broadside) load

Shift (in direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J - \bar{K} inputs. These inputs permit the first stage to perform as a J - \bar{K} , D-, or T-type flip-flop as shown in the truth table.

TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	\bar{K}	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	L	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

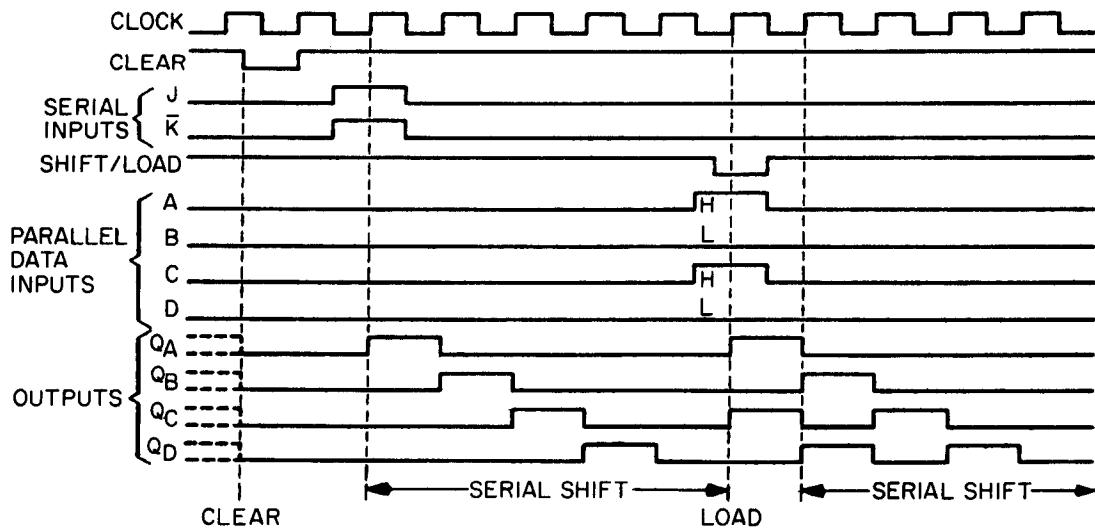
H = high level, L = low level

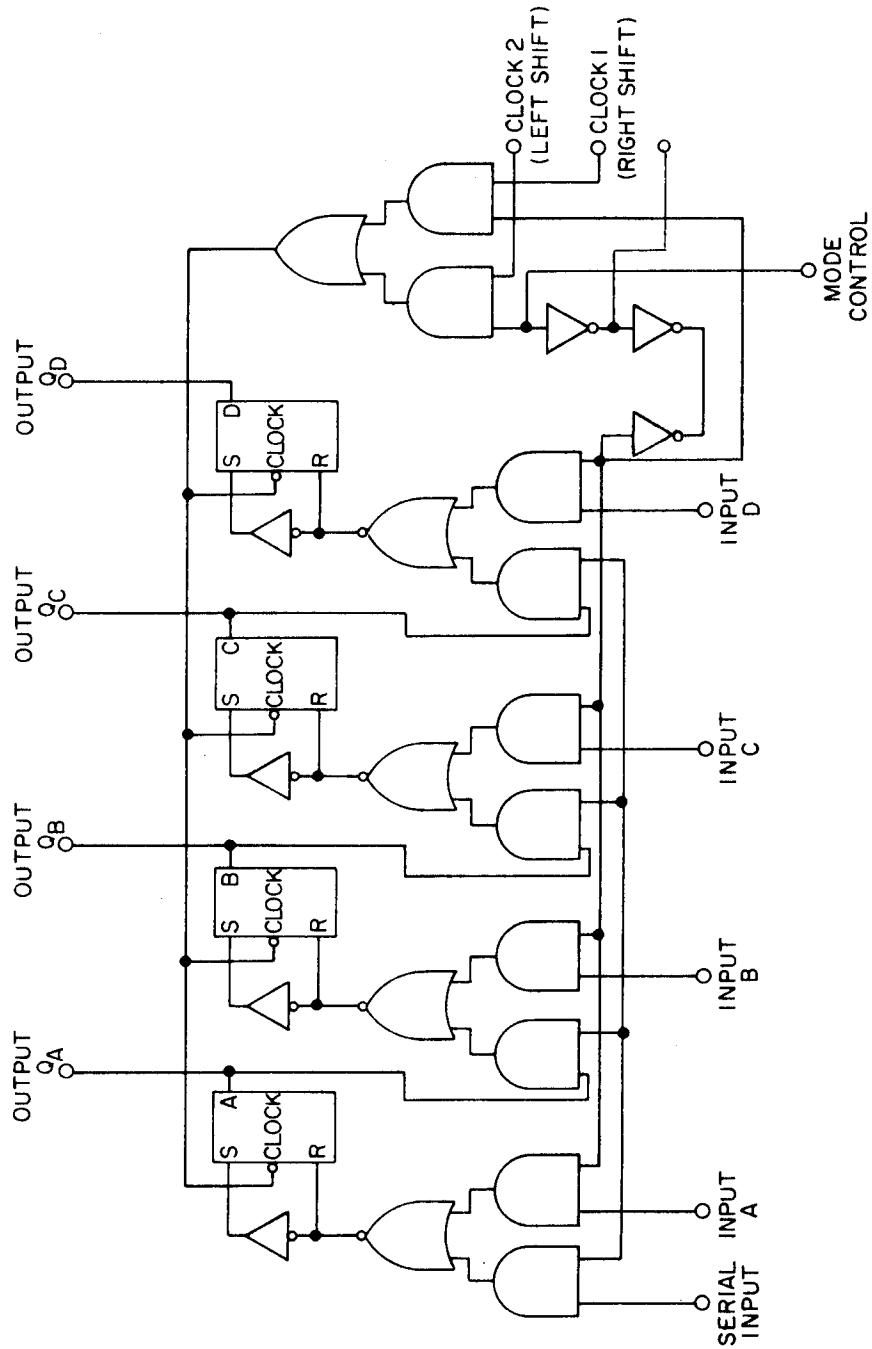
NOTES: 1. t_n = bit time before clock pulse

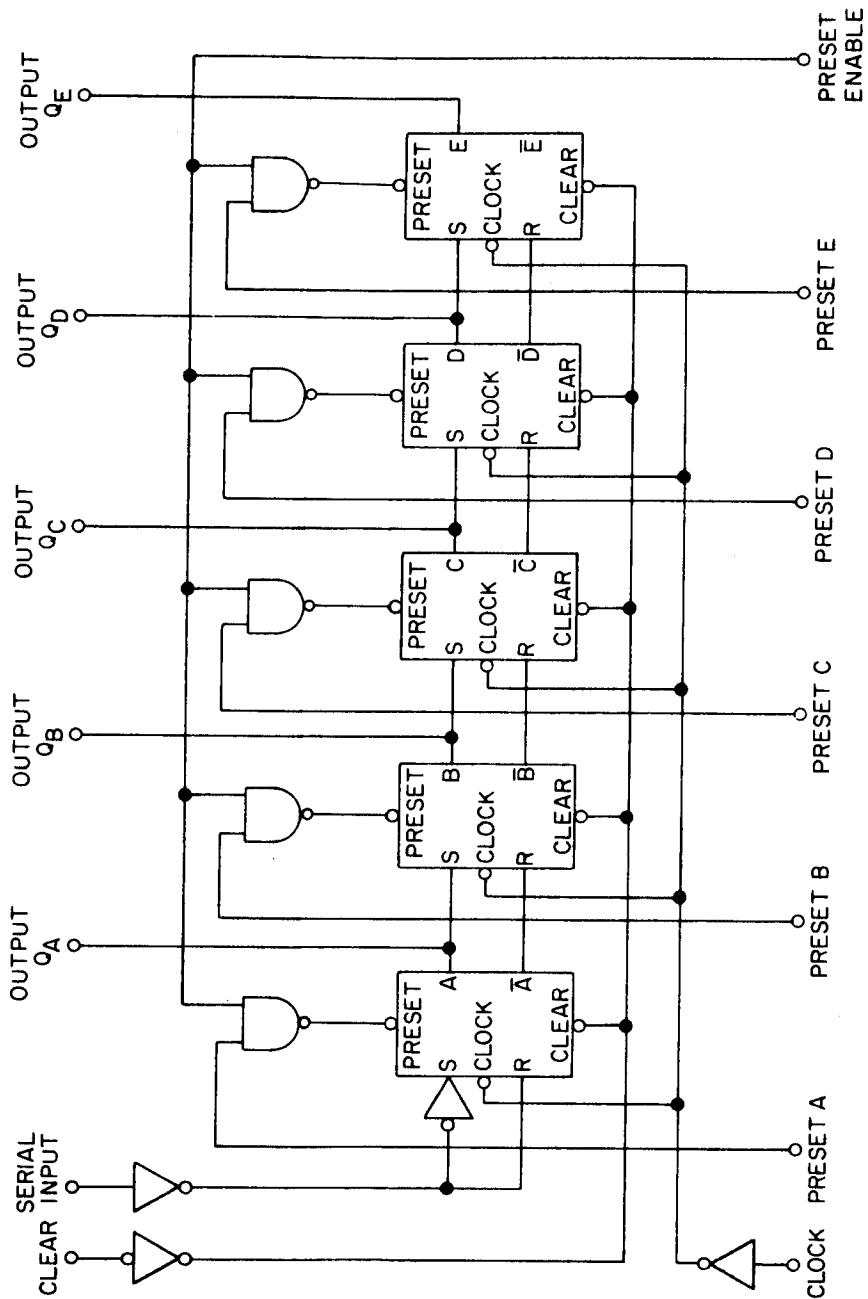
2. t_{n+1} = bit time after clock pulse

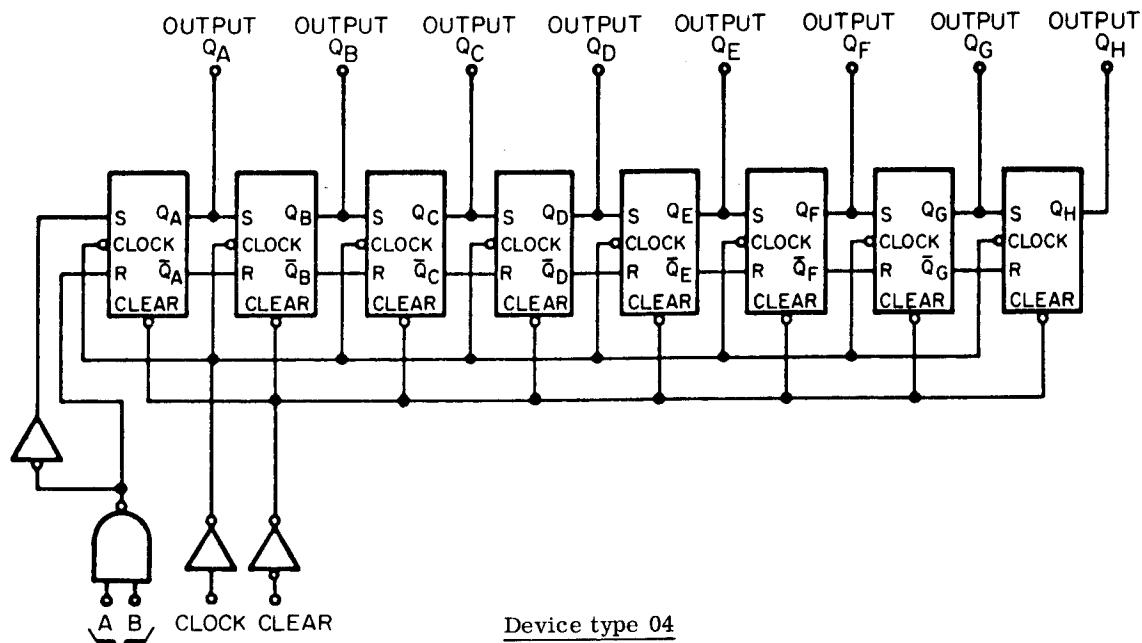
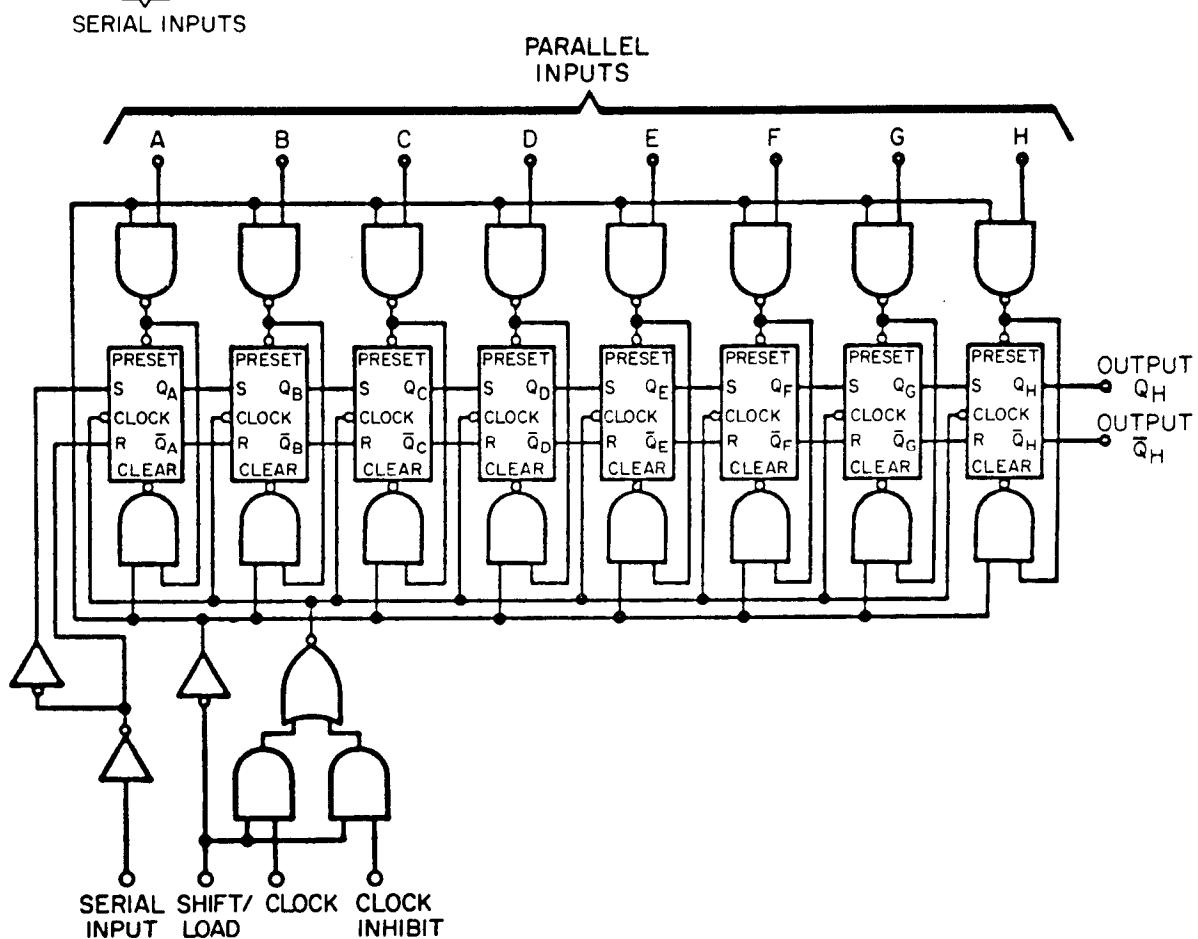
3. Q_{An} = state of Q_{An} at t_n .

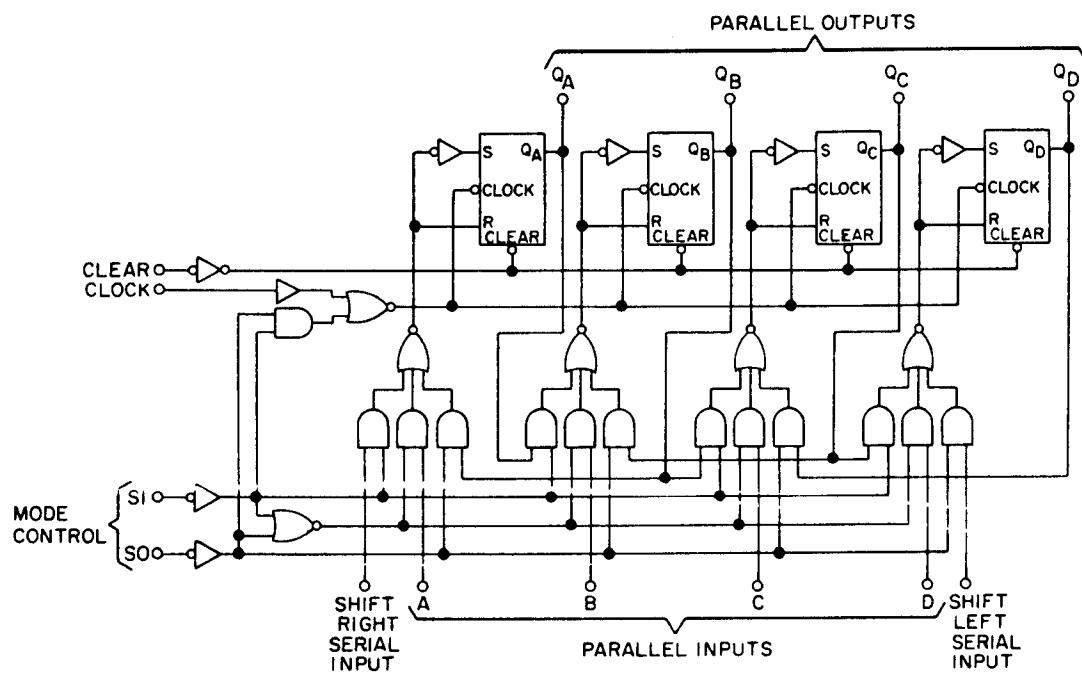
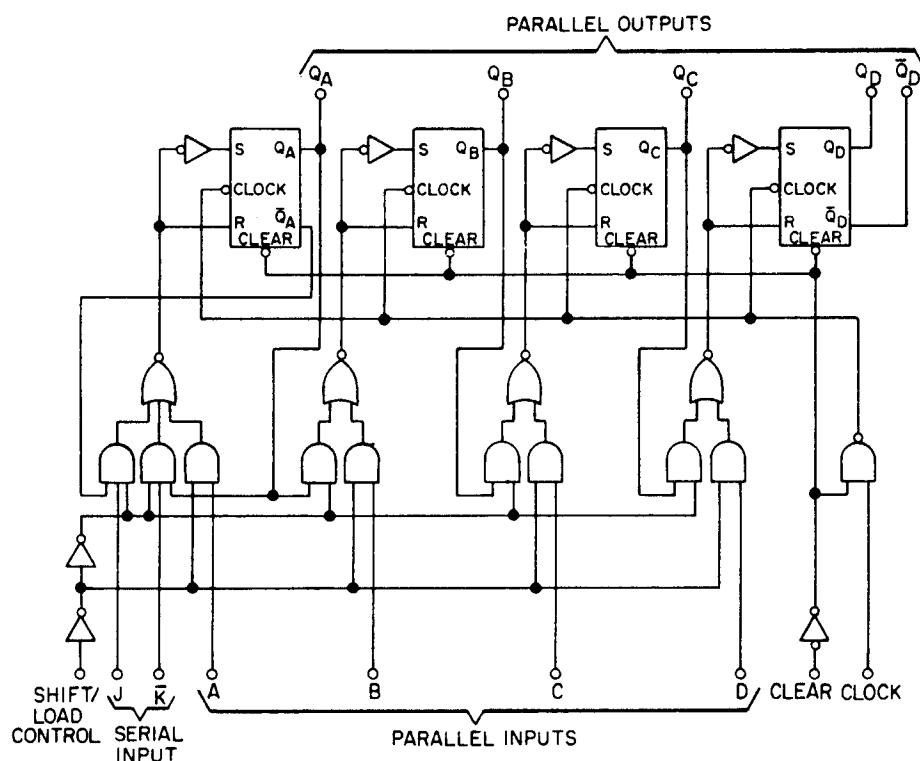
typical clear, shift, and load sequences

FIGURE 2. Truth tables and timing diagrams - continued.

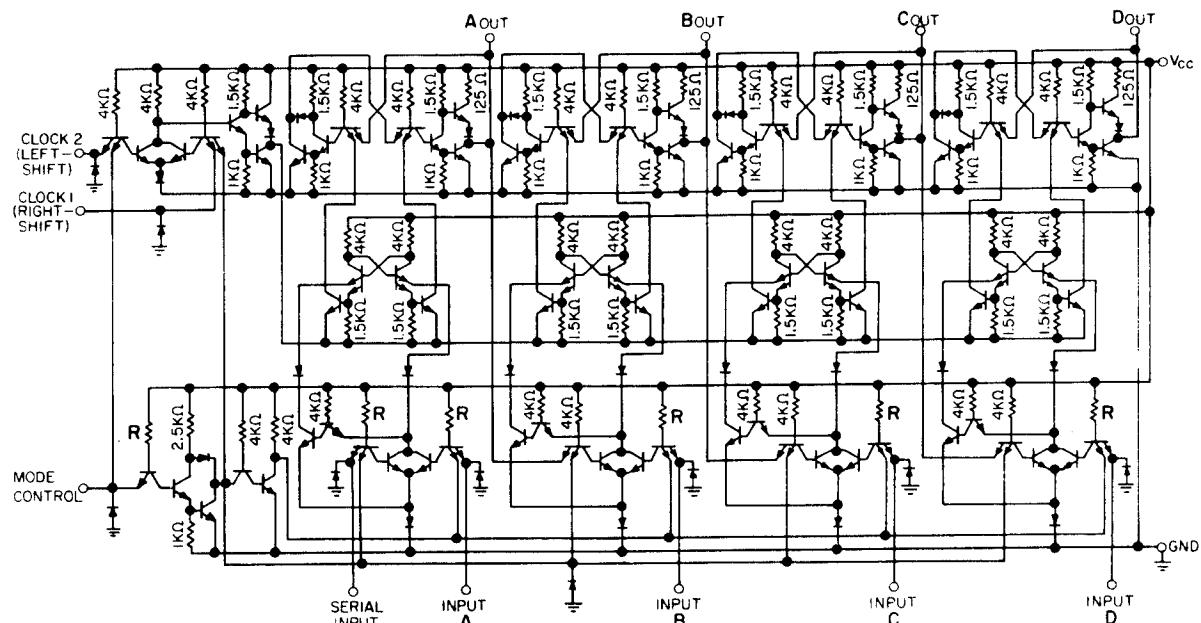
Device type 01FIGURE 3. Logic diagrams.

Device type 02FIGURE 3. Logic diagram - Continued.

Device type 03Device type 04FIGURE 3. Logic diagrams - continued.

Device type 05Device type 06FIGURE 3. Logic diagrams - continued.

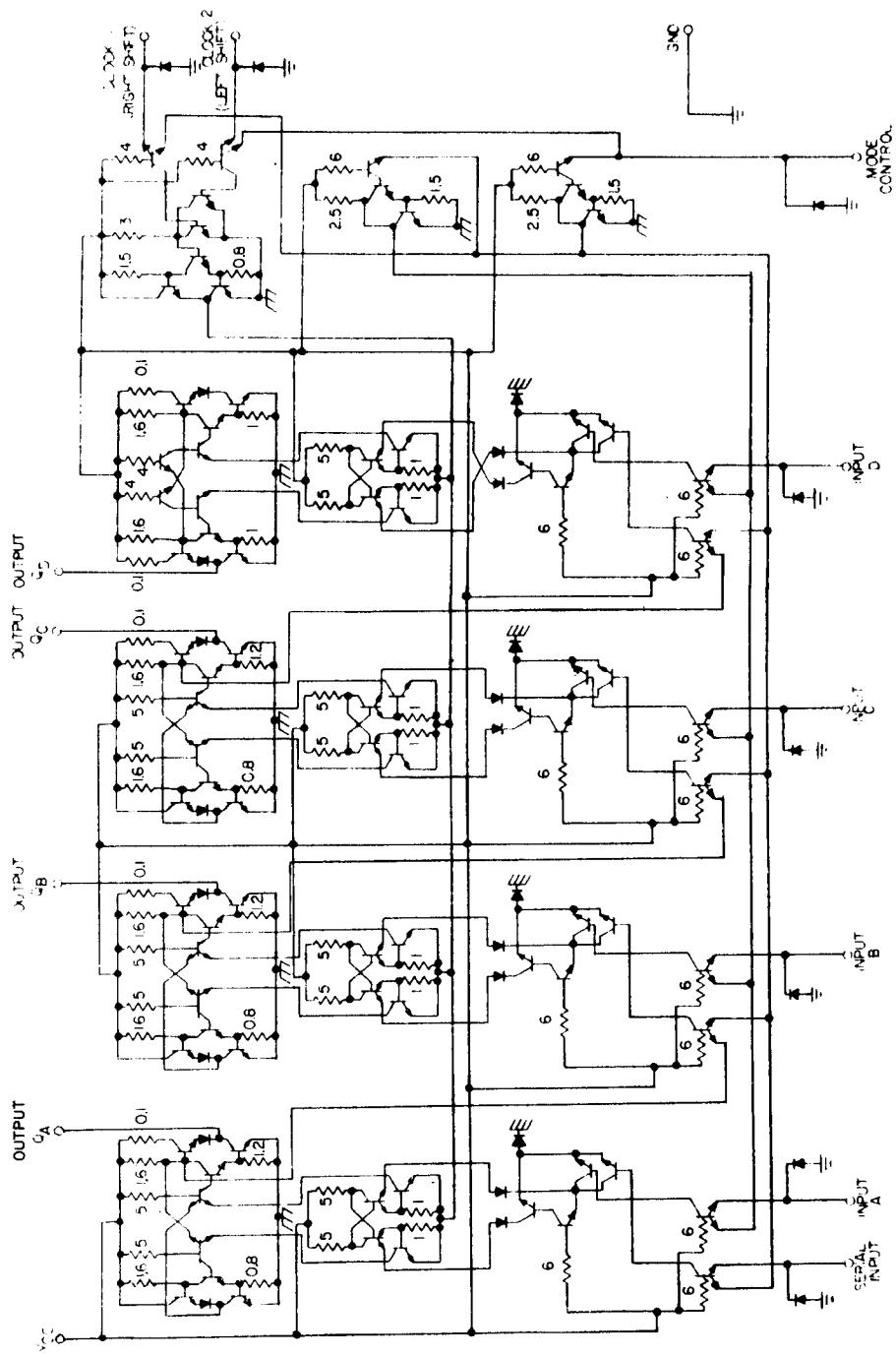
Device type 01, circuit A



NOTES:

1. COMPONENT VALUES SHOWN ARE NOMINAL
2. R VALUES ARE EITHER 4K OR 6K.

FIGURE 4. Schematic circuits.

Device type 01, circuit BFIGURE 4. Schematic circuits - Continued.

NOTES:
 1. Resistor values are in kilohms.
 2. Component values shown are nominal.

Device type 02, circuit A

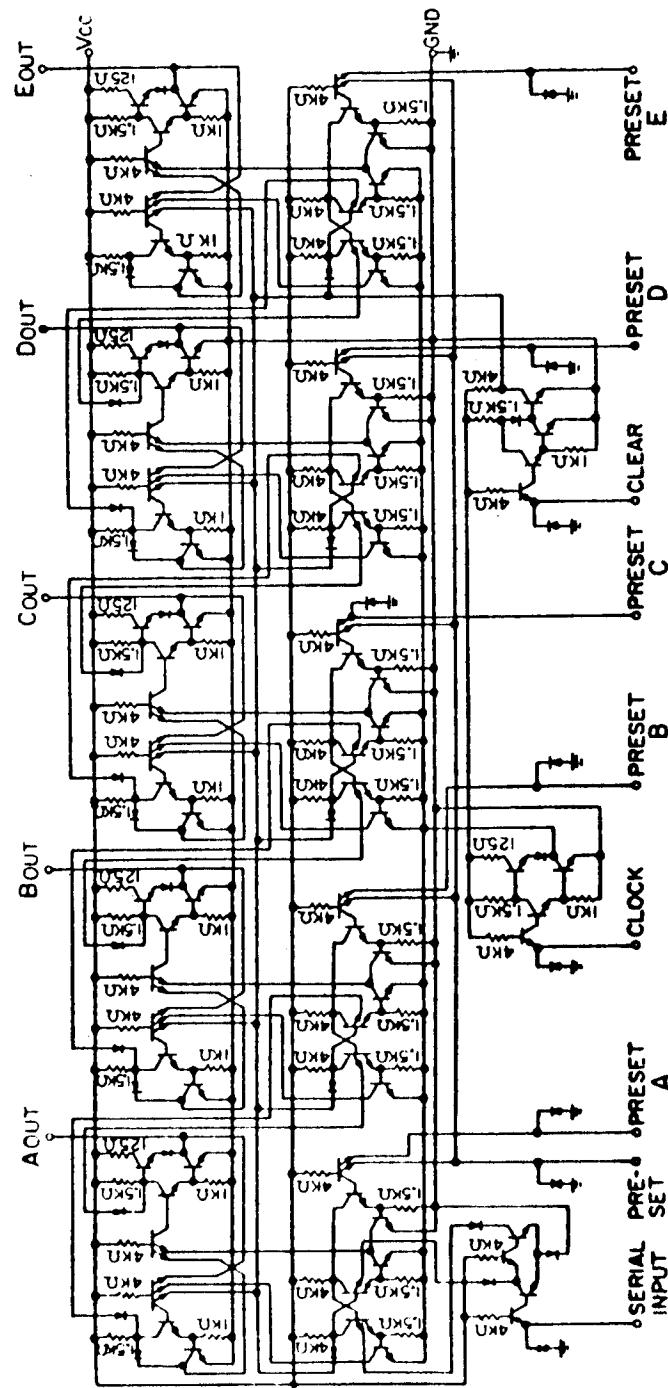


FIGURE 4. Schematic circuits - Continued.

COMPONENT VALUES SHOWN ARE NOMINAL

Device type 02, circuit B

- NOTES:
1. Component values shown are nominal.
 2. Resistor values are in kilohms.

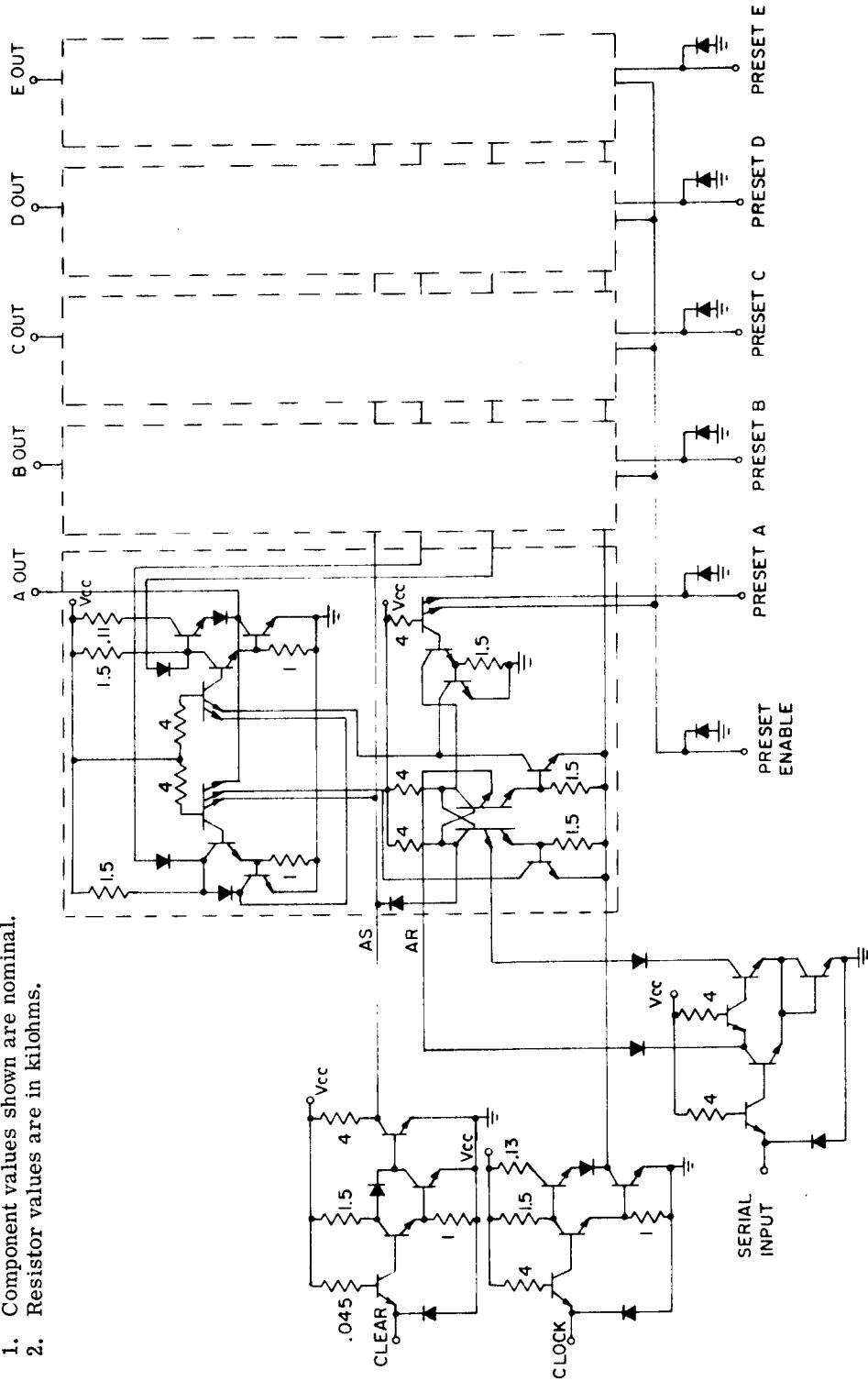


FIGURE 4. Schematic circuits - Continued.

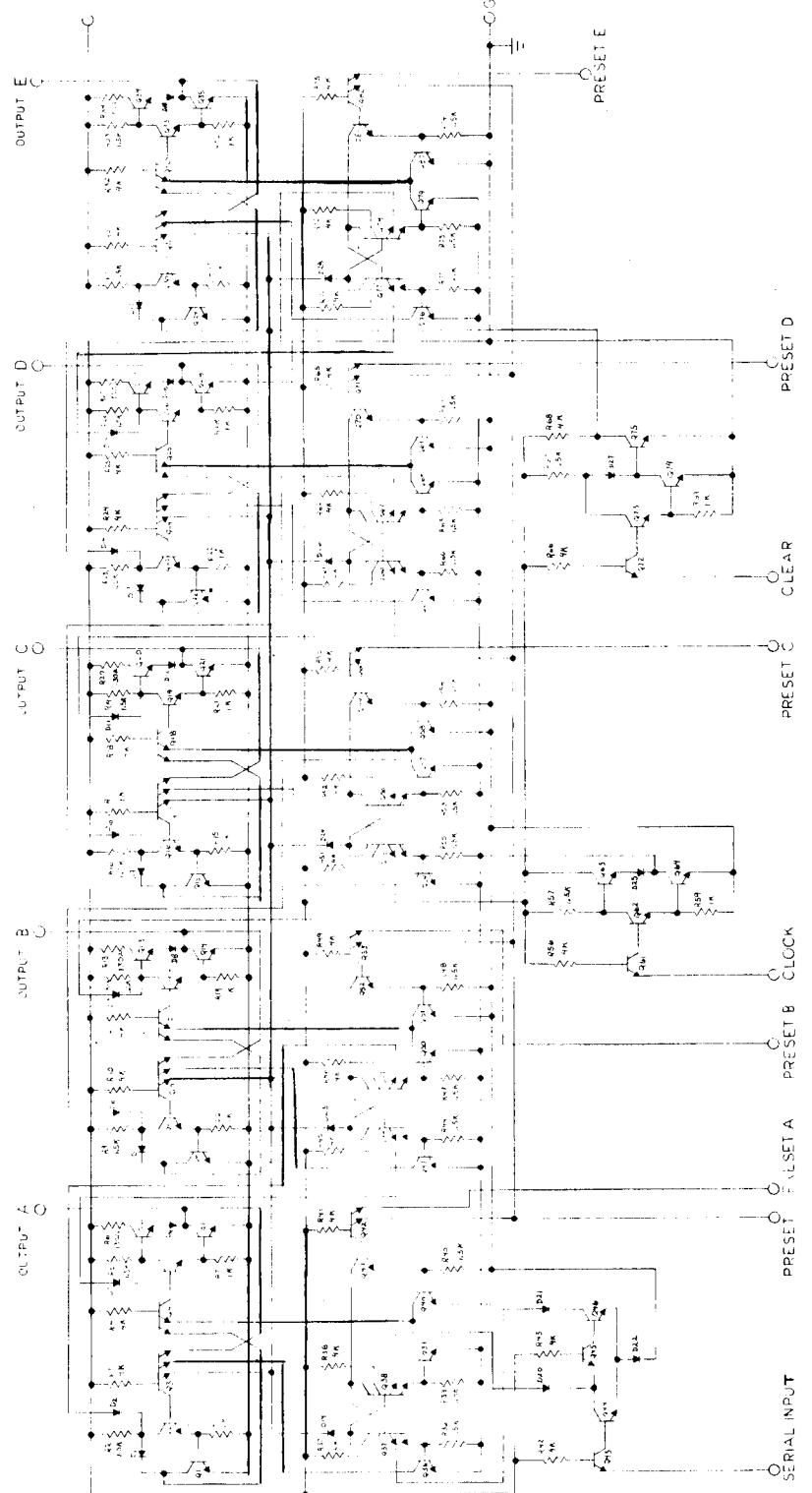


FIGURE 4. Schematic circuits - Continued.

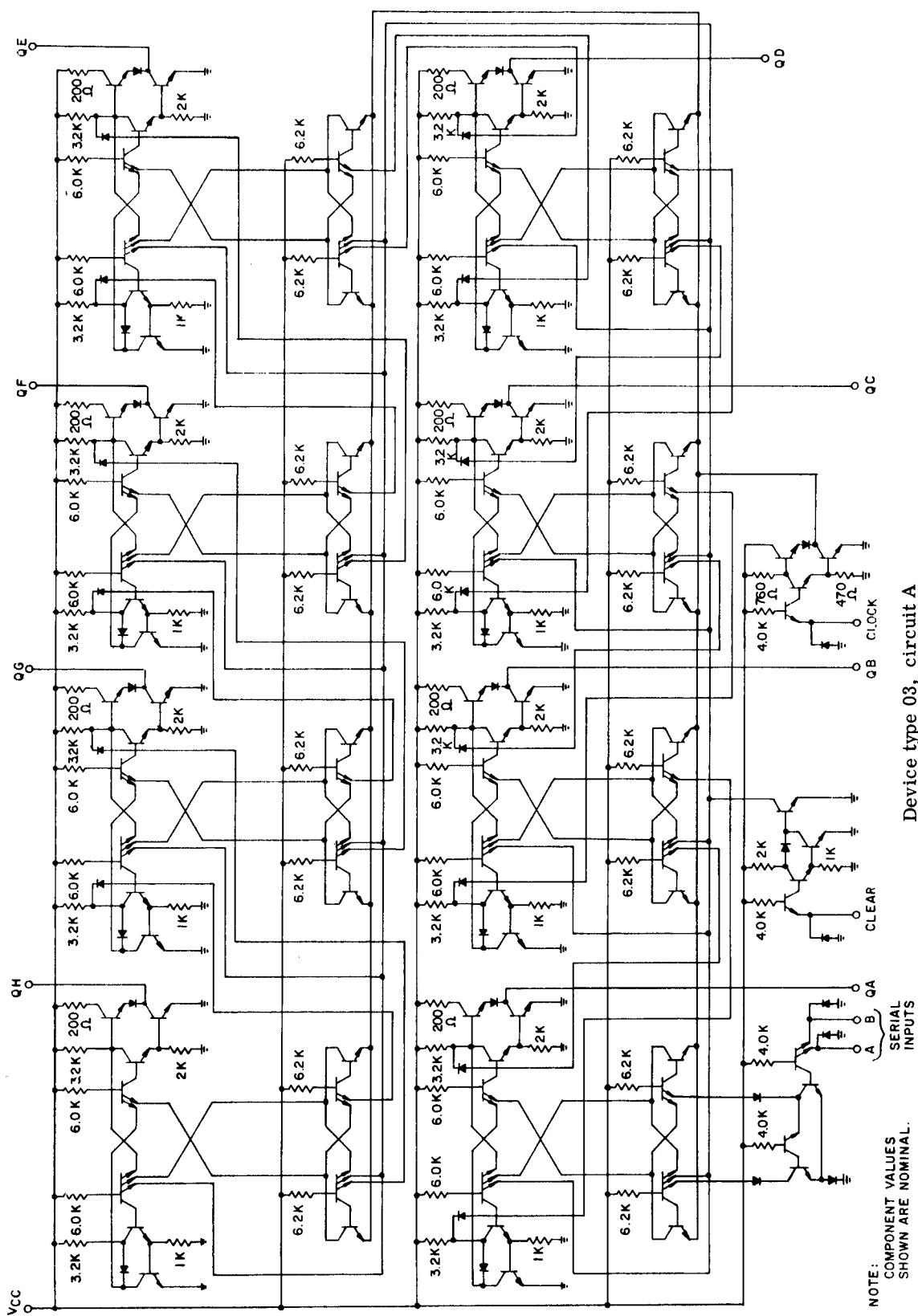


FIGURE 4. Schematic circuits - Continued.

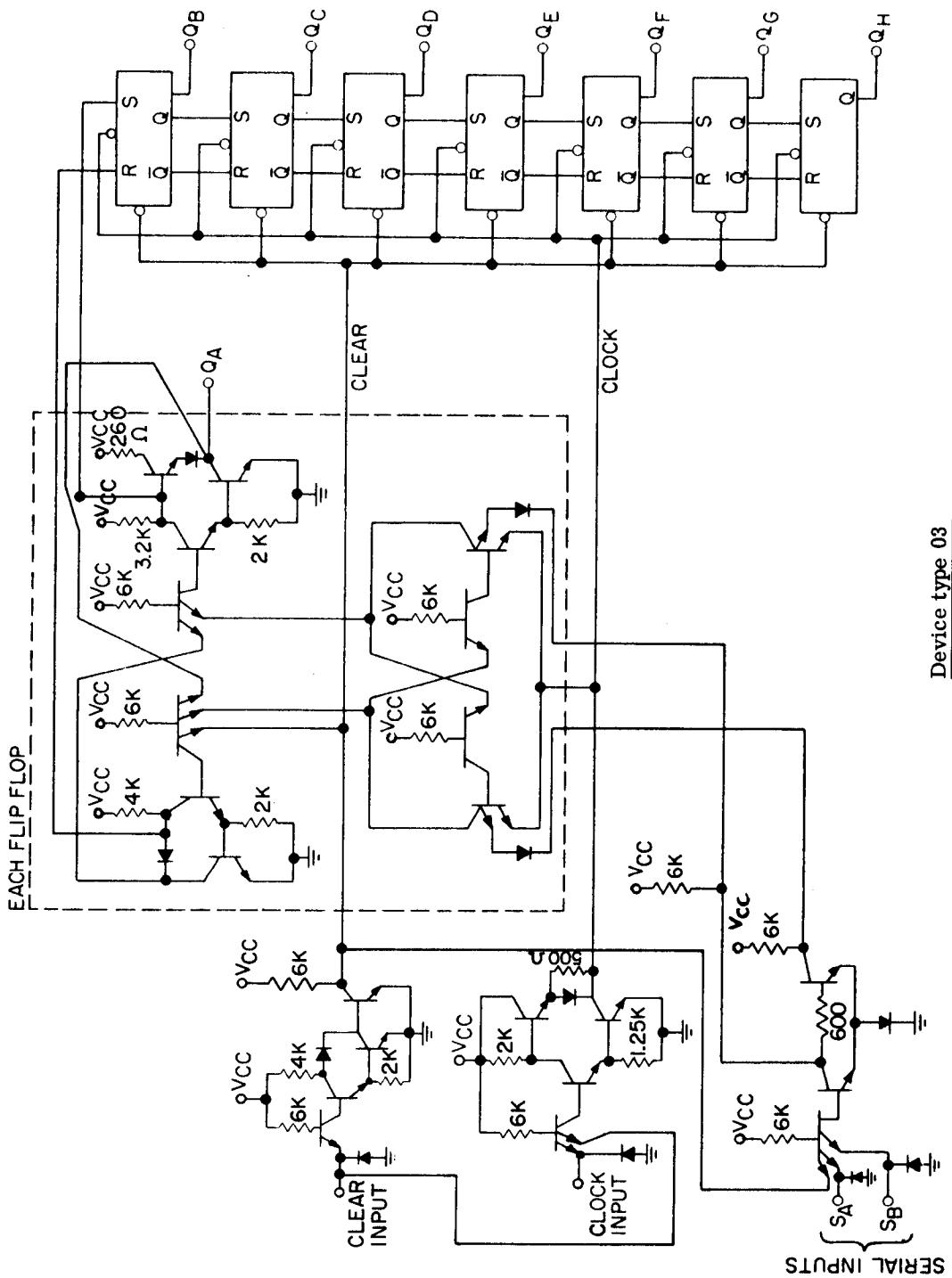
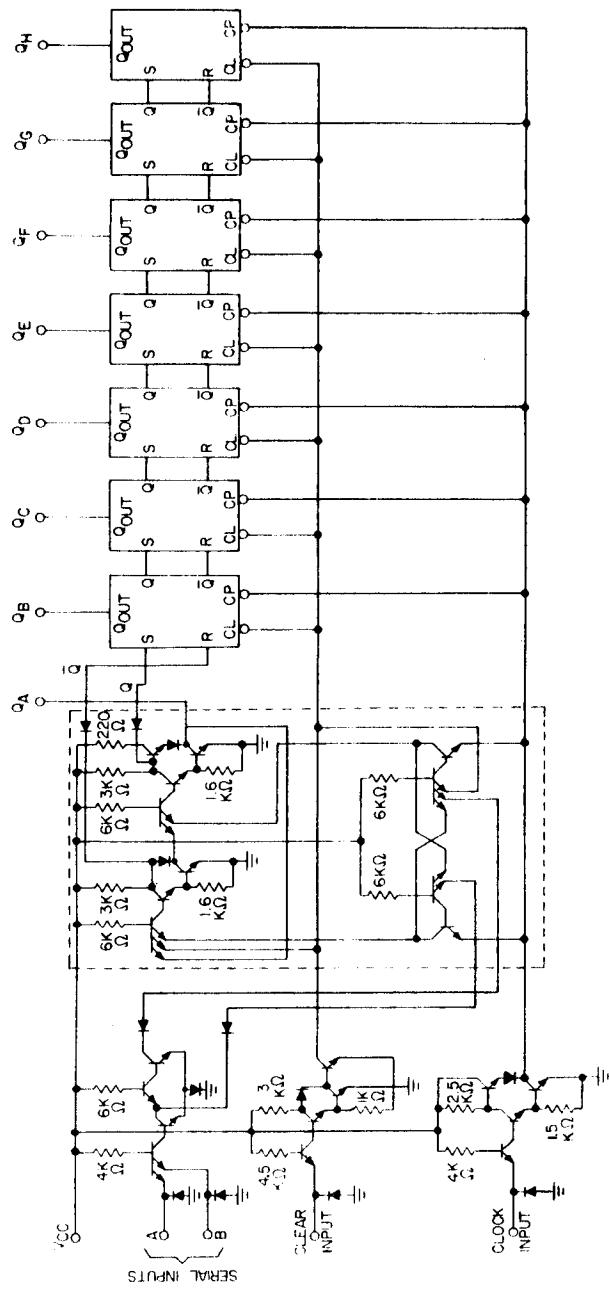


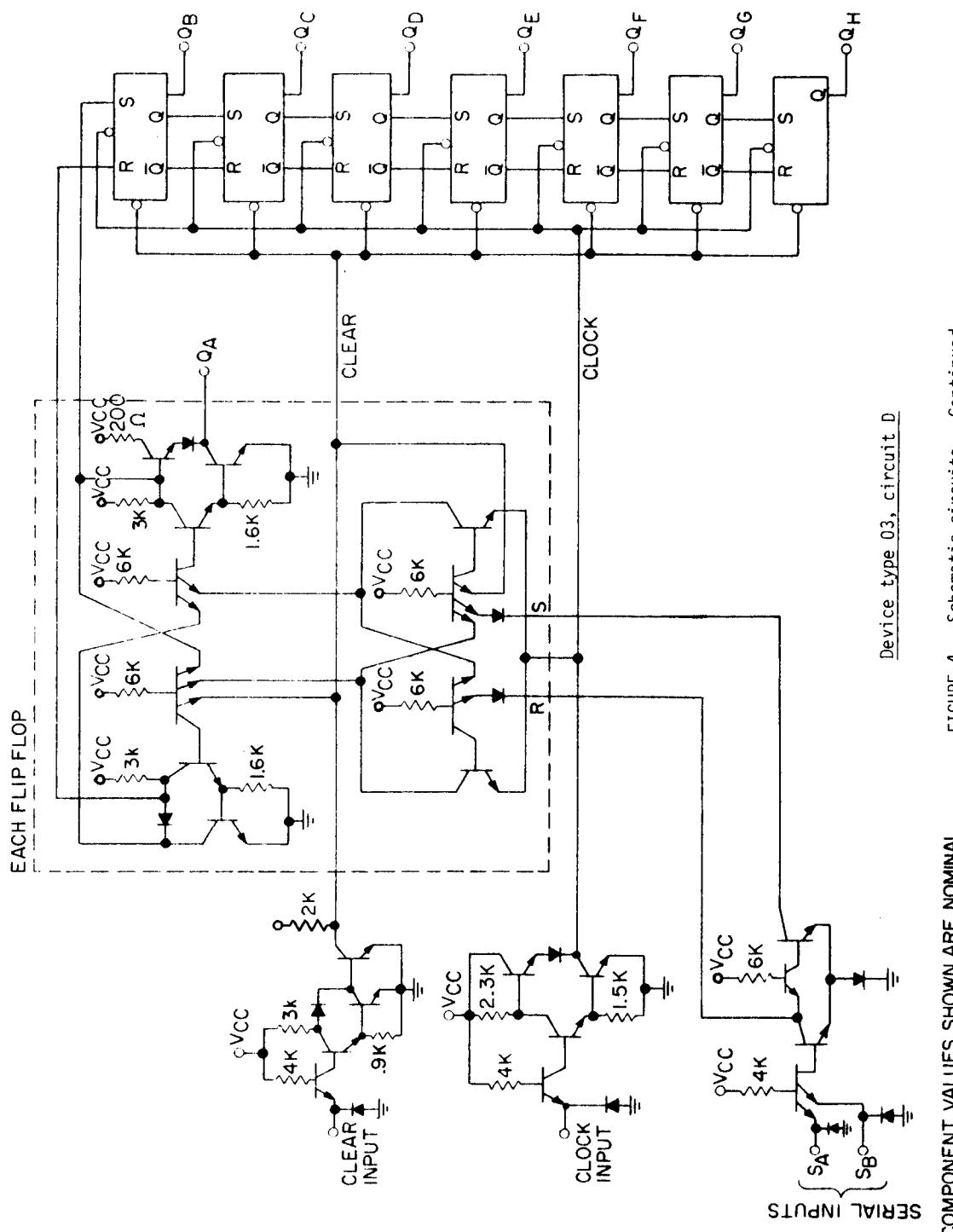
FIGURE 4. Schematic circuits - Continued.
Device type 03
Circuit B

COMPONENT VALUES SHOWN ARE NOMINAL

Device type 03, circuit C

Component values shown are nominal.

FIGURE 4. Schematic circuits - Continued.



COMPONENT VALUES SHOWN ARE NOMINAL

FIGURE 4. Schematic circuits - Continued.

Device type 03, circuit D

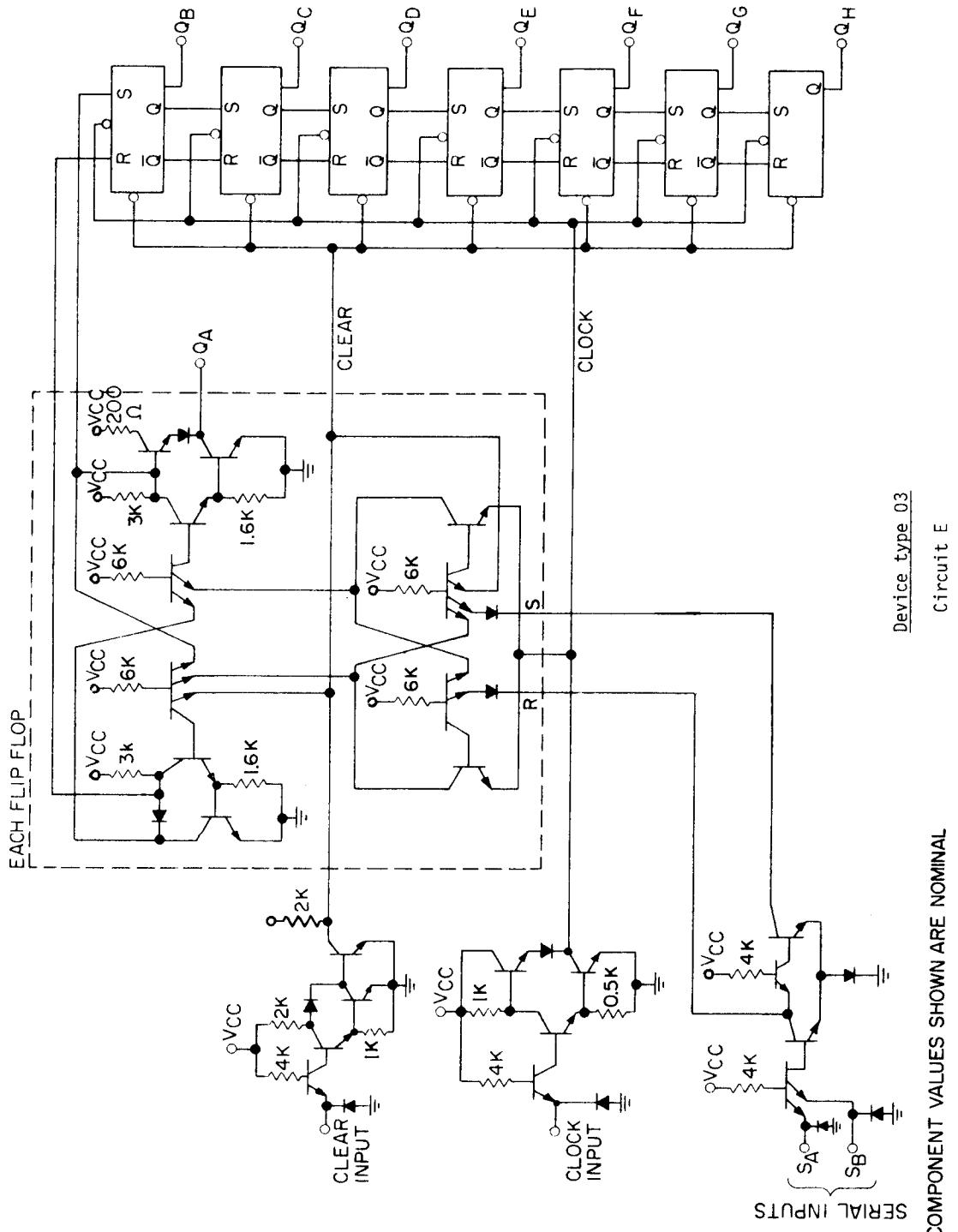
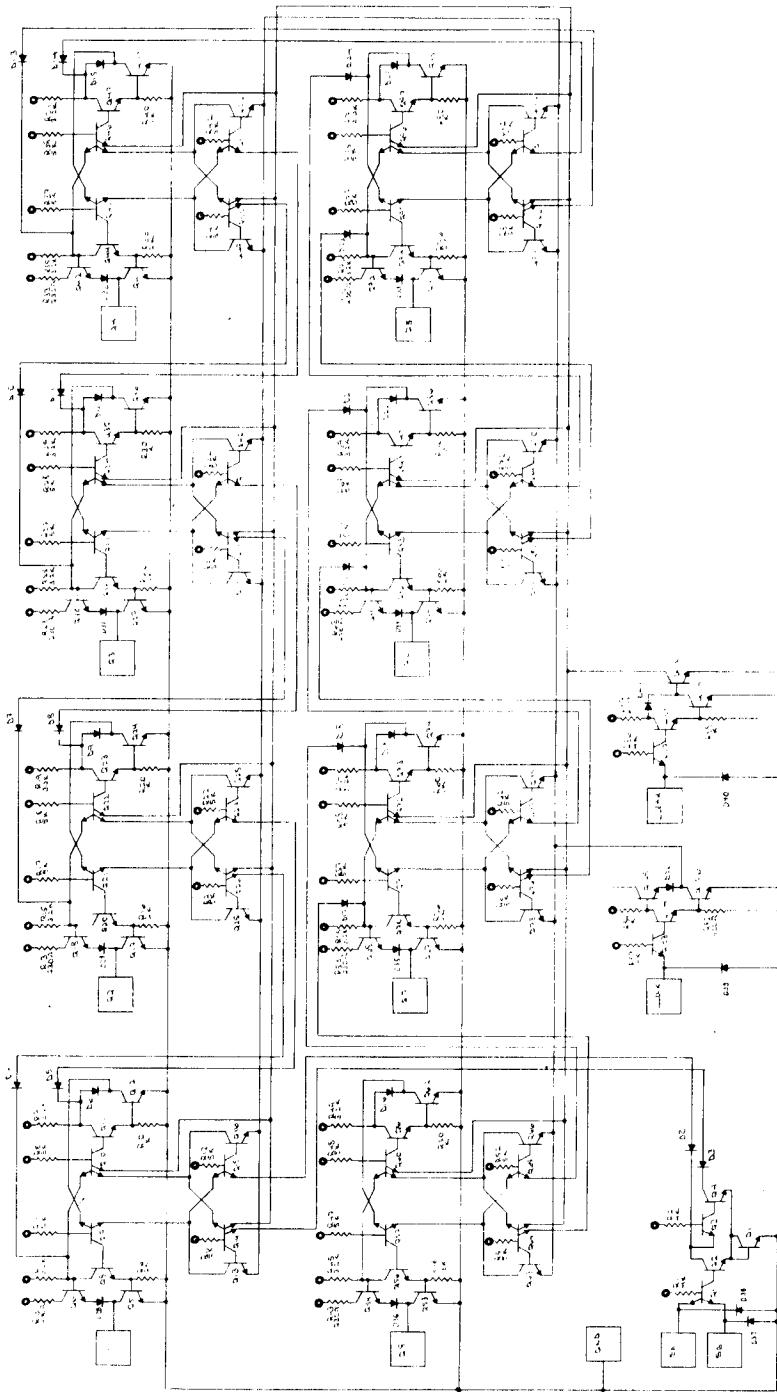


FIGURE 4. Schematic circuits - Continued.



Device type 03

Circuit F

- NOTES:**
1. Component values shown are nominal.
 2. $V_{CC} = 1$

FIGURE 4. Schematic circuits - Continued.

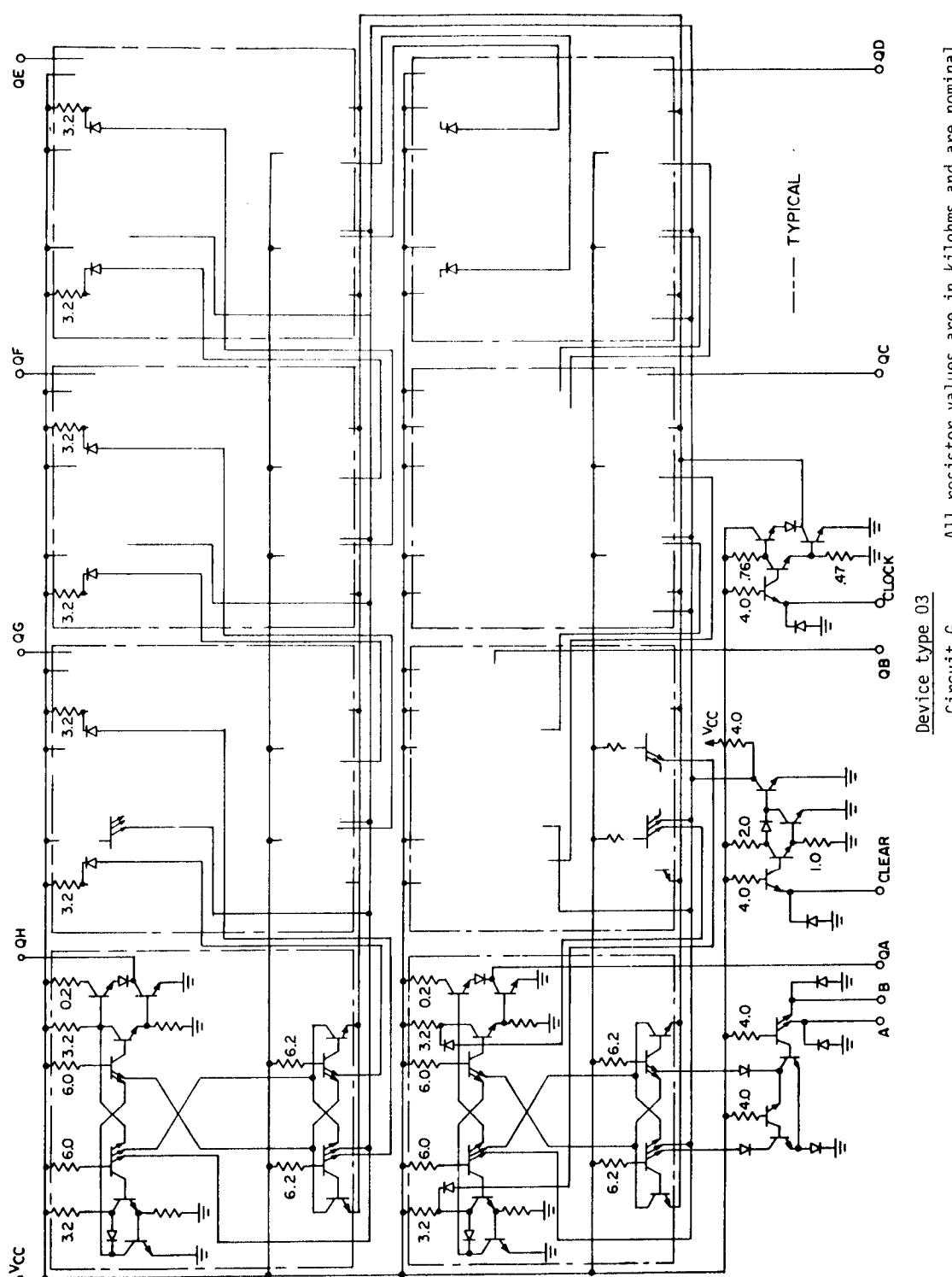
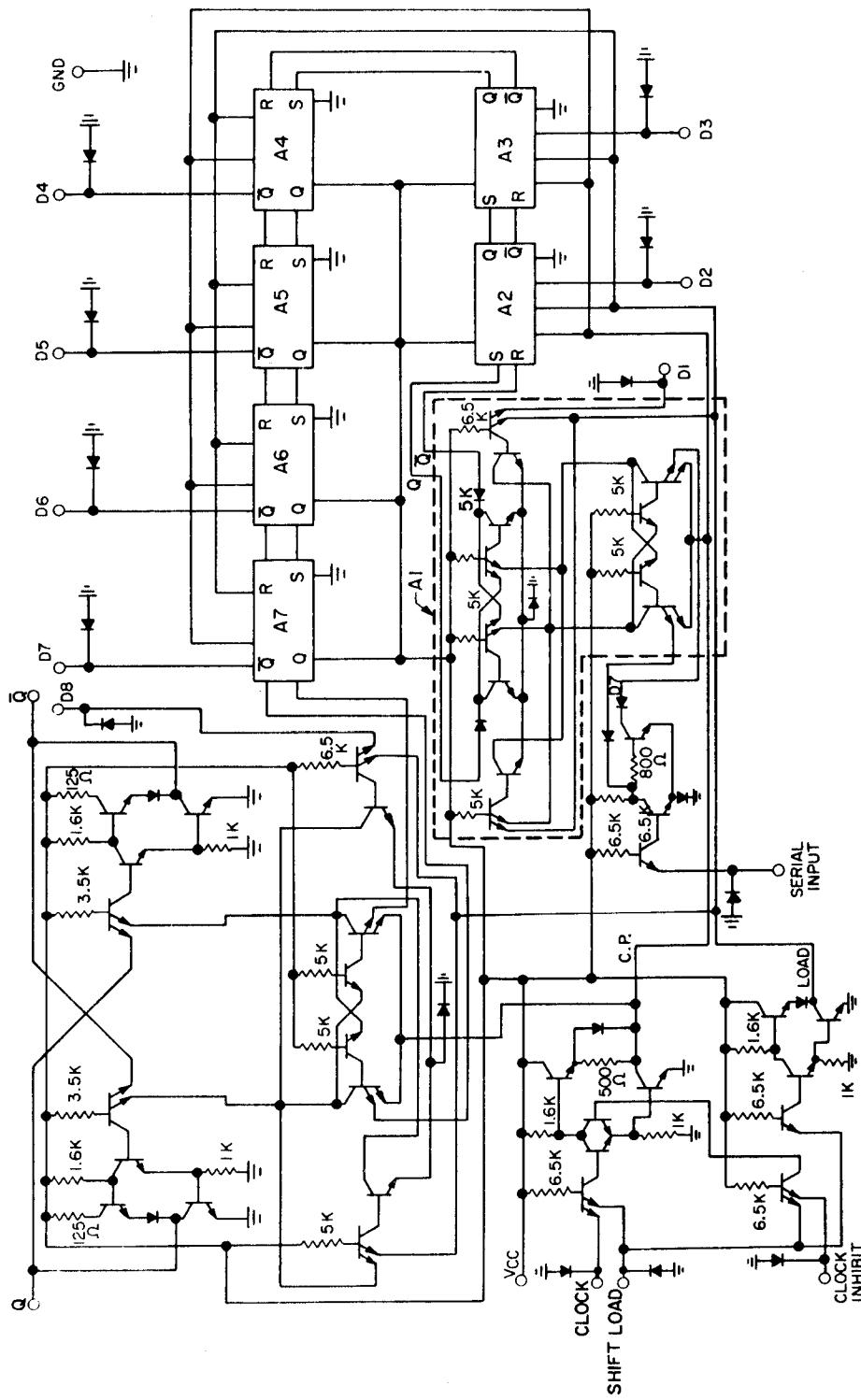


FIGURE 4. Schematic circuits - Continued.



Device type 04, circuit A

FIGURE 4. Schematic circuits - continued.

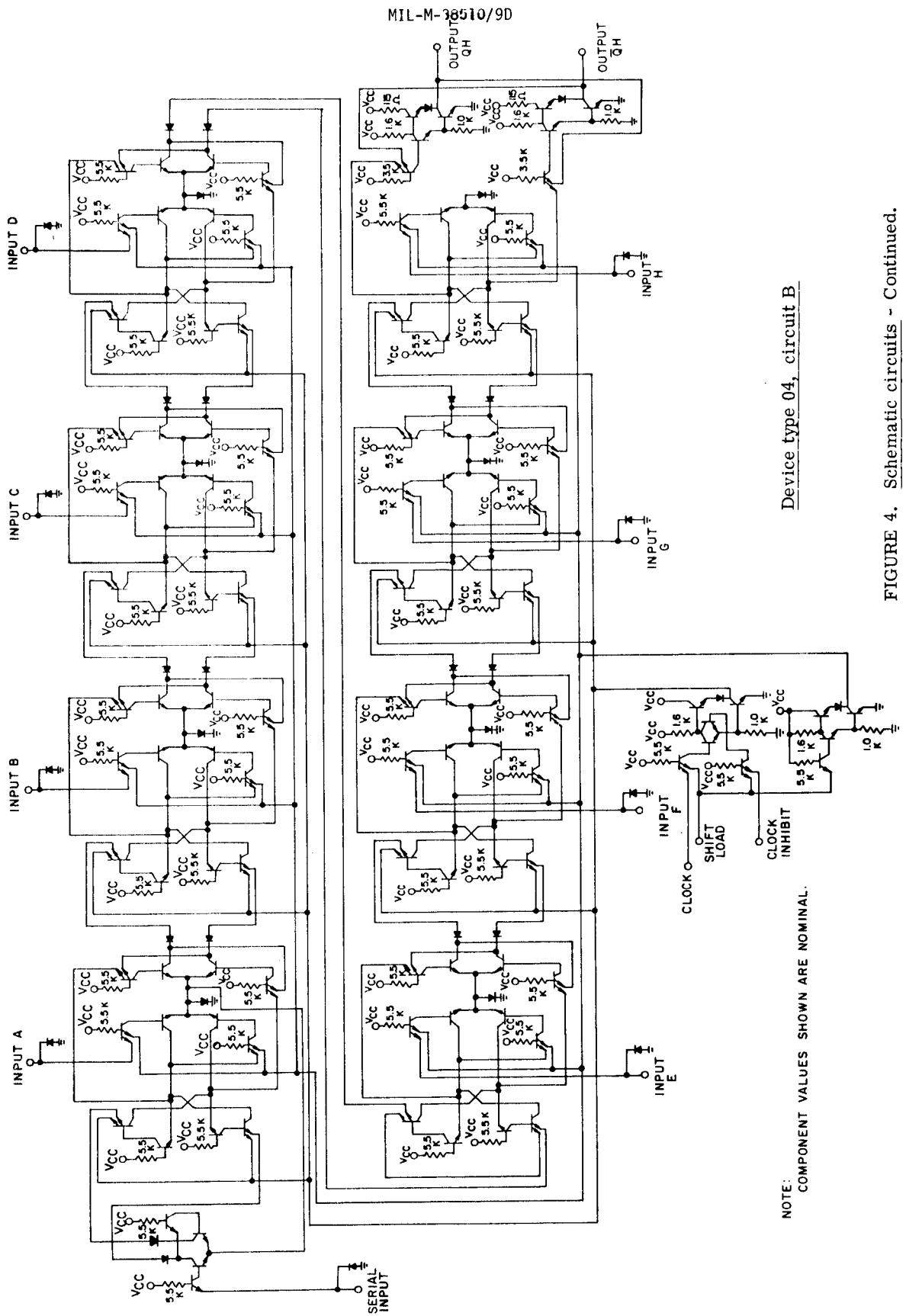
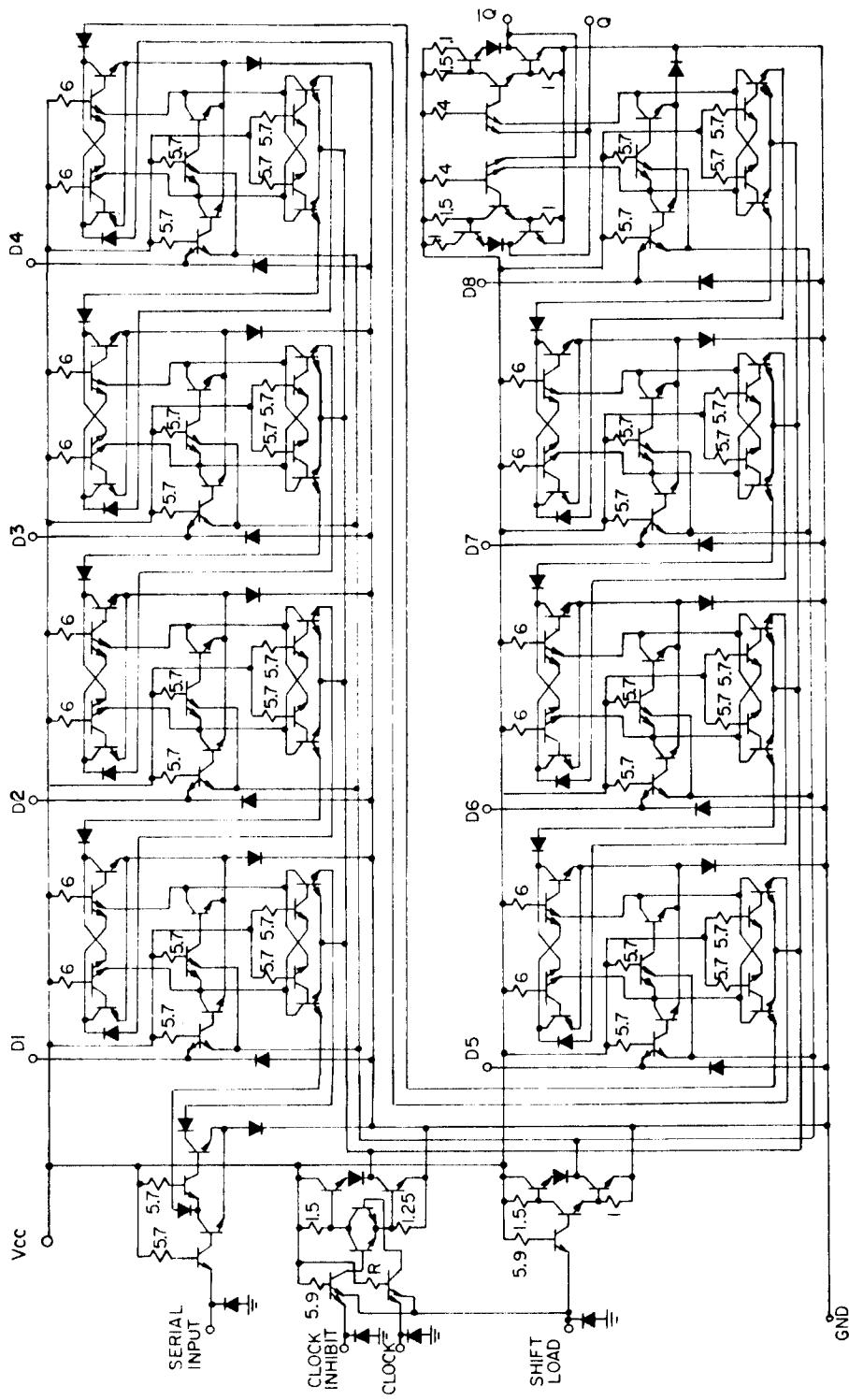


FIGURE 4. Schematic circuits - Continued.

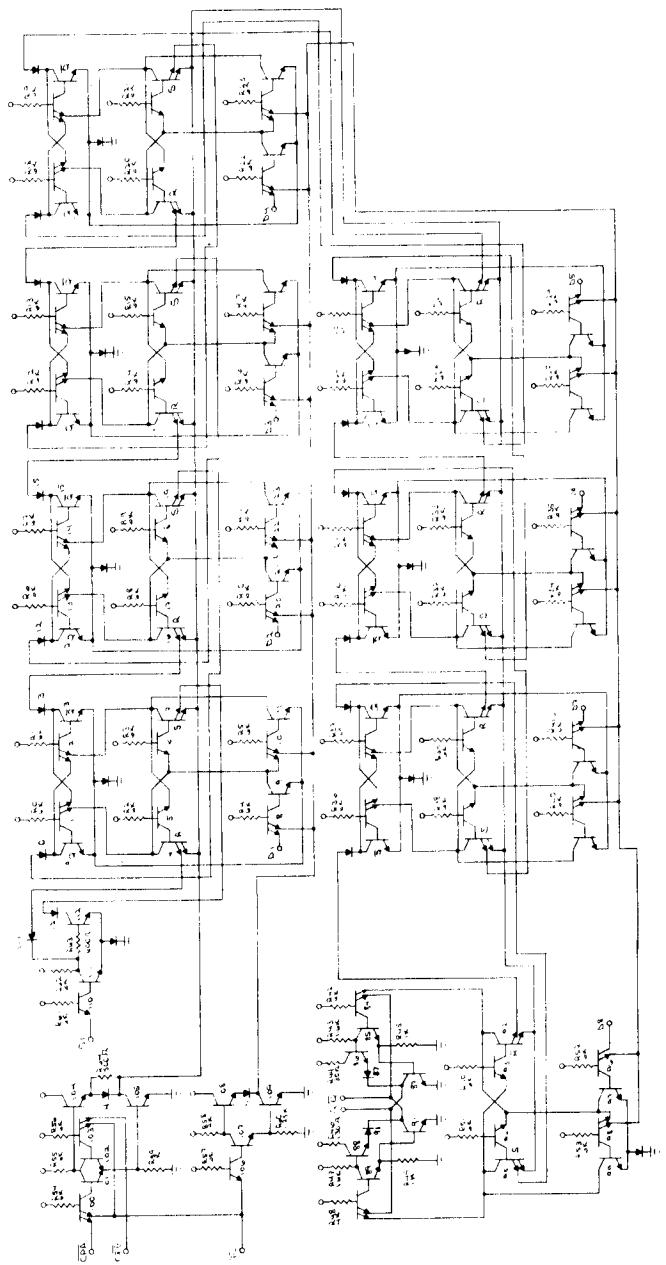


Device type 04, circuit C

NOTES:

1. Component values shown are nominal.
2. R value is either 4 k Ω or 6 k Ω .
3. Resistor values are in kilohms.

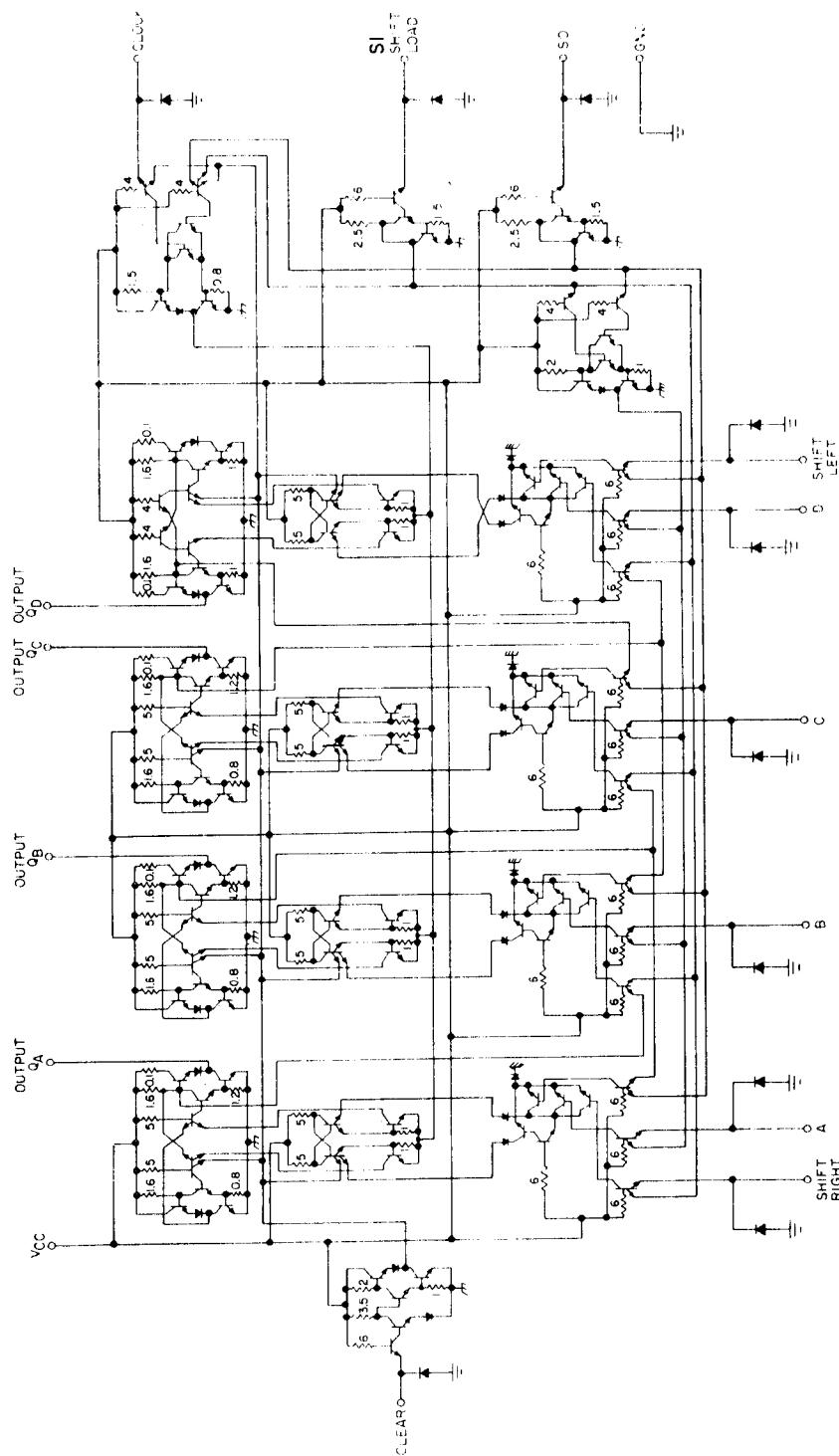
FIGURE 4. Schematic circuits - Continued.



Device type 04
Circuit D

NOTES:
 1. Component values shown are nominal.
 2. V_{CC} = 

FIGURE 4. Schematic circuits - Continued.

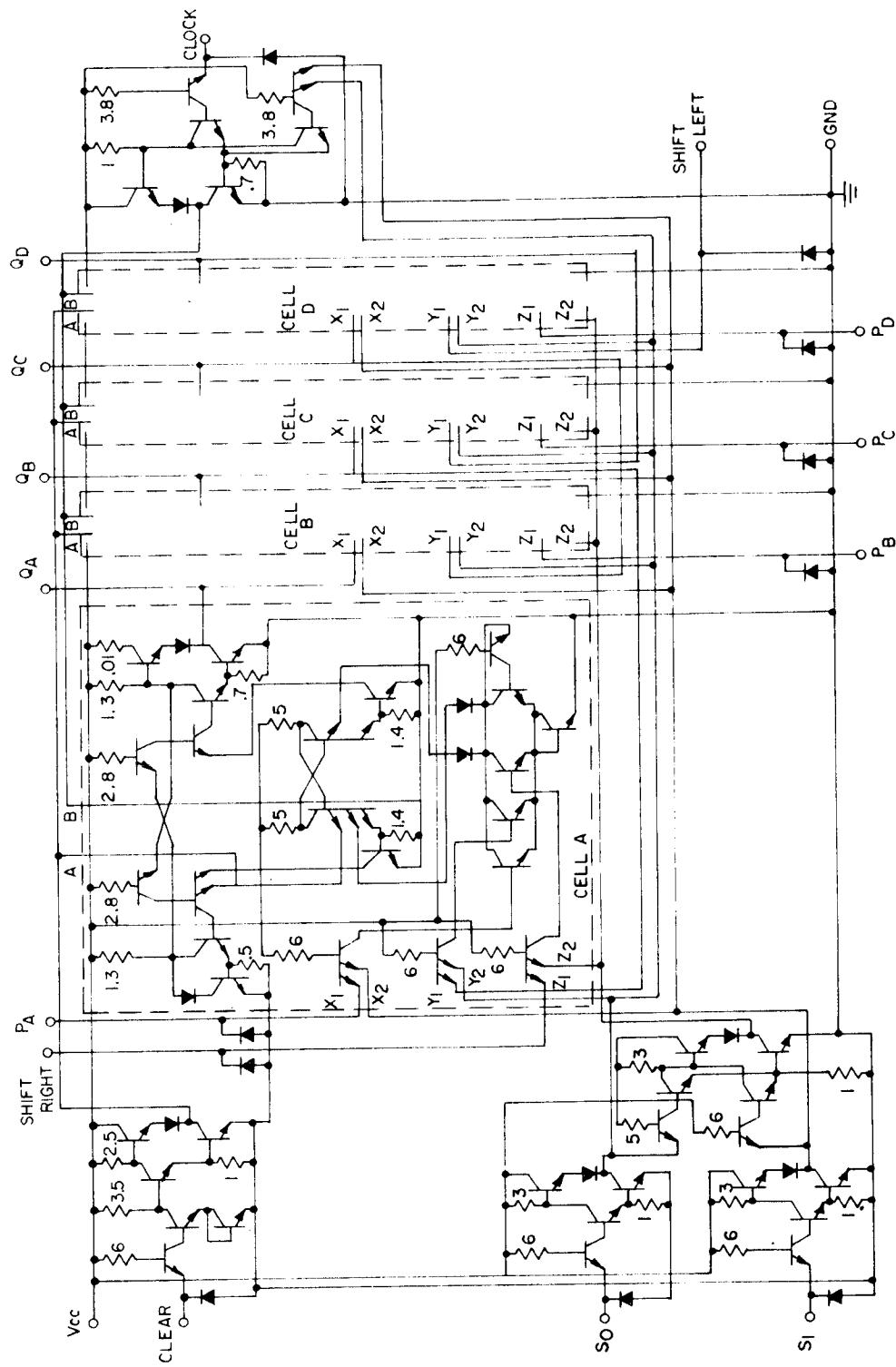


- NOTES:**
1. Resistor values are in kilohms.
 2. Component values shown are nominal.

Device type 05, circuit A

FIGURE 4. Schematic circuits - Continued.

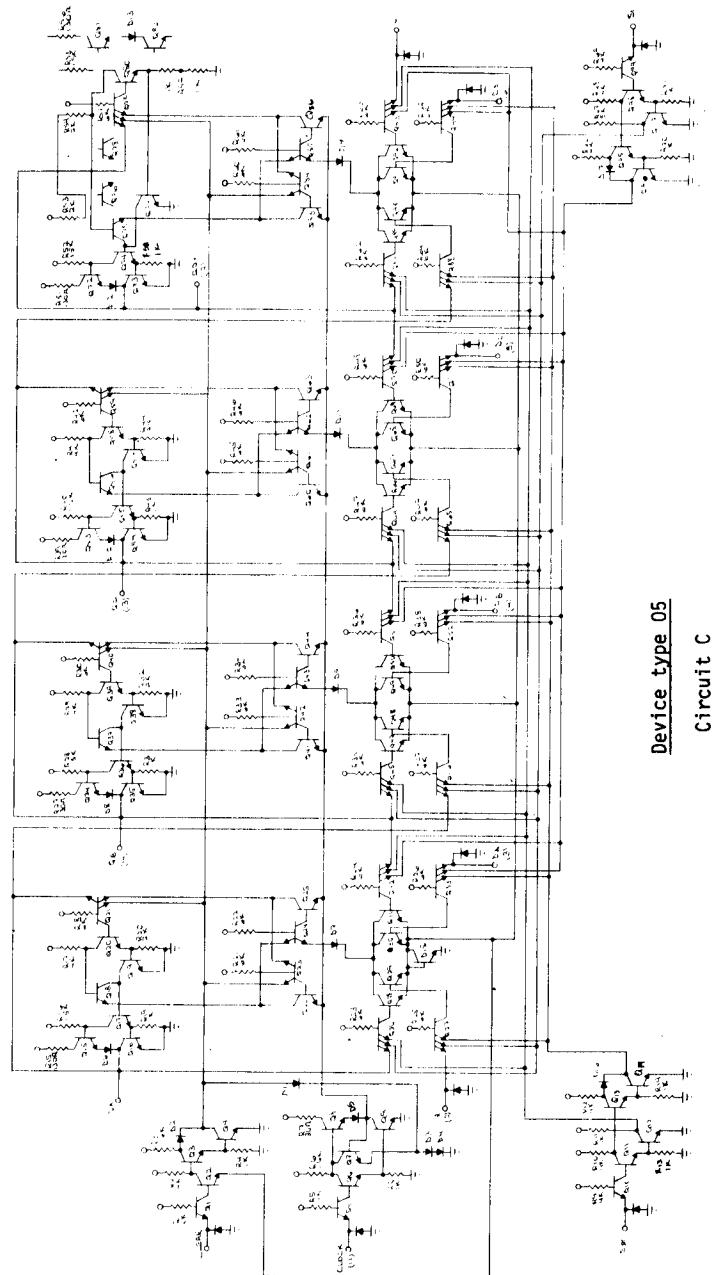
Device type 05, circuit B



NOTES

1. Component values shown are nominal.
2. Resistor values are in kilohms.

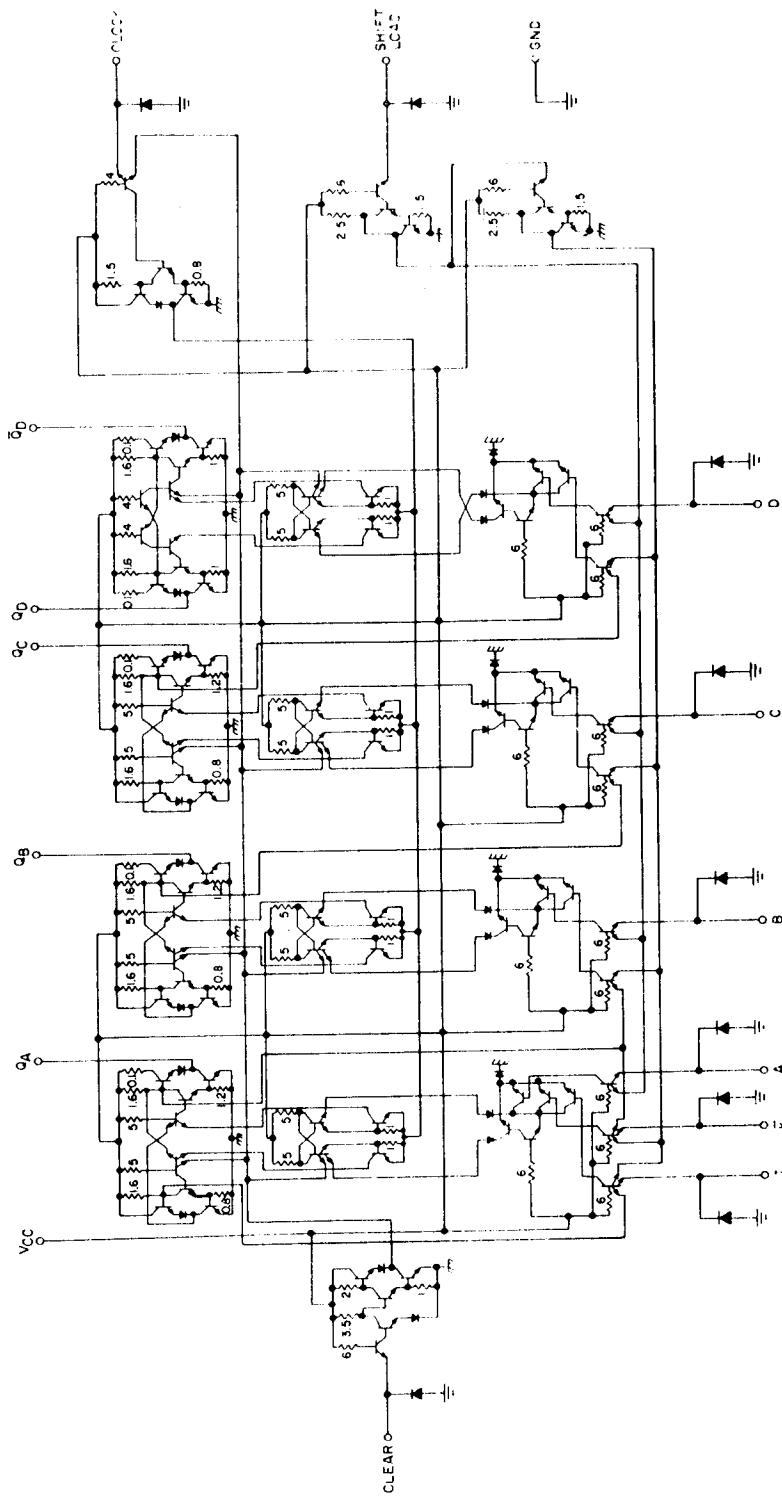
FIGURE 4. Schematic circuits - Continued.



NOTES:

1. Component values shown are nominal.
2. $V_{CC} = 9$

FIGURE 4. Schematic circuits - Continued.

Device type 06, circuit A

NOTES:

1. Component values shown are nominal.
2. Resistor values are in kilohms.

FIGURE 4. Schematic circuits - Continued.

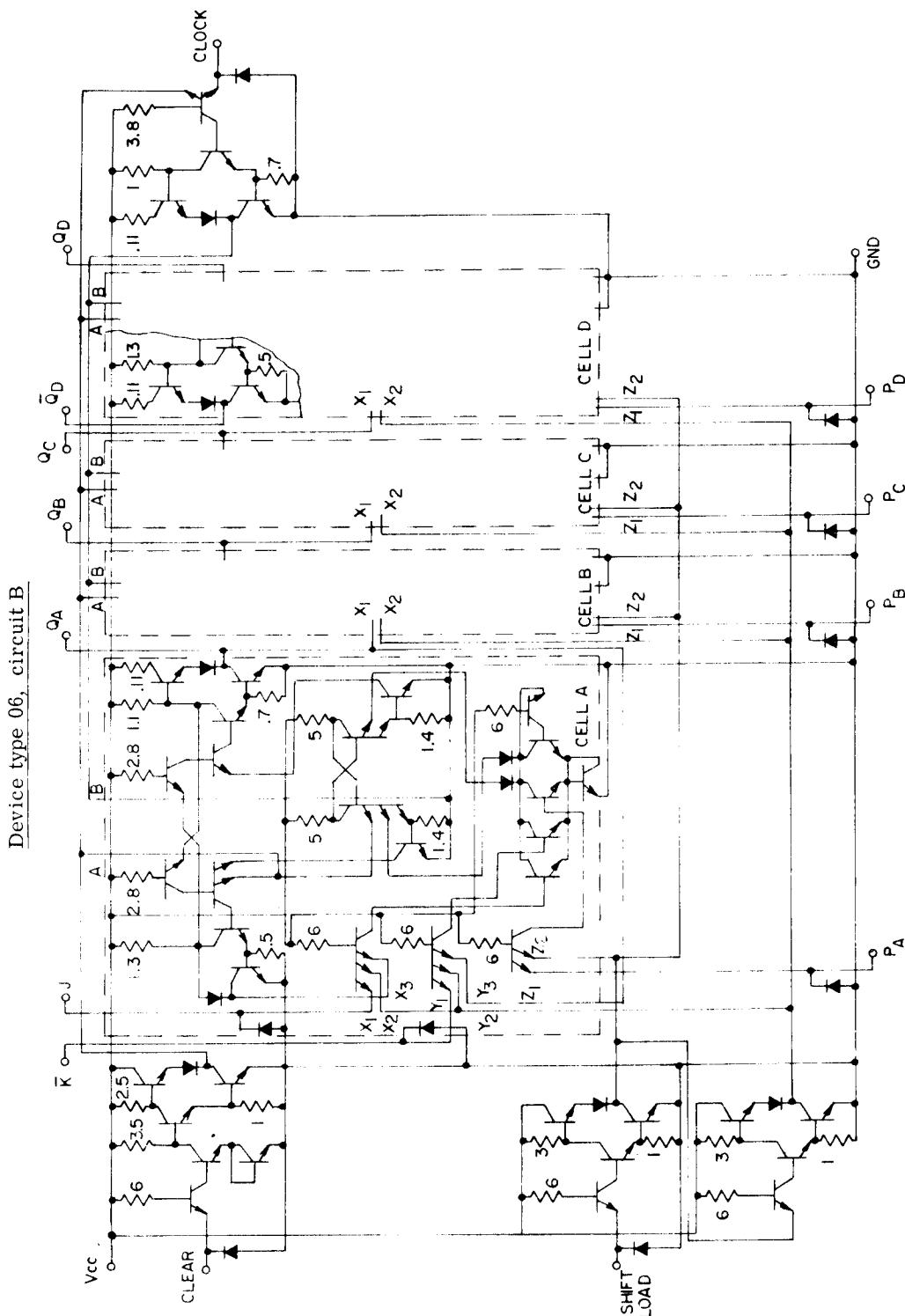
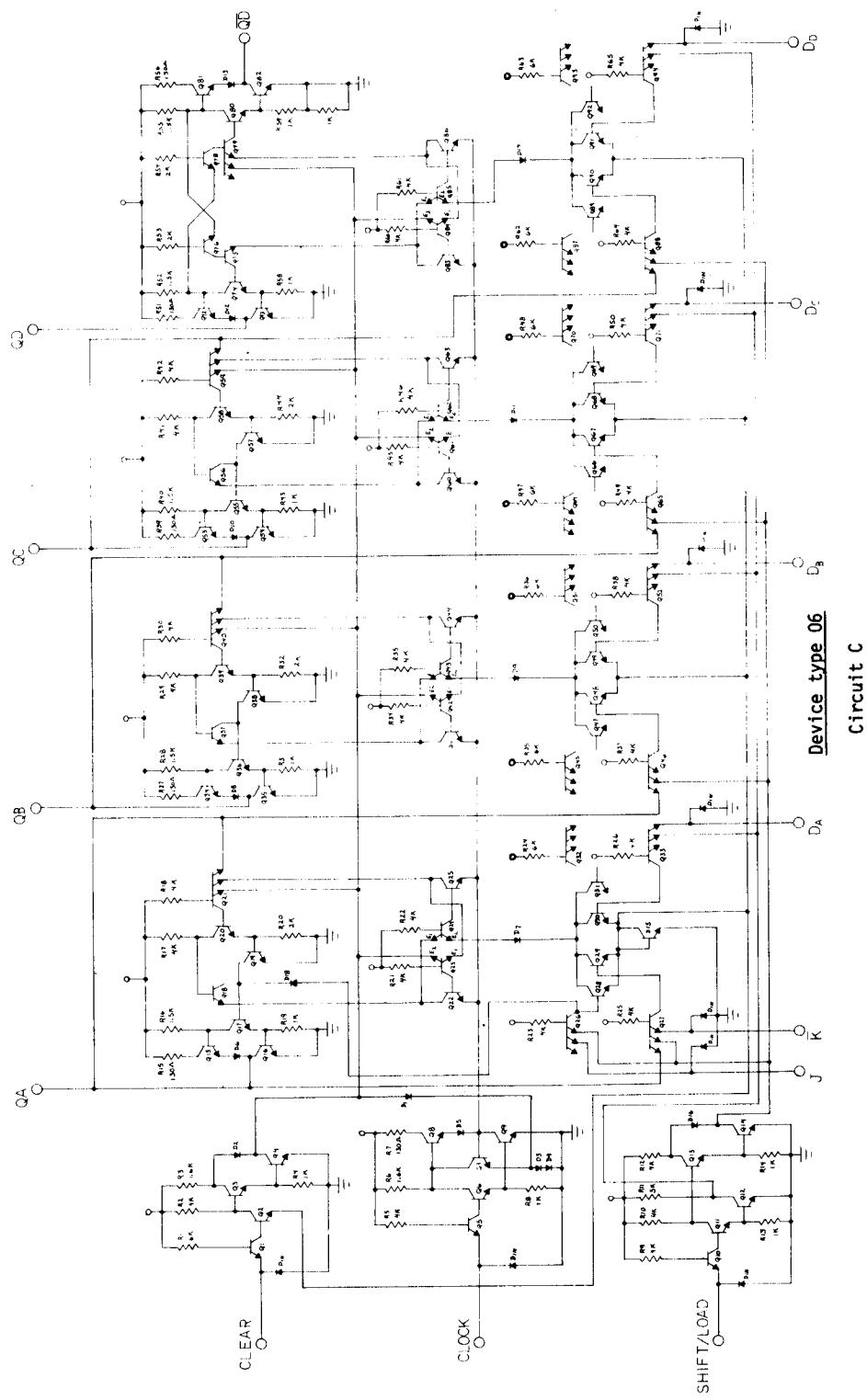
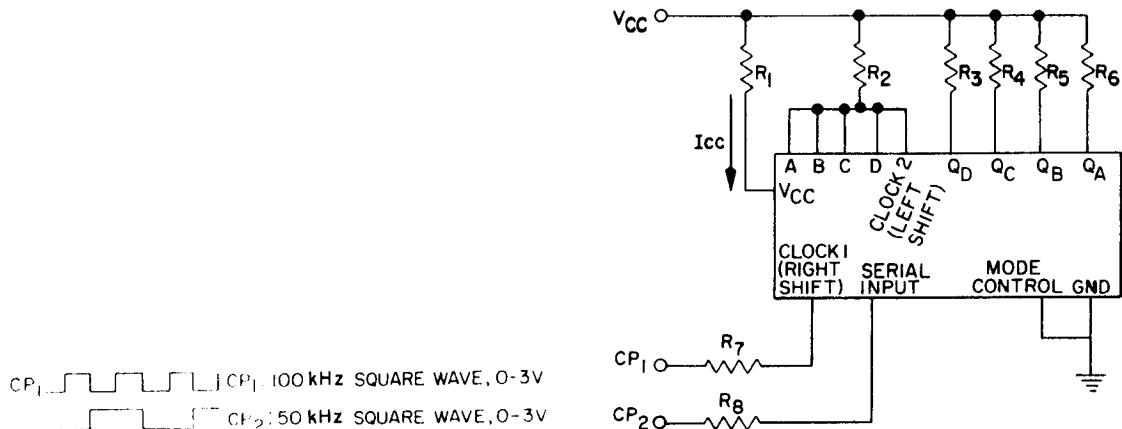


FIGURE 4. Schematic circuits - Continued.

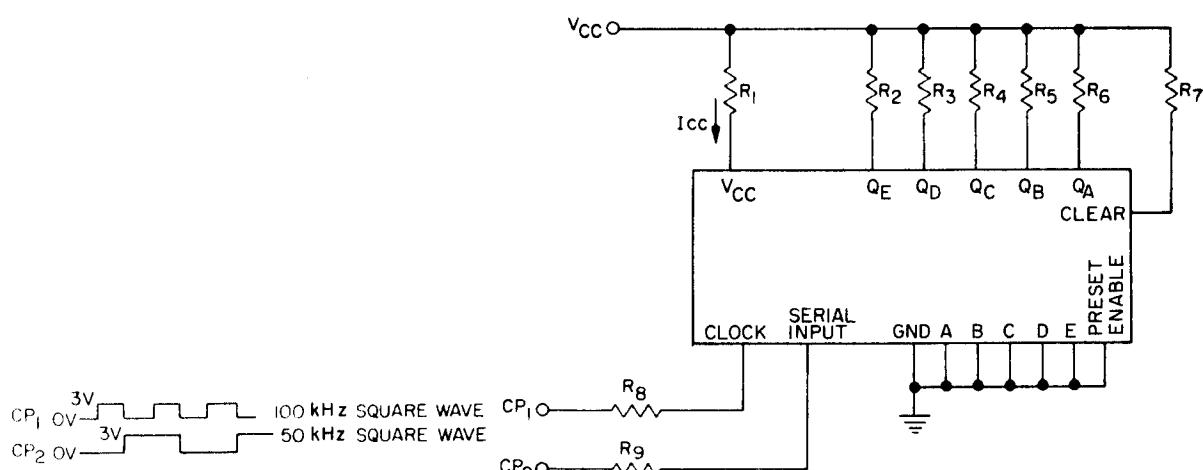


- NOTES:
1. Component values shown are nominal.
 2. $V_{CC} = 1$

FIGURE 4. Schematic circuits - Continued.

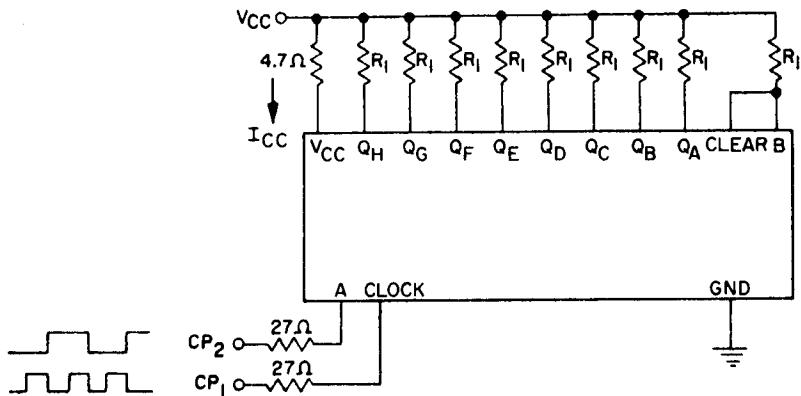
Device Type 01

NOTES:

 $R_1 = 10\Omega$ maximum. $R_2 = R_7 = R_8 = 27\Omega$ maximum. $R_3 = R_4 = R_5 = R_6 = 220\Omega \pm 5\%$. I_{CC} maximum = 72 mA. V_{CC} shall be of such a value as to provide 5 V minimum at device terminals. CP_2 voltage transitions shall occur at least 5 ns after CP_1 transitions.Device Type 02

NOTES:

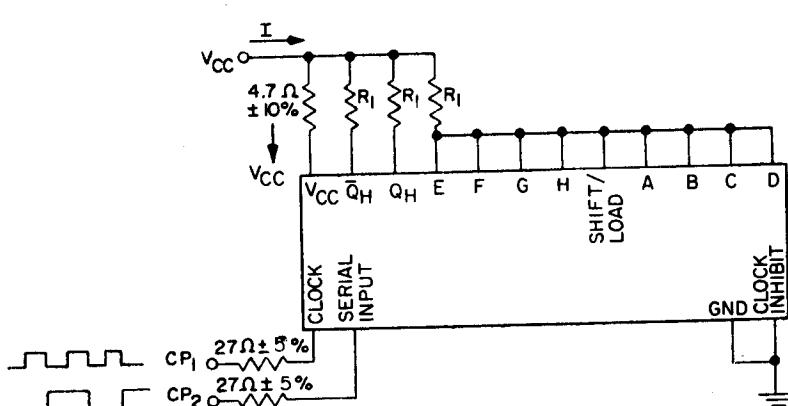
 $R_1 = 10\Omega$ maximum. $R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = 220\Omega \pm 5\%$. $R_8 = R_9 = 27\Omega$ maximum. I_{CC} maximum = 68 mA. V_{CC} shall be of such a value as to provide 5 V minimum at device terminals. CP_2 voltage transitions shall occur at least 5 ns after CP_1 transitions.FIGURE 5. Burn-in and life test circuits.

Device Type 03

NOTES:

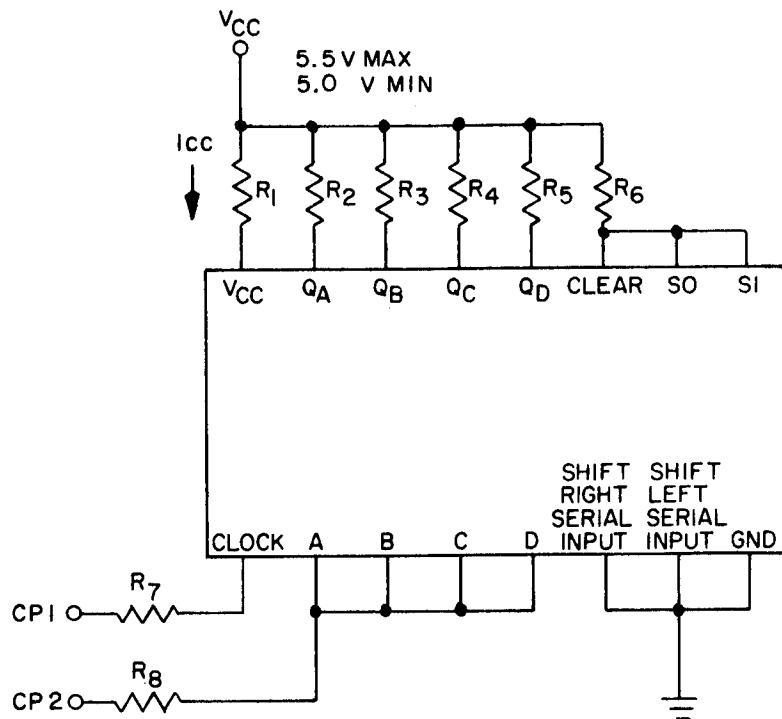
I_{CCMAX} = 54mA.CP₁ = 100 kHz, 50% duty cycle, square wave, 0-3VCP₂ = 50 kHz, 50% duty cycle, square wave, 0-3VCP₂ = voltage transitions shall occur at least 5 ns after CP₁ transitions.

All resistors, ± 5 %

R₁ = 220ΩV_{CC} shall provide 5V min. at device terminals.Device Type 04

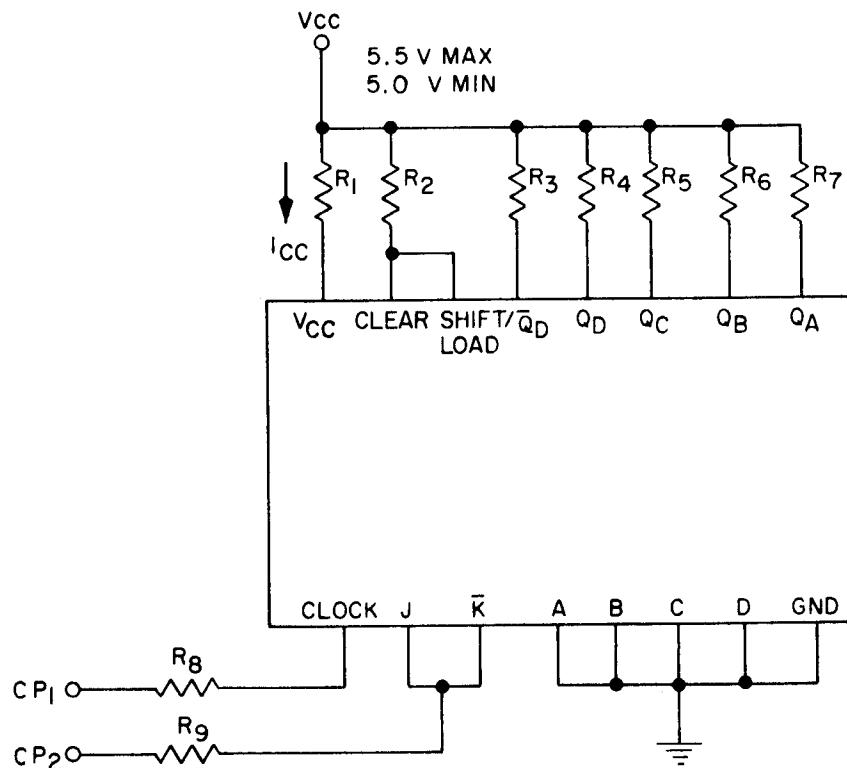
NOTES:

I_{CCMAX} - 63mACP₁ = 100 kHz, 50% duty cycle, square wave, 0-3VCP₂ = 50kHz, 50% duty cycle, square wave, 0-3VCP₂ voltage transitions shall occur at least 5 ns after CP₁ transitions.R₁ = 220Ω ± 5 %V_{CC} shall provide 5V min. at device terminals.FIGURE 5. Burn-in and life test circuits - Continued

Device type 05

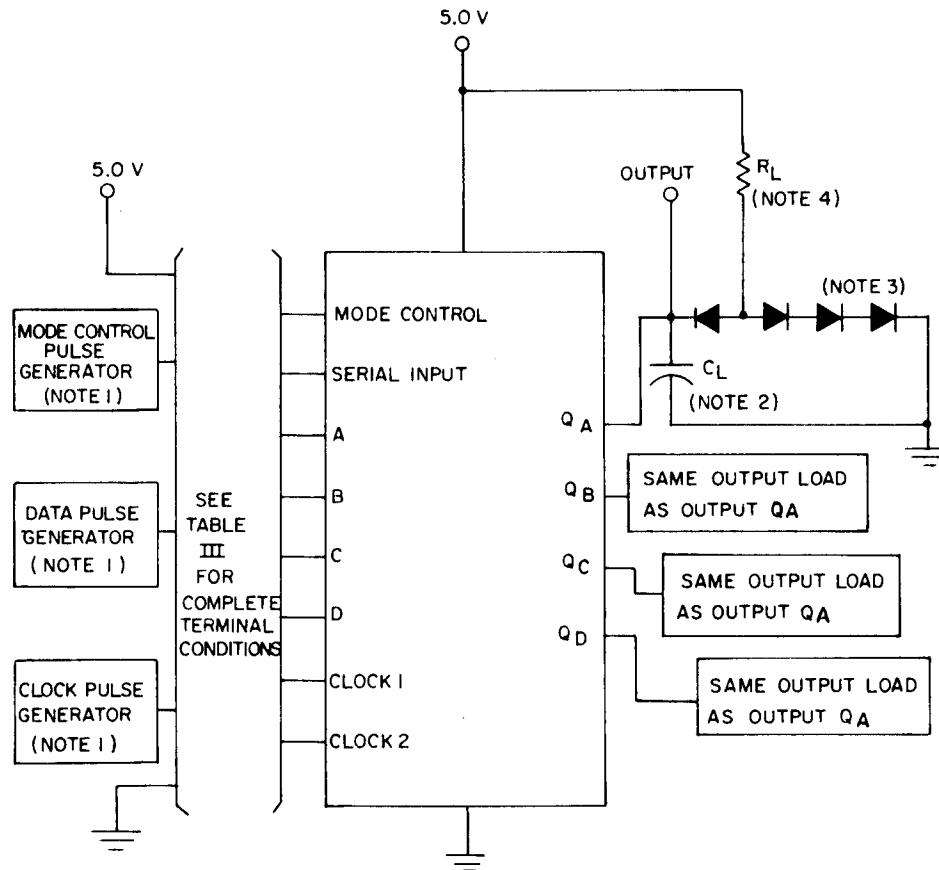
NOTES:

 $R_1 = 4.7 \text{ ohms} \pm 5\%$ $R_2 = R_6 = 220 \text{ ohms} \pm 5\%$ $R_7 = R_8 = 27 \text{ ohms} \pm 5\%$ $CP1 = 100 \text{ kHz}, 50\% \text{ duty cycle, } 0-3V$ $CP2 = 50\text{kHz}, 50\% \text{ duty cycle, } 0-3V$ $I_{CCmax} = 63\text{mA}$ V_{CC} shall provide 5V min. at device terminals.FIGURE 5. Burn-in and lift test circuits - continued.

Device type 06

NOTES:

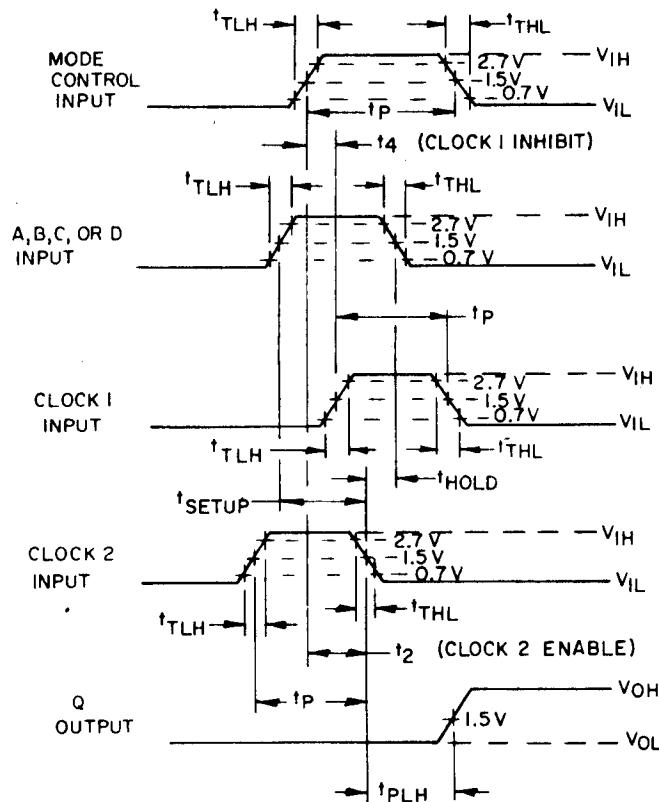
 $I_{CC\max} = 63\text{mA}$. $CP_1 = 0 - 3.0V; 100\text{kHz}; 50\%$ duty cycle $CP_2 = 0 - 3.0V; 50\text{ kHz}; 50\%$ duty cycle $R_1 = 4.7\Omega \pm 10\%$ $R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = 220\Omega \pm 10\%$ $R_8 = R_9 = 27\Omega \pm 10\%$.V_{CC} shall provide 5V min. at device terminals.FIGURE 5. Burn-in and life test circuits - continued.



NOTES:

1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\Omega \pm 5\%$.

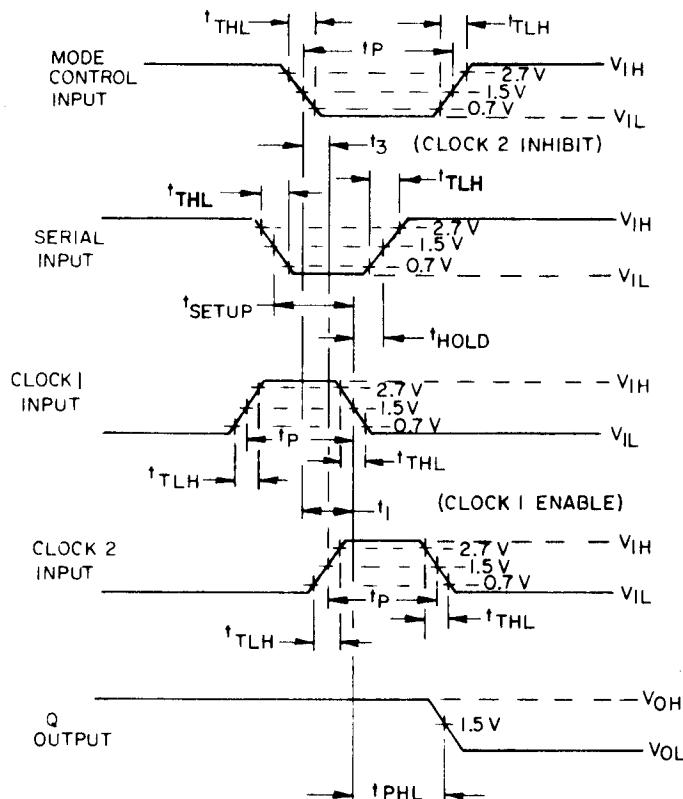
FIGURE 6. Switching test circuits and waveforms for device type 01.

MAXIMUM SHIFT FREQUENCY (f_{MAX}) and CLOCK TO OUTPUT (t_{PLH})

NOTES:

1. Mode control input characteristics: For f_{MAX}, PRR = 22 MHz at TA = 25°C and PRR = 16 MHz at -55°C ≤ TA ≤ 125°C. For t_{PLH}, PRR = 1 MHz, t_p = 35 ns, t_{T LH} = t_{T HL} ≤ 10 ns.
2. A, B, C, or D input characteristics: For f_{MAX}, PRR = 11 MHz at TA = 25°C and PRR = 8 MHz at -55°C ≤ TA ≤ 125°C. For t_{PLH}, PRR = 500 kHz, t_p = t_{SETUP} + t_{HOLD}. t_{SETUP} = 20 ns, t_{HOLD} = 5 ns, t_{T LH} = t_{T HL} ≤ 10 ns.
3. Clock 1 input characteristics: When testing f_{MAX}, PRR = 11 MHz at 25°C and PRR = 8 MHz at -55°C ≤ TA ≤ 125°C. For t_{PLH}, PRR = 500 kHz, t_p = 20 ns minimum, t_{T LH} = t_{T HL} ≤ 10 ns.
4. Clock 2 input characteristics: When testing f_{MAX}, PRR = 22 MHz at 25°C and PRR = 16 MHz at -55°C ≤ TA ≤ 125°C. For t_{PLH}, PRR = 1 MHz, t_p = 20 ns minimum, t_{T LH} = t_{T HL} ≤ 10 ns.
5. Serial input = GND.
6. Except for input under test, all other data inputs are open.

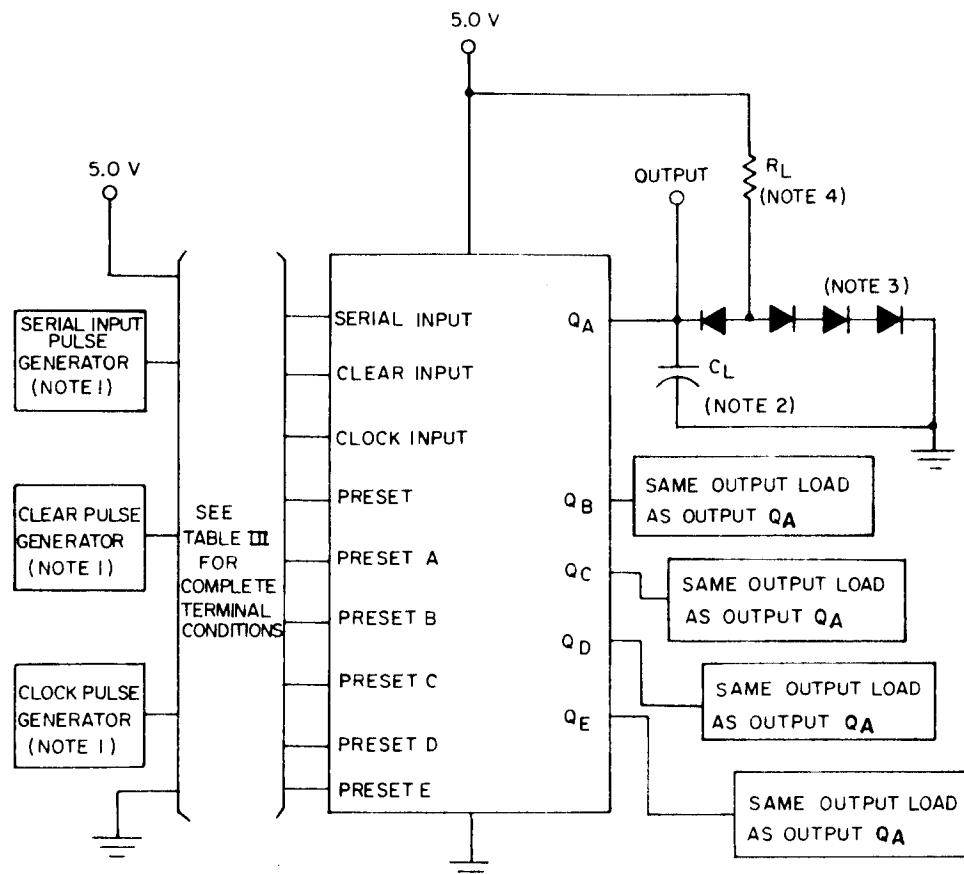
FIGURE 6. Switching test circuits and waveforms for device type 01 - Continued.

CLOCK TO OUTPUT (t_{PHL})

NOTES:

1. Mode control input characteristics: PRR = 1 MHz, $t_p = 35$ ns, $t_{TLH} = t_{THL} \leq 10$ ns.
2. Serial input characteristics: PRR = 500 kHz, $t_p = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 20$ ns minimum, $t_{HOLD} = 5$, $t_{TLH} = t_{THL} \leq 10$ ns.
3. Clock 1 input characteristics: PRR = 1 MHz, $t_p = 20$ ns minimum, $t_{TLH} = t_{THL} \leq 10$ ns.
4. Clock 2 input characteristics: PRR = 500 kHz, $t_p = 20$ ns minimum, $t_{TLH} = t_{THL} \leq 10$ ns.
5. Inputs A thru D = OPEN.

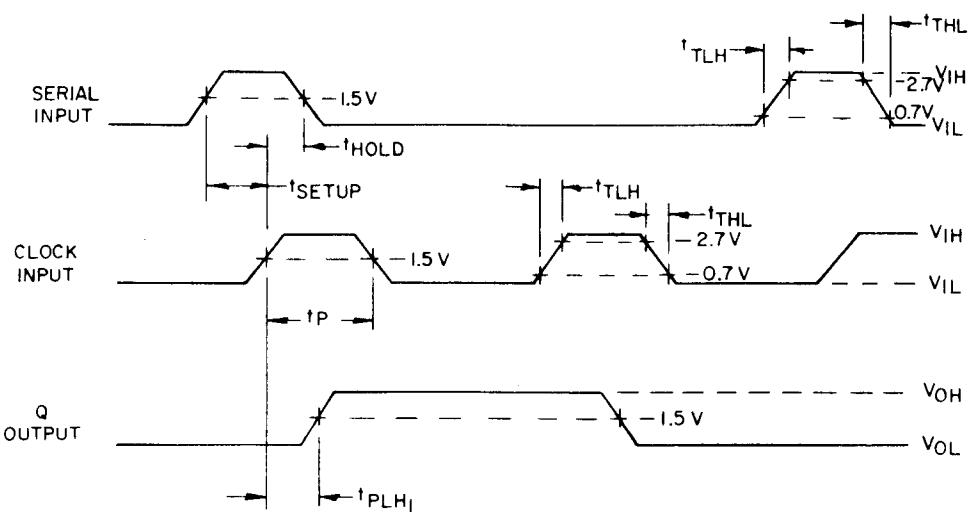
FIGURE 6. Switching test circuits and waveforms for device type 01 - Continued.



NOTES:

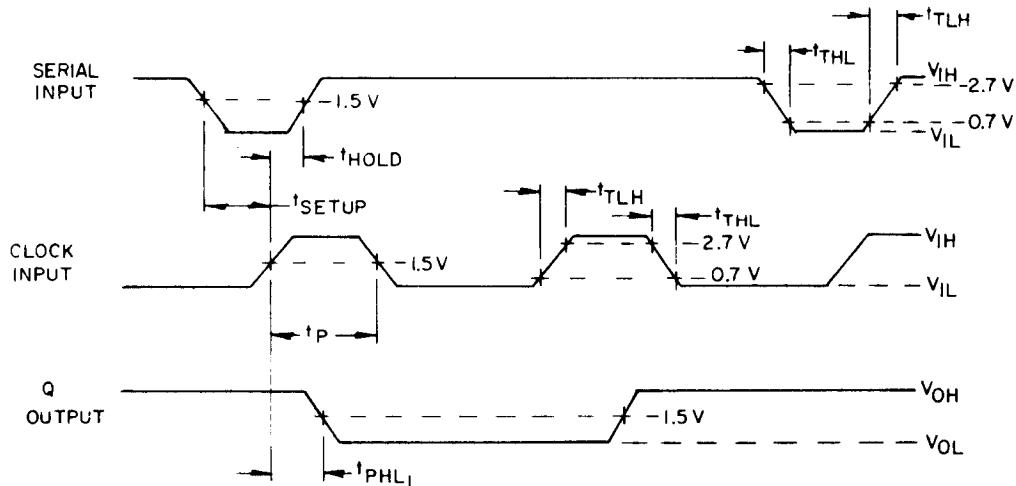
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\Omega \pm 5\%$.

FIGURE 7. Switching test circuits and waveforms for device type 02.

MAXIMUM CLOCK FREQUENCY (f_{MAX}) and CLOCK TO OUTPUT (t_{PLH1}).

NOTES:

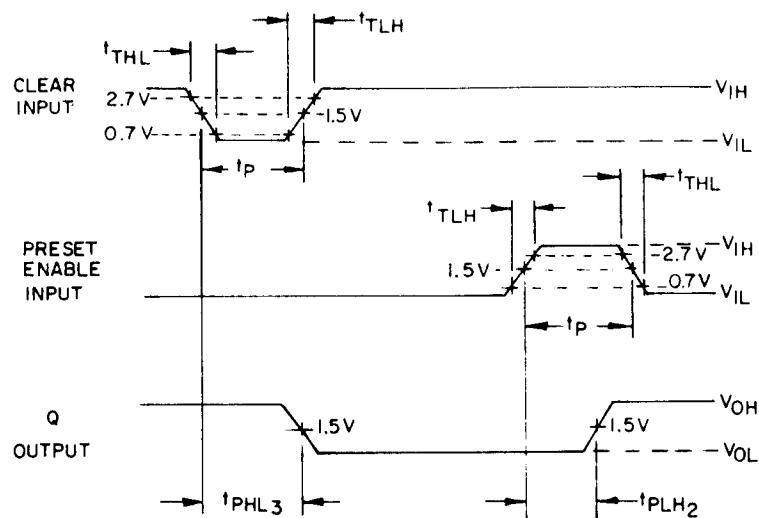
1. Serial input characteristics: For f_{MAX} , PRR = 5 MHz at $TA = 25^\circ C$, PRR = 3.5MHz at $-55^\circ \leq TA \leq 125^\circ C$. For t_{PLH1} , PRR = 500 kHz, $t_p = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 30$ ns, $t_{HOLD} = 0$ ns, $t_{THL} = t_{TLH} \leq 10$ ns.
2. Clock input characteristics: For f_{MAX} , PRR = 10 MHz at $TA = 25^\circ C$, PRR = 7 MHz at $-55^\circ \leq TA \leq 125^\circ C$. For t_{PLH1} , PRR = 1 MHz, $t_p = 35$ ns, $t_{TLH} = t_{THL} \leq 10$ ns.
3. Clear = 4.5 V, preset enable = GND, preset A thru E = OPEN.

CLOCK TO OUTPUT (t_{PHL1})

NOTES:

1. Serial input characteristics: PRR = 500 kHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_p = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 30$ ns, $t_{HOLD} = 0$ ns.
2. Clock input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_p = 35$ ns.
3. Clear = 4.5 V, preset enable = GND, preset A thru E = OPEN.

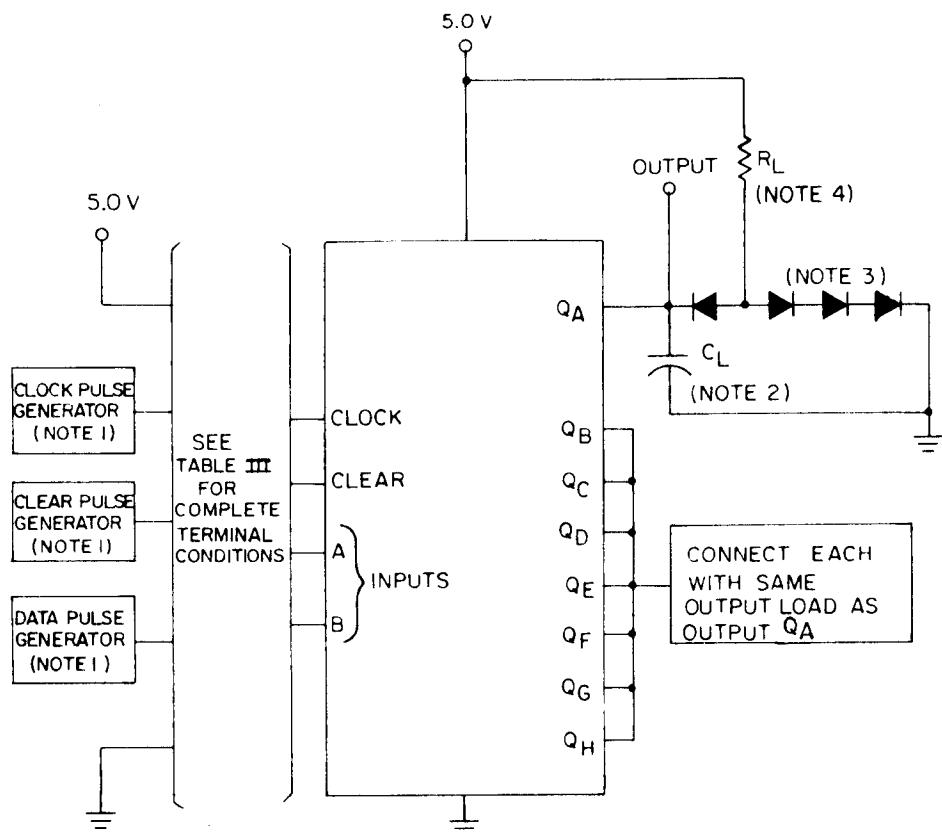
FIGURE 7. Switching test circuits and waveforms for device type 02 - Continued.

PRESET ENABLE TO OUTPUT (t_{PLH2}) and CLEAR TO OUTPUT (t_{PHL3})

NOTES:

1. Clear input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_p = 30$ ns.
2. Preset enable characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_p = 30$ ns.
3. Preset A thru E = 4.5 V, clock = GND, serial = OPEN.

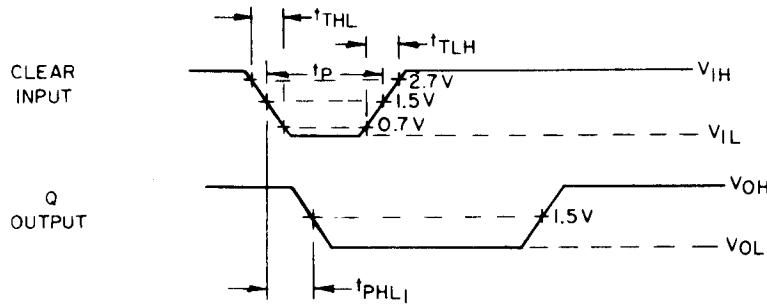
FIGURE 7. Switching test circuits and waveforms for device type 02 - Continued.



NOTES:

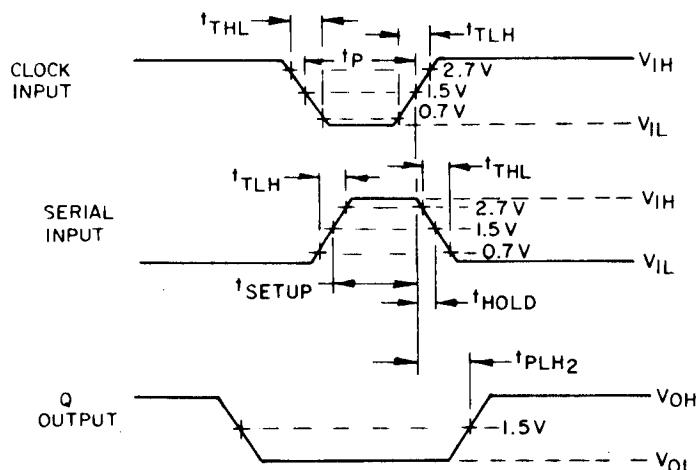
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 800\Omega \pm 5\%$.
5. Q_A outputs are illustrated in the individual waveforms. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.

FIGURE 8. Switching test circuit and waveforms for device type 03.

CLEAR INPUT TO Q OUTPUTS (tPHL1)

NOTES:

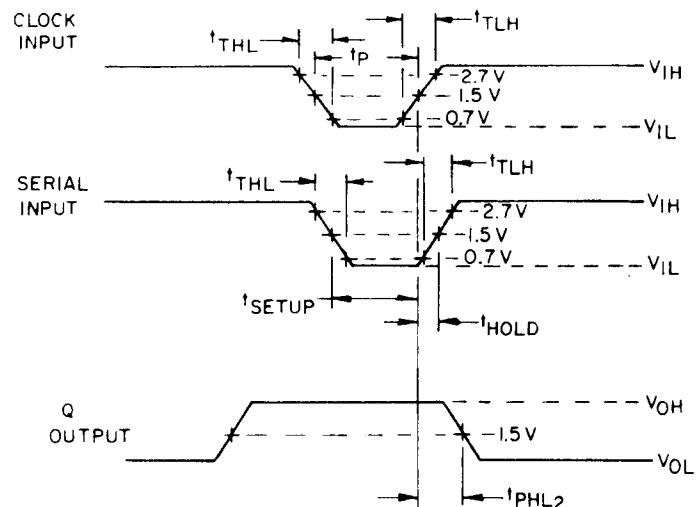
1. Clear input characteristics: PRR = 1 MHz, t_{THL} = t_{TLH} \leq 10 ns, t_p = 50 ns maximum.
2. Clock = GND, serial inputs A and B = OPEN.

MAXIMUM CLOCK FREQUENCY, (f_{MAX}) and CLOCK INPUT TO Q OUTPUT (tPLH2).

NOTES:

1. Clock input characteristics: For f_{MAX}, PRR = 22 MHz at TA = 25°C, PRR = 18 MHz at -55°C \leq TA \leq 125°C. For t_{PLH2}, PRR = 1 MHz, t_p = 30 ns maximum, t_{THL} = t_{TLH} \leq 10 ns.
2. Serial input characteristics: For f_{MAX}, PRR = 11 MHz at 25°C, PRR = 9 MHz at -55°C \leq TA \leq 125°C. For t_{PLH2}, PRR = 500 kHz, t_p = t_{SETUP} + t_{HOLD}, t_{SETUP} = 15 ns minimum, t_{HOLD} = 10 ns maximum, t_{THL} = t_{TLH} \leq 10 ns.
3. Clear = 4.5 V.

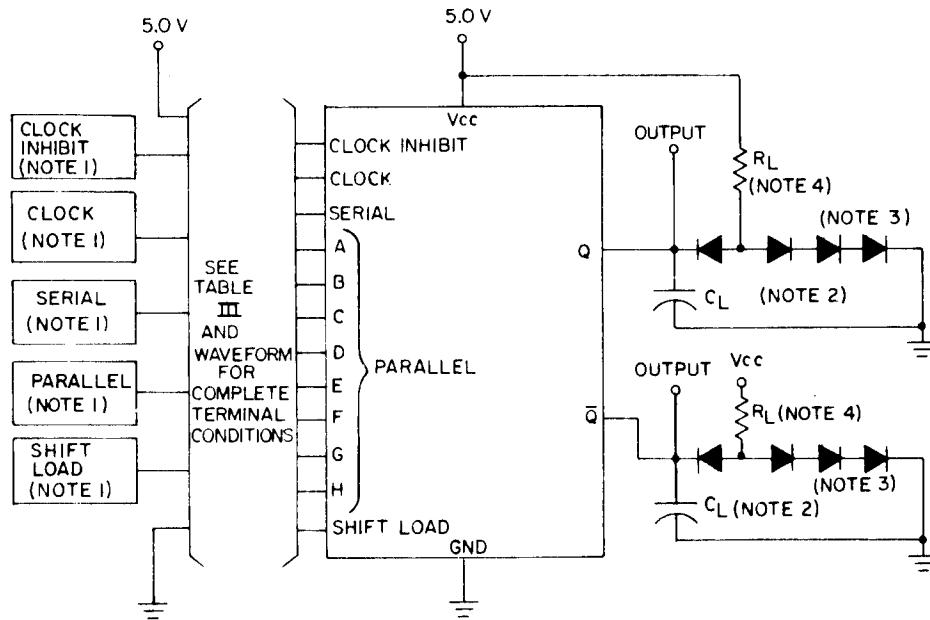
FIGURE 8. Switching test circuit and waveforms for device type 03 - Continued.

CLOCK INPUT TO Q OUTPUT (tPHL2)

NOTES:

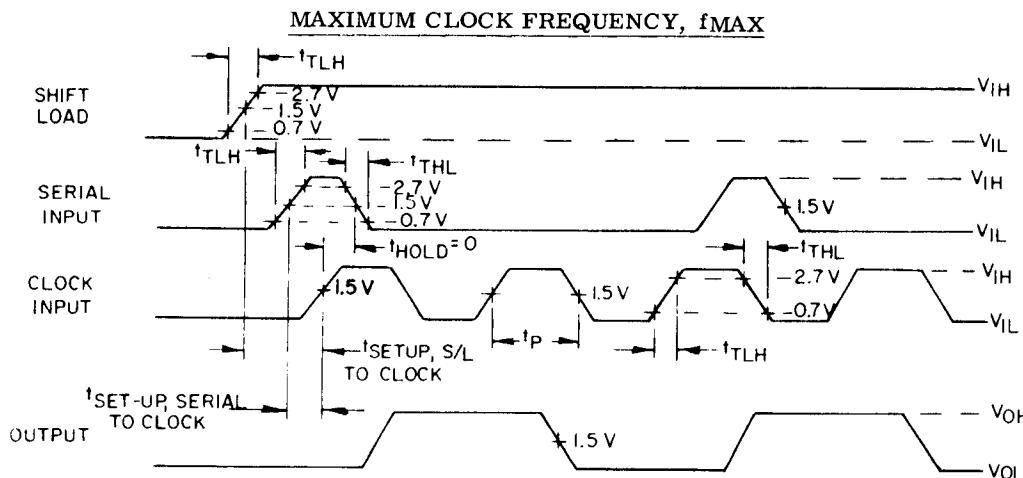
1. Clock input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_p = 30$ ns maximum.
2. Serial input characteristics: PRR = 500 kHz, $t_p = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 15$ ns minimum, $t_{HOLD} = 10$ ns maximum, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Clear = 4.5 V.

FIGURE 8. Switching test circuit and waveforms for device type 03 - Continued.

**NOTES:**

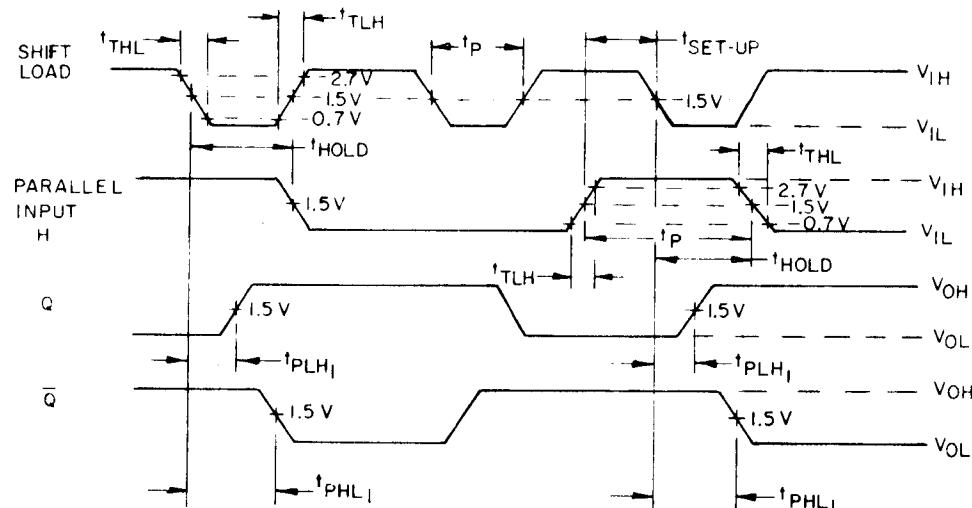
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} \approx 50\Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\Omega \pm 5\%$.

FIGURE 9. Switching test circuit and waveforms for device type 04.



NOTES:

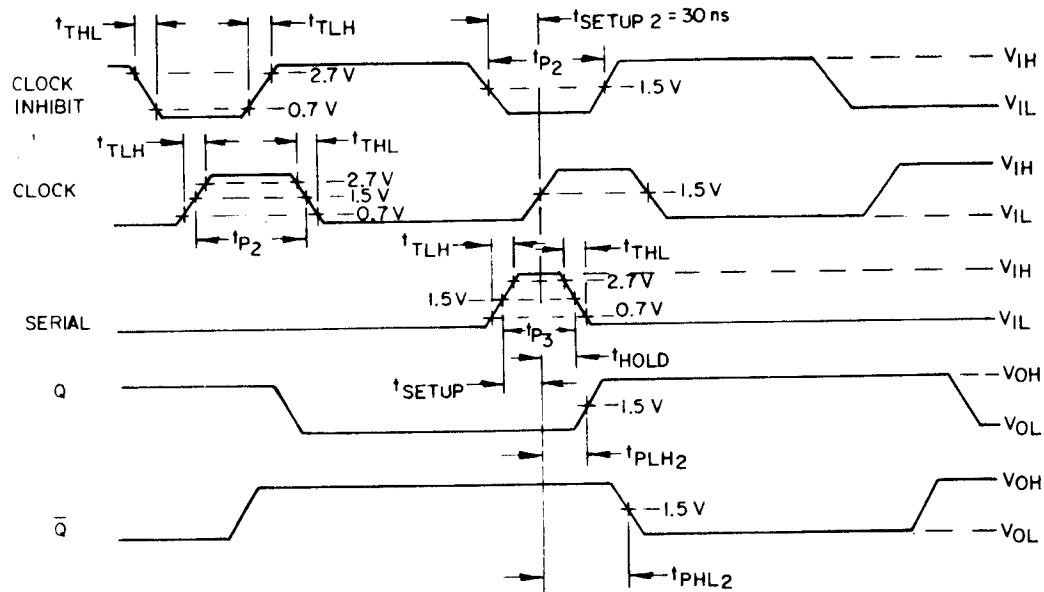
1. Clock pulse characteristics: PRR = 18 MHz at TA = 25°C, PRR = 14 MHz at -55°C ≤ TA ≤ 125°C, $t_{TLH} = t_{THL} \leq 10$ ns, $t_P = 20$ ns minimum.
2. Serial pulse characteristics: PRR = 9 MHz at TA = 25°C, 7 MHz at -55°C ≤ TA ≤ 125°C, $t_P = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 35$ ns minimum, $t_{HOLD} = 0$, $t_{TLH} = t_{THL} \leq 5$ ns.
3. Shift load characteristics: $t_{TLH} = < 10$ ns, $t_{SETUP} = 45$ ns.
4. Clock inhibit = GND, A thru H = GND.

SHIFT LOAD TO OUTPUT (t_{PHL1} , t_{PLH1})

NOTES:

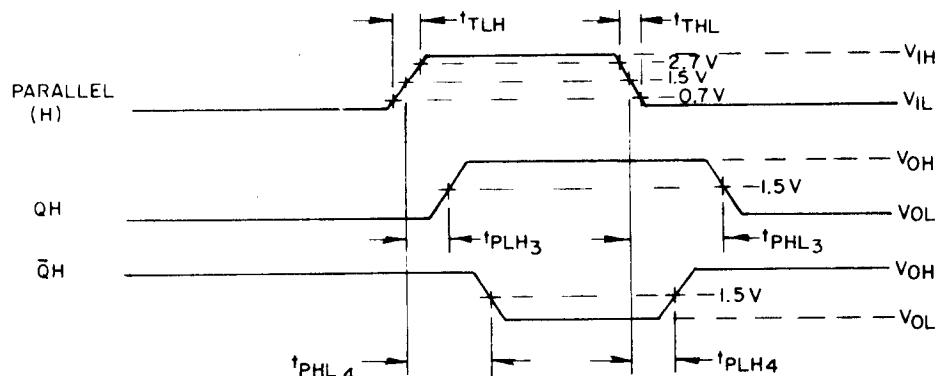
1. Shift load characteristics: PRR = 1 MHz, $t_P = 25$ ns, $t_{THL} = t_{TLH} \leq 10$ ns.
2. Parallel input characteristics: PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD} = 40$ ns, $t_{SETUP} = 10$ ns, $t_{HOLD} = 30$ ns, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Clock = clock inhibit = GND, A thru G = GND, serial = OPEN.

FIGURE 9. Switching test circuit and waveforms for device type 04 - Continued.

CLOCK TO OUTPUT (tPHL2 and tPLH2)

NOTES:

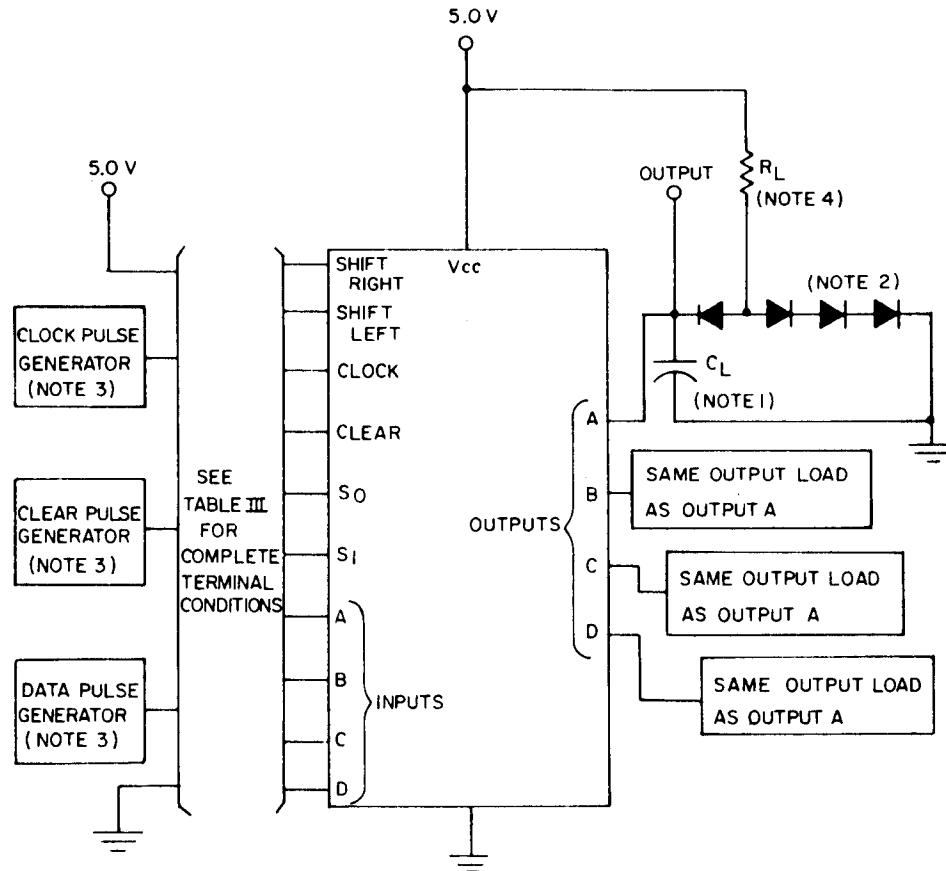
1. Clock inhibit characteristics: PRR = 1 MHz, $t_{p2} = 50\ ns$, $t_{TTLH} = t_{TLH} \leq 10\ ns$, $t_{SETUP2} = 30\ ns$.
2. Clock pulse characteristics: PRR = 1 MHz, $t_{p1} = 25\ ns$, $t_{TTHL} = t_{THL} \leq 10\ ns$.
3. Serial pulse characteristics: PRR = 500 kHz, $t_{p3} = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 35\ ns$, $t_{HOLD} = 0$, $t_{TTLH} = t_{THL} \leq 5\ ns$.
4. Shift/load = 5.0 V.

(H) INPUT TO QH and $\bar{Q}H$ OUTPUTS (tPHL3 and tPLH3) (tTHL4 and tPLH4)

NOTES:

1. (H) input characteristics: PRR = 1 MHz, 50% duty cycle, $t_{TTLH} = t_{THL} \leq 10\ ns$.
2. Shift/load = GND, clock inhibit = GND, serial = GND, A thru G = GND, clock = GND.

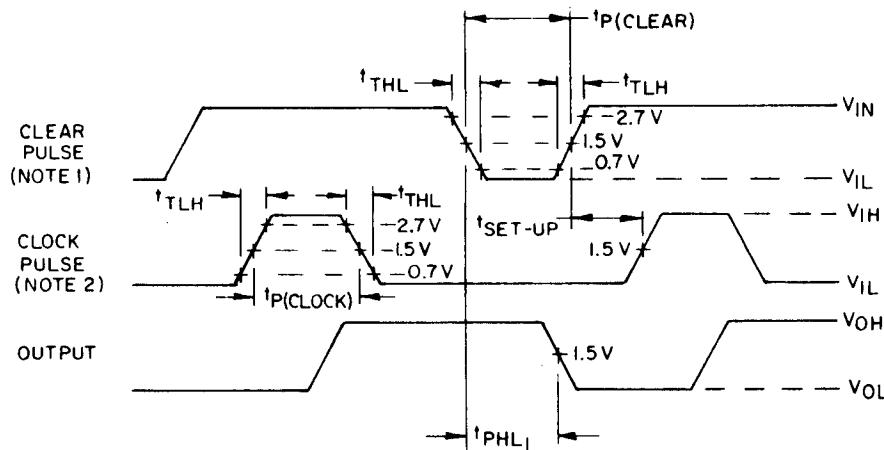
FIGURE 9. Switching test circuit and waveforms for device type 04 - Continued.



NOTES:

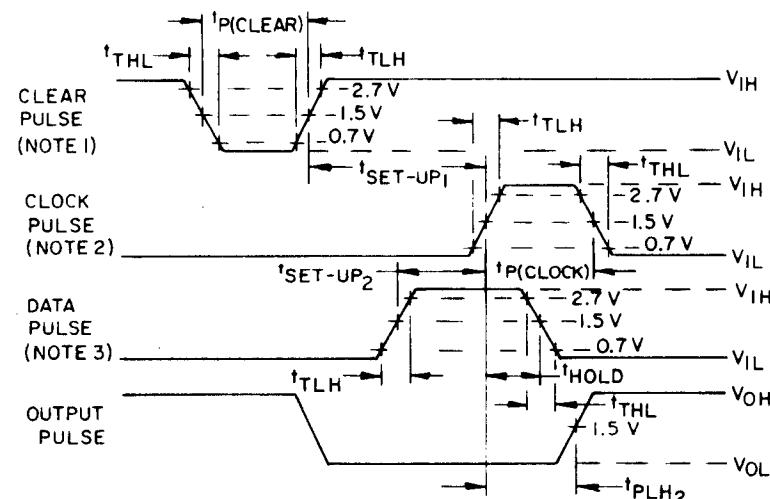
1. $C_L = 50 \text{ pF}$ minimum including probe and jig capacitance.
2. All diodes are 1N3064, or equivalent.
3. Unless otherwise specified in the notes associated with the individual tests, all pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_{TLH} \leq 7 \text{ ns}$, $t_{TTHL} \leq 7 \text{ ns}$, $V_{IH} = 3.0 \text{ V}$ minimum, $V_{IL} = 0$.
4. $R_L = 400\Omega \pm 5\%$.

FIGURE 10. Switching test circuit and waveforms for device type 05.

CLEAR TO OUTPUT

NOTES:

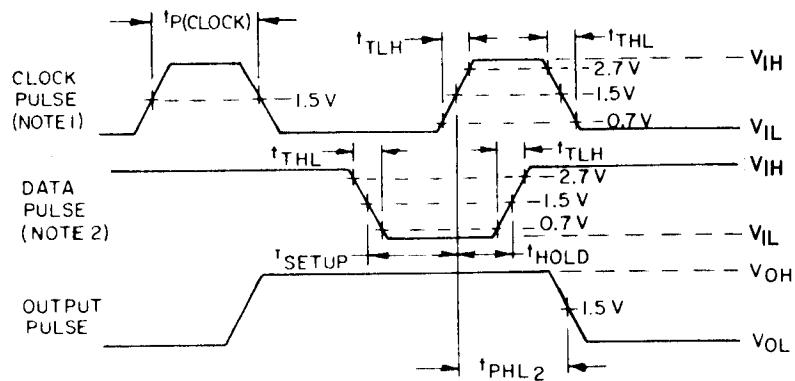
1. The clear pulse has the following characteristics: $t_{P(CLEAR)} = 20$ ns, $t_{SETUP} = 25$ ns, PRR = 1 MHz.
2. The clock pulse has the following characteristics: $t_{P(CLOCK)} = 20$ ns, PRR = 1 MHz.

CLOCK TO OUTPUT, DATA PULSE TO PARALLEL INPUT (t_{PLH_2})

NOTES:

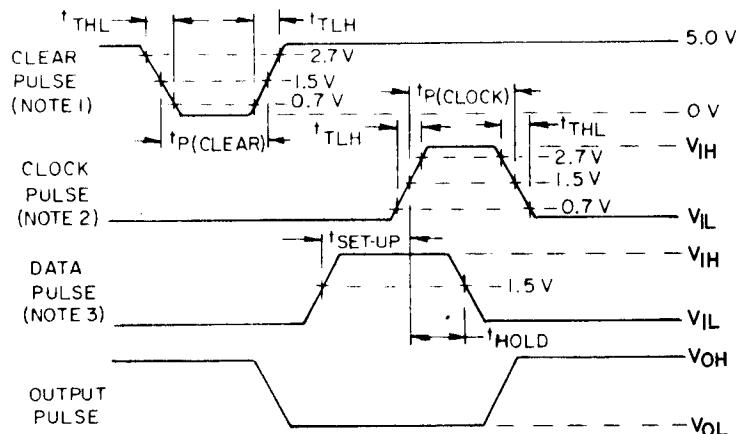
1. The clear pulse is a momentary ground, then V_{IH} is applied to the input. $t_{P(CLEAR)} \leq 75$ ns, $t_{THL} \leq 15$ ns and $t_{TLH} \leq 15$ ns, $t_{SETUP} = 25$ ns.
2. Clock pulse characteristics: $t_{P(CLOCK)} = 20$ ns, PRR = 2 MHz.
3. Data pulse characteristics: $t_{P(DATA)} = t_{(SETUP2)} + t_{HOLD}$, $t_{SETUP2} = 20$ ns, $t_{HOLD} = 7$, PRR = 1 MHz.

FIGURE 10. Switching test circuit and waveforms for device type 05 - Continued.

CLOCK TO OUTPUT, DATA PULSE TO PARALLEL INPUT (tPHL2)

NOTES:

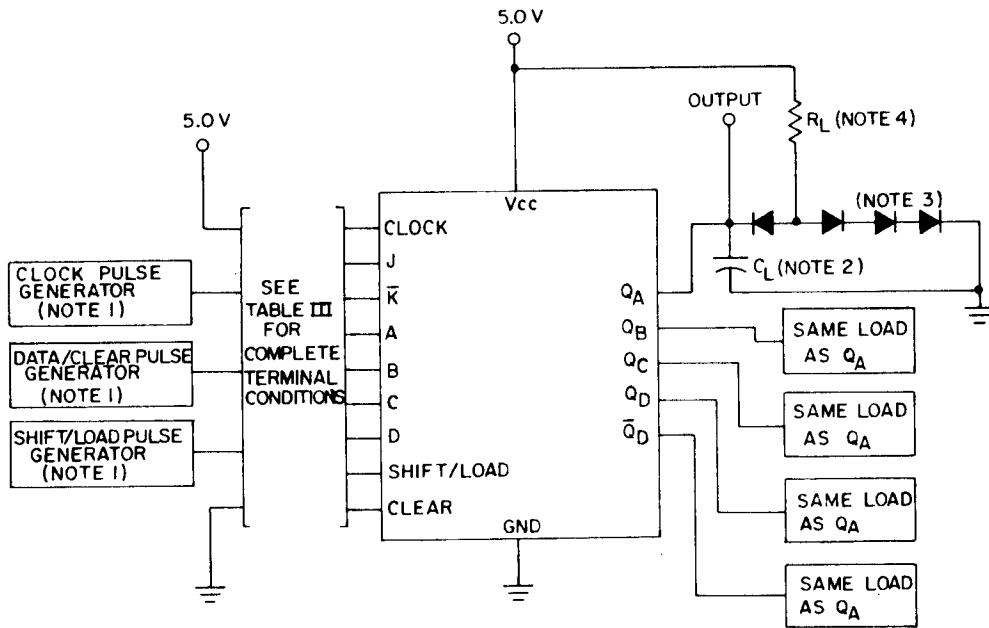
1. Clock pulse characteristics: $t_P(CLOCK) = 20$ ns, PRR = 2 MHz.
2. Data pulse characteristics: $t_P(DATA) = t_{SETUP} = 20$ ns, PRR = 1 MHz.

MAXIMUM CLOCK FREQUENCY (f_{MAX})

NOTES:

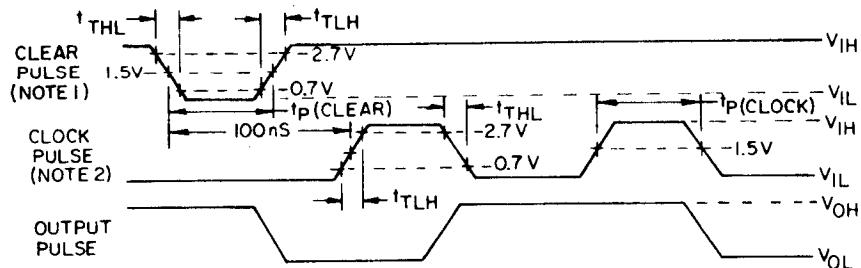
1. The clear pulse is a momentary GND, then V_{IH} is applied to the input, $t_P(CLEAR) \leq 20$ ns, $t_{THL} \leq 15$ ns, $t_{TLH} \leq 15$ ns.
2. Clock pulse characteristics: $t_P(CLOCK) = 20$ ns, PRR = 18 MHz at $-55^\circ C \leq TA \leq 125^\circ C$ (22 MHz at $TA = 25^\circ C$).
3. Data pulse characteristics: $t_P(DATA) = t_{SETUP} = 20$ ns, PRR = 9 MHz at $-55^\circ C \leq TA \leq 125^\circ C$ (11 MHz at $TA = 25^\circ C$).

FIGURE 10. Switching test circuit and waveforms for device type 05 - Continued.



NOTES:

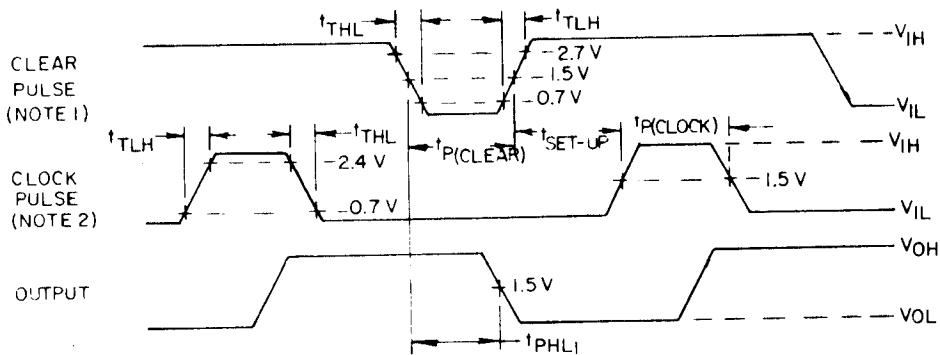
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 7$ ns, $t_{TTHL} \leq 7$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$, $Z_{OUT} \approx 50\Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\Omega \pm 5\%$.

MAXIMUM CLOCK FREQUENCY, f_{MAX}

NOTES:

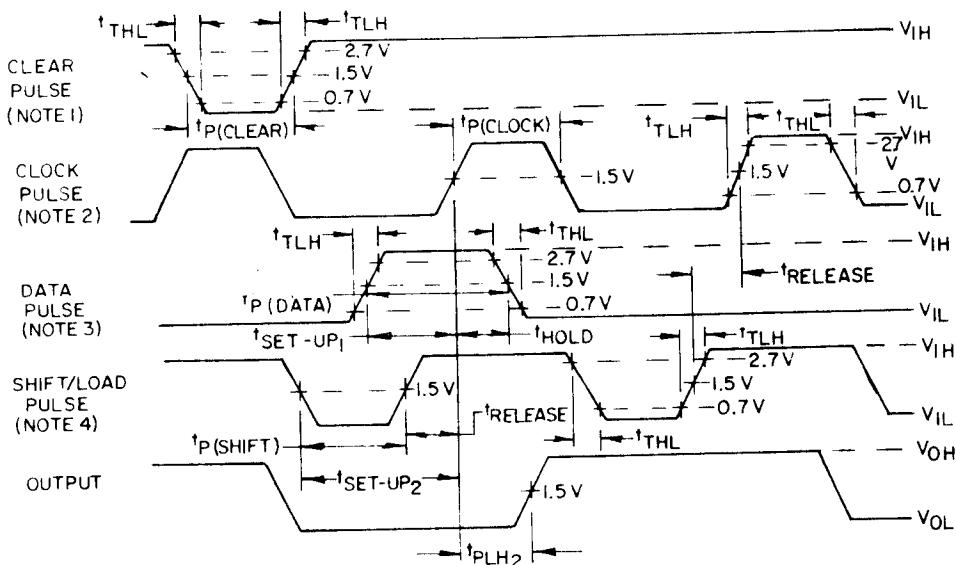
1. The clear pulse is a momentary GND, then V_{IH} is applied to the input. $t_{THL} \leq 15$ ns, $t_{TLH} \leq 15$ ns, $t_P(CLEAR) \leq 75$ ns.
2. Clock pulse characteristics: $t_P(CLOCK) = 16$ ns, $PRR = 24$ MHz at $-55^\circ C \leq T_A \leq 125^\circ C$ (30 MHz at $T_A = 25^\circ C$), $V_{IH} = 3.0$ V minimum, $V_{IL} = GND$.

FIGURE 11. Switching test circuit and waveforms for device type 06.

CLEAR TO OUTPUT (tPHL1)

NOTES:

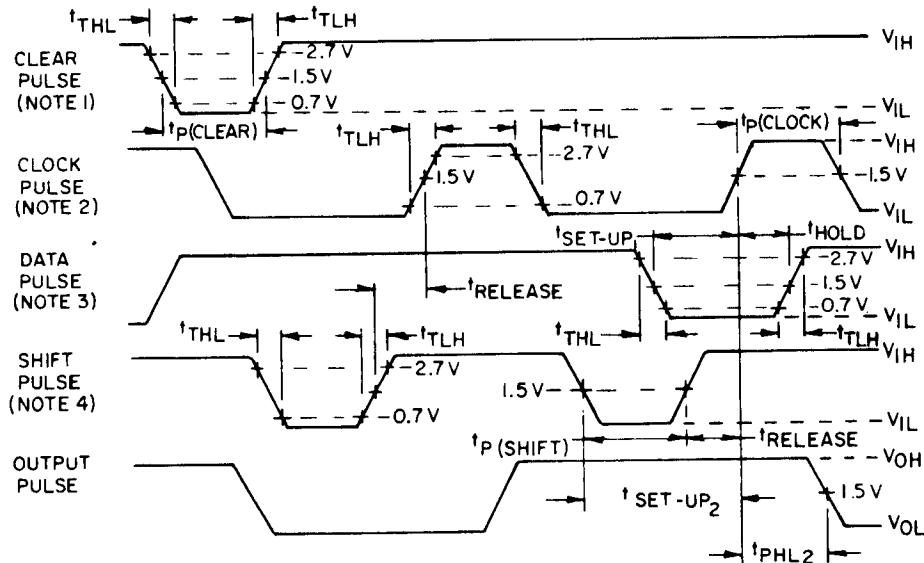
1. Clear pulse characteristics: $t_P(CLEAR) = 12 \text{ ns}$, $t_{SETUP} = 25 \text{ ns}$, PRR = 1 MHz.
2. Clock pulse characteristics: $t_P(CLOCK) = 16 \text{ ns}$, PRR = 1 MHz.

CLOCK TO OUTPUT (tPLH2)

NOTES:

1. The clear pulse is a momentary GND, then V_{IH} is applied to the input. $t_{THL} \leq 15 \text{ ns}$, $t_{TLH} \leq 15 \text{ ns}$, $t_P(CLEAR) \leq 100 \text{ ns}$.
2. Clock pulse characteristics: $t_P(CLOCK) = 16 \text{ ns}$, PRR = 2 MHz.
3. Data pulse characteristics: $t_P(DATA) = 25 \text{ ns}$, $t_{SETUP1} = 25 \text{ ns}$, $t_{HOLD} = 0$, PRR = 1 MHz.
4. Shift/load pulse characteristics: $t_P(SHIFT) = 17 \text{ ns}$, $t_{RELEASE} = 10 \text{ ns}$, $t_{SETUP2} = 27 \text{ ns}$, PRR = 2 MHz.

FIGURE 11. Switching test circuit and waveforms for device type 06 - Continued.

CLOCK TO OUTPUT (t_{PHL2})

NOTES:

1. The clear pulse is a momentary GND, then V_{IH} is applied to the input. $t_{THL} \leq 15$ ns, $t_{TLH} \leq 15$ ns, $t_P(CLEAR) \leq 100$ ns.
2. Clock pulse characteristics: $t_P(CLOCK) = 16$ ns, PRR = 2 MHz.
3. Data pulse characteristics: $t_P(DATA) = t_{SETUP} + t_{HOLD} = 20$ ns, $t_{SETUP1} = 20$ ns, $t_{HOLD} = 0$, PRR = 1 MHz.
4. Shift/load pulse characteristics: $t_P(SHIFT) = 22$ ns, $t_{RELEASE} = 10$ ns, $t_{SETUP2} = 32$ ns, PRR = 2 MHz.

FIGURE 11. Switching test circuit and waveforms for device type 06 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	Test No.	Meas. terminal										Test limits	
					1	2	3	4	5	6	7	8	9	10	11	
1 $T_A = 25^\circ C$	VOH	3006	1	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	GND	A 1/ Clock 2	QD	QC	QA	VCC
	VOL	3007	2	3	4	5	6	7	8	9	10	11	12	13	14	2.4 V
	VIC															0.4 V
																-1.5 V
	IIL1	3009	9	-12 mA												Input serial
			10		-12 mA	-12 mA	-12 mA	-12 mA	-12 mA	-12 mA						Input A
			11													Input B
			12													Input C
			13													Input D
			14													Mode control
			15													Clock 2
			16													Clock 1
	IIL2		17	0.4 V							GND					5.5 V
			18	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	4.5 V					Input serial
			19													Input A
			20													Input B
			21													Input C
			22													Input D
			23													Clock 2
			24													Clock 1
	IHH1	3010	25	2.4 V							4.5 V					40 μA
			26		2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	GND					2 /
			27													3 /
			28													
			29													
			30													
			31													

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits		
			Test No.	Input serial	Input A	Input B	Input C	Input D	Mode control	GND	Clock 1	QD	QC	QB	QA	VCC	Meas. terminal	Min	Max	Unit
TA = 25°C	I _{H2}	3010	32	5.5 V	5.5 V	5.5 V	5.5 V		4.5 V	GND						5.5 V	Input serial	100	μA	
	I _{H3}		33							GND							Input A			
	I _{H4}		34														Input B			
	I _S		35														Input C			
	I _S		36														Input D			
	I _S		37														Clock 2			
	I _S		38														Clock 1			
2	I _C	3005	39														Mode control	80		
	I _C		40														Mode control	200		
	I _S		41														QA	-18	-57	mA
	I _S		42														QB			
	I _S		43														QC			
	I _S		44														QD			
	I _C		45														VCC	72		
3	Same tests, terminal conditions and limits as for subgroup 1, except TA = +125°C and VIC tests are omitted.																			
	TA = 25°C	3014	46	B	B	B	B	A	A	GND	B	B	X	X	X	X	4.5 V			
	TA = 7°C		47																	
	Truth table test 5/		48																	
			49																	
			50	A																
			51	A																
			52	A																
			53	B																
			54	B																
			55	B																
			56	A																
			57	A																
			58	A																
6	Same tests, terminal conditions and limits as for subgroup 1, except TA = -55°C and VIC tests are omitted.																			
	TA = 7°C	3014	59	B																
			60	B																
			61	B																
			62	A																
			63	A																
			64	A																
			65	B																
			66																	
			67																	
			68																	
			69																	
			70																	
			71																	
			72																	
			73																	
			74																	

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits		
			Test No.	Input serial	Input A	Input B	Input C	Input D	Mode control	GND	Clock 2	Clock 1	QD	QC	QB	QA	VCC	Meas. terminal	Min Max Unit	
7	TA = 25°C	Truth table test	3014	75	B	A	B	A					L	L	L	L	4.5 V			
TA = 25°C			5/	76	A	A	B	B					H	H	H	H				
				77	A	A	B	A					H	H	H	H				
				78	B	B	A	B					L	L	L	L				
				79	B	B	B	B					H	H	H	H				
				80	B	B	B	B					L	L	L	L				
				81	A	A	A	A					H	H	H	H				
				82	A	A	A	A					L	L	L	L				
				83	B	B	B	B					H	H	H	H				
				84	B	B	B	B					L	L	L	L				
				85	B	B	B	B					H	H	H	H				
				86	B	B	B	B					L	L	L	L				
8					Repeat subgroup 7 at TA = +125°C and TA = -55°C.															
9	TA = 25°C	f _{MAX} (Fig 6) t _{TPLH} (Fig 6)	3003	87	GND												5.0 V	QD	11	MHz
				88														QA	10	ns
				89														QB	30	
				90														QC		
				91														QD	35	
10	TA = 125°C	f _{MAX} (Fig 6) t _{TPLH} (Fig 6)	3003	96	GND												5.0 V	QD	8	MHz
				97														QA	10	ns
				98														QB	42	
				99														QC	49	
				100														QD		
11					Same tests, terminal conditions and limits as for subgroup 10, except TA = -55°C.															

1/ A = normal clock pulse, except for subgroups 7 and 8 (see 4/).

2/ For device type 01, with schematics incorporating a 4 kΩ base resistor, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively. For schematics incorporating a 6 kΩ base resistor, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.

3/ For device type 01, with schematics incorporating a 4 kΩ base resistor in the mode control input circuit, the minimum and maximum limits shall be -1.4 and -3.2 mA, respectively. For schematics incorporating a 6 kΩ base resistor in the mode control input circuit, the minimum and maximum limits shall be -0.8 and -2.6 mA, respectively.

4/ For subgroups 7 and 8, A = VCC, B = GND, and X = indeterminate.

5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

6/ Output voltages shall be either:

(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or

(b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

7/ Only a summary of attributes data is required.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		
																				Min	Max	Unit
1 $T_A = 25^\circ C$	V_{OH}	3006	1	2.0 V	2.0 V	4.5 V	2.0 V	0.8 V	-4 mA	-4 mA	-4 mA	2.0 V	QA	2.4		V						
	V_{OL}	3007	6	7	8	9	10					-0.8 V	-4 mA	-4 mA	-4 mA	0.8 V	QB	2.4		V		
	V_{IC}											16 mA	16 mA	16 mA	16 mA	0.8 V	QC	2.4		V		
												16 mA	16 mA	16 mA	16 mA	0.8 V	QD	2.4		V		
												16 mA	16 mA	16 mA	16 mA	0.8 V	QE	2.4		V		
																Clock	-1.5					
																Preset A						
																Preset B						
																Preset C						
																Preset D						
																Preset E						
																Preset enable						
																Serial input						
																Clear						
																Clock	-0.7	-1.6	mA			
																Preset A						
																Preset B						
																Preset C						
																Preset D						
																Preset E						
																Serial input						
																Clear						
																Preset	-3.0	-8.0	mA			
																enable						
																Clock	40	μA				
																Preset A						
																Preset B						
																Preset C						
																Preset D						
																Preset E						
																Serial input						
																Clear						
																Clock	100					
																Preset A						
																Preset B						
																Preset C						
																Preset D						
																Preset E						
																Serial input						
																Clear						
																Clock	5.5 V					
																Preset						
																enable						
																Clock	5.5 V					

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
																				200 μ A	500 μ A			
$T_A = 25^\circ C$	IH3	3010	45																		Preset enable	Preset enable		
	IH4	3010	46																		Preset enable	Preset enable		
	IS6	3011	47																		Q _A	-20 mA		
			48																		Q _B	-57 mA		
			49																		Q _C			
			50																		Q _D			
																					Q _E			
	ICCH	3005	52																		5.5 V	V _{CC}	68	
	ICCL	3005	53																		GND	V _{CC}	68	
2																								
3																								
$T_A = 25^\circ C$	7	3014	54	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	L	L	L	B	
			55	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	L	L	L		
			56	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	L	L	L		
			57																					
			58																					
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2/

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MLT-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits				
					Preset	Clock	Vcc	D	Preset	Enable	serial	Input	Preset	enable	Q _E	Q _D	GND	Q _C	Q _B	Q _A	Clear	Meaning terminal	Min	Max
7 $T_A = 25^\circ C$ $\frac{1}{4}$ / $\frac{1}{4}$	3014	Truth table test 3/	88	B	B	B	4.5 V	B	B	B	B	B	B	A	L	H	H	H	H	A				
			89	A	B	A																		
			90	B	A	A																		
			91	B	B	A																		
			92	A																				
			93	A																				
			94	B																				
			95	A																				
			96	B																				
			97	A																				
			98	B																				
			99	A																				
			100	B																				
			101	A																				
			102	B																				
			103	A																				
			104	B																				
			105	A																				
			106	B																				
			107	A																				
			108	B																				
			109	A																				
			110	B																				
			111	A																				
			112	B																				
			113	A																				
			114	B																				
			115	A																				
			116	B																				
			117	A																				
			118	B																				
			119	A																				
			120	B																				
			121	A																				
			122	B																				
			123	A																				
8																								
9 $T_A = 25^\circ C$	tMAX	(Fig 7)	124	IN																				
			3003																					
			(Fig 7)																					
			125																					
			126																					
			127																					
			128																					
			129																					
			130																					
			131																					
			132																					
			133																					
			134																					

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STU-833 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits	
			Test No.	Clock	Preset	Preset	VCC	Preset	VCC	Preset	VCC	Input serial	QE	QB	QC	QA	Clear terminal	Meas. terminal	Unit		
9 $T_A = 25^\circ C$	tPLH2	3003 (Fig 7)	135	GND	4.5 V	4.5 V	4.5 V	5.0 V	4.5 V	4.5 V	4.5 V	IN		GND	QD	GND	QE	QA	QA	ns	
	tPHL3		136														OUT	OUT	QB	QB	12 42
			137														OUT	OUT	QC	QC	
10 $T_A = 125^\circ C$	tPLH1	3003 (Fig 7)	138														OUT	OUT	QC	QC	
			139														OUT	OUT	QE	QE	
	tPHL1		140														OUT	OUT	QA	QA	
			141														OUT	OUT	QB	QB	
11	tPLH2		142														OUT	OUT	QC	QC	
			143														OUT	OUT	QE	QE	
	tPHL3		144														OUT	OUT	QA	QA	
			145														OUT	OUT	QB	QB	
	tPLH1		146														OUT	OUT	QC	QC	
12	tPHL1		147														OUT	OUT	QE	QE	
			148														OUT	OUT	QA	QA	
	tPLH1		149														OUT	OUT	QB	QB	
			150														OUT	OUT	QC	QC	
	tPHL1		151														OUT	OUT	QE	QE	
13	tPLH2		152														OUT	OUT	QA	QA	
			153														OUT	OUT	QB	QB	
	tPHL1		154														OUT	OUT	QC	QC	
			155														OUT	OUT	QE	QE	
	tPLH2		156														OUT	OUT	QA	QA	
14	tPHL1		157														OUT	OUT	QB	QB	
			158														OUT	OUT	QC	QC	
	tPLH1		159														OUT	OUT	QE	QE	
			160														OUT	OUT	QA	QA	
	tPHL3		161														OUT	OUT	QB	QB	
15	tPLH1		162														OUT	OUT	QC	QC	
			163														OUT	OUT	QE	QE	
	tPHL1		164														OUT	OUT	QA	QA	
			165														OUT	OUT	QB	QB	
11 Same tests, terminal conditions, and limits as for subgroup 10, except $T_A = -55^\circ C$.																					

1/ For subgroups 7 and 8, A = VCC and B = GND.

2/ Output voltages shall be either:

(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or

(b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.

3/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

4/ Only a summary of attributes data is required.

TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	Test No.												Test limits		
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	Unit
1	$T_A = 25^\circ C$	3006	V _{OH}	1	2.0 V	2.0 V	-0.4 mA	4.5 V	QA QB QC QD QE QF QG QH	V								
			V _{OL}	2														
		3007	V _{IC}	3	0.8 V	0.8 V	8 mA	0.4 V	QA QB QC QD QE QF QG QH	V								
			III.1	4														
		3009	III.2	5														
			IH1	6	0.4 V	0.4 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V
			IH2	7														
		3010	IH3	8														
			IH4	9														

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	Case A,B,C,D	MIL-STND-883 Test No.	Terminal conditions and limits as for subgroup 1, except $T_A = +125^\circ\text{C}$ and VIC tests are omitted.														Test limits					
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit		
1 $T_A = 25^\circ\text{C}$	Ios	3011	33 34 35 36 37 38 39 40	4.5 V	4.5 V	GND	GND	GND	GND	A	4.5 V						5.5 V	QA QB QC QD QE QF QG QH	-10	-27.5	mA		
				Icc1	3005	41	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	44	54			
2	Same tests, terminal conditions and limits as for subgroup 1, except $T_A = +125^\circ\text{C}$ and VIC tests are omitted.																						
	Same tests, terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ\text{C}$ and VIC tests are omitted.																						
3	3014	43	A	A	L	L	L	L	L	L	L	L	L	L	L	L	4.5 V						
7 $T_A = 25^\circ\text{C}$	Truth table test 5/	44	45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60																				
4	3014	43	A	A	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D		1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits
			Input serial A	Input serial B	QA	QB	QC	QD	GND	Clock	Clear	QE	QF	QG	QH	VCC	Min.	Max.		
7	3014	Truth table test 5/	79	A	A	L	L	L	L	GND	B	A	L	L	L	4.5 V				
TA = 25°C 3/ 6/			80			H	L	H			A	B	A	B	A					
			81				L				A	B	A	B	A					
			82					H			A	B	A	B	A					
			83								A	B	A	B	A					
			84								A	B	A	B	A					
			85								A	B	A	B	A					
			86								A	B	A	B	A					
			87								A	B	A	B	A					
			88								A	B	A	B	A					
			89								A	B	A	B	A					
			90								A	B	A	B	A					
			91								A	B	A	B	A					
			92								A	B	A	B	A					
			93								A	B	A	B	A					
			94								A	B	A	B	A					
			95								A	B	A	B	A					
			96								A	B	A	B	A					
			97								A	B	A	B	A					
			98								A	B	A	B	A					
			99								A	B	A	B	A					
			100								A	B	A	B	A					
			101								A	B	A	B	A					
			102								A	B	A	B	A					
			103								A	B	A	B	A					
			104								A	B	A	B	A					
			105								A	B	A	B	A					
			106								A	B	A	B	A					
			107								A	B	A	B	A					
			108								A	B	A	B	A					
			109								A	B	A	B	A					
			110								A	B	A	B	A					
			111								A	B	A	B	A					
			112								A	B	A	B	A					
			113								A	B	A	B	A					
			114								A	B	A	B	A					
			115								A	B	A	B	A					
			116								A	B	A	B	A					
			117								A	B	A	B	A					
			118								A	B	A	B	A					
			119								A	B	A	B	A					
			120								A	B	A	B	A					
			121								A	B	A	B	A					
			122								A	B	A	B	A					
			123								A	B	A	B	A					
			124								A	B	A	B	A					
			125								A	B	A	B	A					
			126								A	B	A	B	A					
			127								A	B	A	B	A					
			128								A	B	A	B	A					

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	Test No.	Test limits														
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	Unit
7	$T_A = 25^\circ C$	Truth table test	3014	129	B	H	H	H	H	GND	Clock	Clear	QE	QF	QG	QH	VCC	4.5 V	
				130	B	H	H	L					A						
				131															
				132															
				133															
				134															
				135															
				136															
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				158															
				159															
				160															
				161															
				162															
				163															
8					Repeat subgroup 7 at $T_A = 125^\circ C$ and $T_A = -55^\circ C$.														
9		f_{MAX} $T_A = 25^\circ C$	(Fig 8)	164	IN	IN	OUT	OUT	OUT	GND	IN	IN	OUT	5.0 V	Q_H	11	MHz		
		t_{PHL1}	(Fig 8)	165											Q_A	12	ns		
				166											Q_B				
				167											Q_C				
				168											Q_D				
				169											Q_E				
				170											Q_F				
				171											Q_G				
				172											Q_H				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	Test No.												Test limits			
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min
9 TA = 25°C	tPLH2	3003 (Fig 8)	173 174 175 176 177 178 179 180	IN OUT OUT OUT OUT OUT OUT OUT	Q _A Q _B Q _C Q _D	Q _A Q _B Q _C Q _D	GND GND GND GND	Clock Clock Clear Clear	IN 4.5 V OUT OUT	QE QE	Q _F Q _G	Q _H V _{CC}	5.0 V 5.0 V	QA QB QC QD QE QE QF QG QH	10 10	30 30	ns ns		
	tPHL2		181 182 183 184 185 186 187 188	OUT OUT OUT OUT OUT OUT OUT OUT						OUT OUT OUT OUT OUT OUT OUT OUT	OUT OUT OUT OUT OUT OUT OUT OUT	OUT OUT OUT OUT OUT OUT OUT OUT					37		
10 TA = 125°C	fMAX (Fig 8)	tPLH1 (Fig 8)	190 191 192 193 194 195 196 197	OUT OUT OUT OUT OUT OUT OUT OUT						GND IN OUT OUT					QH	9	MHz		
	tPLH2		198 199 200 201 202 203 204 205	IN OUT OUT OUT OUT OUT OUT OUT						IN 4.5 V OUT OUT					QA QB QC QD QE QF QG QH	12 12	63 ns		
	tPHL2		206 207 208 209 210 211 212 213	OUT OUT OUT OUT OUT OUT OUT OUT						OUT OUT OUT OUT OUT OUT OUT OUT					QA QB QC QD QE QF QG QH	10 10	42 42		
11																			

1/¹ A = normal clock pulse, except for subgroups 7 and 8 (see 3/).

2/² B = momentary GND, then 4.5 V to clear register prior to test, except for subgroups 7 and 8 (see 3/).

3/³ For subgroups 7 and 8, A = V_{CC} and B = GND.

4/⁴ Output voltages shall be either:

(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or

(b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

5/⁵ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

6/⁶ Only a summary of attributes data is required.

7/⁷ For device type 03, with schematics incorporating 4 kΩ base resistors, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.

For schematics incorporating 6 kΩ base resistors, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.

8/⁸ For device type 03, schematic circuits A, C, D, E, and F, the minimum and maximum limits shall be -0.7 and -1.8 mA, respectively.

For schematic circuit B, the minimum and maximum limits shall be -0.8 and -2.8 mA, respectively.

9/⁹ For device type 03, schematic circuits A, C, D, E, and F, the maximum limit shall be 40 uA.

For schematic circuit B, the maximum limit shall be 80 uA.
For device type 03, schematic circuits A, C, D, E, and F, the maximum limit shall be 200 uA.
For schematic circuit B, the maximum limit shall be 100 uA.

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STRU-833 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Clock inhibit	VCC	Meas. terminal	Test limits	
		Test No.	Shift load	Clock	E	F	G	H	\bar{Q}_H	GND	Q_H	Serial input	A	B	C	D			4.5 V	QH	2.4	V		
1		V _{OH} V _{OL}	3008 3008 3007 3007	1 2	0.8 V				2.0 V	0.8 V	-8 mA								QH	2.4				
T _A = 25°C		V _{OH} V _{OL}	3008 3007	3 4					2.0 V	16mA									QH	2.4				
	VIC		5		-12mA				0.8 V	16mA														
			6			-12mA																		
			7				-12mA																	
			8					-12mA																
			9						-12mA															
			10							-12mA														
			11								-12mA													
			12									-12mA												
			13										-12mA											
			14											-12mA										
			15												-12mA									
			16													-12mA								
IIL1		3009	17		0.4 V	4.5 V													4.5 V	5.5 V				
IIL2			18																					
			19																					
			20																					
			21																					
			22																					
			23																					
			24																					
			25																					
			26																					
			27																					
IIL3			28																					

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E _L , F Test No.	Shift lead	Clock	E	F	G	H	Q _H	GND	Q _H	Serial input	A	B	C	D	VCC	Meas. terminal				
																			Min	Max	Unit		
1 T _A = 25°C	I _{H1}	3010	29		GND						GND		2.4 V						5.5 V	2.4 V			
			30	5.5 V																40	μ A		
			31																				
			32																				
			33																				
			34																				
			35	2.4 V																			
			36		2.4 V																		
			37			2.4 V																	
			38				2.4 V																
			39	GND	2.4 V																		
			40																				
	I _{H2}		41	GND															5.5 V				
			42	5.5 V															5.5 V				
			43																5.5 V				
			44																5.5 V				
			45																5.5 V				
			46																5.5 V				
			47																5.5 V				
			48																5.5 V				
			49	GND	5.5 V														5.5 V				
			50		2.4 V	GND													5.5 V				
	I _{H3}		51																GND				
			52		5.5 V	GND													GND				
	I _{H4}		53	C ₁	4.5 V														GND				
			54	C ₁	4.5 V														4.5 V				
	I _S		55	C ₁	4.5 V	4.5 V													4.5 V				
	I _{CC}		3011																4.5 V				
			3005																4.5 V				
2																			4.5 V				
3																			4.5 V				
																			4.5 V				
																			4.5 V				
	T _A = 25°C 2/5/	3014	56	B	B	B	B	B	B	H	GND	L	A	B	B	B	B	4.5 V					
			57	A	B	B	A	B	B	A													
			58																				
			59																				
			60																				
			61																				
			62																				
			63																				
			64																				
			65																				
			66																				
			67																				
			68																				
			69																				

Same tests, terminal conditions and limits as for subgroup 1, except T_A = +125°C and VIC tests are omitted.

Same tests, terminal conditions and limits as for subgroup 1, except T_A = -35°C and VIC tests are omitted.

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		
																				Min	Max	Unit
7 $T_A = +25^\circ C$ 2/ 5/	3Q14	Truth table test 4/	70	A	A	A	A	A	A	H	H	L	L	A	A	A	A	A	4.5 V			
			71																			
			72																			
			73																			
			74																			
			75																			
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			120																			

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See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MLL- STD-883 method	Case E, F	Shift load	Clock	E	F	G	H	\bar{Q}_H	GND	Q_H	Serial input	A	B	C	D	Clock inhibit	VCC	Meas. terminal	Test limits			
																					Min	Max	Unit	
7	Truth table test <u>4/</u>	3Q14	121	A	A	A	A	A	A	L	GND	H	B	A	A	A	A	B	4.5 V					
$T_A = 25^\circ C$	$T_A = 2/5/$		122	A	B	A				H		L	A											
			123							H		L	B											
			124							H		L	B											
			125							H		L	B											
			126							H		L	B											
			127							H		L	B											
			128							H		L	B											
			129							H		L	B											
			130							H		L	B											
			131							H		L	B											
			132							H		L	B											
			133							H		L	B											
			134							H		L	B											
			135							H		L	B											
			136							H		L	B											
			137							H		L	B											
			138							H		L	B											
			139							H		L	B											
			140							H		L	B											
			141							H		L	B											
			142							H		L	B											
			143							H		L	B											
			144							H		L	B											
			145							H		L	B											
			146							H		L	B											
			147							H		L	B											
			148							H		L	B											
			149							H		L	B											
			150							H		L	B											
			151							H		L	B											
			152							H		L	B											
			153							H		L	B											
			154							H		L	B											
			155							H		L	B											
			156							H		L	B											
			157							H		L	B											
			158							H		L	B											
			159							H		L	B											
			160							H		L	B											
			161							H		L	B											
			162							H		L	B											
			163							H		L	B											
			164							H		L	B											
			165							H		L	B											
			166							H		L	B											
			167							H		L	B											
			168							H		L	B											
			169							H		L	B											
			170							H		L	B											
			171							H		L	B											

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See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits						
			Shift load	Test No.	Clock	E	F	G	H	\bar{Q}_H	GND	Q_H	H	B	A	A	B	C	D	VCC	Meas. terminal	Min	Max	Unit			
7 $T_A = 25^\circ C$ <u>2/</u> <u>5/</u>	3014	3014	172	A	B	A	A	A	A	L	GND	H	B	A	A	A	A	B	4.5 V								
	Truth table test		173																								
			174																								
			175																								
			176																								
			177																								
			178																								
			179																								
			180																								
			181																								
			182																								
			183																								
			184																								
			185																								
			186																								
			187																								
8		Repeat subgroup 7 at $T_A = +125^\circ C$ and $T_A = -55^\circ C$.	188	IN	IN	GND	GND	GND	GND	GND	IN	GND	OUT	IN	GND	GND	GND	GND	GND	GND	GND	GND	5.0 V	QH	18	MHz	
			189	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	Shift-QH	6	35 ns	
			190	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	IN	IN	IN	IN	IN	IN	IN	IN	IN	Shift-QH	7	44 ns	
			191	5.0 V	5.0 V	IN	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Clock-QH	5	28 ns	
			192	5.0 V	5.0 V	IN	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Clock-QH	6	35 ns	
			193	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	5	21 ns	
			194	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	7	21 ns	
			195	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	6	31 ns	
			196	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	6	31 ns	
9		fMAX (Fig 9)	197	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	IN	IN	IN	IN	IN	IN	IN	IN	IN	QH	14 MHz		
		tPLH1 (Fig 9)	198	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Shift-QH	10	40 ns
		tPLH1 (Fig 9)	199	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Shift-QH	11	60 ns
		tPLH2	200	5.0 V	5.0 V	IN	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Clock-QH	6	37 ns
		tPLH3	201	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clock-QH	5	47 ns	
		tPLH4	202	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Clock-QH	10	47 ns	
10		fMAX (Fig 9)	197	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	Shift-QH	10	40 ns
		tPLH1 (Fig 9)	198	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Shift-QH	11	60 ns
		tPLH1 (Fig 9)	199	IN	IN	GND	GND	GND	GND	GND	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Shift-QH	11	60 ns
		tPLH2	200	5.0 V	5.0 V	IN	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	Clock-QH	5	47 ns
		tPLH3	201	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	11	54 ns	
		tPLH4	202	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	10	54 ns	
		tPLH4	203	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	10	54 ns	
		tPLH4	204	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	10	54 ns	
		tPLH4	205	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	H - QH	10	54 ns	
11																											

1/ $C =$ after all other input conditions, but prior to measurement, apply momentary GND, then 4.5 V.

2/ For subgroups 7 and 8, A = VCC and B = GND.

3/ Output voltages shall be either:

(a) $H = 2.4 V$ minimum and $L = 0.4 V$ maximum when using a high speed checker double comparator.

(b) $H \geq 1.5 V$ and $L \leq 1.5 V$ when using a high speed checker single comparator.

4/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

5/ Only a summary of attributes data is required.

6/ For device type 04, schematics incorporating a 4 k Ω base resistor in the clock input circuit, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively. For schematics incorporating a 6 k Ω base resistor in the clock input circuit, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.

TABLE III. Group A inspection for device type 05.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits	
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S ₀	S ₁	Clock	Q _D	Q _B	Q _A	V _{CC}	Min	Max	Unit	
1 $T_A = 25^\circ C$	V_{0H}	3006	1	2.0 V		2.0 V	2.0 V	2.0 V			GND	2.0 V	2.0 V	A /		-0.8 mA	4.5 V	Q _A	2.4	v		
	V_{0L}	3007	5			0.8 V	0.8 V	0.8 V							-0.8 mA		-0.8 mA		Q _B			
			6																Q _C			
			7																Q _D	0.4	v	
			8																			
	V_{IC}		9	-12 mA																		
			10		-12 mA																	
			11			-12 mA																
			12				-12 mA															
			13					-12 mA														
			14						-12 mA													
			15							-12 mA												
			16								-12 mA											
			17									-12 mA										
			18										-12 mA									
	I_{IL1}	3009	19	0.4 V																		
			20	0.4 V																		
			21		0.4 V																	
			22			0.4 V																
			23				0.4 V															
			24					0.4 V														
			25						0.4 V													
	I_{IL2}		26																			
	I_{IL2}		27																			
	I_{IL3}		28	5.5 V																		

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	Input A	Input B	Input C	Input D	Shift left	GND	S ₀	S ₁	Clock	Q _D	Q _C	Q _B	Q _A	v _{CC}	Meas. terminal	Test limits			
																											Min	Max	Unit
1 $T_A = 25^\circ\text{C}$	I _{TH1}	3010	29	2.4 V												GND									5.5 V	Clear	40	μA	
			30		2.4 V																				Shift R				
			31			2.4 V																			Input A				
			32				2.4 V																		Input B				
			33					2.4 V																	Input C				
			34						2.4 V																Input D				
			35							2.4 V															Shift L				
			36								2.4 V														S ₀				
			37									2.4 V													S ₁				
			38										2.4 V												Clock				
	I _{TH2}		39	5.5 V																					100	Clear			
			40		5.5 V																				Shift R				
			41			5.5 V																			Input A				
			42				5.5 V																		Input B				
			43					5.5 V																	Input C				
			44						5.5 V																Input D				
			45							5.5 V															Shift L				
			46								5.5 V														S ₀				
			47									5.5 V													S ₁				
			48										5.5 V												Clock				

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S ₀	S ₁	Clock	Q _D	Q _B	Q _C	Q _A	V _{CC}	GND	5.5 V	QA	QB	QC	QD	V _{CC}	Meas. terminal	Min	Max	Unit	Test limits	
1 TA = 25°C	LOS	3011	49	5.5 V																																	
	ICC	3005	50		5.5 V																																
2																																					
3																																					
7 TA = 25°C 3/6/	3014	54																																			
	Truth table test 5/		55																																		
			56																																		
			57																																		
			58																																		
			59																																		
			60																																		
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See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S ₀	S ₁	Clock	Q _D	Q _C	Q _B	Q _A	V _{CC}	Min	Max	Unit	
7 $T_A = 25^\circ C$ $\underline{3}/\underline{6}/$	3014	Truth table test 5/	99	A	B	B	B	B	B	A	GND	B	A	A	L	L	L	L	5.0 V				
			100																				
			101																				
			102																				
			103																				
			104																				
			105																				
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			107																				
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			118																				
			119																				
			120																				
			121																				
			122																				
			123																				
8			Repeat subgroup 7 at $T_A = 125^\circ C$ and $T_A = -55^\circ C$.																				
9 $T_A = 25^\circ C$	t _{MAX} (Fig 10)	3003 (Fig 10)	124	B	IN	GND	GND	GND	GND	5.0 V	5.0 V								OUT	OUT	OUT	OUT	OUT
	t _{PHL1}		125	IN		5.0 V	5.0 V	5.0 V	5.0 V														
	t _{PLH1}		126																				
	t _{PHL2}		127																				
	t _{PLH2}		128																				
			129	B		5.0 V	IN	5.0 V	IN														
			130			5.0 V	5.0 V	5.0 V	5.0 V														
			131			5.0 V	5.0 V	5.0 V	5.0 V														
			132			5.0 V	5.0 V	5.0 V	5.0 V														
			133	5.0 V		IN	5.0 V	5.0 V	5.0 V	IN													
			134			5.0 V	5.0 V	5.0 V	5.0 V														
			135			5.0 V	5.0 V	5.0 V	5.0 V														
			136			5.0 V	5.0 V	5.0 V	5.0 V														

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Meas. terminal	Test limits
			Test No.	Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	GND	S ₀	S ₁	Clock	Q _D	Q _C	Q _B	Q _A	V _{CC}	
10 TA = 125°C	f _{MAX} t _{PHL1}	(Fig 10) 3003 (Fig 10)	1.37 1.38 1.39 1.40 1.41	B IN	IN	GND 5.0 V	GND 5.0 V	GND 5.0 V	GND 5.0 V									OUT	5.0 V	QA	9 MHz
	t _{PILH2}		1.42 1.43 1.44 1.45	B IN	IN	5.0 V 5.0 V 5.0 V 5.0 V	IN 5.0 V 5.0 V 5.0 V	IN 5.0 V 5.0 V 5.0 V	IN 5.0 V 5.0 V 5.0 V								OUT	OUT	OUT	OUT	Clear QA Clear QB Clear QC Clear QD
	t _{PHL2}		1.46 1.47 1.48 1.49	5.0 V IN	IN	5.0 V 5.0 V 5.0 V 5.0 V								OUT	OUT	OUT	OUT	Clock QA Clock QB Clock QC Clock QD			
																					36 ns
11																					44

1/₂/ A = normal clock pulse, except for subgroup 7 and 8 (see 3/).

2/₃/ B = momentary GND, then V_{IN} (except for subgroups 7 and 8). For subgroups 1, 2 and 3, V_{IN} = V_{CC}; for subgroups 9, 10 and 11, V_{IN} = 3.0 V minimum (see figure 10).

3/₄/ For subgroups 7 and 8, A = V_{CC} and B = GND.

4/₅/ Output voltages shall be either:

(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or

(b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

5/₆/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

6/₇/ Only a summary of attributes data is required.

7/₈/ For device type 05, schematic circuits A and B, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively. For schematic C, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.

TABLE III. Group A inspection for device type 06.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits	
			Test no.	Clear				Input A	Input B	Input C	Input D	GND	Shift/Clock Load	Q _E	Q _B	Q _A	V _{CC}	Meas. terminal	Min	Max	Unit
T _A = 25°C	V _{DH}	3006	1	2.0 V				2.6 V	2.0 V	2.0 V		GND	0.8 V	A 1/		-0.3 mA	4.5 V	Q _A	2.4	V	
			2													-0.8 mA		Q _B			
			3													-0.8 mA		Q _C			
			4													-0.8 mA		Q _D			
			5					0.8 V	0.8 V	0.8 V						-0.8 mA		Q _D			
V _{OL}		3007	6														16 mA		Q _A	0.4	
			7														16 mA		Q _B		
			8														16 mA		Q _C		
			9														16 mA		Q _D		
			10														16 mA		Q _D		
V _{IC}			11	-12 mA														1.5	Clear	J	
			12		-12 mA														K		
			13			-12 mA													A		
			14				-12 mA												B		
			15					-12 mA											C		
			16						-12 mA										D		
			17							-12 mA									Shift/ Load/ Clock		
			18								-12 mA										
I _{IL1}		3009	20	0.4 V													5.5 V		Clear	-0.4	1.3 mA
I _{IL2}			21	GND	0.4 V													J			
			22	B 2/	5.5 V	0.4 V	5.5 V											K			
			23					0.4 V										A			
			24						0.4 V									B			
			25							0.4 V								C			
			26								0.4 V							D			
			27									0.4 V						Shift/ Load/ Clock			
I _{IL3}			28	5.5 V													0.4 V			-0.7	-1.6 mA

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06.- Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 Clear	2 J	3 K	Input A	Input B	Input C	Input D	GND	Shift/Load	Clock	\overline{Q}_0	Q_D	Q_C	Q_B	Q_A	V_{CC}	Meas. terminal	Test limits	Max	Unit
1	I_{IH1}	$T_A = 25^\circ C$	3010	29	2.4 V						GND								5.5 V	Clear	J	40	μA
				30	5.5 V	2.4 V		5.5 V												K			
				31	GND			2.4 V												A			
				32					2.4 V											B			
				33						2.4 V										C			
				34																D			
				35																Shift/Load Clock			
				36																Clear	J	100	
				37																K			
				38																A			
				39																B			
				40																C			
				41																D			
				42																Shift/Load Clock			
				43																			
				44																			
				45																			
				46																			

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits			
																				Min	Max	Unit	
1 $T_A = 25^\circ C$	I _{OS}	3011	47	5.5 V				5.5 V	5.5 V	5.5 V	GND	GND	A							-20	-57	mA	
	I _{CC}	3005	48					49	50	GND	5.5 V	GND	5.5 V	QA	QC	QD							
2	Same tests, terminal conditions and limits as subgroup 1, except $T_A = 125^\circ C$ and VIC tests are omitted.																				63		
3 $T_A = 25^\circ C$ $3 / 6 /$	Truth table test	3014	53	B	B	B	B	B	B	B	GND	A	A	A	H	L	L	L	L	5.0 V			
			54	A				55															
			56					57															
			58					59															
			60					61															
			62					63															
			64					65															
			66					67															
			68					69															
			70					71															
			72					73															
			74					75															
			76					77															
			78					79															
			80					81															
			82					83															
			84					85															
			86					87															
			88					89															
			90					91															

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case E, F		1	2	3	4	5	6	7	8	Shift/ load	Clock	\bar{Q}_D	Q_D	Q_C	Q_B	Q_A	V _{CC}	Meas. terminal	Test limits
			Test No.	Clear	J	K	Input A	Input B	Input C	Input D	GND									Min	Max	Unit
7	Truth table test	3Q14	92	B	A	A	A	A	A	A	GND	B	A	H	L	L	L	L	5.0 V			
			93	A								B	A									
			94	B								B	B									
			95	A								B	B									
			96	A								B	B									
			97	A								B	B									
8	Repeat subgroup 7 at $T_A = 125^\circ\text{C}$ and $T_A = -55^\circ\text{C}$.																					
9	I _{MAX} $T_A = 25^\circ\text{C}$	tPHL1 (Fig 11) 3003 (Fig 11)	98	B	5.0 V	GND	5.0 V	5.0 V	5.0 V	5.0 V	GND	5.0 V	GND	5.0 V	GND	5.0 V	OUT	OUT	OUT	OUT	OUT	ns
			99	IN																		
			100																			
			101																			
			102																			
			103	B																		
			104																			
			105																			
			106																			
			107																			
			108																			
			109																			
			110																			
10	I _{MAX} $T_A = 125^\circ\text{C}$	tPHL1 (Fig 11) 3003 (Fig 11)	111	5.0 V	GND	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	GND	5.0 V	GND	5.0 V	GND	5.0 V	OUT	OUT	OUT	OUT	OUT	ns
			112	IN																		
			113																			
			114																			
			115																			
			116	B																		
			117																			
			118																			
			119																			
			120																			
			121																			
			122																			
			123																			
11	Same tests, terminal conditions and limits as subgroup 10, except $T_A = -55^\circ\text{C}$.																					

1/ A = normal clock pulse, except for subgroups 7 and 8 (see 3/).
2/ B = momentary GND, then IN, except for subgroups 7 and 8. For subgroups 1, 2 and 3, VIN = VCC; for subgroups 9, 10 and 11, VIN = 3.0 V minimum (see figure 11).

3/ For subgroups 7 and 8, A = V_{CC} and B = GND.
4/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H \geq 1.5 V and L \leq 1.5 V when using a high speed checker single comparator.

5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
6/ Only a summary of attributes data is required.

7/ For device type 06, schematic circuits A and B, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively. For schematic circuit C, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 5 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - 1. Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - 2. $T_A = 125^\circ\text{C}$ minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Percent defective allowable (PDA) - The PDA for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for group A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for group A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B and C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Operating life test (method 1005 of MIL-STD-883) conditions, or equivalent:
 - 1. Test condition D or E, using the circuit shown on figure 8, or equivalent.
 - 2. $T_A = 125^\circ\text{C}$ minimum.
 - 3. Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883; end-point electrical parameters shall be specified in table II herein.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Packaging inspection. The sampling and inspection of the preservation-packaging, packing, and container marking shall be in accordance with the requirements of MIL-M-38510, except that the rough handling test shall not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic support.

6.3 Ordering data. Procurement documents should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for packing and packaging.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- i. Requirement for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal)
V_{IN}	- - - - -	Voltage level at an input terminal
V_{IC}	- - - - -	Input clamp voltage
I_{IN}	- - - - -	Current flowing into an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2) and lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification shall functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	5495, 7495
02	5496, 7496
03	54164, 74164
04	54165, 74165
05	54194, 74194
06	54195, 74195

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17

Review activities:
 Army - AR, MI
 Air Force - 11, 85, 99
 NASA - NA
 DLA - ES

Agent:
 DLA - ES

(Project 5962-0339)

User activities:
 Army - SM, WC
 Navy - AS, CG, MC, OS, SH
 Air Force - 19