MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, THYRISTOR (CONTROLLED RECTIFIER), SILICON
TYPES 2N4199 through 2N4206

1. SCOPE

1.1 Scope.- This specification covers the detail requirements for silicon, diffused-junction, PNPN, thyristors for application, particularly, as controlled rectifier, fast pulse-switching devices in compatible equipment circuits. (See 3.4 and 6.2 herein.)

1.2 Outline and dimensions.- See Figure 1 herein.

1.3 Ratings.- (At T_C = +85°C, unless otherwise specified.)

	$P_{(AV)}$	P_{GM}	I_F	$i_{FM(rep)}$	v_{GKM} 2/	v_{KGM} 2/	V_{GNT} 3/	T_J	T_{stg}
	W	W	A	A	v	v	V	°C	°C
Min	1/	---	---	100	6	6	0.2	-65	-65
Max	1/	20	2	---	10	10	---	+100	+150

1/ See Fig. 2 herein. 2/ At T_A = +25°C. 3/ At T_C = +100°C.

1.4 Particular electrical characteristics.-

	V_{FBO}	I_{FBO}	I_{HOO}	I_{GT}	V_{GT}	V_F(on)	i_{RBOM}	v_{RM}	Switching 3/ t_r
	Vdc	mAdc	mAdc 1/	mAdc 2/	Vdc 2/	Vdc 2/	mAdc	vdc	nsec
2N4199	300	2	5	50	1.5	25	4	50	200
2N4200	400	2	5	50	1.5	25	4	50	200
2N4201	500	2	5	50	1.5	25	4	250	150
2N4202	600	2	5	50	1.5	25	4	250	130
2N4203	700	2	5	50	1.5	25	4	250	100
2N4204	800	2	5	50	1.5	25	4	250	100
2N4205	900	2	5	50	1.5	25	4	250	100
2N4206	1000	2	5	50	1.5	25	4	250	100

1/ Minimum. 2/ Maximum. 3/ Also, for all types: t_d=200 nsec, max.
t_{off}=15 usec, max.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-S-19500	Semiconductor Devices, General Specification For

STANDARDS

MILITARY

MIL-STD-202	Test Methods For Electronic and Electrical Component Parts
MIL-STD-750	Test Methods For Semiconductor Devices

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

2.2 Other publications.- The following document forms a part of the specification to the extent specified herein. Unless otherwise indicated, the issue in effect on date of invitation for bids or request for proposal shall apply.

NATIONAL BUREAU OF STANDARDS

Handbook H28 Screw-Thread Standards for Federal Services.

(Application for copies should be addressed to the Superintendent of Documents, Government Printing Office, Washington, D. C. 20402.

3. REQUIREMENTS

3.1 Requirements.- Requirements for the thyristor shall be in accordance with Specification MIL-S-19500 and as otherwise specified herein.

3.2 Abbreviations and symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500, and as follows:

dV_F/dt . . . . . rate of forward-voltage rise

P(AV) . . . . . average power dissipated by the thyristor while operating under specified conditions

3.3 Design and construction.- The thyristor shall be of the design, construction, and physical dimensions specified on Figure 1.

3.3.1 Terminal arrangement.- The terminal arrangement on the thyristor shall be as indicated in Figure 1.

3.3.2 Operating position.- The thyristor shall be capable of proper operation in any position.

3.4 Performance characteristics.- The thyristor performance characteristics shall be as specified in Tables I, II, and III herein. Except where specifically differentiated for respective thyristor types (see 1.3, 1.4, and Tables I, II, and III herein), the performance requirements, including characteristics, ratings, and test conditions, apply equally to all thyristor types covered herein.

3.5 Marking.- Except as otherwise specified herein, marking shall be in accordance with Specification MIL-S-19500. If any specification-requirements waiver has been granted, the product-identification marking shall consist of the "classification" type designation only. The "manufacturer's identification" and "country of origin" may, at option of the manufacturer, be omitted from being marked directly on the semiconductor device covered herein.

4. QUALITY ASSURANCE PROVISIONS

4.1 General.- Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.1.1 Inspection lot.- Applicable to the semiconductor device(s) covered herein, the term "Inspection lot" shall be as defined in paragraph 4.3.2.1 of Specification MIL-S-19500 except that the 6-week-period time limitation stipulated therein shall be considered as not compulsory.

4.1.1.1 Preconditioned-unit constituency of inspection lots.- All semiconductor devices covered herein, in each inspection lot presented for Quality Conformance inspection, shall have been subjected to the following preconditioning:

(a) Operated for 4 hours, minimum, under the following steady-state conditions:

(1) $T_C = +100° \, ^{+5°}_{-0°} C$

(2) V_{FBO} = rating pertinent to the respective thyristor.

(b) Subjected, after (a) above to the following end-point test(s):

(1) D.C. Forward Blocking (Leakage) Current test as specified in Table I, subgroup 4, herein.

(b) All thyristors that fail to meet the above process-conditioning and testing requirements shall be removed from the respective lot, and the test-failure identity and quantity removed shall be recorded in the permanent lot history. Where the total of failures encountered exceeds 20% of the lot quanitity, this shall be considered cause for rejection of the entire lot. (See (d), immediately below.)

(d) The manufacturer shall maintain and make available for perusal and review at any time, throughout a minimum period of 3 years, to the authorized Government representative or other contracting customer concerned, complete lot-by-lot records of the thyristors subjected to, and the results found for, the process-conditioning and testing requirements herein. (See 6.3 herein.)

(e) The preconditioning and testing requirements specified above need not be repeated if previously effected during standard production procedures by manufacturer (see (d), immediately above), and if such compliance is determined as acceptable beforehand by the responsible Government representative.

4.2 Qualification and Acceptance Inspection.- Qualification and Acceptance Inspection shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions, and as otherwise specified herein. Groups A, B, and C inspection shall consist of the examinations and tests specified in Tables I, II, and III respectively, herein. Acceptance Inspection shall include inspection of Preparation for Delivery. (See 5.1 herein.)

4.2.1 Qualification inspection of lots containing multiple thyristor types. - Where the qualification inspection lot is made up of sublots, the constituency of lot sample(s), subjection of sample(s) to tests, and lot evaluation will be acceptable in accordance with a and b below:

a. For the highest-voltage (V_{FBO}) type in the lot, the sample size shall be the applicable statistical-sampling, tightened-LTPD quantity of units (per Table C-1 in Specification MIL-S-19500). The sample units shall be subjected to customary Group A, B, and C testing. Relative to failures encountered as result of tests, the following shall be cause for rejection of the entire lot and denial of qualification.

   (1) More than two (2) failures in Group A tests.

   (2) More than two (2) failures in Group B and C tests, exclusive of Life tests.

   (3) More than one (1) failure in each Life test. Hereto, the sample quantity shall be based upon a sample size for an Acceptance Number of 1, per Table C-1 of Specification MIL-S-19500.

b. For each lower-voltage (V_{FBO}) type (below the highest voltage type - - see a, above) in the lot, ten (10) sample units for each voltage-level type shall be subjected to Group A and C tests only. Relative to failures encountered as a result of tests, the following shall be cause for rejection of the entire lot and denial of qualification.

   (1) More than one (1) failure within each sample representing any particular lower-voltage type.

   (2) More than four (4) failures, combined, in instance where four (4) or more sublot samples (representing respective lower-voltage types) have been subjected to tests.

4.2.2 Quality conformance inspection of lots containing multiple thyristor types. - For lots containing more than one thyristor type covered herein, subjection of adequate samples on a sublot basis to tests in accordance with a, b, c, and d, below, will be acceptable.

a. The sublot containing the highest-voltage type shall be subjected to Group A and B, and Group C test (when the Group C tests are incumbent to be performed).

b. The sublot containing the highest-volume type shall be subjected to Group A and B, and Group C testing (when the Group C tests are incumbent to be performed.

c. Where the coincidence of the highest-volume type being also the highest-voltage type occurs in a presented lot, only one sublot need be subjected to tests in fulfillment of the requirements of both a and b above.

d. The sublot(s) containing thyristor types other than those concerned in a and b, above, shall be subjected to all Group A tests and to all Group C tests (when the Group C tests are incumbent to be performed). Hereto, the manufacturer may exercise an option to subject a sample of ten (10) each units for each sublot through all Group A tests and through all Group C tests (when Group C tests are incumbent to be performed), except that the following evaluation criteria shall pertinently apply:

   (1) More than one (1) failure in any such sublot sample shall be cause for rejection of the lot; or

   (2) Where four or more such sublot samples are subjected to tests, the incidence of more than four (4) failures for all the sublots tested shall be cause for rejection of the lot.

4.2.3 Specified LTPD for subgroups.- The LTPD specified for a subgroup in Table I, II, and III herein shall apply for all of the tests, combined, in the subgroup.

4.2.4 Group B-Group C life test samples.- Samples that have been subjected to Group B, 340-hour life test may be continued on test for 1000 hours in order to satisfy Group C life test requirements. These samples shall be predesignated, and shall remain subject to the Group C 1000-hour acceptance evaluation after they have passed the Group B, 340-hour acceptance criteria; hereto, the following shall apply:

a. The cumulative total of failures found during 340-hour test and during the subsequent interval up to 1000 hours on these samples shall be computed for 1000-hour acceptance criteria.

4.2.5 Group C testing.- Unless otherwise specified, Group C tests shall be performed on the initial lot and thereafter on a lot every 6 months. (See Table III herein.) The contractor shall, throughout the course of a contact or order, permit the Government representative to scrutinize all test data and findings covering manufacturer's test program on Group C characteristics and parameters for the product concerned. Upon determination by the Government inspector (in advance of Group C, 6-month, test results) that Group C parameters are not being adequately met, the Government inspector may require lot-by-lot inspection, normally for a minimum of 3 consecutive lots, to be performed for required Group C tests.

4.2.6 Disposition of sample units.- Sample units that have been subjected to Group B, Subgroup 2, and Group C, Subgroup 4 tests shall not be delivered on the contact or order. Sample units that have been subjected to and have passed Group B, Subgroups 1, 3, 4, and 5 tests and Group C, Subgroup 1, 2, 3, 5, and 6 tests, (these tests to be considered non-destructive), may be delivered on the contract or order provided that, after Group B and Group C inspection is terminated, those sample units are subjected to and pass Group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.3 Particular examination and test requirements.-

4.3.1 Interval for End-Point Test measurements.- All applicable End-Point Test measurements shall be performed after sample units have been subjected to required physical-mechanical or environmental test(s), in accordance with the following time-delay limitations:

(a) For Qualification inspection: within 24 hours.

(b) For Quality Conformance inspection: within 96 hours; however, at discretion of the Government inspector, a more protracted interval may be allowed.

4.3.2 Mechanical damage resulting from tests.- Except for intentionally deforming, mutilating, or dismembering mechanical-stress tests to which samples are subjected, there shall be no evidence of mechanical damage to any sample unit as a result of any of the Group A, B, or C tests. (See 4.3.3 below.)

4.3.3 Chipped-paint damage resulting from tests.- Where units having a paint finish have had chipping of paint result from mounting procedure or other application of test implements, the manifestation of chipping of paint shall not be cause for indication of the unit(s) as a test failure. Any refinishing of such units (other than those subjected to destructive tests) relative to acceptability for shipment on contract or order, shall satisfy applicable "workmanship" requirements in Specification MIL-S-19500 and shall be acceptable to the responsible inspection authority.

4.3.4 Turn-off time (pulse, forward) test.- The device (thyristor under test) shall be triggered "ON" and remain conducting until the equilibrium forward anode current has been reached. Then the anode current shall be abruptly reduced to zero, and a negative gate bias applied. During the application of the forward blocking voltage at 250 V/uSec, max., the device must remain in the "OFF" state. Turn-off time is then measured as the time interval between the 10% decay of forward anode current and the instant when forward blocking voltage may be applied. The circuit in Figure 5 herein, or equal, shall be used to perform this measurement.

4.3.5 Gate non-trigger voltage test.- Test procedure shall be based upon the following description: Gate non-trigger voltage is the maximum value of gate voltage which may be applied without causing the device to switch from the blocking state to the "ON" state.

4.3.6 Durability of terminal lugs.- The lug ends of all terminals shall remain intact on terminals throughout all physical, mechanical, and environmental tests herein.

4.3.7 Terminal Strength (Stud Torque) test.- Acceptance criteria after the stud torque for external threaded parts (dimension of Figure 1 herein) shall be in accordance with Handbook H-28.

4.3.8 Repetitive Pulsing Life test.- The thyristors under test shall be subjected to the prescribed forward pulses at the prescribed repetition rate. Case temperature shall be maintained at the level specified, throughout the test.

Table I. Group A inspection.

Test Method per MIL-STD-750	Examination or test 1/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		5				
2071	Visual and mechanical examination	---		---	---	---	---
	Subgroup 2		7				
4221	Gate trigger current	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		I_{GT}	---	50	mAdc
4221	Gate trigger voltage	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		V_{GT}	---	1.5	Vdc
4201	Holding current	Gate open		I_{HOO}	5	---	mAdc
---	Dynamic forward "on" voltage	Test circuit per Fig. 3 herein; I_F(pulse) = 30 A I_{GK}(pulse) = 200 mA *min* @ t_p = 1.5 ± 0.5 usec $t_r(i_{gk})$ = 20 nsec max Rep.rate ≤ 100 pps V_1 = adjust V_{FBXM} per Fig. 3 data		V_F	---	25	v

Table I. Group A inspection. - (Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 3		10				
---	Forward-current delay time	Test circuit per Fig. 4 herein; I_F(pulse) = 30 A; i_{GK}(pulse) = 200 mA min @ t_p = 1.5 ± 0.5 usec; $t_r(i_{gk})$ = 20 nsec max; Rep.rate ≤ 100 pps; V_1 = adjust V_{FBXM} per Fig. 3 data		t_d	---	200	nsec
---	Forward-current rise time:	Test circuit per Fig. 4 herein; I_F(pulse) = 30 A; i_{GK}(pulse) = 200 mA min @ t_p = 1.5 ± 0.5 usec; $t_r(i_{gk})$ = 20 nsec max; Rep.rate ≤ 100 pps; V_1 = adjust V_{FBXM} per Fig. 3 data		---	---	---	---
	2N4199			t_r	---	200	nsec
	2N4200			t_r	---	200	nsec
	2N4201			t_r	---	150	nsec
	2N4202			t_r	---	130	nsec
	2N4203			t_r	---	100	nsec
	2N4204			t_r	---	100	nsec
	2N4205			t_r	---	100	nsec
	2N4206			t_r	---	100	nsec

Table I. Group A inspection. - (Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 3 - (Cont'd)						
2/	Turn-off time (pulse, forward)	Test circuit per Fig. 5 herein; T_C = +85°C; I_F(pulse) = 30 A @t_p = 10 usec V_{GK} = -6 V (during OFF state only) dV_F/dt=250 v/usec		t_{off}	---	20	usec
---	Turn-off time (conventional)	Test circuit per Fig. 6 (or equiv. circuit) I_F(pulse) = 2 A PW = 100 usec		t_{off}	---	15	usec
	Subgroup 4			10			
4206	D.C. forward blocking (leakage) current:	T_C = +100°C Bias Cond. D					
	2N4199	V_{FBO} = 300 V		I_{FBO}	---	2	mAdc
	2N4200	V_{FBO} = 400 V		I_{FBO}	---	2	mAdc
	2N4201	V_{FBO} = 500 V		I_{FBO}	---	2	mAdc
	2N4202	V_{FBO} = 600 V		I_{FBO}	---	2	mAdc
	2N4203	V_{FBO} = 700 V		I_{FBO}	---	2	mAdc
	2N4204	V_{FBO} = 800 V		I_{FBO}	---	2	mAdc
	2N4205	V_{FBO} = 900 V		I_{FBO}	---	2	mAdc
	2N4206	V_{FBO} = 1000 V		I_{FBO}	---	2	mAdc

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4 - (Cont'd)						
4211	Peak reverse blocking (leakage) current:	T_C = +100°C A. C. meth., Bias Cond. D					
	2N4199	v_{RM} = 50 vdc		i_{RBOM}	---	4	mAdc
	2N4200	v_{RM} = 50 vdc		i_{RBOM}	---	4	mAdc
	2N4201	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
	2N4202	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
	2N4203	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
	2N4204	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
	2N4205	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
	2N4206	v_{RM} = 250 vdc		i_{RBOM}	---	4	mAdc
4221	Gate non-trigger voltage	3/ T_C = +100°C V_1 = 0.2 Vdc V_2 = V_{FBO} (resp. rating for ea. type) R_e = 200 ohms R_L = 1 kohms		V_{GNT}	0.2	---	Vdc
---	Rate of linear forward voltage rise	T_J = +100°C V_{AA} = V_{FBO} (resp. rating for ea. type); 4/		dV_F/dt	250	---	V/usec

1/ See 3.4 and 4.3.3 herein.

2/ See 4.3.4 herein.

3/ See 4.3.5 herein.

4/ See Fig. 5 herein.

Table II. Group B inspection.

Test Method per MIL-STD-750	Examination or test 1/	Conditions 2/	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		10				
2066	Physical dimensions	---		---	---	---	---
	Subgroup 2		15				
2026	Solderability	Omit aging; 3/		---	---	---	---
1051	Temperature cycling	Test Cond. F.		---	---	---	---
1056	Thermal shock (glass strain)	Test Cond. B		---	---	---	---
2036	Terminal strength (stud torque)	Test Cond. D2 Torque=15 lb-in. t=15 sec. 4/		---	---	---	---
2036	Terminal strength (bending stress), cathode terminal	Test Cond. F, Method B Weight = 1 lb t=15 sec.		---	---	---	---
2036	Terminal strength (bending stress), gate terminal	Test Cond. F, Method B Weight=0.5 lb t=15 sec		---	---	---	---
2036	Terminal strength (terminal torque)	Test Cond. D1 5/ Torque=10 oz-in. t=15 sec		---	---	---	---
1021	Moisture resistance	No initial conditioning		---	---	---	---
	End-Point tests:						
4221	Gate trigger current	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		I_{GT}	---	50	mAdc
4221	Gate trigger voltage	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		V_{GT}	---	1.5	Vdc

Table II. Group B inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions 2/	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 2 End-Point tests Cont'd):						
4206	D.C forward blocking (leakage) current:	T_C = +100°C Bias Cond. D					
	2N4199	V_{FBO}= 300 V		I_{FBO}	---	2	mAdc
	2N4200	V_{FBO}=400 V		I_{FBO}	---	2	mAdc
	2N4201	V_{FBO}=500 V		I_{FBO}	---	2	mAdc
	2N4202	V_{FBO}=600 V		I_{FBO}	---	2	mAdc
	2N4203	V_{FBO}=700 V		I_{FBO}	---	2	mAdc
	2N4204	V_{FBO}=800 V		I_{FBO}	---	2	mAdc
	2N4205	V_{FBO}=900 V		I_{FBO}	---	2	mAdc
	2N4206	V_{FBO}=1000 V		I_{FBO}	---	2	mAdc
4211	Peak reverse blocking (leakage) current:	T_C= +100°C A.C.meth., Bias Cond. D					
	2N4199	v_{RM}=50 vdc		i_{RBOM}	---	4	mAdc
	2N4200	v_{RM}=50 vdc		i_{RBOM}	---	4	mAdc
	2N4201	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	2N4202	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	2N4203	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	2N4204	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	2N4205	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	2N4206	v_{RM}=250 vdc		i_{RBOM}	---	4	mAdc
	Subgroup 3		15				
2016	Shock	Non-operating 1500 G 5 blows of 0.5 msec ea. in orientations X1, Y1, Y2 (total = 15 blows)		---	---	---	---

Table II. Group B inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions 2/	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 3-(cont'd)						
2056	Vibration, variable frequency	---		---	---	---	---
2006	Constant acceleration	10.000 G Orientations X1, Y1, Y2					
	End-Point tests: Same as for Subgroup 2 above						
	Subgroup 4		10				
6/	Seal (leak rate)	Test Cond. C, procedure III; Test Cond. A for gross leaks 7/		---	---	10^{-7}	atm cc/sec
	Subgroup 5		7				
1031	High-temperature life (non-operating)	T_{stg} = +150°C t = 340 hrs 8/		---	---	---	---
	End-Point tests:						
4221	Gate trigger current	V_2=7 Vdc R_e = 200 ohms R_L = 100 ohms		I_{GT}	---	60	mAdc
4221	Gate trigger voltage	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		V_{GT}	---	1.6	Vdc

Table II. Group B inspection-(Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions 2/	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 5, End-Point tests (Cont'd).						
4206	D.C. forward blocking (leakage) current:	T_C = +100°C Bias Cond. D					
	2N4199	V_{FBO}=300V		I_{FBO}	---	3	mAdc
	2N4200	V_{FBO}=400V		I_{FBO}	---	3	mAdc
	2N4201	V_{FBO}=500V		I_{FBO}	---	3	mAdc
	2N4202	V_{FBO}=600V		I_{FBO}	---	3	mAdc
	2N4203	V_{FBO}=700V		I_{FBO}	---	3	mAdc
	2N4204	V_{FBO}=800V		I_{FBO}	---	3	mAdc
	2N4205	V_{FBO}=900V		I_{FBO}	---	3	mAdc
	2N4206	V_{FBO}=1000V		I_{FBO}	---	3	mAdc
4211	Peak reverse blocking (leakage) current:	T_C = +100°C A.C.meth., BiasCond.D					
	2N4199	v_{RM}=50 vdc		i_{RBOM}	---	6	mAdc
	2N4200	v_{RM}=50 vdc		i_{RBOM}	---	6	mAdc
	2N4201	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc
	2N4202	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc
	2N4203	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc
	2N4204	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc
	2N4205	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc
	2N4206	v_{RM}=250 vdc		i_{RBOM}	---	6	mAdc

Table II. Group B inspection-(Cont'd).

Test Method per MIL-STD-750	Examination or test 1/	Conditions 2/	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 5		10				
9/	Repetitive pulsing life	T_C=+65°C 8/ V_{FBO}=resp. rating for ea. type IF(pulse)=30 Adc @t_p = 2±0.1 usec & prr = 3±0.3 kHz Gate:pulse=200 mAdc @ t_r =20 nsec V_{GK}= -6 Vdc (during OFF state only) t=340 hrs		---	---	---	---
	End-point tests: Same as for Subgroup 4 above						

1/ See 3.4, 4.3.1, and 4.3.3 herein.

2/ See 4.3.6 herein.

3/ Immersion time = 10±1 sec., immersion depth = sufficient to cover entire flatted portion of gate and cathode terminal.

4/ See 4.3.7 herein.

5/ Applied to flat of ea. terminal.

6/ Per Method 112 in Standard MIL-STD-202.

7/ Unpainted units from the pertinent lot may be used for this test.

8/ See 4.2.2 herein.

9/ See 4.3.8 herein.

Table III. Group C inspection. 1/

Test Method per MIL-STD-750	Examination or test 2/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		20				
1001	Barometric pressure, reduced (altitude operation):	Pressure: 3/ Normal mounting t=1 min., minimum		---	---	---	---
	Measurement during test:						
4206	D.C. forward blocking (leakage) current:	Bias Cond. D					
	2N4199	V_{FBO}=300 V		I_{FBO}	---	2	mAdc
	2N4200	V_{FBO}=400 V		I_{FBO}	---	2	mAdc
	2N4201	V_{FBO}=500 V		I_{FBO}	---	2	mAdc
	2N4202	V_{FBO}=600 V		I_{FBO}	---	2	mAdc
	2N4203	V_{FBO}=700 V		I_{FBO}	---	2	mAdc
	2N4204	V_{FBO}=800 V		I_{FBO}	---	2	mAdc
	2N4205	V_{FBO}=900 V		I_{FBO}	---	2	mAdc
	2N4206	V_{FBO}=1000 V		I_{FBO}	---	2	mAdc
	Subgroup 2		20				
4/	Low-Temperature operation:	$T_A = -65°^{-5°}_{+0°}C$		---	---	---	---
4206	D.C. forward blocking (leakage) current:	Bias Cond. D					
	2N4199	V_{FBO}=300 V		I_{FBO}	---	2	mAdc
	2N4200	V_{FBO}=400 V		I_{FBO}	---	2	mAdc
	2N4201	V_{FBO}=500 V		I_{FBO}	---	2	mAdc
	2N4202	V_{FBO}=600 V		I_{FBO}	---	2	mAdc
	2N4203	V_{FBO}=700 V		I_{FBO}	---	2	mAdc
	2N4204	V_{FBO}=800 V		I_{FBO}	---	2	mAdc
	2N4205	V_{FBO}=900 V		I_{FBO}	---	2	mAdc
	2N4206	V_{FBO}=1000 V		I_{FBO}	---	2	mAdc

Table III. Group C Inspection. 1/ - (Cont'd).

Test Method per MIL-STD-750	Examination or test 2/	Conditions	LTPD	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 2 -(Cont'd)						
	Low Temp. Oper-(Cont'd):						
4221	Gate trigger current	V_2=7 Vdc R_e=200 ohms R_L=100 ohms		I_{GT}	---	100	mAdc
4221	Gate trigger voltage	V_2=7 Vdc R_e=200 ohms R_L= 100 ohms		V_{GT}	---	1.8	Vdc
	Subgroup 3		20				
---	Peak forward gate voltage	Test circuit and test conditions (procedure) per Fig. 7 herein.		v_{GK}	6	10	Vdc
---	Repetitive peak forward current	Pulse width = 10 usec @ prr=60 Hz V_{FBO}=300V, min, applied T_C= +85°C Gate pulse: i_{GK}=200 mAdc t_r=20 nsec, max t =1 sec., min		i_{FM}(rep)	100	---	A
---	Burn-out by pulsing (non-repetitive)	Test circuit and test conditions (procedure) per Fig. 8 herein.		$I_{(pulse)}$	150	---	A

Table III. Group C inspection. 1/ (Cont'd).

Test Method per MIL-STD-750	Examination or test 2/	Conditions	LTPD	Symbol	Limits Min.	Max.	Unit
	Subgroup 3 End-point tests:						
4221	Gate trigger current	V_2 = 7 Vdc R_e = 200 ohms R_L = 100 ohms		I_{GT}	---	60	mAdc
4221	Gate Trigger voltage	V_2=7 Vdc R_e = 200 ohms R_L = 100 ohms		V_{GT}	---	1.6	Vdc
4206	D.C. forward blocking (leakage) current: 2N4199 2N4200 2N4201 2N4202 2N4203 2N4204 2N4205 2N4206	T_C = +100°C Bias Cond. D V_{FBO}=300 V V_{FBO}=400 V V_{FBO}=500 V V_{FBO}=600 V V_{FBO}=700 V V_{FBO}=800 V V_{FBO}=900 V V_{FBO}=1000 V		I_{FBO} I_{FBO} I_{FBO} I_{FBO} I_{FBO} I_{FBO} I_{FBO} I_{FBO}	--- --- --- --- --- --- --- ---	3 3 3 3 3 3 3 3	mAdc mAdc mAdc mAdc mAdc mAdc mAdc mAdc
4211	Peak reverse blocking (leakage) current 2N4199 2N4200 2N4201 2N4202 2N4203 2N4204 2N4205 2N4206	T_C = +100°C A.C. meth., Bias Cond. D v_{RM}= 50 vdc v_{RM}= 50 vdc v_{RM}= 250 vdc v_{RM}=250 vdc v_{RM}=250 vdc v_{RM}=250 vdc v_{RM}=250 vdc v_{RM}=250 vdc		i_{RBOM} i_{RBOM} i_{RBOM} i_{RBOM} i_{RBOM} i_{RBOM} i_{RBOM} i_{RBOM}	--- --- --- --- --- --- --- ---	6 6 6 6 6 6 6 6	mAdc mAdc mAdc mAdc mAdc mAdc mAdc mAdc
	Subgroup 4		20				
1041	Salt atmosphere (corrosion)	---		---	---	---	---

Table III. Group C inspection, 1/ - (Cont'd)

Test Method per MIL-STD-750	Examination or test 2/	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 5		λ=10				
1031	High-temperature life (non-operating)	T_{stg}=+150°C t=1000 hrs 5/	---	---	---	---	---
	End-point tests: Same as for Subgroup 3 above						
	Subgroup 6		λ=15				
1036	Repetitive pulsing life	T_C= +65°C 5/; 6/ V_{FBO}= resp. rating for ea.type iF(pulse)=30 Adc @t_p = 2± 0.1 usec & prr =3± 0.3 kHz Gate: pulse=200 mAdc @ t_r = 20 nsec V_{GK} = -6 Vdc (during OFF state only) t=1000 hrs	---	---	---	---	---
	End-point tests: Same as for Subgroup 3 above						

1/ See 4.2.3 herein

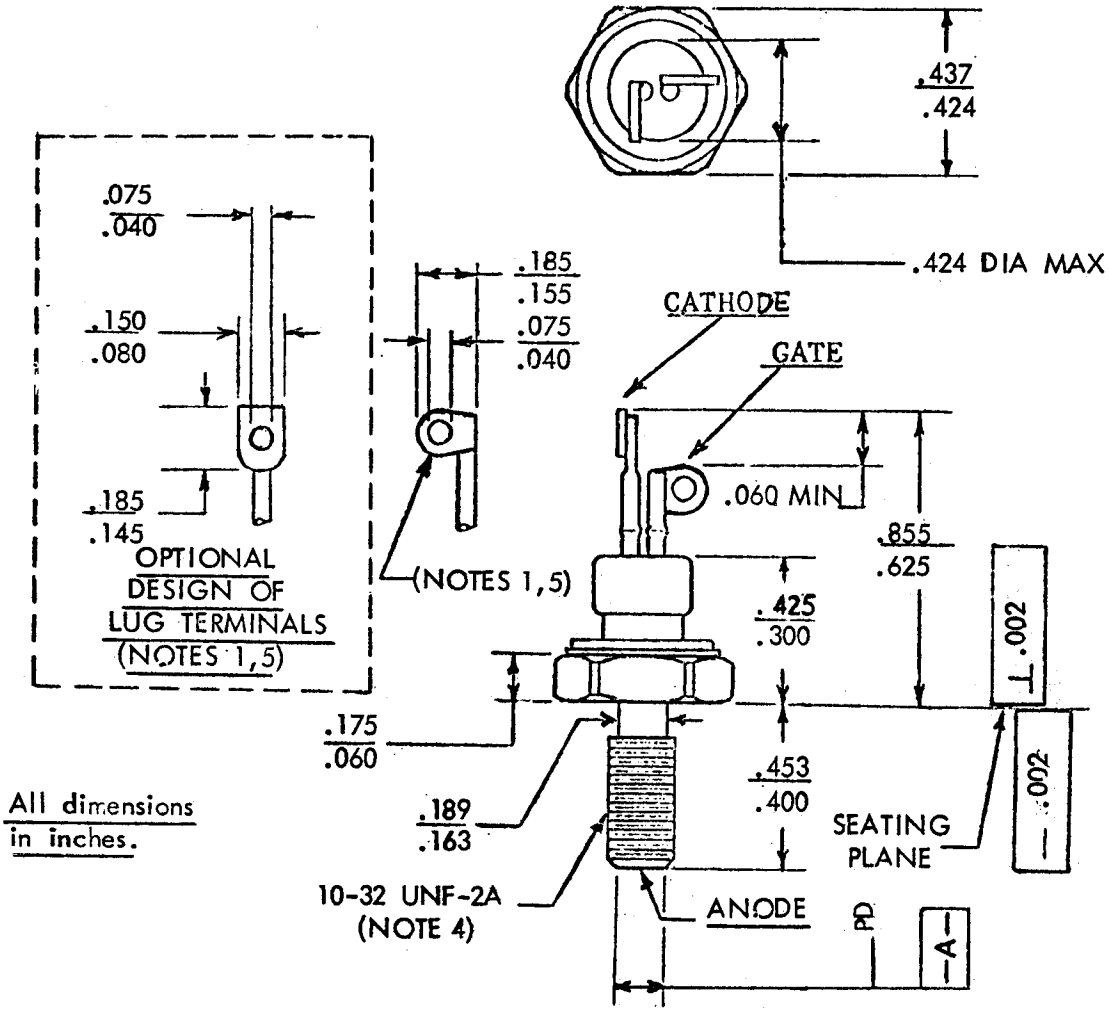
2/ See 3.4, 4.3.1, 4.3.3, and 4.3.6 herein.

3/ At 8 mmHg (pressure) for Types 2N4199 thru 2N4202; at 15 mmHg (pressure) for Types 2N4203 thru 2N4206.

4/ Measurement(s) shall be made after thermal equilibrium has been reached at the temperature specified.

5/ See 4.2.2 herein.

6/ See 4.3.9 herein.



NOTES:

1. Square, or radius-arc, on end of terminal is optional.
2. Angular orientation of terminals to each other and to hexagonal device-seat is undefined.
3. A chamfer (or undercut) on one or both ends of hexagonal portions is optional.
4. Complete threads to extend to within 2-1/2 threads of head (seat).
5. Flag (-lug) portion of terminal shall not extend to beyond the periphery of of hexagonal seat.

Figure 1. Outline and dimensions.

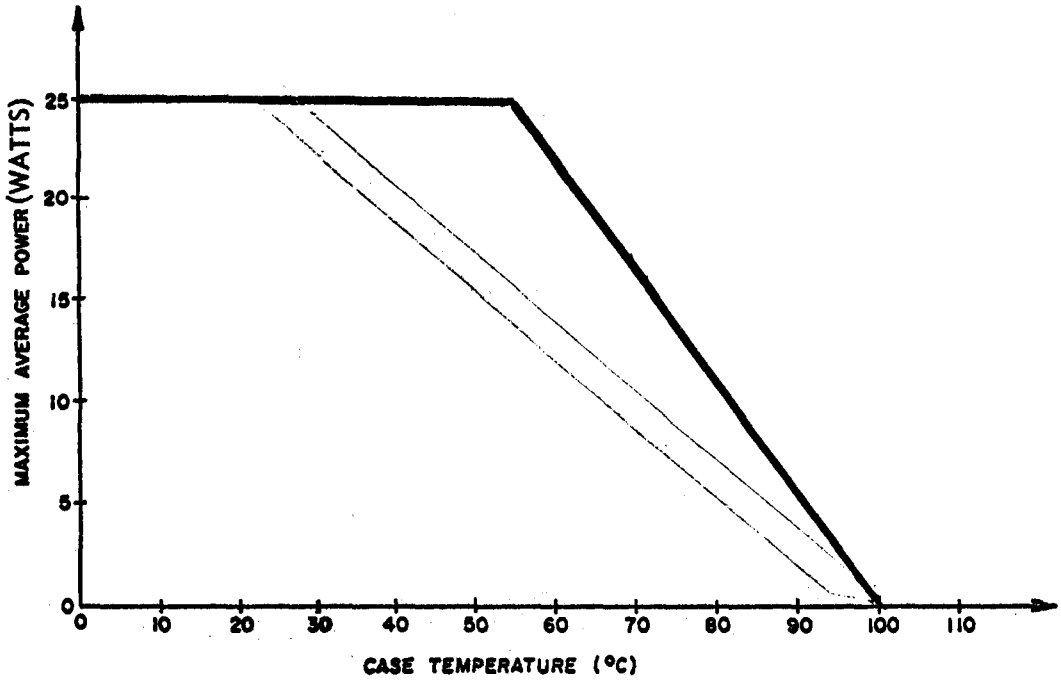
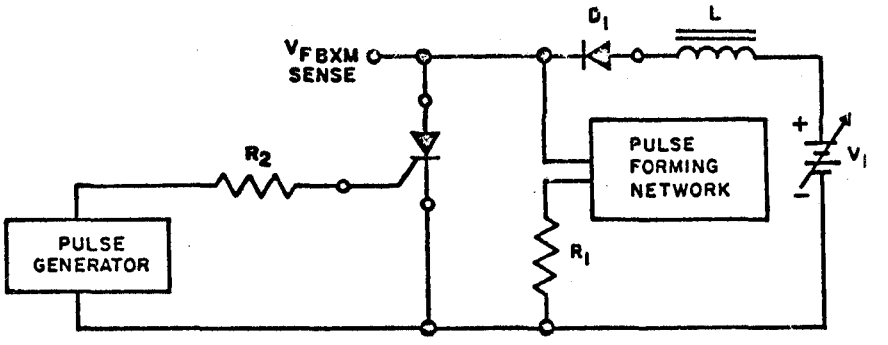
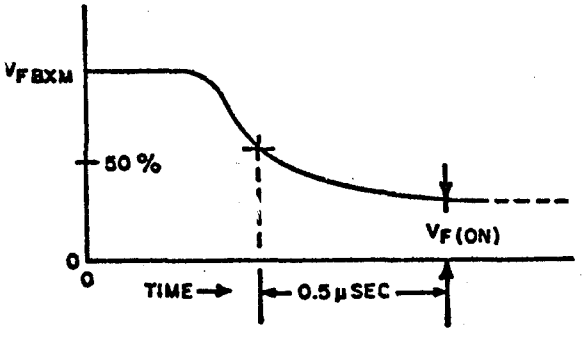


Figure 2. Power Dissipation, $P_{(AV)}$, vs T_C nomograph.





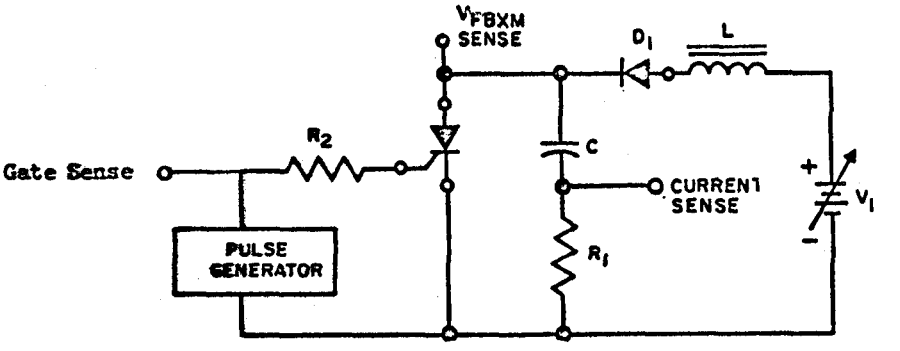
CIRCUIT ELEMENTS:

R_1 = See text below.
R_2 = 47 Ω
L = 200 hy, 15 kΩ
D_1 = 1N4007 or equal

PROCEDURAL REQUIREMENTS:

The device shall be triggered "ON" and remain conducting until the equilibrium forward current has been reached. The forward voltage drop from anode to cathode shall be measured at a point 0.5 µSec after V_{FBXM} has decreased to one-half of the specified operating voltage. Forward anode current and pulse repetition rate shall be as specified. Adjust V_1 until the V_{FBXM} peak equals the V_{FBO} specified for each device type. The pulse forming network shall be designed to produce a 1.5 ± .5µSec current pulse width, with the ripple of the flat portion of the current pulse limited to ± 3 amps. The combination of the pulse forming network and load resistor R_1 shall be selected to produce a peak current to be switched as specified for the level of V_{FBO}. The gate trigger pulse i_{GK} (pulse) from the generator shall be as specified.

Figure 3. Dynamic Forward "On" Voltage, (V_F), test circuit.



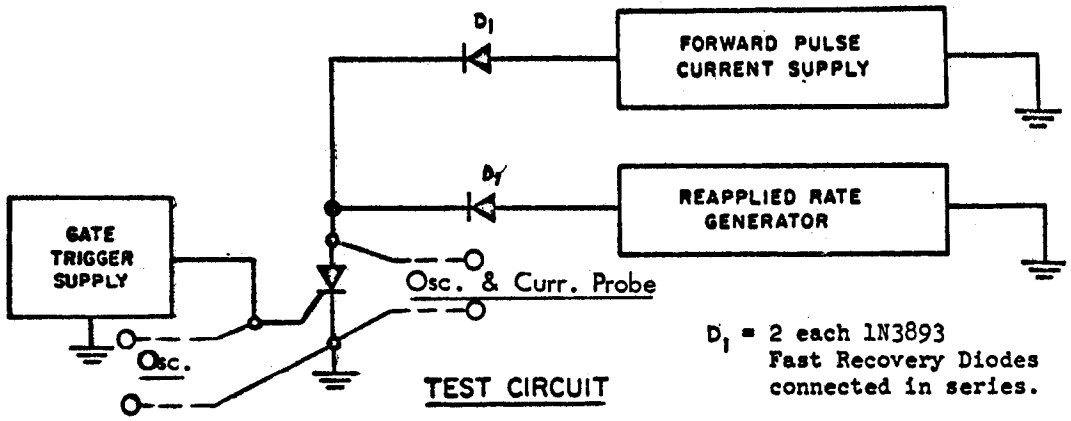
CIRCUIT ELEMENTS:

R_1 = See text below.
R_2 = 47 Ω
D_1 = 1N4007 or equal
L = 200 hy, 15 kΩ
C = 0.1 uF, 1.6 kV, ceramic-disc
(10 ea., .01 pF, in parallel)

PROCEDURAL REQUIREMENTS:

Adjust the gate trigger current i_{GK} (pulse) from the generator to the conditions specified. Adjust V_1 until the V_{FBXM} peak equals the V_{FBO} specified for each device type. The delay time shall be the time interval between the 10% point of gate current rise (monitored at Gate Sense Point) and the 10% point of anode current rise (monitored at Current Sense Point). The rise time shall be the time interval between the 10% and 90% points on the forward anode current pulse. R_1 is composed of the parallel combination of 2 watt carbon resistors selected so that the total value of R_1 (between 8 Ω and 30Ω) will allow a peak forward current flow of 30±2A.

Figure 4. Forward-Current t_d and t_r test circuit.



TEST CIRCUIT & PROCEDURE

A 30 amp forward current pulse is initiated by the gate trigger supply. The forward current pulse shall be 3 to 10 µSec long measured at the 50% points and shall decay to zero within 0.4 µSec. 20 µSec after a 10% decay in forward current, the rate generator shall reapply a forward voltage at a maximum rate of 250 v/µSec. The thyristor shall not revert to the conducting state during application of the reapplied voltage. A short duration reverse current spike may occur due to the abrupt removal of forward current, but will be limited by the fast recovery diode D_1.

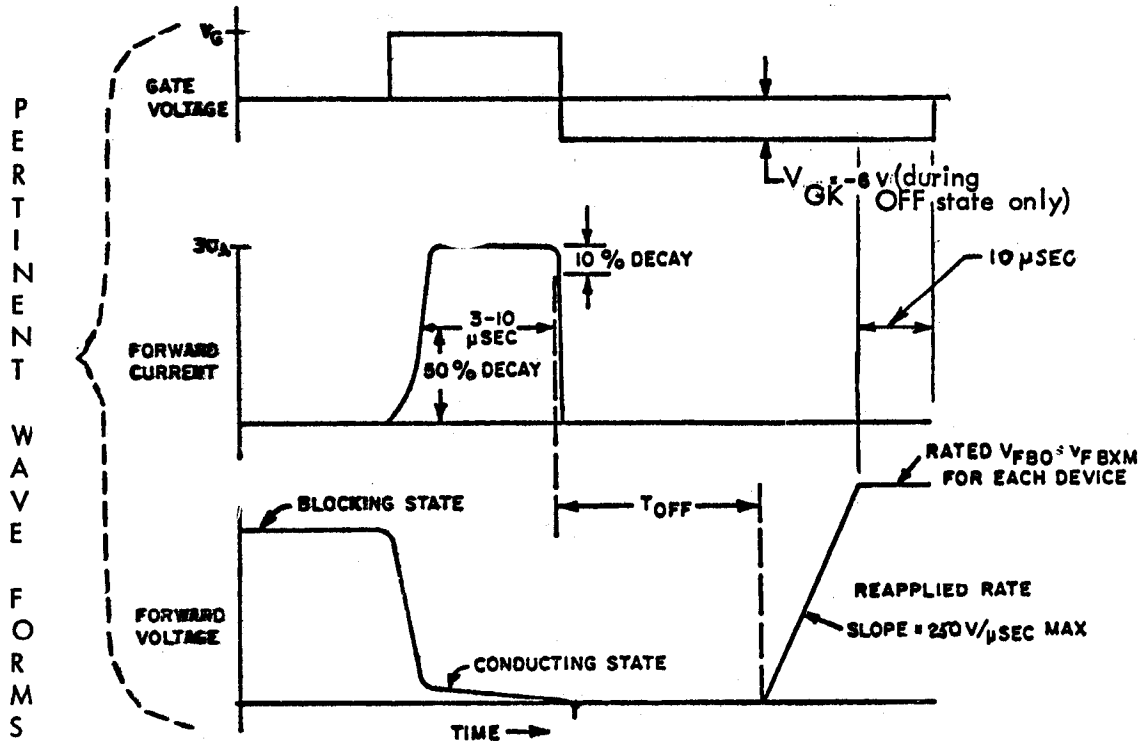
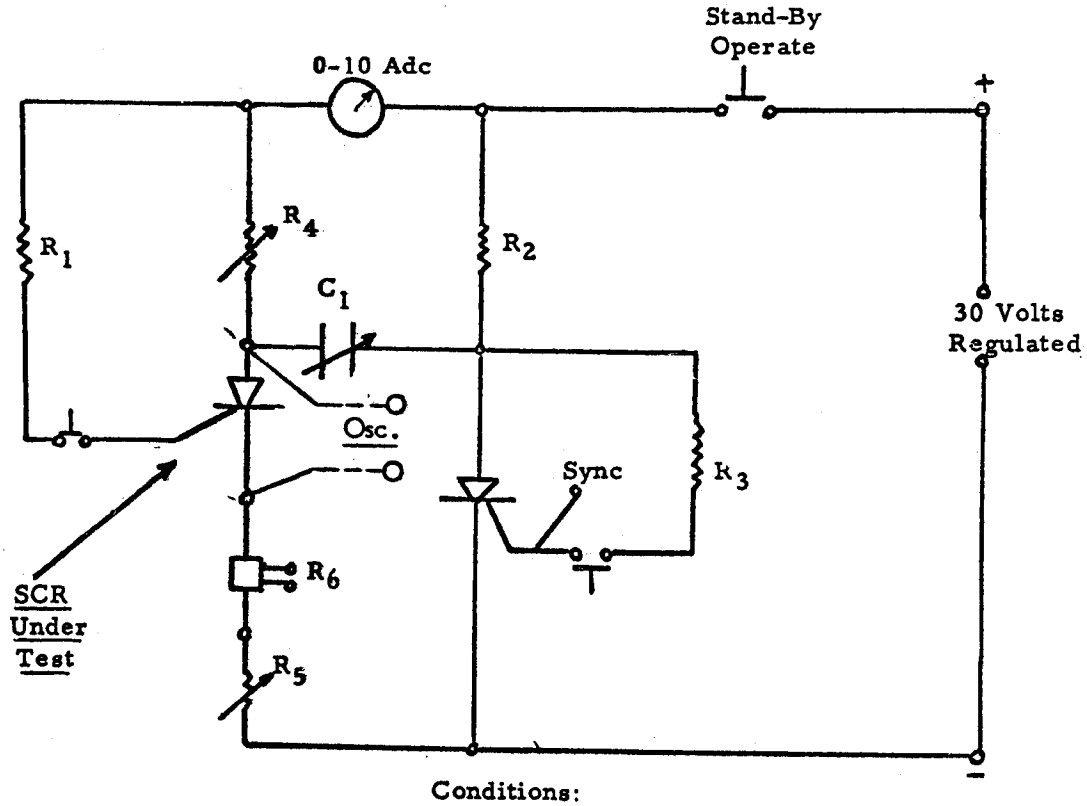


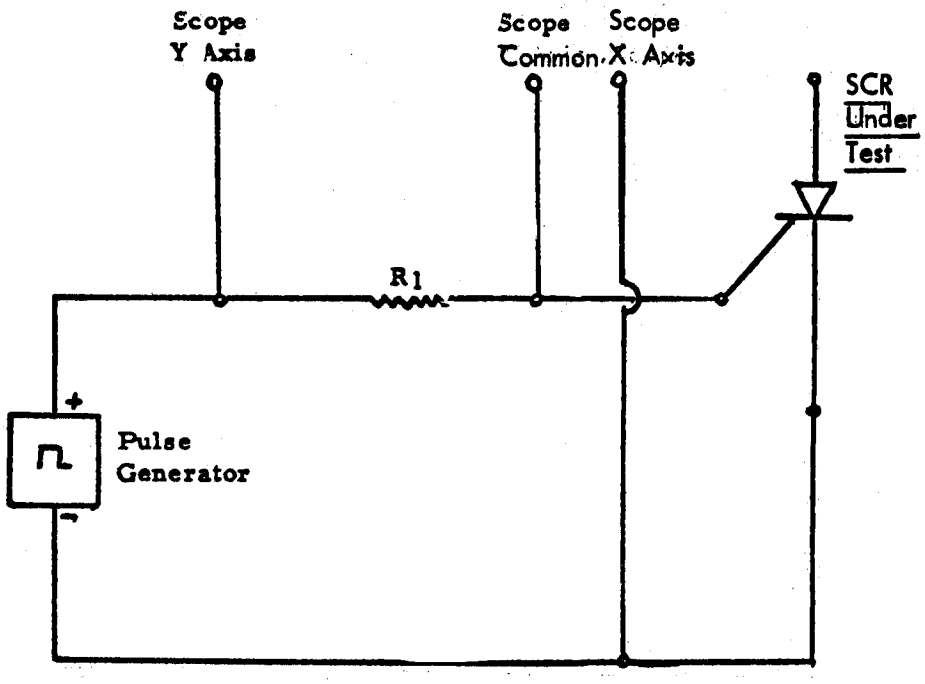
Figure 5. Turn-Off Time (Pulse, Forward) test circuit.



Conditions:

R_1, R_3	=	470Ω, 1 Watt
R_2	=	10KΩ, 1 Watt
R_4	=	Variable Resistor, 0-2Ω
R_5	=	Variable Resistor, 0.5Ω
R_6	=	Non-Inductive Shunt, 0.22Ω
C_1	=	0-20 uf Capacitors

Figure 6. Turn-Off Time (Conventional) test circuit.



CIRCUIT ELEMENTS and CONDITIONS:

R_1 = 2 Ω, 50 W, ±1%

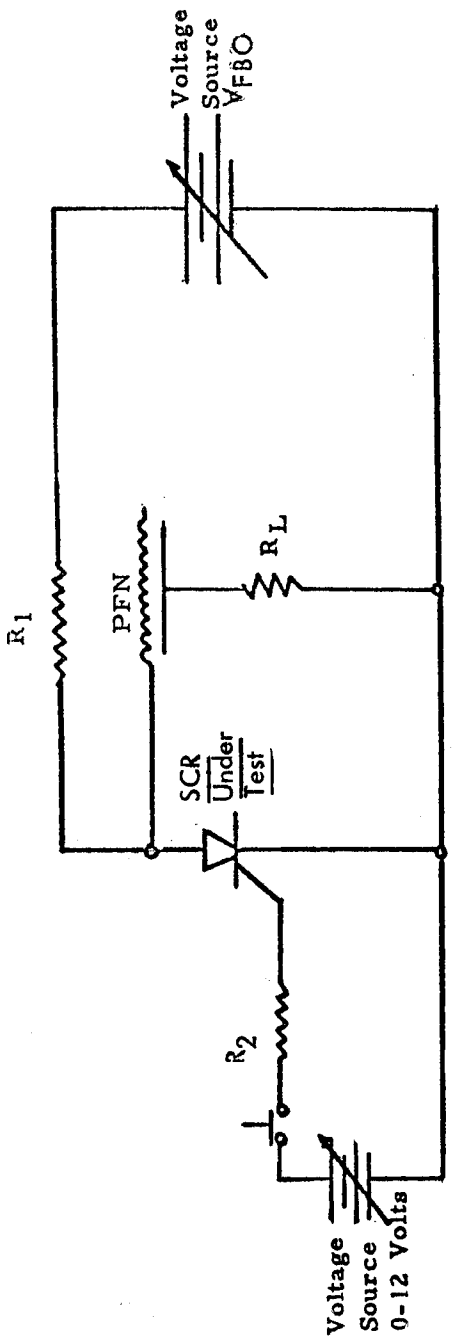
V_{GT}=10V max; I_{GT}=5A; t_p=10 usec; prr=100 pps

t = 1sec., min

Note:

The maximum gate voltage that can be applied to the gate-cathode junction of the device under test in the forward direction will be limited by the peak gate current of 5 amperes.

Figure 7. Peak Forward Gate Voltage, V_{GK}, test circuit.



CIRCUIT ELEMENTS AND CONDITIONS:

R_1 = 220 kΩ
R_2 = 47 kΩ
I_G = 200 mA (set before applying anode voltage)
PFN = provide: 10 pulses @ 1 minute intervals (non-repetitive);
I_A = 150 A; t_p = 0.5 usec.
V_{FBO} = respective rating (for each type) applied

Figure 8. Burn-out By Pulsing test circuit.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery.- Preparation for delivery, and the inspection of prepatation for delivery, shall be in accordance with Specification MIL-S-19500.

6. NOTES

6.1 Notes.- The notes included in Specification MIL-S-19500, with the following additions or exceptions, are applicable to this document.

6.2 Application guidance.

a. The thyristors conforming to requirements in this document issue are interchangeable with the thyristors covered by previous issue(s) of this document.

b. To insure proper circuit application, particular attention should be given to the differential voltage-and-current requirements, ratings, and performance characteristics pertinent to the individual thyristor types covered herein.

c. The guidance in Specification MIL-S-19500, Appendix A, relative to "absolute maximum ratings" should be heeded in connection with the Ratings data presented herein for the respective thyristors.

d. Thyristor type 2N4202 covered herein is intended, for use in compatible military-equipment circuits, as the preferred, direct replacement for thyristor type (Part No.) SCR 201-8 previously procured per U. S. Army Drawing No. SM-B-482473.

6.3 Preconditioning test records.- When requested, a copy of manufacturer's test data and findings covering the preconditioning accomplishment on the thyristors being shipped shall accompany the devices concerned.

6.4 Qualification.- With respect to products requiring qualification, awards will be made only for such products as have, prior to the time set for opening of bids, been tested and approved for inclusion in Qualified Products List (QPL)-19500, whether or not such products have actually been so listed by that date. Information pertaining to qualification of products covered by this specification should be requested from the Commanding General, U. S. Army Electronics Command, Fort Monmouth, New Jersey 07703, attention: AMSEL-PP-EM-2.

6.5 Changes from previous issue.- Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

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		$

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☐ DIRECT GOVERNMENT CONTRACT. ☐ SUBCONTRACT

1. HAS ANY PART OF THE SPECIFICATION CREATED PROBLEMS OR REQUIRED INTERPRETATION IN PROCUREMENT USE?

A. GIVE PARAGRAPH NUMBER AND WORDING.

B. RECOMMENDATIONS FOR CORRECTING THE DEFICIENCIES

2. COMMENTS ON ANY SPECIFICATION REQUIREMENT CONSIDERED TOO RIGID

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☐ YES ☐ NO IF "YES", IN WHAT WAY?

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