The documentation and process conversion measures necessary to comply with this revision shall be completed by 09-30-92.

MIL-S-19500/388B
30 June 1992
SUPERSEDING
MIL-S-19500/388A
11 July 1983

MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTOR, PN, SILICON, UNIJUNCTION TYPES 2N4947, 2N4948, AND 2N4949 JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for PN, silicon, unijunction transistors. Four levels of product assurance are provided for each device type as specified in MIL-S-19500.

1.2 Physical dimensions. See figure 1.

1.3 Maximum ratings.

P_T 1/ $T_A = 25°C$	P_T 2/ $T_C = 25°C$	I_e	i_e 3/	V_{B2E}	T_{STG} and T_J
W	W	mA (rms)	A (pk)	V dc	°C
0.36	N/A	50	1	30	-65 TO +200

1/ Derate linearly 2.057 mW/°C for $T_A > 25°C$.
2/ Derate linearly N/A mW/°C for $T_C > 25°C$.
3/ This value applies for a capacitor discharge through the emitter-base-one diode. The current must fall to 0.37 A within 3 ms and pulse-repetition rate must not exceed 10 pps.

1.4 Primary electrical characteristics at $T_A = 25°C$.

Type	R_{BBO} $V_{B2B1} = 3$ V dc $I_E = 0$		$V_{B2B1} = 10$ V dc (see figure 5)		$V_{EB1}(sat)$ 1/ $V_{B2B1} = 10$ V dc $I_E = 50$ mA dc	V_{OB1} (see figure 9)
	kΩ				V dc	V (pk)
	Min	Max	Min	Max	Max	Min
2N4947	4	9.1	0.51	0.69	3	3
2N4948	4	12.0	0.55	0.82	3	6
2N4949	4	12.0	0.74	0.86	3	3

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Electronics Supply Center, ATTN: DESC-ECT, 1507 Wilmington Pike, Dayton, OH 45444-5280 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5961

Type	(I_{EB20}) 1/ V_{EB2} = -30 V dc I_{B1} = 0 nA dc	I_{B2}(mod) 1/ V_{B2B1} = 10 V dc I_E = 50 mA dc mA dc	$R_{\Theta JA}$ °C/mW	$R_{\Theta JC}$ °C/mW
	Max	Min	Max	Max
2N4947	-5	8	0.486	
2N4948	-5	8	0.486	N/A
2N4949	-5	8	0.486	

1/ Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 Government documents

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards(DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

STANDARD

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Document Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Associated detail specification. The individual item requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500, and as follows:

I_{B2}(mod)- - Modulated interbase current. The resultant base-two (B2) current for specified values of emitter current and interbase voltage.

I_e- - - - - Emitter current, rms.

i_e- - - - - Instantaneous emitter current (capacitor discharge).

I_{EB20} - - - Emitter reverse current (dc), base-one (B1) open circuited.

I_P- - - - - Peak point emitter current. This is the minimum value emitter current for which the slope of the static emitter characteristic curve (see figure 3) is zero for a specified value of interbase voltage.

I_V- - - - - Valley point emitter current. This is the maximum value of emitter current for which the slope of the static emitter characteristic curve (see figure 3) is zero for a specified value of interbase supply voltage and base-two (B2) resistance.

- - - - - (eta) Intrinsic standoff ratio. This is defined by the relationship:

$$\eta = \frac{V_P - V_D}{V_{B2B1}}$$

B2 - - - - Resistance in series with the base-two (B2) lead.

R_{BBO}- - - - Interbase resistance. The resistance measured between base-one (B1) and base-two (B2) with the emitter open circuited.

αR_{BBO}- - - - Interbase resistance temperature coefficient. This is determined by the following formula:

$$\alpha R_{BBO} = \left[\frac{(R_{BBO} \text{ at } T_1) - (R_{BB}) \text{ at } T_2)}{(R_{BBO} \text{ at } 25^\circ C)}\right] \frac{100\%}{T_1 - T_2}$$

V_{BB} - - - - Interbase power supply voltage (dc).

V_{B2B1}- - - - - Interbase voltage, (dc) voltage from base-two (B2) to base-one (B1).

V_{B2E} - - - - - Voltage (dc) from base-two (B2) to emitter (E).

V_D - - - - - - Emitter diode voltage, for intrinsic standoff ratio test. (0.565 ±0.01 V dc at 50 μA dc, T_A = 25°C.)

V_{EB1} - - - - - Voltage (dc) from emitter to base-one (B1).

V_{EB1}(sat)- - - Emitter saturation voltage. The resultant dc voltage measured between the emitter and base-one (B1) for specified values of emitter current and interbase voltage.

V_{OB1} - - - - - Base-one (B1) peak pulse voltage. The base-one (B1) peak pulse voltage is defined as shown in figure 9. This parameter is a relative indicator of the peak emitter current available for use in firing circuits.

V_P - - - - - - Peak point emitter voltage. The voltage from emitter to base-one (B1) when the peak point emitter current flows for a specified value of interbase voltage.

3.2.1 Symbol. The graphic symbol for the unijunction transistor is shown on figure 4.

3.3 Design, construction, and physical dimensions. Transistors shall be of the design, construction, and physical dimensions shown on figure 1.

3.3.1 Lead material and finish. Lead material shall be Kovar or Alloy 52. Lead finish shall be gold, tin, or solder. Lead finish shall be specified in the acquisition document (see 6.2) without affecting the qualified product status of the device or applicable JAN marking.

3.4 Marking. Device marking shall be in accordance with MIL-S-19500.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-S-19500.

4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with MIL-S-19500 (table II) and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table II of MIL-S-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
4	See 4.5.9	See 4.5.9
9	$(I_{EB20})_1$, R_{BBO}	Not applicable.
10	See 4.3.1.	See 4.3.1.
11	$(I_{EB20})_1$, R_{BBO}, and ; $\Delta(I_{EB20})_1$ = 100% of initial value or 2 nA dc, whichever is greater; ΔR_{BBO} = ±15% of initial value; Δ = ±10% of initial value.	$(I_{EB20})_1$, R_{BBO}, and $\Delta(I_{EB20})_1$
12	See 4.3.2.	See 4.3.2.
13	Subgroups 2 and 3 of group A herein. $\Delta(I_{EB20})_1$ = 100% of initial value or 2 nA dc, whichever is greater; ΔR_{BBO} = ±15% of initial value; Δ = ±10% of initial value.	Subgroup 2 of group A herein. $\Delta(I_{EB20})_1$ = 100% of initial value or 2 nA dc, whichever is greater; ΔR_{BBO} = ±15% of initial value; Δ = ±10% of initial value.

4.3.1 High temperature reverse bias test conditions. High temperature reverse bias test conditions shall be as follows: Test method 1039, condition A of MIL-STD-750. Emitter to base-one open circuit.

V_{B2E} = 24 V dc; I_{B1} = 0 for 48 hours minimum at T_A = 150°C (minimum).

4.3.2 Power burn-in test conditions. Power burn-in test conditions shall be as follows:

V_{B2B1} = 10 V dc; I_E = 30 mA dc at T_A = 25°C ±3°C

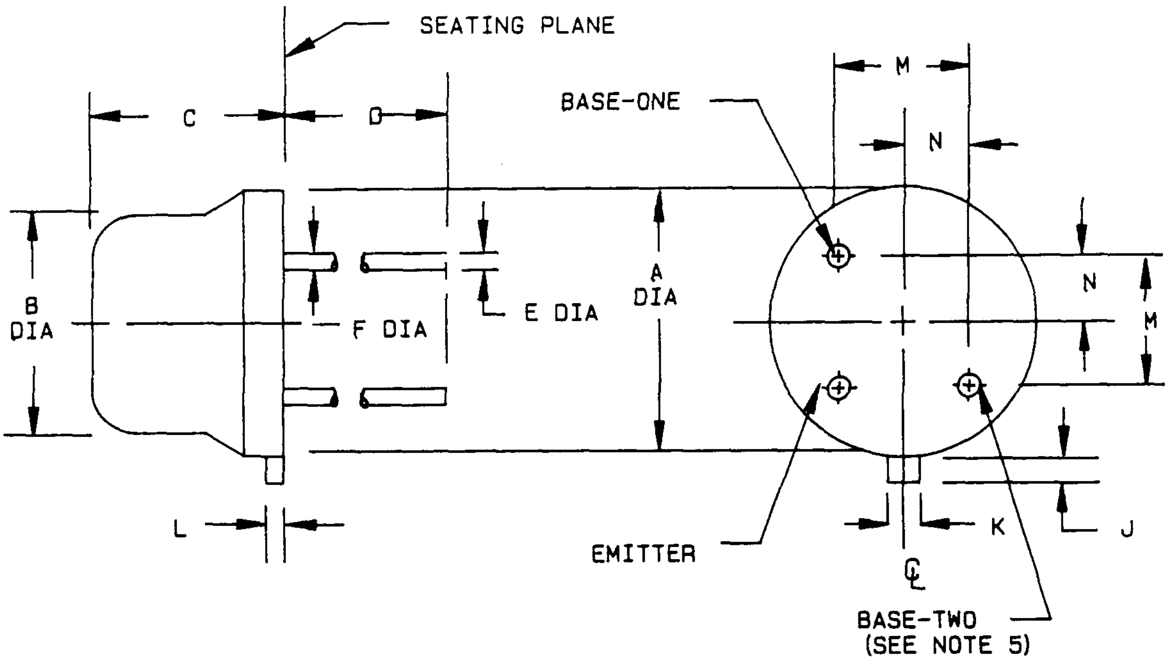
No heat sink or forced air cooling on the devices shall be permitted.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-S-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-S-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IVa (JANS) and table IVb (JAN, JANTX, and JANTXV) of MIL-S-19500, and tables IIa and IIb herein. Electrical measurements (end points) and delta requirements shall be in accordance with the applicable steps of table IV herein.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table V of MIL-S-19500, and table III herein. Electrical measurements (end points) and delta requirements shall be in accordance with the applicable steps of table IV herein.



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.209	.230	5.31	5.84	
B	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	----	12.70	----	7
E	----	.021	----	.53	2,7
F	.016	.019	.41	.48	3,7
J	.028	.048	.71	1.22	6
K	.036	.046	.91	1.17	
L	----	.020	----	.51	
M	.0707 Nominal		1.80 Nominal		4
N	.0354 Nominal		0.90 Nominal		4

NOTES:
1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Measured in the zone beyond .250 (6.35 mm) from the seating plane.
3. Measured in the zone .050 (1.27 mm) and .250 (6.35 mm) from the seating plane.
4. When measured in a gauging plane .054 +.001/-.000 (1.37 +.03/-.00 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 (.18 mm) of their true location relative to a maximum diameter lead tolerance. Figure 2 preferred measuring method.
5. Base-two shall be internally connected to the case.
6. Measured from the maximum diameter of the actual device. 1.00 inch = 25.4 mm.
7. All 3 leads.

FIGURE 1. Physical dimensions.

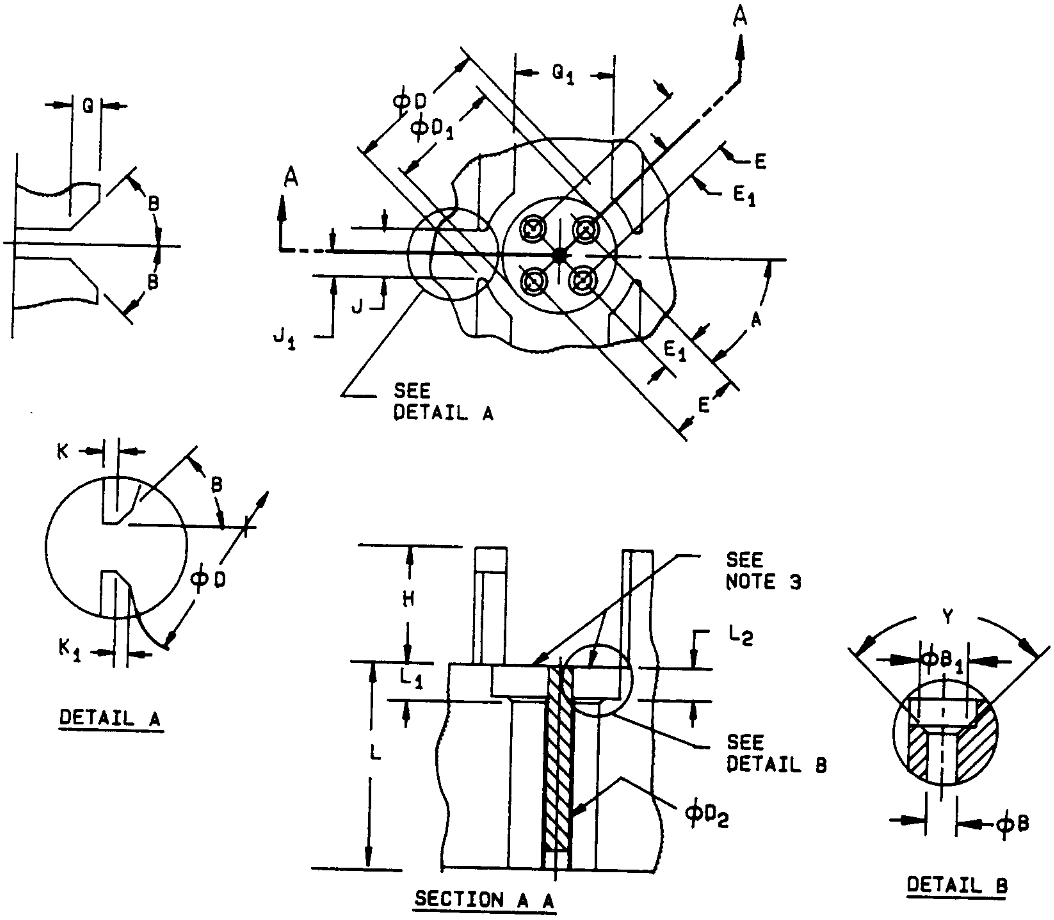


FIGURE 2. Gauge for lead and tab location.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
ϕB	.0325	.0335	.8255	.8509	4
ϕB_l	.043 Nominal		1.09 Nominal		4
ϕD	.2310	.2315	5.867	5.880	
ϕD_1	.159	.161	4.04	4.09	
ϕD_2	.040 Nominal		1.02 Nominal		5
E	.0995	.1005	2.527	2.553	
E_1	.0495	.0505	1.257	1.283	
H	.145	.155	3.68	3.94	
J	.0470	.0475	1.194	1.207	
J_1	.0235	.0245	.597	.622	
K	.009	.011	.229	.279	
K_1	.005 Nominal		.127 Nominal		
L	.372	.378	9.45	9.60	
L_1	.054	.055	1.37	1.40	
L_2	.043 Nominal		1.09 Nominal		
Q	.040 Nominal		1.02 Nominal		
Q_1	.123	.127	3.12	3.23	
A	44.90°	45.10°	-----	-----	
B	45° Nominal		-----		
Y	90° Nominal		-----		

NOTES:
1. Metric equivalents are given for general information only and are based upon 1 inch = 25.4 mm.
2. The following gauging procedures shall be used: The device being measured shall be inserted until its seating plane is .125 (3.18 mm) +.010 (.254 mm) from the seating surface of the gauge. A force of 8 ±.5 ounce shall then applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gauge. The use of a pin straightener prior to insertion in the gauge is permissible. A spacer may be used to obtain the .125 (3.18 mm) distance from gauge seat prior to force application.
3. These surfaces to be parallel and in same plane within ±.001 (.025 mm).
4. Four holes.
5. Pressed in.

FIGURE 2. Gauge for lead and tab location - Continued.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.5.2 Interbase resistance. The specified interbase voltage (see tables I and IV) is applied and the corresponding resistance is measured for the emitter open circuited.

4.5.3 Intrinsic standoff ratio. Either of the two alternate methods below may be used at the option of the manufacturer.

4.5.3.1 Method a. The circuit of figure 5a shall be used for this measurement. The specified interbase voltage (see tables I and IV) shall be applied and the variable resistor shall be adjusted to obtain a null. Eta is then read directly from the calibration of the variable resistor. The following equation shall be used to calibrate the variable resistor:

$$n = \frac{V_P - V_D}{V_{B2B1}}$$

4.5.3.2 Method b. The circuit of figure 5b, or a suitable equivalent, shall be used for this measurement. Switch S1 is closed, applying the specified V_{B2B1} (see tables I and IV) and causing the unijunction to fire. The voltage across the 100 kilohm resistor, V_R, is measured and ratio is computed as follows:

$$n = \frac{V_R}{V_{B2B1}} = \frac{V_P - V_D}{V_{B2B1}} \quad (V_D = 0.565 \text{ V dc at } 50\ \mu\text{A dc and } T_A = 25^\circ\text{C})$$

4.5.4 Modulated interbase current and emitter saturation voltage. The specified values (see tables I and IV) of interbase voltage and emitter current are applied. The base-two (B2) current is measured as the modulated interbase current. The emitter to base-one (B1) voltage is measured as the emitter saturation voltage. The test circuit of figure 6 may be used to measure these parameters.

4.5.5 Peak point emitter current. This parameter shall be measured in the circuit of figure 7 or a suitable equivalent. The potentiometer is adjusted to apply a low resistance between the emitter and base-one (B1). The specified V_{B2B1} (see table I) is applied and the resistance between the emitter and base-one (B1) is increased until the transistor fires as determined by oscillation of I_E. Peak point emitter current is the maximum value of I_E just prior to oscillation.

4.5.6 Valley point emitter current. For the specified interbase supply voltage (see table I) and base-two (B2) resistance, the emitter current corresponding to the valley point operating condition is measured. The test circuit of figure 8, or suitable equivalent, shall be used for this measurement. The specified interbase supply voltage, V_{BB}, and base-two (B2) series resistance shall be applied. R_1 shall be of sufficient value to adequately control the emitter current. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{EB1}. The I_E corresponding to this minimum value of V_{EB1} is the I_V of the device under test.

4.5.7 Emitter reverse current. This test shall be conducted in accordance with method 3041 of MIL-STD-750 except that the words "collector", "base", and "emitter" shall be replaced with "base-two (B2)", "emitter (E)", and "base-one (B1)", respectively.

4.5.8 Interbase resistance temperature coefficient. The interbase resistance temperature coefficient shall be determined by measuring the interbase resistance in accordance with 4.5.2 at the specified temperatures and computing the temperature coefficient by the following formula:

$$\alpha R_{BBO} = \frac{(R_{BBO} \text{ at } T_1) - (R_{BBO} \text{ at } T_2)}{(R_{BBO} \text{ at } 25^\circ\text{C})} \cdot \frac{100\%}{T_1 - T_2}$$

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Intrinsic standoff ratio		V_{B2B1} = 10 V dc (see 4.5.3)				
2N4947				0.51	0.69	
2N4948				0.55	0.82	
2N4949				0.74	0.86	
Interbase resistance		V_{B2B1} = 3 V dc; I_E = 0 (see 4.5.2)	R_{BBO}			
2N4947				4	9.1	kΩ
2N4948				4	12.0	kΩ
2N4949				4	12.0	kΩ
Modulated interbase current		V_{B2B1} = 10 V dc (see 4.5.4); I_E = 50 mA dc Pulsed (see 4.5.1)	I_{B2}(mod)	8		mA dc
Emitter saturation voltage		V_{B2B1} = 10 V dc (see 4.5.4); I_E = 50 mA dc Pulsed (see 4.5.1)	V_{EB1}(sat)		3	V dc
Emitter reverse current	3041	Bias cond D (see 4.5.7); V_{EB2} = -30 V dc; I_{B1} = 0	$(I_{EB20})_1$		-5	nA dc
Valley point emitter current		V_{BB} = 20 V dc; R_{B2} = 100 ohms (see 4.5.6)	I_{V1}			
2N4947				4		mA dc
2N4948				2		mA dc
2N4949				2		mA dc
Peak point emitter current		V_{B2B1} = 25 V dc (see 4.5.5)	I_P			
2N4947					2	μA dc
2N4948					2	μA dc
2N4949					1	μA dc
Base-one peak pulse voltage		See figure 9	V_{OB1}			
2N4947				3		V pk
2N4948				6		V pk
2N4949				3		V pk

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
Interbase resistance temperature coefficient		V_{B2B1} = 3 V dc; I_E = 0 (see 4.5.8); T_1 = 100°C; T_2 = -65°C	αR_{BBO}	0.1	0.9	%/°C
High temperature operation:		T_A = 125°C				
Emitter reverse current	3041	Bias cond D (see 4.5.7) V_{EB2} = -30 V dc; I_{B1} = 0	$(I_{EB20})_2$		-1	μA dc
Valley pointer current		V_{BB} = 20 V dc; R_{B2} = 100 ohms (see 4.5.6)	I_{V2}			
2N4947				3.0		mA dc
2N4948				1.5		mA dc
2N4949				1.5		mA dc
Subgroups 4, 5, 6, 7						
Not applicable						

1/ For sampling plan, see MIL-S-19500.

TABLE IIa. Group B inspection for JANS devices.

Inspection 1/	MIL-STD-750	
	Method	Conditions
Subgroup 1		
Physical dimensions	2066	(See figure 1)
Subgroup 2		
Solderability	2026	
Resistance to solvents	1022	
Subgroup 3		
Thermal shock (temperature cycling)	1051	
Hermetic seal a. Fine b. Gross	1071	
Electrical measurements		See table IV, steps 1, 2, 3, 4, and 5
Decap internal visual design verification	2075	
Bond strength	2037	Test cond A All internal wires for each device shall be pulled separately.
Die shear	2017	Devices previously subjected to the bond strength test may be used for this test.
Subgroup 4		
Intermittent operation life	1037	V_{B2B1} = 10 V dc; I_E = 30 mA dc at T_A = 25°C ±3°C; t_{on} = t_{off} = 3 minutes minimum for 2000 cycles. No heat sink forced air on the devices shall be permitted.
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, and 10
Subgroup 5		
Steady-state operation life (accelerated)	1027	V_{B2B1} = 10 V dc; I_E = 30 mA dc at T_A = 100°C for 96 hours. Marking legibility requirements shall not apply.
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 7, 8, and 9

See footnotes at end of table.

TABLE IIa. Group B inspection for JANS devices - Continued.

Inspection 1/	MIL-STD-750	
	Method	Conditions
Subgroup 6		
Not applicable		
Subgroup 7		
Constant acceleration	2006	One minute minimum in the Y_1 orientation at 30,000 G minimum. Only required when lot complies with 4.5.9.
Electrical measurements		See table IV, steps 1, 2, 3, 4, and 5

1/ For sampling plan, see MIL-S-19500.

TABLE IIb. Group B inspection for JAN, JANTX, and JANTXV devices.

Inspection 1/	MIL-STD-750	
	Method	Conditions
Subgroup 1		
Solderability	2026	
Resistance to solvents	1022	
Subgroup 2		
Thermal shock (temperature cycling)	1051	
Hermetic seal	1071	
a. Fine leak		
b. Gross leak		
Electrical measurements		See table IV, steps 1, 2, and 5
Subgroup 3		
Steady-state operation life	1027	V_{B2B1} = 10 V dc, I_E = 30 mA dc at T_A = 25°C ±3°C. No heat sink or forced air cooling on the device shall be permitted.
Electrical measurements		See table IV, steps 1, 2, and 6
Subgroup 4 2/		
Decap internal visual (design verification)	2075	
Bond strength	2037	Test condition A
Subgroup 5		
Not applicable		
Subgroup 6		
High temperature (non-operating life)	1032	T_A = 200°C
Electrical measurements		See table IV, steps 1, 2, and 6
Subgroup 7		
Constant acceleration	2006	One minute minimum in the Y_1 orientation at 30,000 G minimum. Only required when lot complies with 4.5.9
Electrical measurements		See table IV, steps 1, 2, and 5

1/ For sampling plan, see MIL-S-19500.
2/ Electrical reject devices from the same inspection lot may be used for all subgroups when electrical end point measurements are not required.

TABLE III. Group C inspection for all quality levels.

Inspection 1/	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Limits Min	Limits Max	Unit
Subgroup 1						
Physical dimensions	2066	See figure 1				
Subgroup 2						
Thermal shock (glass strain)	1056	Test condition A				
Terminal strength	2036	Test condition E				
Hermetic seal	1071					
a. Fine leak b. Gross leak						
Moisture resistance	1021					
External visual	2071					
Electrical measurements		See table IV, steps 1, 2, 3, 4, an 5 (JANS) and steps 1, 2, and 5 (JAN, JANTX, and JANTXV)				
Subgroup 3						
Shock	2016					
Vibration, variable frequency	2056					
Constant acceleration	2006					
Electrical measurements		See table IV, steps 1, 2, 3, 4, and 5 (JANS) and steps 1, 2, and 5 (JAN, JANTX and JANTXV)				
Subgroup 4						
Salt atmosphere (corrosion)	1041					
Subgroup 5						
Not applicable						

See footnotes at end of table.

TABLE III. Group C inspection for all quality levels) - Continued.

Inspection 1/	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Limits Min	Limits Max	Unit
Subgroup 6						
Steady-state operation life	1026	V_{B2B1} = 10 V dc, I_E = 30 mA dc at T_A = 25°C ±3°C. No heat sink or forced air cooling on the devices shall be permitted.				
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 7, 8, and 9 (JANS) and steps 1, 2, and 6 (JAN, JANTX, and JANTXV)				

1/ For sampling plan, see MIL-S-19500.

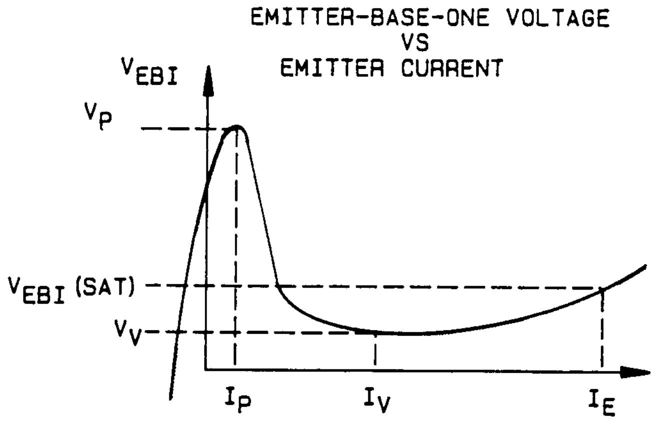


FIGURE 3. Unijunction transistor static emitter characteristic curve.

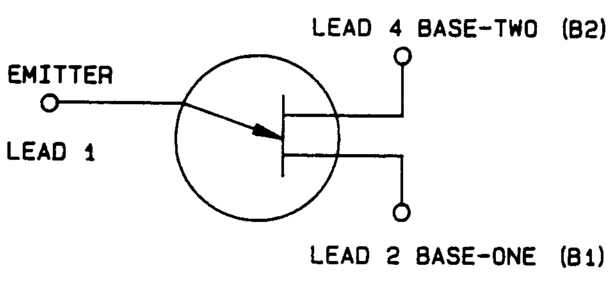
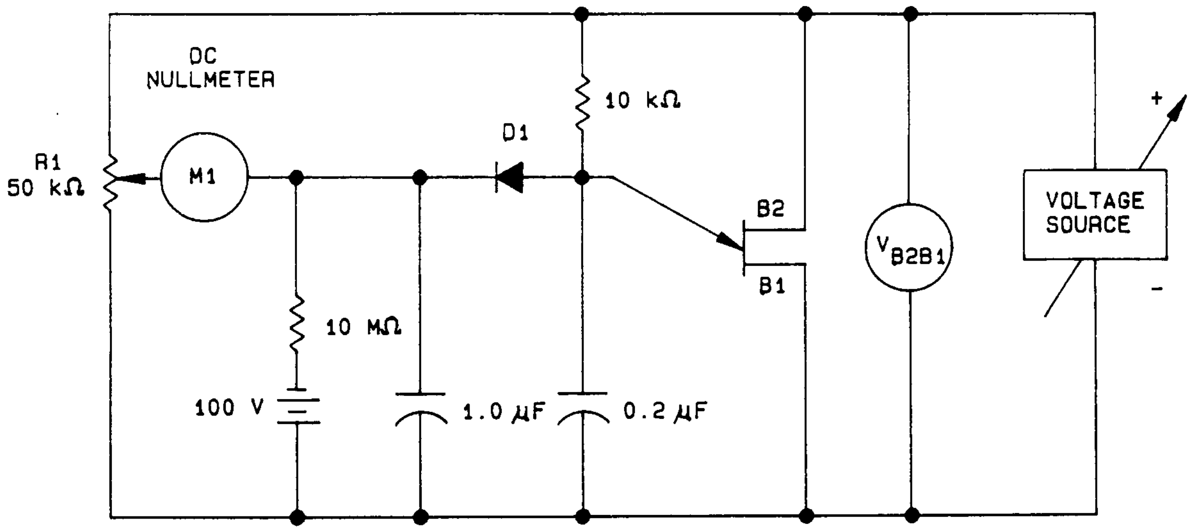


FIGURE 4. Graphic symbol for the unijunction transistor (see 3.2.1).

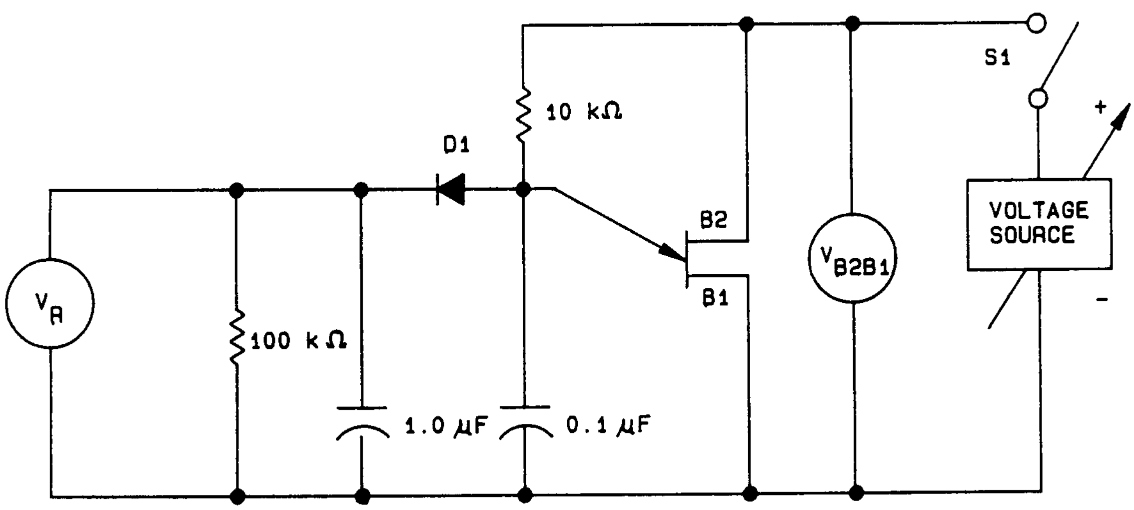
TABLE IV. Groups B and C electrical measurements.

Step	Inspection	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Limits Min	Limits Max	Unit
1	Intrinsic standoff ratio		V_{B2B1} = 10 V dc (see 4.5.3)				
	2N4947				0.51	0.69	
	2N4948				0.55	0.82	
	2N4949				0.74	0.86	
2	Interbase resistance		V_{B2B1} = 3 V dc; I_E = 0 (see 4.5.2)	R_{BBO}			
	2N4947				4	9.1	kΩ
	2N4948				4	12.0	kΩ
	2N4949				4	12.0	kΩ
3	Modulated interbase current		V_{B2B1} = 10 V dc (see 4.5.4) I_E = 50 mA dc, Pulsed (see 4.5.1)	$I_{B2}(mod)$	8		mA dc
4	Emitter saturation voltage		V_{B2B1} = 10 V dc (see 4.5.4) I_E = 50 mA dc, Pulsed (4.5.1)	$V_{EB1}(sat)$		3	V dc
5	Emitter reverse current	3041	Bias cond. D (see 4.5.7) V_{EB2} = -30 V dc; I_{B1} = 0	$(I_{EB20})_1$		5	nA dc
6	Emitter reverse current	3041	Bias cond. D (see 4.5.7) V_{EB2} = -30 V dc; I_{B1} = 0	$(I_{EB20})_1$		10	nA dc
7	Intrinsic standoff ratio		V_{B2B1} = 10 V dc (see 4.5.3)	Δ		±15% of initial value	
8	Interbase resistance		V_{B2B1} = 3 V dc; I_E = 0 (see 4.5.2)	ΔR_{BBO}		±20% of initial value	
9	Emitter reverse current	3041	Bias cond. D (see 4.5.7) V_{EB2} = -30 V dc; I_{B1} = 0	$\Delta(I_{EB20})_1$		±100% of initial value or 4 nA dc, whichever is greater	
10	Emitter saturation voltage		V_{B2B1} = 10 V dc (see 4.5.4) I_E = 50 mA dc, Pulsed (see 4.5.1)	$\Delta V_{EB1}(sat)$		±50 mV dc change from initial value	



NOTES:
1. R1 - Calibrated helipot (n).
2. Voltage source shall have less than 10 mV ripple (peak to peak).
3. D1 - Silicon diode, forward voltage of .565 ±.010 volt at forward current of 50 μA dc and a reverse leakage of less than 1 μA dc at 20 volts.

FIGURE 5a. Intrinsic standoff ratio test circuit (method a).



NOTES:
1. Voltage source shall have less than 10 mV ripple (peak to peak) and be readily controllable to less than 10 mV.
2. D1 - Silicon diode, forward voltage of .565 ±.010 volt at forward current of 50 μA dc and a reverse leakage of less than 1 μA dc at 20 volts.

FIGURE 5b. Intrinsic standoff ratio test circuit (method b).

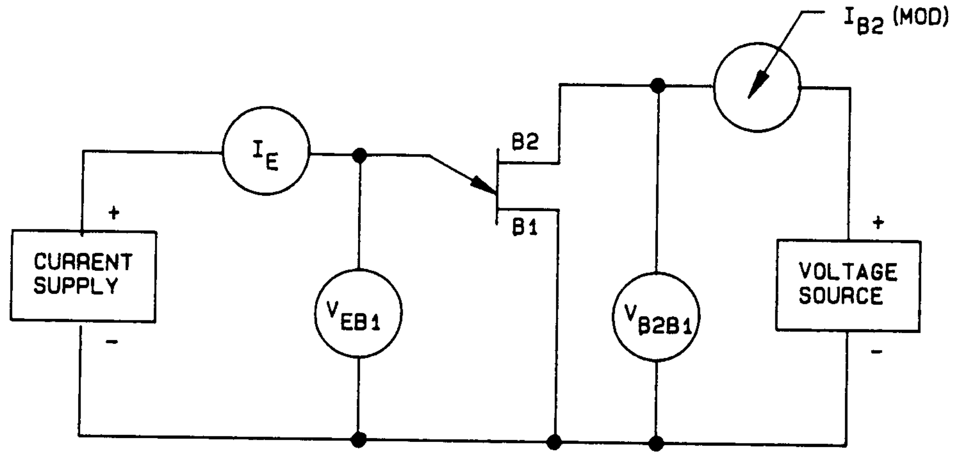
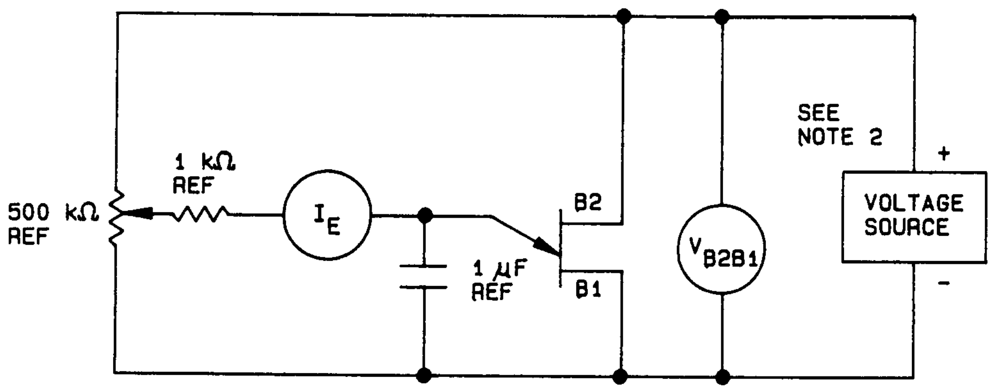
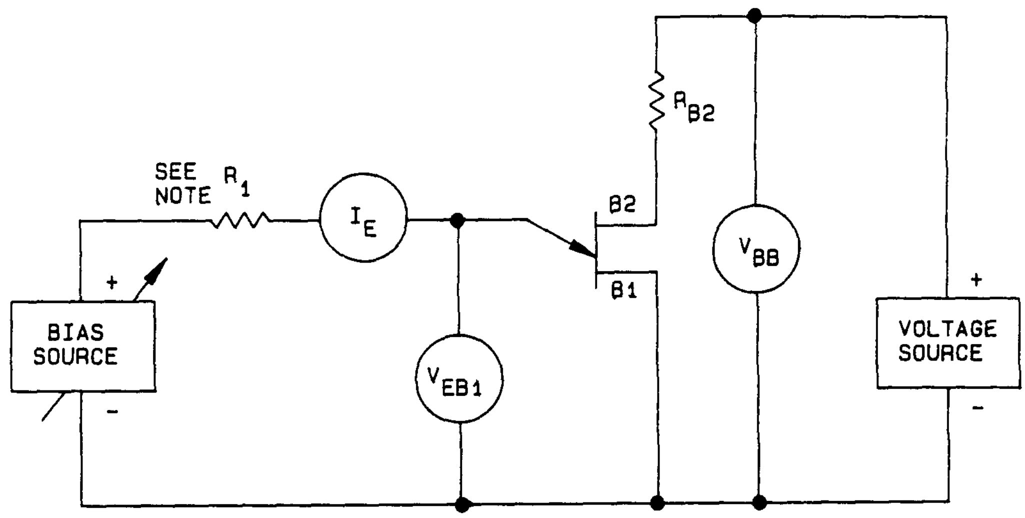


FIGURE 6. Modulated interbase current and emitter saturation voltage circuit.



NOTES:
1. 500 kΩ potentiometer must be noiseless to prevent false triggering.
2. Voltage source with less than 1 mV peak-to-peak ripple.

FIGURE 7. Peak point emitter current circuit.



NOTE: R_1 chosen to limit current to a safe value.

FIGURE 8. Valley point emitter current circuit.

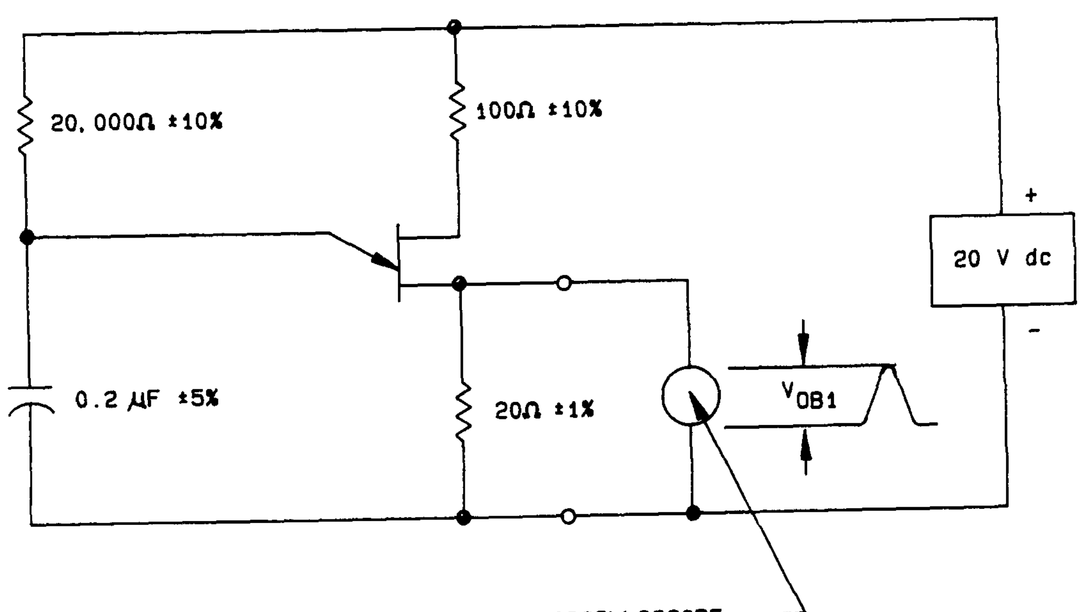


FIGURE 9. Base-one (B1) peak pulse voltage test circuit.

4.5.9 Constant acceleration. Only devices constructed with aluminum bonding wire which successfully pass three consecutive lots with zero failures shall not require this test as a 100 percent screen on future inspection lots. In the event the sample fails the LTPD requirements of group B inspection, and the failures are catastrophic (i.e., open or shorted condition), as verified by failure analysis, then 100 percent screening shall be re-instituted. The 100 percent screen shall be required on the failed lot and following lots until three successive inspection lots pass the constant acceleration test with zero failures. Only then may sampling inspection be resumed. End point measurements for this screening test shall be those required by screen 11. Only device failures, verified by failure analysis, caused by the constant acceleration test shall be counted as failures for this screening test. All sample devices which are drawn for constant acceleration inspection shall have successfully completed thermal shock inspection (minimum of 25 cycles).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-S-19500.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and ate of the specification.

b. Issue of DODISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced herein (see 2.1).

c. Lead finish (see 3.3.1).

d. Type and quality assurance level.

6.3 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI
Navy - SH
Air Force - 11, 19, 85, 80
NASA - LRC, MSF
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC, OS
Air Force - 13

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5961-1369)