MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, THYRISTOR (CONTROLLED RECTIFIER), SILICON
TYPES 2N3027 THROUGH 2N3032, AND
TX2N3027 THROUGH TX2N3032

1. SCOPE

1.1 Scope.- This specification covers the detail requirements for silicon, PNPN, thyristors for application particularly as controlled rectifier, reverse-blocking triode devices in compatible electronic-equipment circuits. (See 3.2, 3.4, and 6.2 herein.) The prefix "TX" identifies devices meeting the special process-conditioning, testing, and screening requirements in 4.4 herein, and the stringent quality-control (LTPD) requirements in Tables I, II, and III herein.

1.2 Outline and dimensions.- See Figure 1 herein. (TO-18)

1.3 Ratings.-

	I_o at: T_A = +100°C		i_{FM} (surge) (See Table II)		v_{KGM} 1/		v_{RBXM}		v_{FBXM}		T_{stg}		$T_{(oper)}$	
	mAdc		adc		v		v		v		°C		°C	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
2N3027	---	175	---	8	---	5	---	30	---	30	-65	+200	-65	+150
2N3028	---	175	---	8	---	5	---	60	---	60	-65	+200	-65	+150
2N3029	---	175	---	8	---	5	---	100	---	100	-65	+200	-65	+150
2N3030	---	175	---	8	---	5	---	30	---	30	-65	+200	-65	+150
2N3031	---	175	---	8	---	5	---	60	---	60	-65	+200	-65	+150
2N3032	---	175	---	8	---	5	---	100	---	100	-65	+200	-65	+150

1/ Gate connected to cathode across 1-Kohm resistor.

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1.4 Particular electrical characteristics.- (At T_A=+25°C; see Table I):

	V_{FM}		I_{HOX}		V_{GT} 1/		I_{GT} 1/		$t_{pg(on)}$		t_{off}	
	Vdc		mAdc		Vdc		uAdc		usec		usec	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
2N3027, 2N3028, 2N3029	0.8	1.5	0.3	5.0	0.4	0.8	-5	200	---	0.2	---	2.0
2N3030, 2N3031, 2N3032	0.8	1.5	0.3	4.0	0.44	0.60	-5	20	---	0.1	---	2.0

1/ Gate connected to cathode across 1-Kohm resistor.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

SPECIFICATIONS
MILITARY
MIL-S-19500 Semiconductor Devices, General Specification For

STANDARDS
MILITARY

MIL-STD-750 Test Methods For Semiconductor Devices
MIL-STD-1276 Leads, Weldable, For Electronic Component Parts

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the thyristors shall be in accordance with Specification MIL-S-19500, and as otherwise specified herein.

3.2 Abbreviations and Symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500, and as follows:

I_{HOX}.....D.C. holding current; special gate and voltage conditions.
R_{GK}.....external resistance between gate and cathode terminals.
V_{RBXM}....peak reverse blocking voltage, gate connected to stated reference terminal through stated impedance or bias (or both).
V_{FBX}.....exponential rate of voltage rise; (as used for test-characteristic determinant herein).

3.3 Design and construction.- The thyristor shall be of the design, construction, and physical dimensions specified in Figure 1.

3.3.1 Terminal arrangement.- The terminal arrangement on the thyristor shall be as indicated in Figure 1.

3.3.2 Operating position.- The thyristor shall be capable of proper operation in any position.

3.3.3 Terminal-lead material and finish.- The terminal-lead material shall be Type K (Kovar) conforming to requirements in Standard MIL-STD-1276, except that a nickel under-plating of thickness: 20 microinches minimum, 100 microinches maximum, shall be used. The terminal-lead finish shall be gold (per pertinent requirements in Standard MIL-STD-1276); however, if so specified in the contract or order, the lead-material finish may be tin, or tin-coating over gold. This tin-finish requirement shall not be construed as affecting adversely the qualified-product status of the device, or applicable JAN marking. (See 6.3a herein.)

3.4 Performance characteristics.- The thyristor performance characteristics shall be as specified in Tables I, II, and III herein. Except where specifically differentiated for respective thyristor types (see 1.3, 1.4, and Tables I, II, III, and IV herein), the performance requirements, including operating characteristics, ratings, test conditions, and test limits, apply equally to all thyristor types covered herein.

3.4.1 "TX" special requirements.- Specified "TX" device-types shall, in addition to all other performance requirements herein, be process-conditioned, tested, and screened in accordance with 4.4 herein. (See 3.5.1 herein.) At option of the manufacturer, the non-TX device-types may be subjected to the same process-conditioning and testing.

3.5 Marking.- Except as otherwise specified herein, marking shall be in accordance with Specification MIL-S-19500. The "manufacturer's identification" and "country of origin" may, at option of the manufacturer, be omitted from being marked directly on the semiconductor device covered herein.

3.5.1 "TX" identification marking.- Marking of devices conforming to "TX" and all other applicable requirements herein (see 3.4.1) shall include the prefix "TX" immediately preceding the type designation.

4. QUALITY ASSURANCE PROVISIONS

4.1 General.- Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.2 Qualification and acceptance inspection.- Qualification and Quality Conformance inspection shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions, and as otherwise specified herein. Groups A, B, and C inspection shall consist of the examinations and tests specified in Tables I, II and III, respectively, herein. Quality Conformance inspection shall include inspection of Preparation for Delivery (see 5.1 herein).

4.2.1 Permissible Group B or Group C combined-subgroup testing.- At option of the manufacturer, all of the tests of one subgroup in Group B (Table II herein) may be combined with all of the tests in one or more other subgroup(s) of Group B for sequential performance; the same option applies to Group C (Table III herein) constituent subgroups. The sample size and accept-reject criteria for such combined-subgroup testing shall be based upon the most stringent, existing LTPD or lambda (λ) for one of the subgroups involved in the particular combination. The following administrative requirements shall apply hereto:

a. It shall be understood that the above option may be adopted by manufacturer for Qualification testing of product, or for Quality Conformance inspection of any individual lot submitted by manufacturer for lot acceptance.

b. Prior notification as to adoption of this testing option, and concurrent information as to the predesignated sample quantities to be used shall be made to the Government inspection authority concerned.

c. Complete record of the combined-subgroup testing-program results shall be maintained and be available to the Government inspection authority.

4.2.2 Qualification testing.- The non-TX device types shall be considered subject to Qualification tests. It shall be understood that procurement of the TX device types will be made from sources for the approved non-TX devices as listed in Qualified Products List (QPL)-19500. Upon request, and validation by the qualifying activity, qualification may be extended (and appropriate QPL-listing effected) to TX devices manufactured by approved sources for the non-TX devices.

4.2.2.1 Special Group A criteria for Qualification inspection.- For Qualification inspection, only 8 failures will be permitted for all Group A tests combined. Hereto, where the manufacturer deems that the data in paragraph 4.4.2 of Specification MIL-S-19500 are invokable, notification shall be made to the Chief, Components and Materials Standardization Branch, Procurement and Production Directorate, Fort Monmouth, New Jersey 07703, attention: AMSEL-PP-EM-2.

4.2.2.2 Groups B and C, and Life Test sampling and requirements for Qualification inspection.-

a. For lots containing more than one thyristor type covered herein, subjection of equal quantities (within the applicable LTPD size for the subgroup) of the highest and lowest voltage types represented in the lot to Groups B and C tests will be acceptable for determination of Qualification of those types and all intermediate types in the lot.

b. For Qualification inspection, continuous required (total-hours duration--through Group C requirement thereto) Life Test(s) shall be effective. (See 4.2.4 herein.)

4.2.3 Acceptance inspection of lots containing multiple thyristor types.- For lots containing more than one thyristor type covered herein, subjection of adequate samples on a sublot basis to customary Group A, B, and C testing shall be effective. (See 4.2.4 immediately below.)

4.2.4 Group B-Group C life test samples.- Samples of non-TX thyristor types, only, that have been subjected to Group B, 340-hour life test may be continued on test for 1000 hours in order to satisfy Group C life test requirements. These samples shall be predesignated, and shall remain subjected to the Group C, 1000-hour evaluation after they have passed the Group B, 340-hour acceptance criteria. The cumulative total of failures found during 340-hour test and during the subsequent interval up to 1000 hours shall be computed for 1000-hour acceptance. (See 4.2.5 below.) "TX" thyristor types shall be subjected to 1000-hour life tests under Group B inspection requirements, and the lambda (λ) established thereto in Table II shall apply.

4.2.5 Group C testing.- Group C tests shall be performed on a lot every 6 months. (See Table III herein.) The contractor shall, throughout the course of a contract or order, permit the Government representative to scrutinize all test data and findings covering manufacturer's test program on Group C characteristics and parameters for the product concerned. Upon determination by the Government inspector (in advance of Group C, 6-month, test results) that Group C parameters are not being adequately met, the Government inspector may require lot-by-lot inspection, normally for a minimum of 3 consecutive lots, to be performed for required Group C tests.

4.2.6 Disposition of sample units.- Sample units have been subjected to Group C, Subgroup 2 and 3 tests shall not be delivered on the contract or order. Sample units that have been subjected to and have passed Group B, Subgroups 1 through 6 and Group C, Subgroups 1, 4, 5 and 6 tests (these tests to be considered non-destructive), may be delivered on the contract or order provided that, after Group B and C inspection is terminated, those sample units are subjected to and pass Group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.2.7 Copies of lot-inspection data.- When specified in the contract or order, one copy of the Quality Conformance inspection data, including manufacturer's test data and findings, covering the device inspection lot being shipped shall accompany the device(s) concerned.

4.3 Particular examination and test requirements.-

4.3.1 Mechanical damage resulting from tests.- Except for intentionally deforming, mutilating, or dismembering mechanical-stress tests to which samples are subjected, there shall be no evidence of mechanical damage to any sample unit as a result of any of the Group A, B, or C tests.

4.3.2 End-point tests.- The test delineated in Table IV and the test limits specified therein shall apply wherever reference to "Table IV" is made herein. These end-point tests shall apply, equally, for a respective, newly-constituted "subgroup" resulting from the subgroup-combination option adopted by manufacturer in accordance with 4.2.1 herein.

4.3.3 Blocking Life Test.- With the thyristor connected into a circuit set-up as follows, the specified D.C. voltage shall be applied from anode to cathode. A thyristor (TUT) that triggers "on" during the specified test time or that fails to meet the specified end-point limits shall be considered a failure (see d, below).

a. The gate terminal shall be connected directly to cathode terminal.

b. The cell stud temperature shall be maintained at +150°C throughout the specified test time.

c. A 5-Kohm resistor shall be connected in series with the voltage power-supply in order to limit current in event of cell voltage breakdown.

d. A means of detecting triggered "on" devices (TUT) shall be incorporated in the test-circuit set-up.

4.4 Process conditioning, testing, and screening for "TX" devices.- All "TX" devices (100% of each lot) shall be subjected to the process conditioning, testing, and screening specified in 4.4.2 through 4.4.6.4 herein, in accordance with the procedural sequence established in Figure 2 herein, prior to submission of the lot to Group A, B, C tests. Those conditioning and screening tests normally performed by manufacturer as standard-production tests, need not be repeated when these are predesignated and acceptable to the Government as being equal to or more severe than those specified herein.

4.4.1 Quality Assurance records and determinations.- The manufacturer shall maintain and make available for perusal and review at any time, during a period of 3 years minimum, to the authorized Government representative or other contracting customer concerned, complete lot-by-lot records for these devices. All devices that fail to meet the process-conditioning, testing, and screening requirements specified herein shall be removed from the respective lot, and the test-failure identity and quantity removed shall be recorded in the permanent lot history. (See 6.3, 6.4, and 6.5 herein.)

4.4.2 High-temperature storage.- The thyristor shall be stored for at least 24 hours at a minimum temperature (Tstg) of +200°C.

4.4.3 Thermal shock (temperature cycling).- The thyristor shall be subjected to (thermal shock) temperature cycling in accordance with Standard MIL-STD-750, Method 1051, Test Condition C, except that $T_{(high)}$ shall be +175°C and the cycling duration shall be 10 continuous cycles and the exposure time at the temperature extremes shall be 15 minutes, minimum.

4.4.4 Acceleration.- The thyristor shall be subjected to the constant acceleration (centrifugal) test per Method 2006 in Standard MIL-STD-750, except that the following shall apply:

a. Centrifugal force = 20,000 G.

b. Orientation = Y1, only.

c. Hold time of 1 minute shall not apply hereto.

4.4.5 Seal (fine-leak) test.- The thyristors shall be subjected to the Seal test per Standard MIL-STD-202, Method 112, Test Condition C, procedure III a or III b (see 4.4.5.1 or 4.4.5.2 below), except that testing for gross leaks shall be in accordance with 4.4.5.3 below.

4.4.5.1 Conditions for procedure IIIa.- The sealed chamber in which the thyristors are placed shall be pressurized with helium gas to 50 psig, minimum, for a minimum of 4 hours. At end of that period, the thyristors shall be removed from the chamber and, within 30 minutes, be subjected to a helium leak-detection test. Those thyristors showing a leakage rate of 1×10^{-7} cc/sec of helium or greater, when measured at a differential pressure of 1 atmosphere, shall be rejected and removed from the lot.

4.4.5.2 Conditions for procedure IIIb.- The devices shall be placed in an activation tank, pressurized with Krypton 85 tracer gas in a nitrogen solution, for sufficient time to detect a leak rate of 1×10^{-8} atmospheric cubic centimeters per second (atm cc/sec). Within four hours after subjection to this pressurization, the leakage rate of the devices shall be determined on an attribute basis using the general equation shown below. Any device exhibiting a leak rate equal to or greater than 1×10^{-8} atm cc/sec shall be rejected and removed from the lot. The general equation for use with radioactive-gas leak test equipment is:

$$Q = \frac{R}{SKT(P_e^2 - P_i^2)}$$

where:

- Q = leak rate in atm cc/sec.
- R = net counting rate of tested part above background in cts/min.
- S = specific activity of the test gas mixture in uCi/atm cc.
- K = counting efficiency of the system for the given part in cts/min uCi.
- P_e = pressure of test gas in activation tank during pressurization in atm abs.
- P_i = pressure inside part under test in atm abs.
- T = duration of pressurization in test gas mixture in seconds.

4.4.5.3 Gross Leak test.- The thyristors shall be subjected to gross-leak evaluation in accordance with requirements of Method 1071, Test Condition A, C, or D, in Standard MIL-STD-750.

4.4.6 Burn-in conditioning, tests, and evaluation (screening).- To enable proper evaluation of the thyristors conditioned and tested in accordance with the following requirements, each thyristor and lot shall be handled or identified in such a manner that results for each individual thyristor and lot can be ascertained and recorded.

4.4.6.1 Pre burn-in measurements.- The thyristor shall be tested for the characteristics listed in Table IV below, and the values found shall be recorded. Those thyristors that fail to meet specified limits shall be rejected and removed from the lot.

Table IV. Pre Burn-In Measurements.

Test Method per MIL-STD-750	Examination or Test 1/	Test Conditions	Symbol	Limits Min	Limits Max	Unit
4211	Reverse blocking current:	D.C.Method Bias Cond. B; R_2=1 Kohms				
	2N3027, 2N3030	V_{RBXM}=30Vdc	i_{RBXM}	---	0.05	uAdc
	2N3028, 2N3031	V_{RBXM}=60Vdc	i_{RBXM}	---	0.05	uAdc
	2N3029, 2N3032	V_{RBXM}=100Vdc	i_{RBXM}	---	0.05	uAdc
4206	Forward blocking current:	D.C. Method Bias Cond B; R_2=1 Kohms				
	2N3027, 2N3030	V_{FBXM}=30Vdc	i_{FBXM}	---	0.02	uAdc
	2N3028, 2N3031	V_{FBXM}=60Vdc	i_{FBXM}	---	0.02	uAdc
	2N3029, 2N3032	V_{FBXM}=100Vdc	i_{FBXM}	---	0.02	uAdc
4221	Gate trigger voltage:	V_2=5V R_L=100 ohms R_e=100 ohms 1/				
	2N3027, 8, 9		V_{GT}	0.40	0.80	Vdc
	2N3030, 1, 2		V_{GT}	0.44	0.60	Vdc
4221	Gate trigger current:	V_2=5V R_L=100 ohms R_e=10 Kohms 1/				
	2N3027, 8, 9		I_{GT}	-5	200	uAdc
	2N3030, 1, 2		I_{GT}	-5	20	uAdc

1/ Gate connected to cathode across 1-Kohm resistor.

4.4.6.2 Burn-in conditioning.- The thyristors shall be operated under the following conditions for 72±4 hours. Thyristors which turn "on" during this burn-in conditioning shall be rejected and removed from the lot (see 4.4.6.4 below).

$T_A = +125^{\circ}C$

$R_2 = R_{GK} = 1$ Kohms

2N3027, 2N3030: v_{FBXM}=30 V

2N3028, 2N3031: v_{FBXM}=60 V

2N3029, 2N3032: v_{FBXM}=100 V

4.4.6.3 Post burn-in tests and measurements.- After burn-in conditioning, the thyristors shall be permitted to return to room-ambient temperature thermal-equilibrium and retested, within a maximum total elapsed time of 96 hours, for the characteristics listed in Table IV above. The values now found for each individual thyristor shall not exceed the following (respectively applicable to the pre burn-in measurements per Table IV above):

$\Delta i_{RBXM} = \pm 0.010$ uAdc

$\Delta i_{FBXM} = \pm 0.005$ uAdc

4.4.6.4 Burn-in conditioning evaluation (screening).- Those thyristors whose measured characteristics exceed the delta (Δ) limits specified in 4.4.6.3, above, or the limits of Table IV, shall be rejected and removed from the lot. The entire lot shall be considered non-acceptable as "TX" devices when 10% or more failures, among all the thyristors subjected to burn-in conditioning and tests, are encountered as follows:

a. Those thyristors which turned "on" during burn-in conditioning per 4.4.6.2 above; plus

b. Those thyristors found to exceed the delta (Δ) limits per 4.4.6.3 above, or the limits of Table IV (during post burn-in measurement).

Table I. Group A inspection.

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		10	10				
2071	Visual and mechanical examination	---			---	---	---	---
	Subgroup 2		5	2				
4211	Reverse blocking current:	D.C. Method Bias Cond B; R_2=1 Kohms						
	2N3027, 2N3030	V_{RBXM}=30 Vdc			i_{RBXM}	---	0.05	uAdc
	2N3028, 2N3031	V_{RBXM}=60 Vdc			i_{RBXM}	---	0.05	uAdc
	2N3029, 2N3032	V_{RBXM}=100 Vdc			i_{RBXM}	---	0.05	uAdc
4206	Forward blocking current:	D.C. Method Bias Cond.B; R_2=1 Kohms						
	2N3027, 2N3030	V_{FBXM}=30 Vdc			i_{FBXM}	---	0.02	uAdc
	2N3028, 2N3031	V_{FBXM}=60 Vdc			i_{FBXM}	---	0.02	uAdc
	2N3029, 2N3032	V_{FBXM}=100 Vdc			i_{FBXM}	---	0.02	uAdc
4219	Reverse gate current (D.C.)	V_{KG}=5 Vdc			I_{KG}	---	0.1	mAdc
4221	Gate trigger current:	V_2=5 V R_L=100 ohms $R_\bullet$=10 Kohms 2/						
	2N3027, 8, 9				I_{GT}	-5	200	uAdc
	2N3030, 1, 2				I_{GT}	-5	20	uAdc
4221	Gate trigger voltage:	V_2=5V R_L=100 ohms $R_\bullet$=100 ohms 2/						
	2N3027, 8, 9				V_{GT}	0.40	0.80	Vdc
	2N3030, 1, 2				V_{GT}	0.44	0.60	Vdc

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 2 - (cont'd)							
4226	Forward "on" voltage	i_{FM}=1A (pulse) PW=250 usec Duty cycle= 2% max			V_{FM}	0.8	1.5	Vdc
4201	Holding current:	Bias Cond. B; R_3=1 Kohms V_{AA}=24 Vdc I_{F1}=100 mAdc I_{F2}=10 mAdc Gate trigger source volt.= 6V; R_2=330 ohms						
	2N3027, 8, 9				I_{HOX}	0.3	5.0	mAdc
	2N3030, 1, 2				I_{HOX}	0.3	4.0	mAdc
	Subgroup 3		5	3				
4231	Exponential rate of voltage rise:	T_A=+25°C Bias Cond. B; R_3=1 Kohm C=0.005 uf R_L=10 ohms Rep. rate= 60 pps; f=60 Hz Test duration= 15 sec.						
	2N3027, 2N3030	V_{AA}=30 Vdc; dv/dt=30 V/ usec			V_{FBX}	27	---	Vdc

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 3-(Cont'd)							
	2N3028, 2N3031	V_{AA}=60 Vdc; dv/dt=15V/usec			V_{FBX}	54	---	Vdc
	2N3029, 2N3032	V_{AA}=100 Vdc; dv/dt=10V/usec			V_{FBX}	90	---	Vdc
---	Forward blocking recovery time:	Test circuit and procedure per Fig. 3 herein. i_{FM}=1A i_{RM}=1A R_{GK}= 1 Kohms t_p=100 usec			t_{fbr}	---	2.0	usec
---	Gate trigger-on pulse width:	Test circuit and procedure per Fig. 4 herein V_{AA}=30 V i_{FM}=1A i_{GF}=10 mA						
	2N3027, 8, 9				t_{pg}(on)	---	0.2	usec
	2N3030, 1, 2				t_{pg}(on)	---	0.1	usec

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4		5	3				
3/	High temperature operation:	T_A=+150°C 4/						
4206	Forward blocking current:	D.C. Method Bias Cond. B; R_2=1 Kohms						
	2N3027, 2N3030	V_{FBXM}=30 Vdc			i_{FBXM}	---	20	uAdc
	2N3028, 2N3031	V_{FBXM}=60 Vdc			i_{FBXM}	---	20	uAdc
	2N3029, 2N3032	V_{FBXM}=100 Vdc			i_{FBXM}	---	20	uAdc
4211	Reverse blocking current:	D.C. Method Bias Cond. B; R_2=1 Kohms						
	2N3027, 2N3030	V_{RBXM}=30 Vdc			i_{RBXM}	---	50	uAdc
	2N3028, 2N3031	V_{RBXM}=60 Vdc			i_{RBXM}	---	50	uAdc
	2N3029, 2N3032	V_{RBXM}=100 Vdc			i_{RBXM}	---	50	uAdc
4221	Gate trigger voltage:	V_2=5V R_L=100 ohms Re=100 ohms 2/						
	2N3027, 8, 9				V_{GT}	0.1	0.6	Vdc
	2N3030, 1, 2				V_{GT}	0.1	0.4	Vdc

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4-(cont'd).							
4201	Holding Current	Bias Cond. B; R_3=1 Kohms V_{AA}=24 Vdc I_{F1}=100 mAdc I_{F2}=10 mAdc Gate trigger source volt.=6V; R_2=330 ohms			I_{HOX}	0.05	---	mAdc
---	Low temperature operation:	T_A=65°C 4/						
4221	Gate trigger voltage:	V_2=5V R_L=100 ohms Re=100 ohms 2/						
	2N3027, 8, 9				V_{GT}	0.6	1.10	Vdc
	2N3030, 1, 2				V_{GT}	0.44	0.95	Vdc
4221	Gate trigger current:	V_2=5V R_L=100 ohms Re=10 Kohms 2/						
	2N3027, 8, 9				I_{GT}	0	1.2	mAdc
	2N3030, 1, 2				I_{GT}	0	0.5	mAdc

Table I. Group A inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4-(cont'd).							
4201	Holding current:	Bias Cond. B; R_3=1 Kohms V_{AA}=24 Vdc I_{F1}=100 mAdc I_{F2}=10 mAdc Gate trigger source voltage=6V; R_2=330 ohms						
	2N3027, 8, 9				I_{HOX}	0.5	10.0	mAdc
	2N3030, 1, 2				I_{HOX}	0.5	8.0	mAdc

1/See 3.4 and 4.2.3 herein.

2/Gate connected to cathode across 1-Kohm resistor.

3/In this Subgroup, the sample units subjected to the High-Temperature Operation test shall be permitted to return to and be stabilized at room ambient temperature prior to their being subjected to the Low-Temperature Operation test.

4/Measurement(s) shall be made after thermal equilibrium has been reached at the temperature specified.

Table II. Group B inspection.

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		10	10				
2066	Physical dimensions	---			---	---	---	---
	Subgroup 2		10	10				
2026	Solderability	---			---	---	---	---
1051	Temperature cycling	Test Cond. C			---	---	---	---
1056	Thermal shock (glass strain)	Test Cond. A			---	---	---	---
2006	Constant acceleration (centrifugal).	20,000 G Orientations Y1, Y2, Z1			---	---	---	---
1021	Moisture resistance	No initial conditioning			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							
	Subgroup 3		10	10				
4066	Surge current	i_{FM}(surge)= 8 Adc I_F=200 mAdc t=8 msec ea. surge 10 surges (½-sine wave ea.) at 1-minute intervals			---	---	---	---

Table II. Group B inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4		10	5				
2/	Blocking life	T_A=+150°C t=168$^{+4}_{-0}$ hrs V_{FBXM}=rated value ea. type (see 1.3 herein)			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							
	Subgroup 5		10	λ=10				
1031	High-temperature life (non-operating)	T_{stg}=+200°±3°C t=340 hrs R_{GK}=0 3/			---	---	---	---
	End Point tests: Per Table IV (see 4.3.2 herein)							

Table II. Group B inspection - (Cont'd).

Test Method per MIL-STD-750	Examination or Test 1/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 6		20	λ=10				
---	Operating life	Test circuit and procedure per Fig. 5 herein T_A=+100°C V_{FBXM}=rated value ea. type (see 1.3 herein) I_0=175 mAdc t=340 hrs;3/			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							

1/ See 3.4, 4.2.1, 4.2.3, and 4.3.2 herein.

2/ See 4.3.3 herein.

3/ See 4.2.4 herein.

Table III. Group C inspection.[1]

Test Method per MIL-STD-750	Examination or Test [2]	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		10	10				
2016	Shock	Non-operating 1500 G 5 blows of 0.5 msec ea. in orientations Y1, Y2, Z1 (total=15 blows)			---	---	---	---
2056	Vibration, variable frequency	---			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							
	Subgroup 2		15	15				
1041	Salt atmosphere (corrosion)	[3]			---	---	---	---
	Subgroup 3		15	15				
2036	Terminal strength, Lead fatigue	Test Cond. E [3]			---	---	---	---
	End-Point tests:							
[4]	Seal (leak rate)	---			---	---	---	---

Table III. Group C inspection - (Cont'd).[1/]

Test Method per MIL-STD-750	Examination or Test 2/	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4		10	10				
4231	Exponential rate of of voltage rise (at high temp.):	T_A=+125°C Bias Cond. B; R_3=1 Kohm C=0.005 uF R_L=10 ohms Rep. rate= 60 pps; f=60 Hz Test duration= 15 sec.						
	2N3027, 2N3030	V_{AA}=30 Vdc; dv/dt=5V/ usec			V_{FBX}	27	---	Vdc
	2N3028, 2N3031	V_{AA}=60 Vdc; dv/dt=3V/ usec			V_{FBX}	54	---	Vdc
	2N3029, 2N3032	V_{AA}=100 Vdc; dv/dt=2V/ usec			V_{FBX}	90	---	Vdc
	Subgroup 5		λ=10	---				
1031	High-temperature life (non-operating)	T_{stg}=+200±3°C t=1000 hrs R_{GK}=0 5/			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							

Alternately for surface mount (US) devices, a minimum of three evenly spaced contrasting color dots a

Table III. Group C inspection - (Cont'd).[1]

Test Method per MIL-STD-750	Examination or Test [2]	Conditions	LTPD Non-TX	LTPD TX	Symbol	Limits Min	Limits Max	Unit
	Subgroup 6		λ=10	---				
---	Operating life	Test circuit and procedure per Fig. 5 herein T_A=+100°C V_{FBXM}=rated value ea. type (see 1.3 herein) I_D=175 mAdc [5]			---	---	---	---
	End-Point tests: Per Table IV (see 4.3.2 herein)							

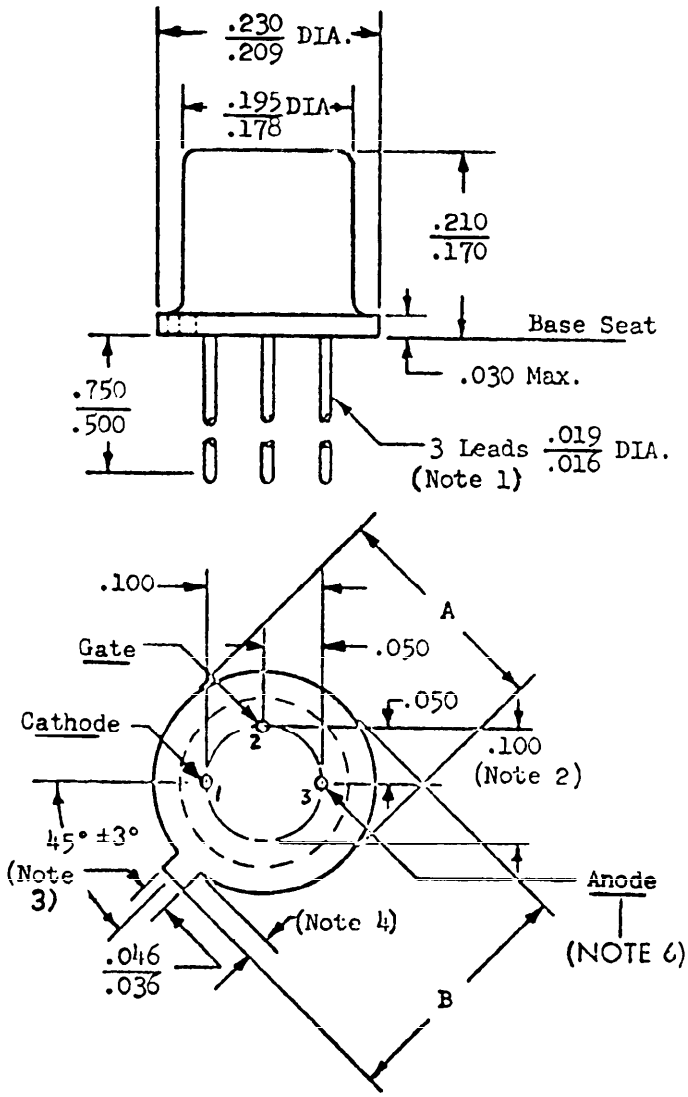
[1] See 4.2.5 herein.

[2] See 3.4, 4.2.1, 4.2.3 and 4.3.2 herein.

[3] Electrical rejects from the same lot under evaluation may be used for this test.

[4] See 4.4.5 herein.

[5] See 4.2.4 herein.



Notes:

1. The specified lead diameter applies to the zone between .050 and .250 from the base seat. Between .250 and end of lead a maximum of .021 is held. Outside of these zones the lead diameter is not controlled.

2. Maximum diameter leads at a gaging plane .054 +.001 -.000 below base seat to be within .007 of their true location relative to Max. width tab and to the maximum .230 diameter measured with a suitable gage. When gage is not used, measurement will be made at base seat.

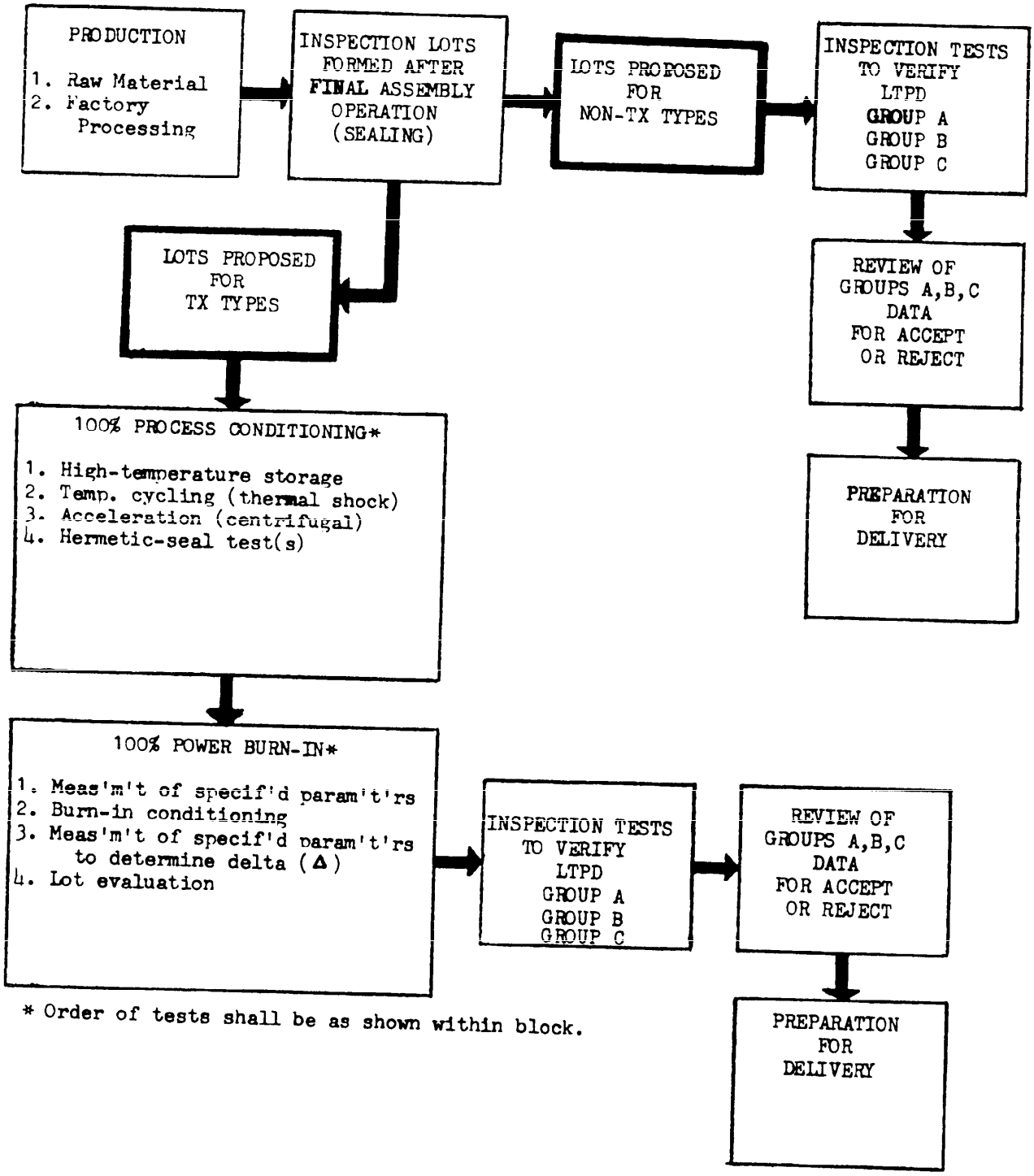
3. Index tab for visual orientation only.

4. Tab length to be .028 minimum -- .048 maximum, and will be determined by subtracting diameter A from dimension B.

5. All dimensions in inches.

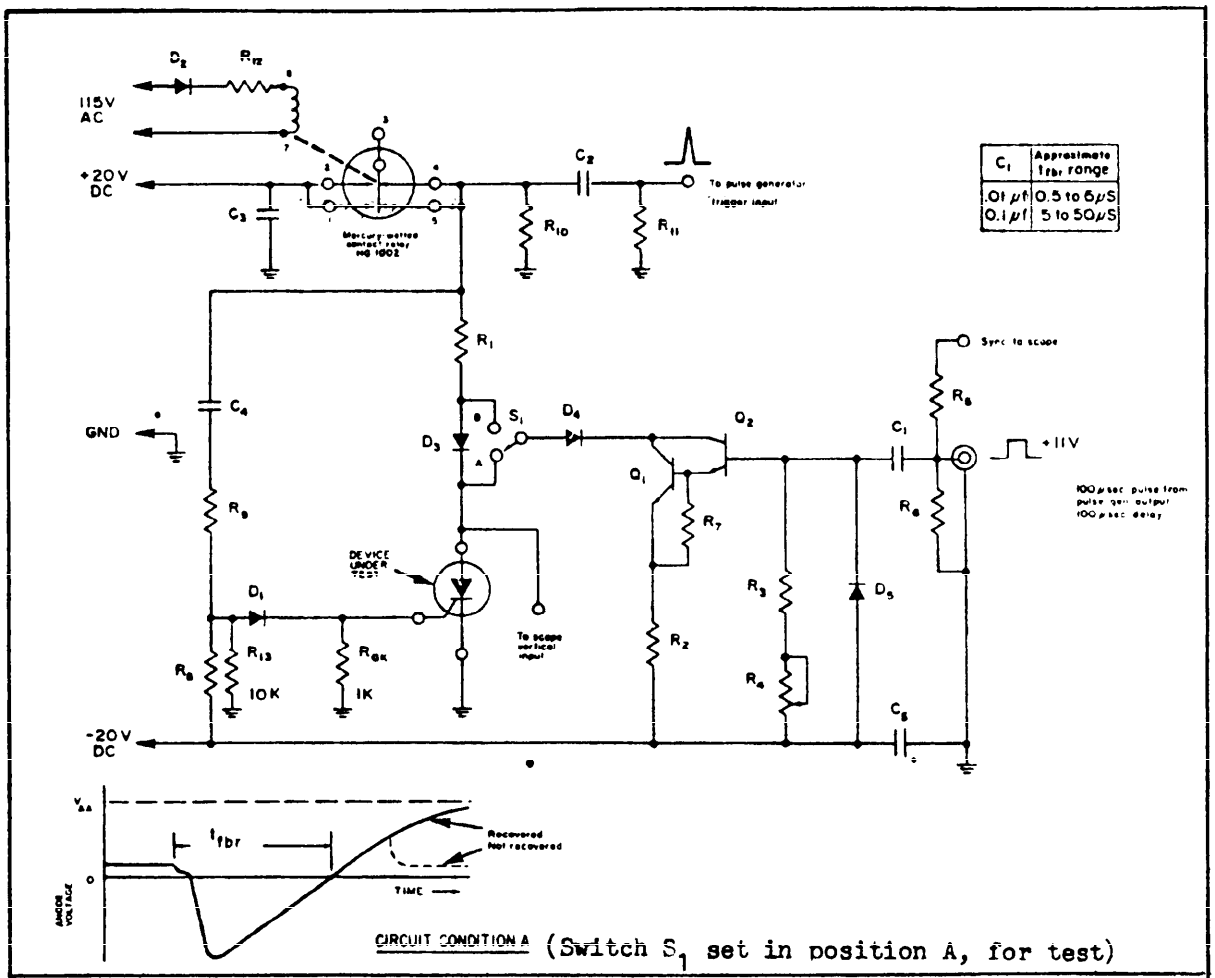
6. Anode is internally connected to the case.

Figure 1. Outline and dimensions.



* Order of tests shall be as shown within block.

Figure 2. Flow chart for non-TX and TX types.



C_1	Approximate t_{fbr} range
.01 μf	0.5 to 6 μS
0.1 μf	5 to 50 μS

Legend of circuit elements:

(See note b)

R_1 - 20Ω
R_2 - 5Ω
R_3 - 100Ω
R_4 - 1K
R_5 - 10K
R_6 - 47Ω
R_7 - 270Ω
R_8 - 27K
R_9 - 1.8K
R_{10} - 1K
R_{11} - 47Ω
R_{12} - 33K
R_{13} - 10K

D_1 - 1N457A
D_2 - 1N1763
D_3 - FD200
D_4 - FD200
D_5 - 1N457A

C_1 - (see table)
C_2 - .01μf
C_3 - 1μf
C_4 - .005μf
C_5 1μf
Q_1 - 2N2854
Q_2 - 2N656A

NOTES:

a. Guidance for testing procedure: on following page(s).
b. Discussion of test circuit: on following pages.

Figure 3. Forward Blocking Recovery Time test circuit and procedural details.

A. t_{fbr} Test Procedure:

1. As the first step in the testing procedure, a pulse generator synced from the test circuit as shown, delivers a 100-usec wide pulse, delayed from the sync pulse by 100 usec, to the defined input point for turn-off of the thyristor under test. ("Circuit Condition A" illustrated in the circuit diagram is the driven-off mode of device operation.) A high-frequency oscilloscope is used to observe the anode voltage of the test device. Capacitor C_1 sets the recovery-time range of the circuit (different values of C_1 are employed to alter the recovery-time range of the circuit); and potentiometer R_4 adjusts the rate of reapplication of forward blocking voltage.

2. The forward blocking recovery time is the time measured from the leading edge of the turn-off pulse to the test device to the time when forward blocking voltage is reapplied. R_4 is adjusted to the point where the device under test turns off each time a turn-off pulse is delivered. (See paragraph B5, below.)

B. t_{fbr} Test-Circuit Analysis:

1. In this circuit, the rate of rise of reapplication of forward blocking voltage (dv/dt) is directly proportional to the measured recovery time. The exponential time constant equals 1.4 times the forward blocking recovery time, which is identical to the many practical circuit applications where the anode is driven negative through a commutating capacitor. (This test circuit allows infinite variation of the exponential turn-off waveform for precise measurements of t_{fbr} which is impossible to achieve by capacitor substitution methods.)

2. With S_1 in position A (see circuit diagram), the anode of the device under test is driven nagative by a current source, resulting in an instantaneous reverse anode current (i_R) which sweeps some of the stored charge out of the device. Anode supply voltage is applied through the contacts of a mercury-wetted contact relay which switches back and forth at power line frequency. All contacts of this relay are momentarily shorted together, for an interval less than 1 millisecond, twice during each line cycle. (This results in a 10% duty cycle which minimizes self heating in the device under test and provides much greater measurement accuracy than with DC test methods.)

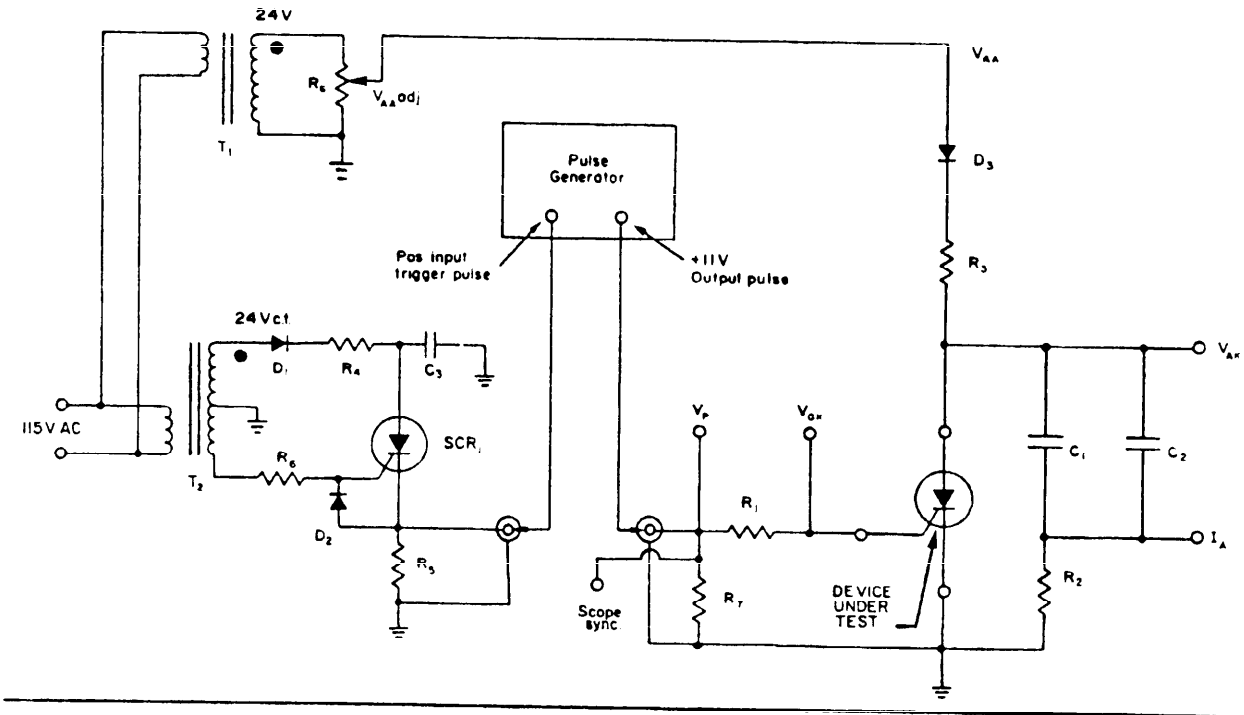
Fig. 3-(Cont'd).- t_{fbr} test circuit and procedural details.

3. Each time the contacts of the mercury relay close, a 10-microsecond wide pulse is delivered through D_1 to the gate of the device under test, turning it on, and at the same time providing a trigger pulse to the pulse generator. The pulse generator supplies a turn-off pulse after a delay of 100 microseconds. During this 100-microsecond period, the device under test conducts forward current (i_F) established by R_1 and the anode supply-voltage (1 Ampere, as shown). This is sufficient time for steady-state conduction to be established, and for D_1 to isolate the gate circuit so that R_{GK} sets the bias condition for the test device.

4. After the 100 microsecond delay period, the pulse generator delivers a 100-microsecond wide 11-volt turn-off pulse. This pulse is differentiated by C_1, R_3, and R_4, and applied to the base of Q_2, developing a 10-volt peak exponential waveform across resistor R_2. The collectors of Q_1 and Q_2 deliver a 2-ampere peak negative current through D_4, so that at this terminal a net negative short-circuit of 1 ampere is applied to the anode of the device under test. The test device will conduct this reverse current for a period of time known as the reverse recovery time, (or turn-off time), during which some of the stored charge is swept out of the device. The anode voltage will then drop to a negative value and commence to go positive in an exponential manner as the negative current source decays exponentially.

5. When the anode voltage crosses zero (proceeding exponentially toward the positive anode supply voltage), if the remaining stored charge is not sufficiently dissipated the device will self-trigger and remain on until the mercury relay contacts finally open. Increasing R_4 will lengthen the exponential time constant until the device regains its forward blocking capability. With R_4 adjusted to this point, the forward blocking recovery time is measured from the leading edge of the output pulse generator to the time the anode voltage crosses zero. (See paragraph A2, above.)

Fig. 3 - (Cont'd).- t_{fbr} test circuit and procedural details.-(Cont'd).



Legend of circuit elements:

R_1 - 1K	R_6 - 2.7 K	C_1 - 1μf
R_2 - 30Ω, non-inductive	R_7 - 56 Ω	C_2 - 0.1μf, ceramic
R_3 - 500Ω, 2W	R_8 - 1K, 2W	C_3 - 0.1μf
R_4 - 1K	SCR_1 - AA100	T_1 - 115V to 24V Step-down transformer
R_5 - 100Ω	D_1, D_2, D_3 - 1N457A	T_2 - 115V to 24V C.T. Step-down transformer

t_{pg} (on) Test Procedure:

1. With specified V_{AA}, i_F, and i_{GF} initially established, connect a high-frequency oscilloscope vertical input to the I_A monitor point. The width of the gate current pulse is then set to a valve that causes triggering to occur.
2. (See applicable waveform depiction on following page.) The waveform shown for the I_A monitor should be observed. The width of the gate current pulse is then gradually reduced to the point where triggering no longer occurs. The pulse width at this point is the gate trigger-on pulse width.

Fig. 4. Gate Trigger-On Pulse Width test circuit and procedural details.

Circuit Waveforms: t_{pg} (on) Test

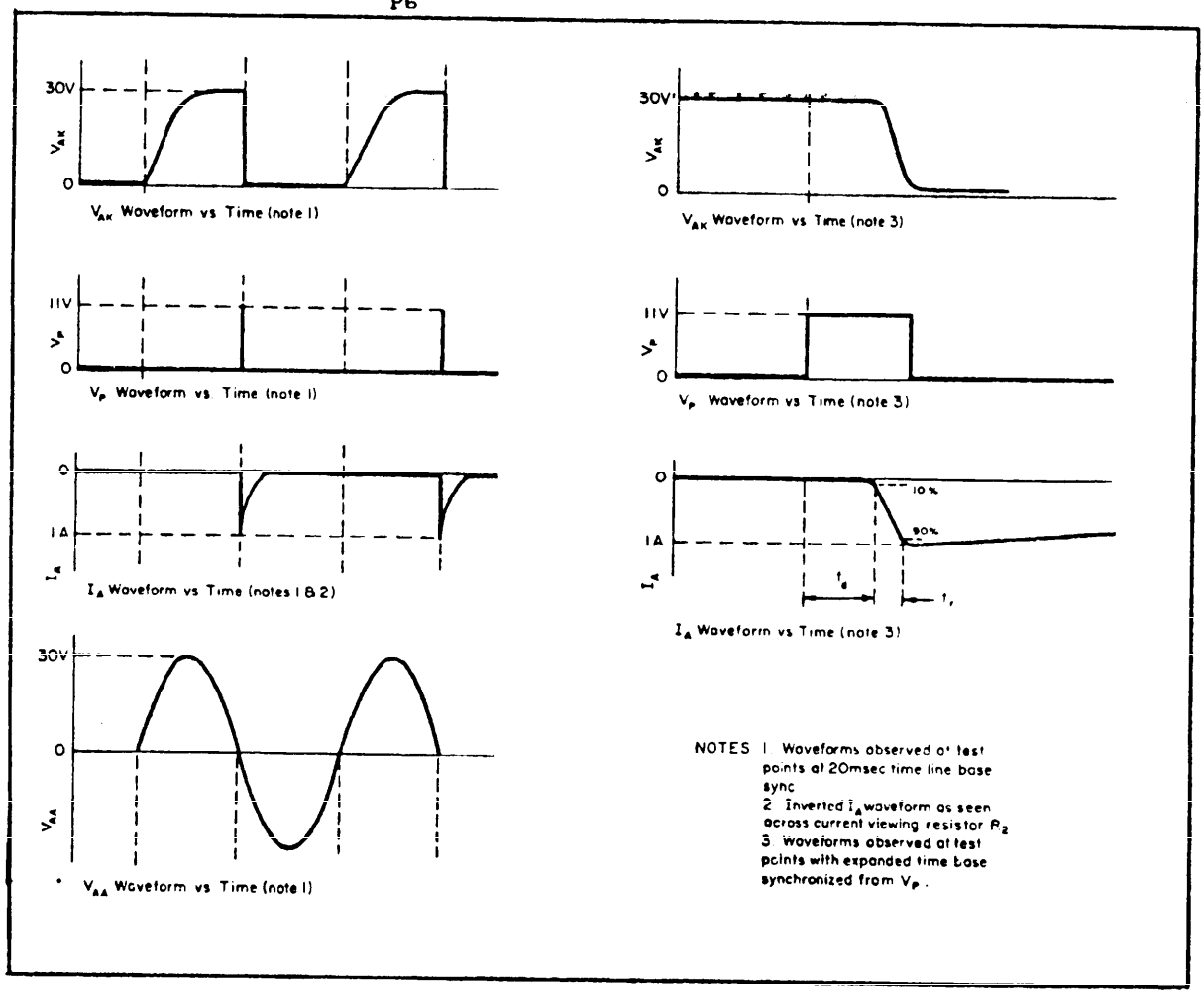
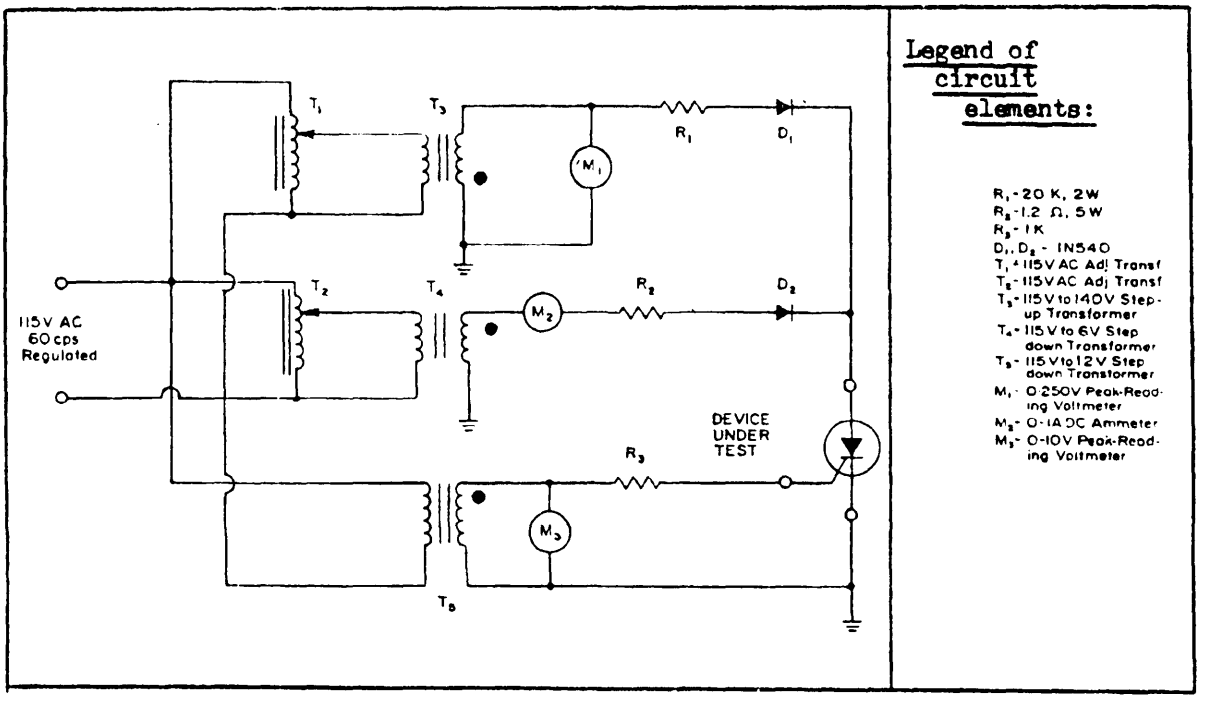


Fig. 4 - (Cont'd).- t_{pg} (on) test circuit and procedural details.



NOTES:

1. The above circuit provides for a mode of operation in which the thyristor under test is subjected alternately to an 8-msec conduction period and an 8-msec forward-blocking period.

PROCEDURAL DETAILS:

1. The general procedural guidances of Method 1036 in Standard MIL-STD-750 apply.
2. Under conformity with specified test conditions:
   a. Transformer T_1 is adjusted to provide a peak secondary voltage from T_3 equal to the specified forward blocking voltage.
   b. Transformer T_2 is adjusted so that the specified average rectified forward current is read on meter M_2.
   c. Transformer T_5 should provide a maximum of 5V, as read on meter M_3, for device triggering.

Figure 5. Operating Life test circuit and procedural details.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery.- Preparation for delivery and the inspection of Preparation For Delivery shall be in accordance with Specification MIL-S-19500.

6. NOTES

6.1 Notes.- The notes included in Specification MIL-S-19500, with the following additions or exceptions, are applicable to this specification.

6.2 Application guidance.-

a. To insure proper equipment-circuit application, particular attention should be given to the differential control (blocking and gate triggering) voltages pertinent to the individual thyristor types covered herein.

b. The thyristors covered herein are intended for single-sided circuit-board wire-in; when used in double-sided circuit-board applications where solder bridging might occur, a dielectric washer or other standoff device to implement the wire-in of the thyristor(s) should be considered.

6.3 Ordering data.-

a. Terminal-lead finish: See 3.3.3 herein.

b. Lot-inspection data: See 4.2.7 herein.

6.4 Procurement of "TX" types.- See 4.2.2 herein.

6.5 Quality assurance for "TX" types.- It is expected that where the permanent lot record, maintained as required in 4.4.1 herein, begins to show a condition of failures in excess of the LTPD rate specified herein, or a condition of entire-lot rejection (see 4.4.6.4 herein) is recorded, the Government procuring activity will determine any additional monitoring controls and evaluation criteria needed to attain restoration of the prescribed (herein) quality assurance for acceptance of product.

6.6 Qualification.- With respect to products requiring qualification, awards will be made only for such products as have, prior to the time set for opening of bids, been tested and approved for inclusion in Qualified Products List (QPL)-19500, whether or not such products have actually been so listed by that date. Information pertaining to qualification of products covered by this specification should be requested from the Commanding General, U. S. Army Electronics Command, Fort Monmouth, New Jersey 07703, Attention: AMSEL-PP-EM-2.

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SPECIFICATION MIL-S-19500/419(EL) THYRISTOR (CONTROLLED RECTIFIER), SILICON TYPES 2N3027 THROUGH 2N3032, AND TX2N3027 THROUGH TX2N3032

ORGANIZATION

CITY AND STATE

CONTRACT NUMBER

MATERIAL PROCURED UNDER A

☐ DIRECT GOVERNMENT CONTRACT ☐ SUBCONTRACT

1. HAS ANY PART OF THE SPECIFICATION CREATED PROBLEMS OR REQUIRED INTERPRETATION IN PROCUREMENT USE?

A. GIVE PARAGRAPH NUMBER AND WORDING.

B. RECOMMENDATIONS FOR CORRECTING THE DEFICIENCIES

2. COMMENTS ON ANY SPECIFICATION REQUIREMENT CONSIDERED TOO RIGID

3. IS THE SPECIFICATION RESTRICTIVE?

☐ YES ☐ NO *(If "yes", in what way?)*

4. REMARKS *(Attach any pertinent data which may be of use in improving this specification. If there are additional papers, attach to form and place both in an envelope addressed to preparing activity)*

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