The documentation and process conversion measures necessary to comply with this document shall be completed by 10 August 2004

INCH-POUND

MIL-PRF-19500/357H
10 May 2004
MIL-PRF-19500/357G
29 August 2002

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, AMPLIFIER TYPES 2N3634 THROUGH 2N3637, 2N3634UB THROUGH 2N3637UB, 2N3634L THROUGH 2N3637L, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, low-power amplifier, and switching transistors. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for unencapsulated devices.

1.2 Physical dimensions. See figure 1 (TO-5 and TO-39), figure 2 (UB), and figure 3 (JANHC and JANKC).

* 1.3 Maximum ratings, unless otherwise specified T_A = +25°C.

Types	P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	P_T (3) T_{SP} = +25°C	$R_{\theta JA}$	$R_{\theta JC}$	$R_{\theta JSP}$	I_C	T_J and T_{STG}	V_{CBO}	V_{CEO}	V_{EBO}
	W	W	W	°C/W	°C/W	°C/W	A dc	°C	V dc	V dc	V dc
2N3634, 2N3634L,	1	5	N/A	175	35	N/A	1	-65 to	140	140	5
2N3634UB	1	N/A	1.5	175	N/A	90	1	+200	140	140	5
2N3635, 2N3635L,	1	5	N/A	175	35	N/A	1		140	140	5
2N3635UB	1	N/A	1.5	175	N/A	90	1		140	140	5
2N3636, 2N3636L,	1	5	N/A	175	35	N/A	1		175	175	5
2N3636UB	1	N/A	1.5	175	N/A	90	1		175	175	5
2N3637, 2N3637L,	1	5	N/A	175	35	N/A	1		175	175	5
2N3637UB	1	N/A	1.5	175	N/A	90	1		175	175	5

(1) See figure 4.
(2) See figure 5.
(3) See figure 6.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://www.dodssp.daps.mil.

1.4 Primary electrical characteristics at T_A = +25°C.

Types	h_{FE} at V_{CE} = 10 V dc							$\|h_{fe}\|$		C_{obo}
	h_{FE1} I_C = 0.1 mA dc (1)	h_{FE2} I_C = 1.0 mA dc (1)	h_{FE3} I_C = 10 mA dc (1)	h_{FE4} I_C = 50 mA dc (1)		h_{FE5} I_C = 150 mA dc (1)		V_{CE} = 30 V dc I_C = 30 mA dc f = 100 Mhz		V_{CB} = 20 V dc I_E = 0 100 Khz ≤f ≤ 1 Mhz
	Min	Min	Min	Min	Max	Min	Max	Min	Max	Max
2N3634, 2N3634L,	25	45	50	50	150	30		1.5	8.0	10
2N3634UB	25	45	50	50	150	30		1.5	8.0	10
2N3635, 2N3635L,	55	90	100	100	300	60		2.0	8.5	10
2N3635UB	55	90	100	100	300	60		2.0	8.5	10
2N3636, 2N3636L,	25	45	50	50	150	30		1.5	8.0	10
2N3636UB	25	45	50	50	150	30		1.5	8.0	10
2N3637, 2N3637L,	55	90	100	100	300	60		2.0	8.5	10
2N3637UB	55	90	100	100	300	60		2.0	8.5	10

	$V_{CE(sat)1}$ I_C = 10 mA dc (1) I_B = 1 mA dc	$V_{CE(sat)2}$ I_C = 50 mA dc (1) I_B = 5 mA dc	$V_{BE(sat)1}$ I_C = 10 mA dc (1) I_B = 1 mA dc	$V_{BE(sat)2}$ I_C = 50 mA dc 1/ I_B = 5 mA dc	Switching parameters			
					t_d	t_r	t_s	t_f
	V dc	V dc	V dc	V dc	ns	ns	ns	ns
Minimum				0.65				
Maximum	0.3	0.6	0.8	0.90	100	100	500	150

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

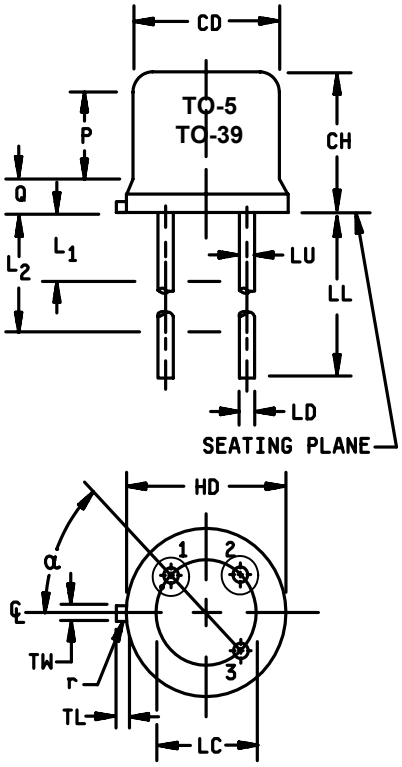
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://www.dodssp.daps.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

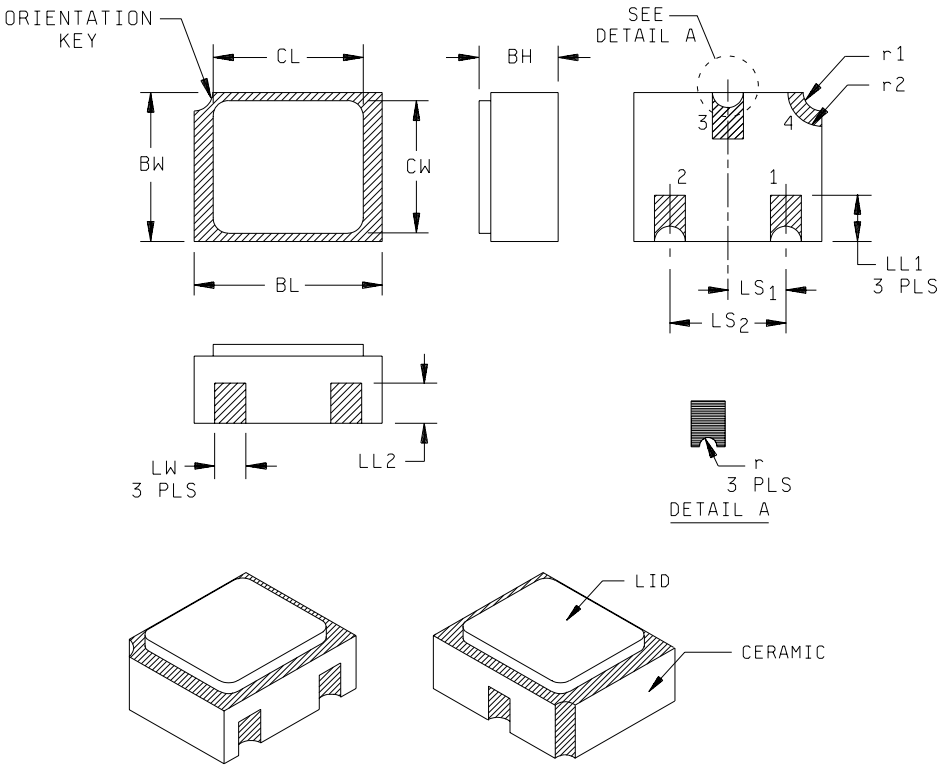
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TYP		5.08 TYP		7
LD	.016	.021	0.41	0.53	6
LL	See notes 7, 9, and 10				
LU	.016	.019	0.41	0.48	7
L1		.050		1.27	7
L2	.250		6.35		7
P	.100		2.54		5
Q		.050		1.27	
r		.010		0.254	8
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
α	45° TP		45° TP		6
Term 1	Emitter				
Term 2	Base				
Term 3	Collector				



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r maximum, TW must be held to a minimum length of .021 inch (0.53 mm).
4. TL measured from maximum HD.
5. CD shall not vary more than ±.010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 - .055 inch (1.37 - 1.40 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at a maximum material condition (MMC) relative to the tab at MMC. The device may be measured by direct methods or by gauge and gauging procedure.
7. LU applies between L1 and L2. LD applies between L2 and L minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. r (radius) applies to both inside corners of tab.
9. For transistor types 2N3634 through 2N3637, LL is .500 inch (12.70 mm) minimum, and .750 inch (19.50 mm) maximum (TO-39).
10. For transistor types 2N3634L through 2N3637L, LL is 1.500 inches (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum (TO-5).
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

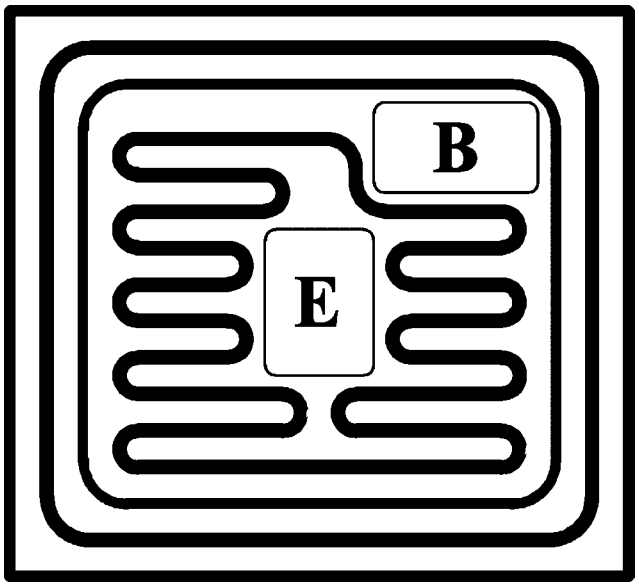
FIGURE 1. Physical dimensions (TO-5 and TO-39).



Symbol	Dimensions				Note	Symbol	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.039	0.89	0.99	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL	.115	.128	2.92	3.25		r		.008		0.20	
CW	.085	.108	2.16	2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 2. Physical dimensions, surface mount 2N3634UB through 2N3637UB (UB version).



1. Chip size.....24 x 26 mils ± 2 mils.
2. Chip thickness.....10 ± 1.5mils nominal.
3. Top metal.....Aluminum 15,000Å minimum, 18,000Å nominal.
4. Back metal.....A. Al/Ti/Ni/Ag 12kÅ/3kÅ/7kÅ/7kÅmin.,15kÅ/5kÅ/10kÅ/10kÅ nominal.
   B. Gold 2,500Å minimum, 3,000Å nominal.
   C. Eutectic Mount – No Gold.
5. Backside. .....Collector.
6. Bonding pad .....B = 4 x 6 mils, E = 4 x 5.5 mils.

* FIGURE 3. JANHCA and JANKCA die dimensions.

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$R_{\theta JSP(AM)}$ ..... Thermal resistance junction to solder pads (adhesive mount to PCB).
$R_{\theta JSP(IS)}$..... Thermal resistance junction to solder pads (infinite sink mount to PCB).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1, 2, and 3 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

* 3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or requalification. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of table II tests, the tests specified in table II herein shall be performed on the first inspection lot to this revision to maintain qualification.

4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
3c	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)
9	I_{CBO2} and h_{FE5}	Not applicable
10	24 hours minimum.	24 hours minimum.
11	I_{CBO2} and h_{FE5} ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater; $\Delta h_{FE5} = \pm 15$ percent of initial value.	I_{CBO2} and h_{FE5}
12	See 4.3.2, 240 hours minimum.	See 4.3.2, 80 hours minimum.
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater. $\Delta h_{FE5} = \pm 15$ percent of initial value.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater. $\Delta h_{FE5} = \pm 15$ percent of initial value.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500; “Discrete Semiconductor Die/Chip Lot Acceptance”. Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc: Power shall be applied to the device to achieve a junction temperature of T_J = +135°C minimum and a minimum power dissipation of P_D = 75 percent of maximum P_T shall be used (see 1.3).

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c and the subgroup 2 of table I shall comply with the thermal impedance graph in figures 7, 8, 9, and 10 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, group A, subgroup 1 and table I, group A, subgroup 2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2 herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, group A, subgroup 2 and 4.5.4 herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, group A, subgroup 2 and 4.5.4 herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 - 30 V dc; 2,000 cycles. No heat sink or forced-air cooling on devices shall be permitted.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum, sample size in accordance with table VIa of MIL-PRF-19500 adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.

* 4.4.2.2 Group B inspection, table VIb (JAN, JANS, JANTX, and JANTXV) of MIL-PRF-19500. Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Subgroup	Method	Condition
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0.
2	1039	HTRB: Test condition A, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANJ, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANJ, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) requirements shall be in accordance with subgroup 2, of table I herein; delta requirements only apply to subgroup C6.

4.4.3.1 Group C inspection (JANS), table VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (not applicable for UB devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
C6	1026	Test condition B, 1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45, c = 0.

* 4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, (see 1.3).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with subgroup 2 of table I herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Noise figure. Noise figure shall be measured using a model 310B Quan Tech Laboratories test set, or equivalent. Conditions shall be as specified in table I herein.

4.5.4 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 100 V dc	ΔI_{CB02} (1)	100 percent of initial value or ± 20 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed see 4.5.1	Δh_{FE5} (1)	± 25 percent change from initial reading.	

(1) Devices which exceed the table I limits for this test shall not be accepted.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical inspection 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Heremetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Group A, subgroup 2				
Decap internal visual (design verification)	2075	n = 4 device, c = 0				
Subgroup 2						
* Thermal impedance	3131	See 4.3.3.	$Z_{\theta JX}$			°C/W
Collector to base, cutoff current	3036	Bias condition D				
2N3634, 2N3634L, UB		V_{CB} = 140 V dc	I_{CBO1}		10	µA dc
2N3635, 2N3635L, UB		V_{CB} = 140 V dc	I_{CBO1}		10	µA dc
2N3636, 2N3636L, UB		V_{CB} = 175 V dc	I_{CBO1}		10	µA dc
2N3637, 2N3637L, UB		V_{CB} = 175 V dc	I_{CBO1}		10	µA dc
Emitter to base, cutoff current	3061	Bias condition D, V_{EB} = 5 V dc	I_{EBO1}		10	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = 10 mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N3634, 2N3634L, UB 2N3635, 2N3635L, UB				140		V dc
2N3636, 2N3636L, UB 2N3637, 2N3637L, UB				175		V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Collector to base cutoff current	3036	Bias condition D, V_{CB} = 100 V dc	I_{CBO2}		100	nA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 3 V dc	I_{EBO2}		50	nA dc
Collector to emitter cutoff current	3041	Bias condition D, V_{CE} = 100 V dc	I_{CEO}		10	µA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 0.1 mA dc pulsed (see 4.5.1)	h_{FE1}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				25		
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				55		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 1.0 mA dc pulsed (see 4.5.1)	h_{FE2}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				45		
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				90		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 10 mA dc pulsed (see 4.5.1)	h_{FE3}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				50		
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				100		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 50 mA dc pulsed (see 4.5.1)	h_{FE4}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				50	150	
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				100	300	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 150 mA dc pulsed (see 4.5.1)	h_{FE5}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				30		
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				60		

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Collector to emitter voltage (saturated)	3071	I_C = 10 mA dc, I_B = 1 mA dc pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.3	V dc
Collector to emitter voltage (saturated)	3071	I_C = 50 mA dc, I_B = 5 mA dc pulsed (see 4.5.1)	$V_{CE(sat)2}$		0.6	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 10 mA dc, I_B = 1.0 mA dc pulsed (see 4.5.1)	$V_{BE(sat)1}$		0.8	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 50 mA dc, I_B = 5 mA dc pulsed (see 4.5.1)	$V_{BE(sat)2}$	0.65	0.90	V dc
Subgroup 3						
High temperature operation:		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D, V_{CB} = -100 V dc	I_{CBO3}		10	µA dc
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 50 mA dc	h_{FE6}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				25		
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				50		
Subgroup 4						
Small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 30 V dc, I_C = 30 mA dc, f = 100 MHz	$\|h_{fe}\|$			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				1.5	8.0	
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				2.0	8.5	
Small-signal short-circuit forward current transfer ratio	3206	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 1 kHz	h_{fe}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				40	160	
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				80	320	

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Small-signal short-circuit input impedance	3201	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 1 kHz	h_{ie}			
2N3634, 2N3634L, UB 2N3636, 2N3636L, UB				100	600	Ω
2N3635, 2N3635L, UB 2N3637, 2N3637L, UB				200	1200	Ω
Small signal open circuit reverse voltage transfer ratio	3211	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 1 kHz	h_{re}		$3x10^{-4}$	
Small signal open circuit output admittance	3216	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 1 kHz	h_{oe}		200	μs
Open circuit output capacitance	3236	V_{CB} = 20 V dc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		10	pF
Input capacitance (output open circuited)	3240	V_{EB} = 1 V dc, I_C = 0, 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		75	pF
Noise figure	3246	V_{CE} = 10 V dc, I_C = 0.5 mA dc, R_G = 1 kΩ (see 4.5.3)	NF			
		f = 100 Hz			5	dB
		f = 10 kHZ			3	dB
		f = 1 kHZ			3	dB
Pulse response		Test condition A				
Switching parameters	3251	See figure 11	t_d		100	ns
Pulse delay time		See figure 11	t_r		100	ns
Pulse rise time		See figure 11	t_s		500	ns
Pulse storage time		See figure 11	t_f		150	ns
Pulse fall time t_{off}		t_s & t_f	t_{off}		600	ns

See footnotes at end of table.

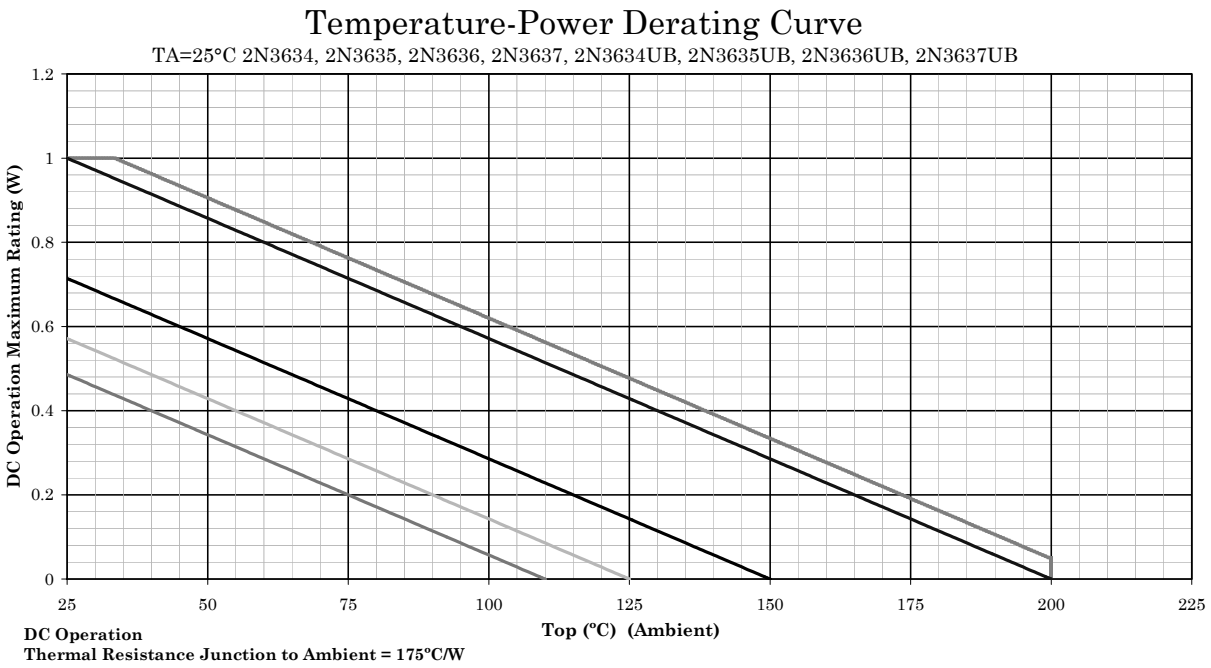
* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = + 25°C, t = 1s, 1 cycle (see figure 12)				
Test 1						
2N3634, 2N3634L, UB 2N3635, 2N3635L, UB		V_{CE} = 100 V dc, I_C = 30 mA dc				
2N3636, 2N3636L, UB 2N3637, 2N3637L, UB		V_{CE} = 130 V dc, I_C = 20 mA dc				
Test 2		V_{CE} = 50 V dc, I_C = 95 mA dc				
Test 3		V_{CE} = 5 V dc, I_C = 1 A dc				
End-point electrical measurements		Subgroup 2 of table I.				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed table I, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) - for qualification only.

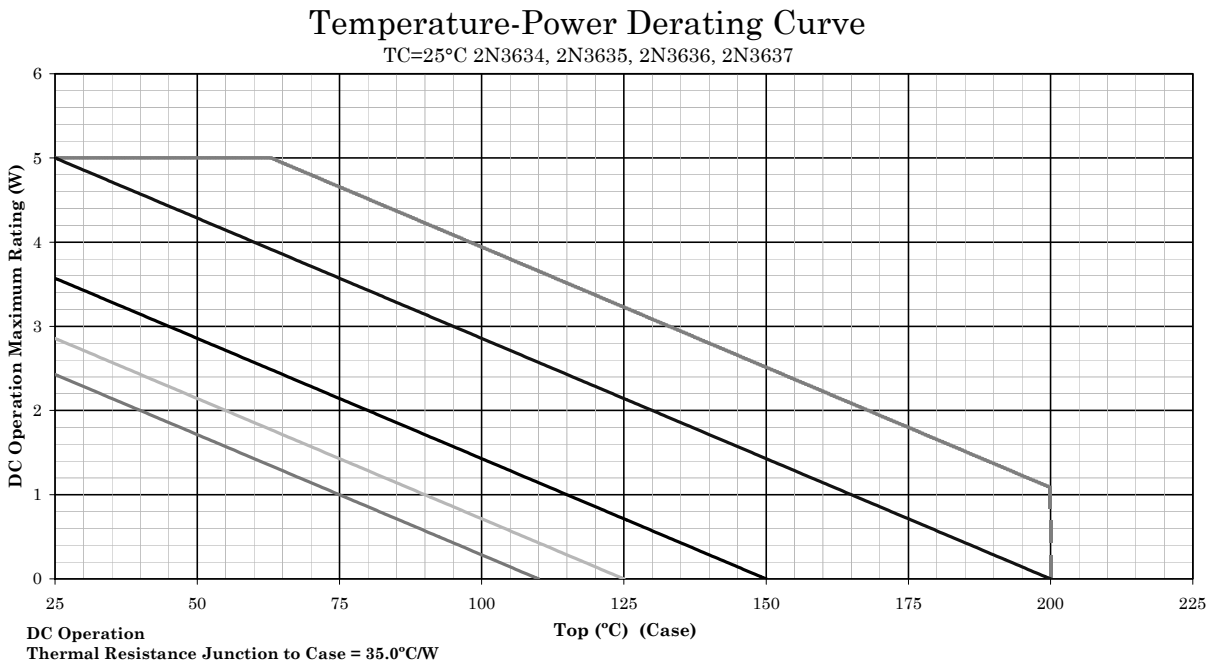
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.4 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles	
Electrical measurements		See subgroup 2 of table I and 4.5.4 herein.	
Subgroup 3			3 devices c = 0
Destructive physical analysis (DPA)	2102		
Subgroup 4			15 devices, c = 0
Thermal resistance	3131	$R_{\theta JSP}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple slash sheets).	
Thermal impedance, thermal resistance curves		Each supplier shall submit their (typical) maximum design thermal impedance curves. In addition, optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices
(Electrocstatic discharge) (ESD)	1020		
Subgroup 8			22 devices c = 0
Reverse stability	1033	Condition A for devices ≥400 volts Condition B for devices < 400 volts	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

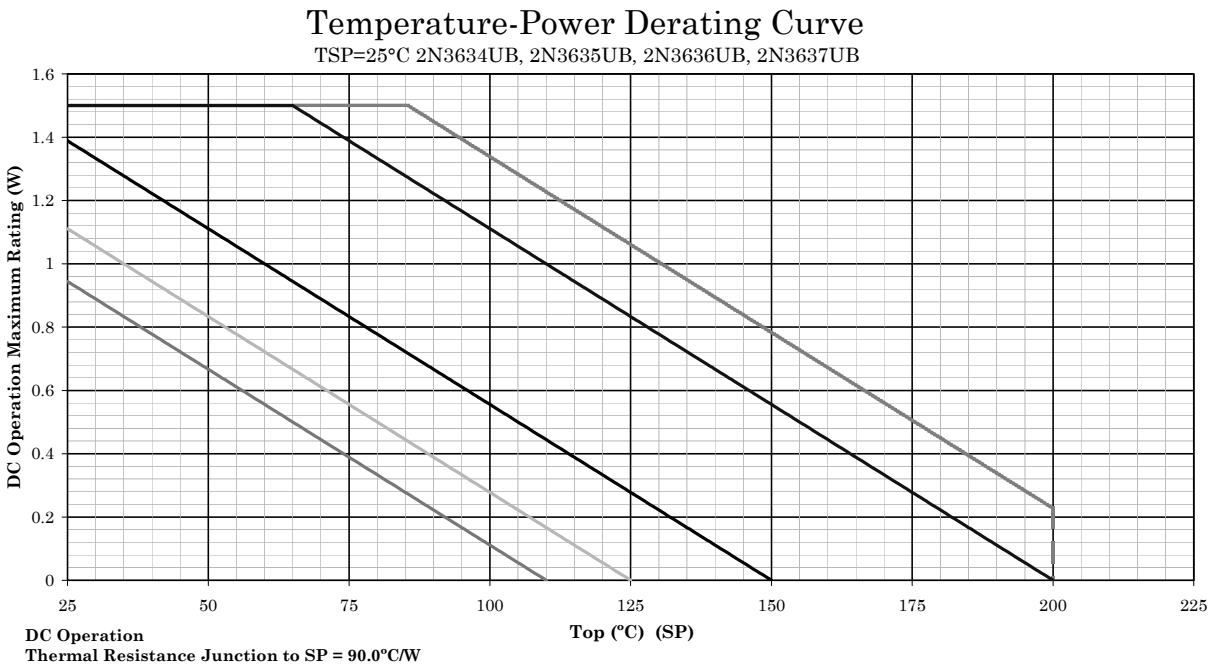
* FIGURE 4. Temperature-power derating for ($R_{\theta JA}$), base case mount (TO-5 and TO-39, and UB).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 5. Temperature-power derating for ($R_{\theta JC}$), base case mount (TO-5 and TO-39 Kovar).

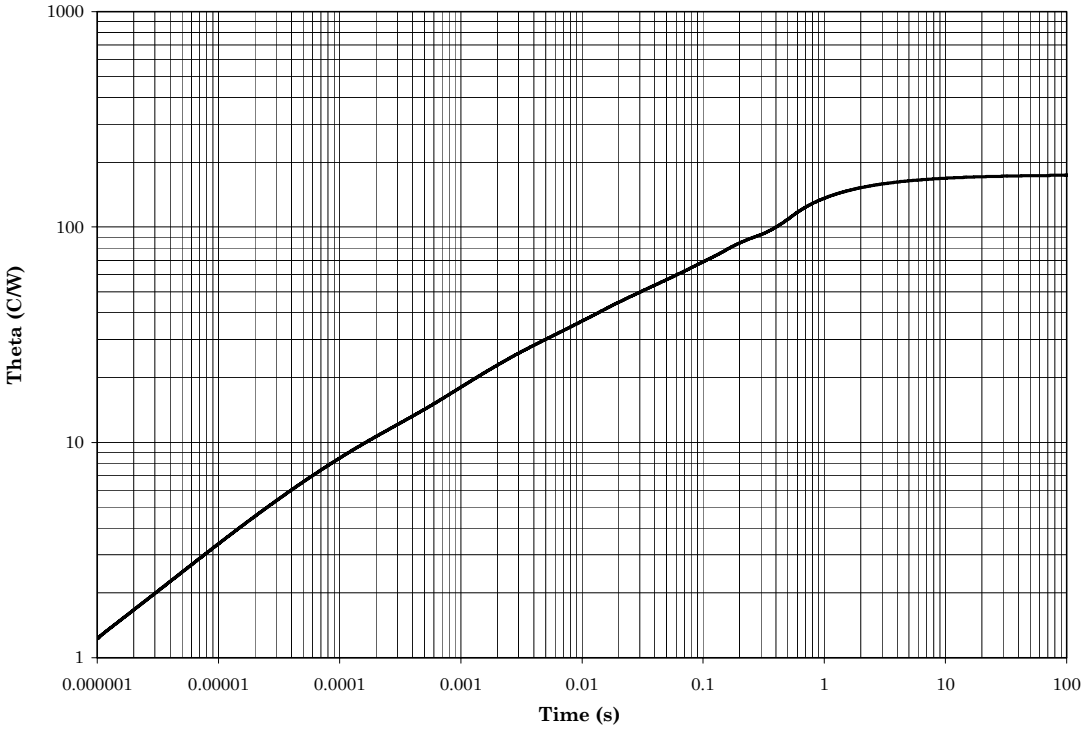


NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

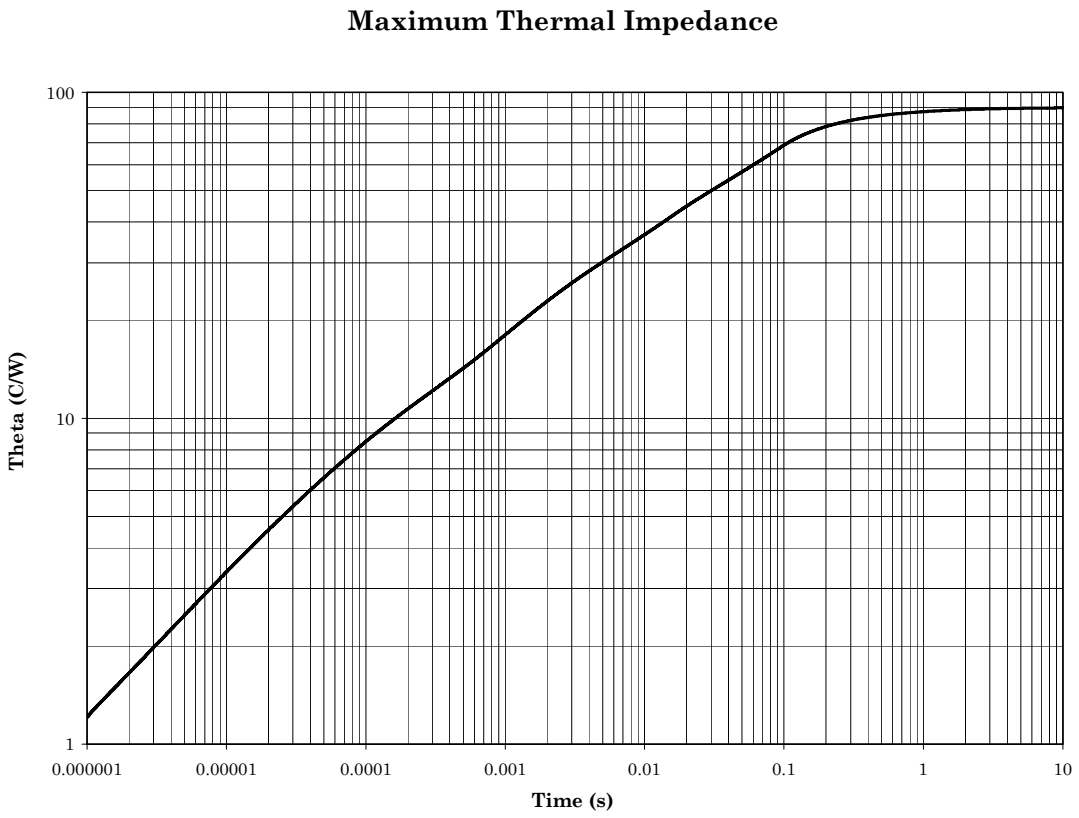
* FIGURE 6. Temperature-power derating for ($R_{\theta JSP}$), base case mount (UB).

Maximum Thermal Impedance



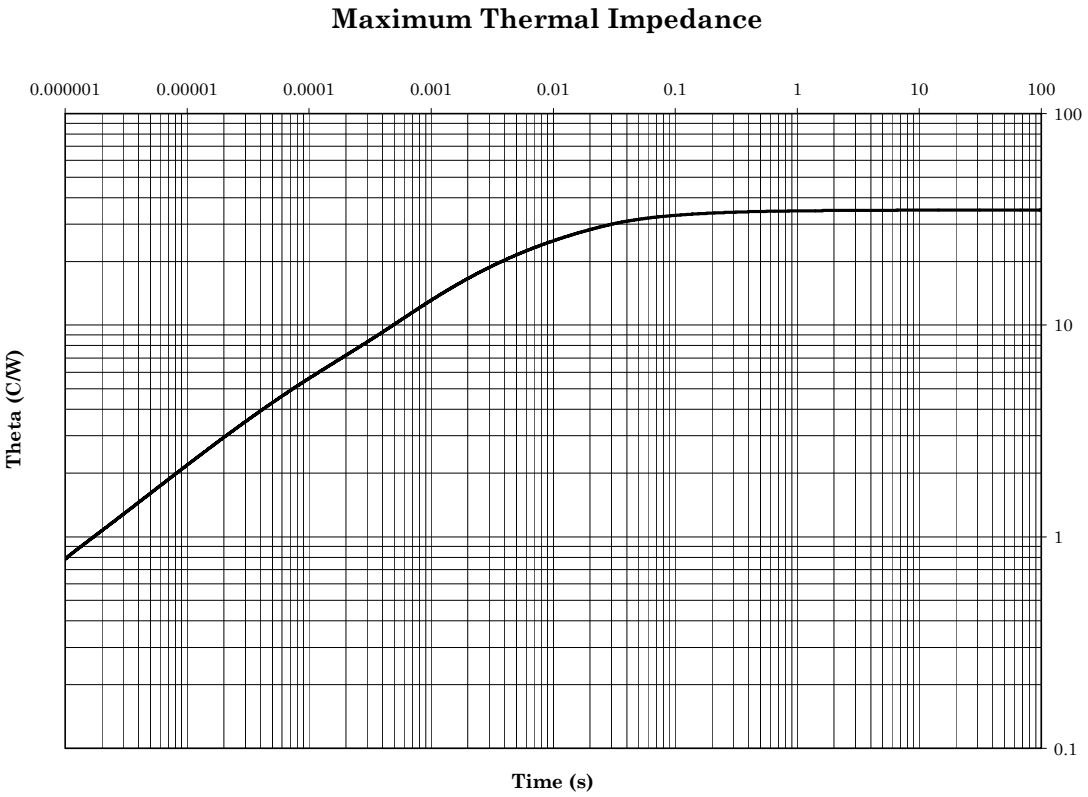
T_A = +25°C, thermal resistance $R_{\theta JA}$ = 175°C/W (Mounted to minimal copper clad PCB).

* FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for 2N3634UB through 2N3637UB (UB).



T_{SP} = +25°C, thermal resistance $R_{\theta JSP}$ = 90°C/W (Solder mounted to heavy copper clad PCB).

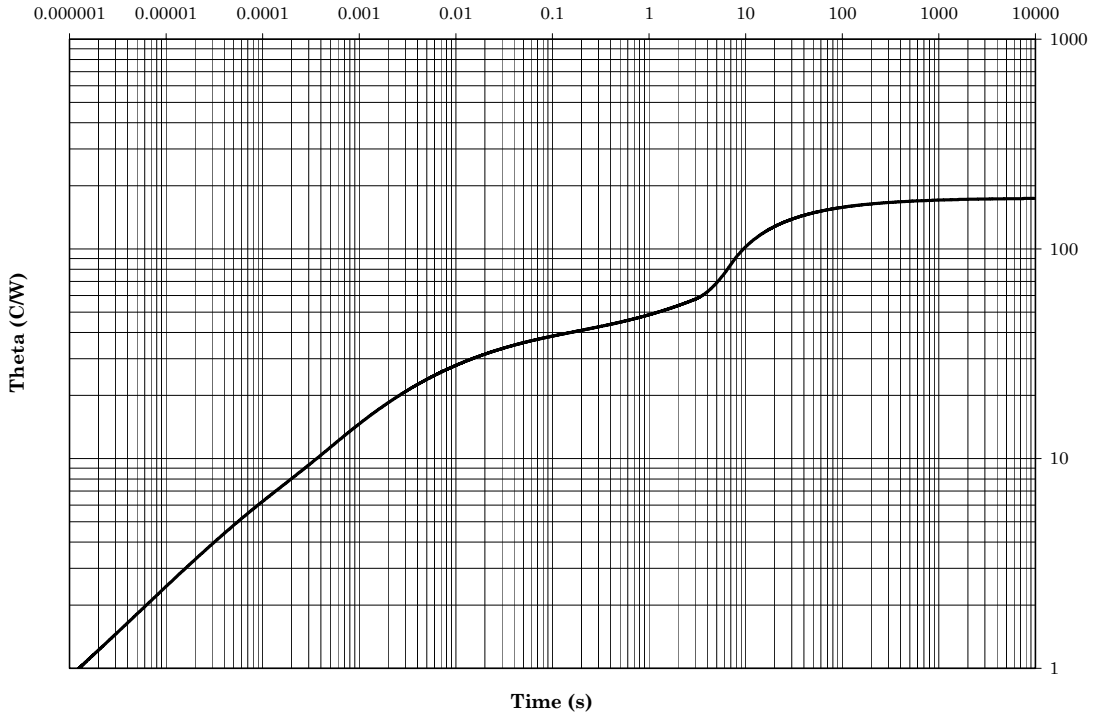
* FIGURE 8. Thermal impedance graph ($R_{\theta JSP}$) for 2N3634UB through 2N3637UB (UB).



T_C = +25°C, thermal resistance $R_{\theta JC}$ = 35°C/W (Ambient case mount).

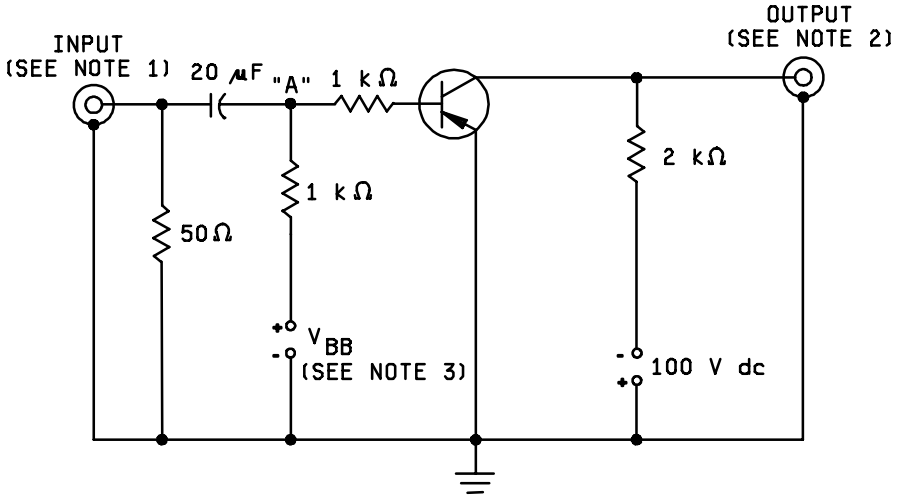
* FIGURE 9. Thermal impedance graph ($R_{\theta JC}$) for 2N3634 through 2N3637 and 2N3634L through 2N3637L (TO-5 and TO-39 Kovar).

Maximum Thermal Impedance

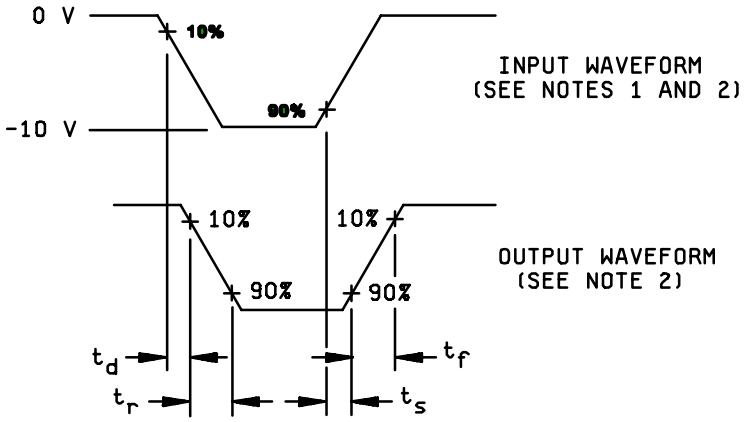


T_A = +25°C, thermal resistance $R_{\theta JA}$ = 175°C/W (Ambient free air cooled).

* FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N3634 through 2N3637 and 2N3634L through 2N3637L (TO-5 and TO-39).



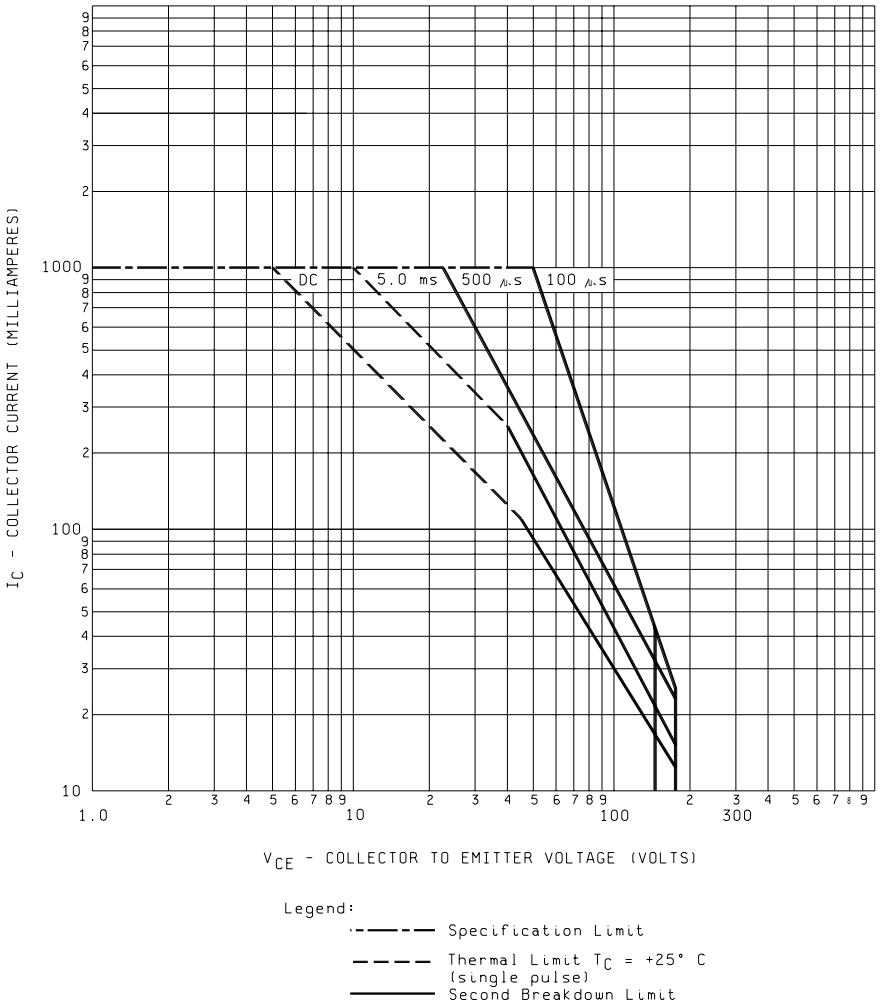
TEST CIRCUIT



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{OUT} = 50\Omega$, PW = 20 µs, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ MΩ, $C_{in} \leq 11.5$ pF.
3. V_{BB} = 4.0 V dc for t_{on}, 4.1 for t_{off} at point "A".
4. Resistors shall be noninductive types.
5. The dc power supplies may require additional by-passing in order to minimize ringing.

FIGURE 11. Pulse response test circuit.



NOTES:
1. T_J = +200°C.
2. Curves are based on a 30 percent derating factor.

FIGURE 12. Maximum safe operating area graph (continuous dc).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figure 3).

f. Surface mount designation if applicable.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

6.4 Supersession information. Devices covered by this specification supersede the manufacturers' and users' Part or Identifying Number (PIN). The term Part or Identifying Number (PIN) is equivalent to the term part number which was previously used in this specification. This information in no way implies that manufacturers' PIN's are suitable as a substitute for the military PIN.

6.5 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N3634) will be identified on the QML.

JANHC and JANKC ordering information	
PIN	Manufacturer
	43611
2N3634	JANHCA2N3634, JANKCA2N3634
2N3635	JANHCA2N3635, JANKCA2N3635
2N3636	JANHCA2N3636, JANKCA2N3636
2N3637	JANHCA2N3637, JANKCA2N3637

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, MC, SH
Air Force - 19, 71

Preparing activity:
DLA - CC

(Project 5961-2778)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://www.dodssp.daps.mil .