

The documentation and process conversion measures necessary to comply with this document shall be completed by 30 September, 2004.

INCH-POUND

MIL-PRF-19500/394H
 30 June 2004
 SUPERSEDING
 MIL-PRF-19500/394G
 5 July 2002

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, POWER SWITCHING,
 TYPES: 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, AND 2N5238S,
 JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power, high voltage transistors. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for each unencapsulated device type.

1.2 Physical dimensions. See figure 1 (TO- 5) and figures 2 and 3 (JANHC and JANKC).

* 1.3 Maximum ratings, unless otherwise specified, T_C = +25°C.

Types	P _T (1) T _A = +25°C	P _T (2) T _C = +25°C	R _{θJA} (max) (4)	R _{θJC} (max) (3)	V _{CBO}	V _{CEO}	V _{EBO}	I _C	T _{STG} and T _J
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>°C</u>
2N4150, S	1.0	15	175	10	100	70	10	10	-65 to
2N5237, S	1.0	15	175	10	150	120	10	10	+200
2N5238, S	1.0	15	175	10	200	170	10	10	

- (1) For derating see figure 4.
- (2) For derating see figure 5.
- (3) For thermal impedance curve see figure 6.
- (4) For thermal impedance curve see figure 7.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dsc.dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://www.dodssp.daps.mil>.

1.4 Primary electrical characteristics, unless otherwise specified, $T_C = +25^\circ\text{C}$.

	h_{FE2} (1)	h_{FE3} (1)	C_{obo}	h_{fe}	$V_{BE(sat)}$ (1)	$V_{CE(sat)}$
Limits	$I_C = 5 \text{ A dc}$ $V_{CE} = 5 \text{ V dc}$	$I_C = 10 \text{ A dc}$ $V_{CE} = 5 \text{ V dc}$	$I_E = 0$ $V_{CB} = 10 \text{ V dc}$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$I_C = 0.2 \text{ A dc}$ $V_{CE} = 10 \text{ V dc}$ $f = 10 \text{ MHz}$	$I_C = 5 \text{ A dc}$ $I_B = 0.5 \text{ A dc}$	$I_C = 5 \text{ A dc}$ $I_B = 0.5 \text{ A dc}$
Min	40	10	μF	1.5	V dc	V dc
Max	120		350	7.5	1.5	0.6

(1) Pulsed, (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://www.dodssp.daps.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

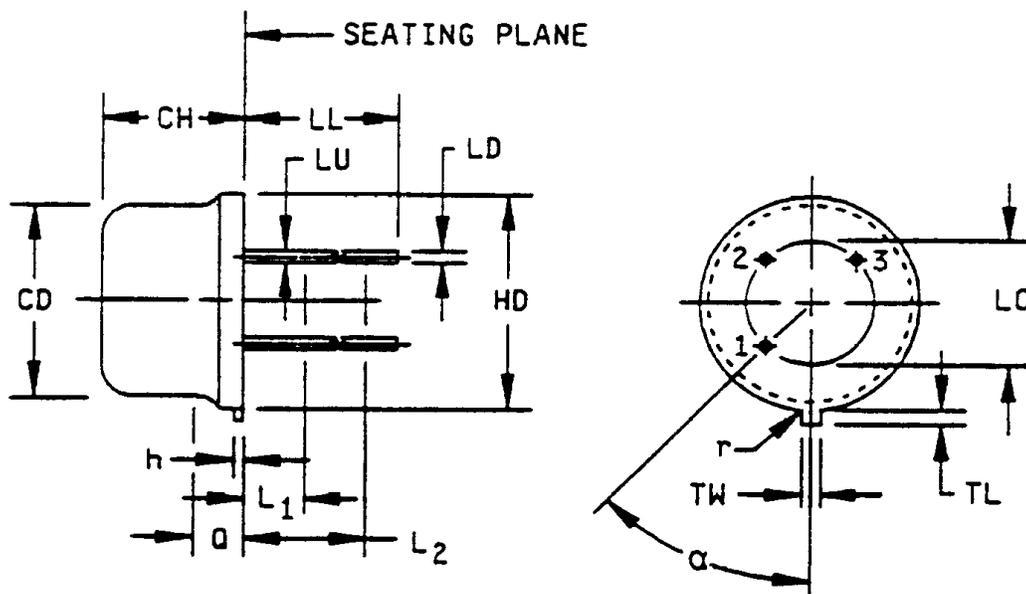


FIGURE 1. Physical dimensions (TO-5).

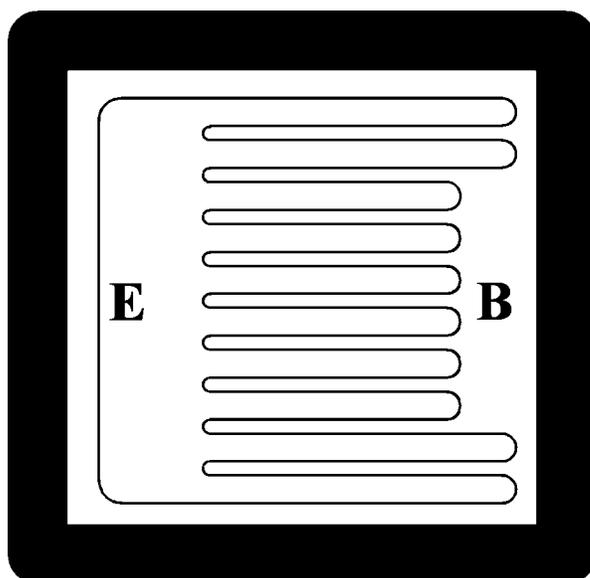
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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	5
CH	.240	.260	6.10	6.60	
h	.009	.041	0.23	1.04	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7
LL	See notes 14 and 15				
LU	.016	.019	0.41	0.48	7
L ₁		.050		1.27	7
L ₂	.250		6.35		7
Q		.050		1.27	13
r		.010		0.25	11,12
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	10
α	45° TP		45° TP		4, 6, 8, 9

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Lead number 4 omitted on this variation.
5. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) + .001 (0.03 mm) - .000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to the tab. The device may be measured by direct methods.
7. LD applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within L₁ and beyond LL minimum.
8. Lead designation is as follows: 1 - emitter; 2 - base; 3 - collector.
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. r (radius) applies to both inside corners of tab.
12. Tab shown omitted.
13. Details of outline in this zone optional.
14. For transistor types 2N4150S, 2N5237S, and 2N5238S, dimension LL = .500 inch (12.70 mm) minimum, and .750 inch (19.05 mm) maximum.
15. For transistor types 2N4150, 2N5237, and 2N5238, dimension LL = 1.500 inch (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum.
16. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

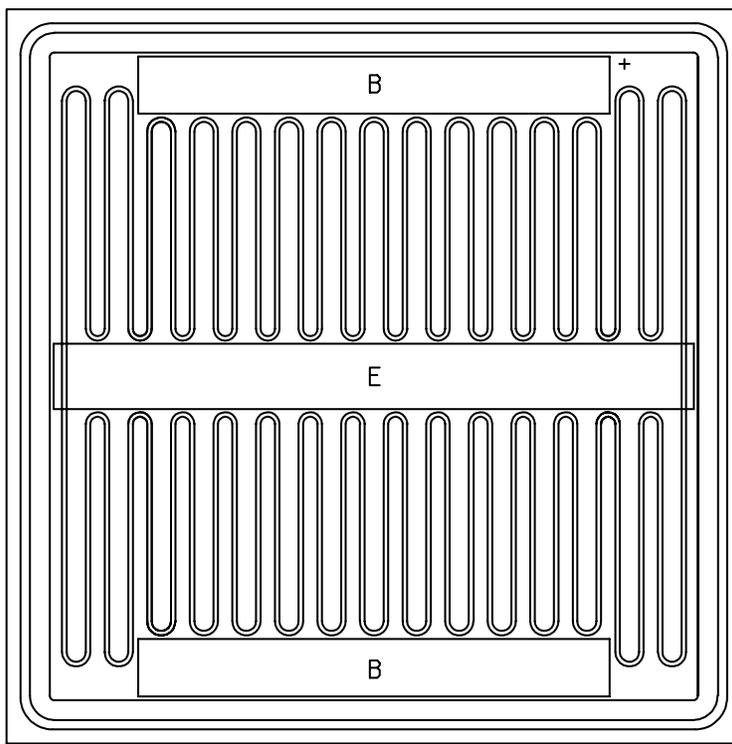
* FIGURE 1. Physical dimensions (TO-5) - Continued.



NOTES:

- | | |
|--------------------|---|
| 1. Chip size: | 120 x 120 mils \pm 2 mils (3.05 x 3.05 \pm 0.051mm). |
| 2. Chip thickness: | 10 \pm 1.5mils (0.254 \pm 0.038 mm) nominal. |
| 3. Top metal: | Aluminum 30,000 \AA minimum, 33,000 \AA nominal. |
| 4. Back metal: | A. Al/Ti/Ni/Ag 12k \AA /3k \AA /7k \AA /7k \AA min. 15k \AA /5k \AA /10k \AA /10k \AA nominal.
B. Gold 2,500 \AA minimum, 3,000 \AA nominal. |
| 5. Backside: | Collector. |
| 6. Bonding pad: | B = 52 x 12 mils (1.321 x 0.305mm), E = 84 x 12 mils (2.134 x 0.305mm). |

* FIGURE 2. JANHC and JANKC A-version die dimensions.



NOTES:

1. Die size: .155 x .155 inch (3.937 x 3.937 mm).
2. Die thickness: .008 ±.0016 inch (0.2032 ±0.04064 mm).
3. Base pad: .012 x .090 inch (0.3048 x 2.286 mm).
4. Emitter pad: .012 x .090 inch.
5. Back metal: Gold, 2400 ±720 Ang.
6. Top metal: Aluminum, 37500 ±7500 Ang.
7. Back side: Collector.
8. Glassivation: SiO₂, 7500 ± 1500 Ang.

FIGURE 3. JANHC and JANKC B-version die dimensions.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, on figure 1 (TO-5) and on figures 2 and 3 (JANHC and JANKC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Construction. These devices shall be constructed in a manner and using materials which enable the devices to meet the applicable requirements of MIL-PRF-19500 and this document.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E qualification shall be performed herein for qualification or requalification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot to this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV, and JANTX levels only). Screening shall be in accordance with table IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750, (see 4.3.3).	Thermal impedance, method 3131 of MIL-STD-750, (see 4.3.3).
7	Hermetic seal (optional) (2)	Hermetic seal (optional) (2)
9	I_{CB02} and h_{FE1}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CB02} ; h_{FE1} ; $\Delta I_{CB02} = 100$ percent of initial value or 50 nA dc, whichever is greater; $\Delta h_{FE1} = \pm 15$ percent of initial value.	I_{CB02} and h_{FE1}
12	See 4.3.2 240 hours minimum	See 4.3.2 80 hours minimum
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CB02} = 100$ percent of initial value or 50 nA dc, whichever is greater; $\Delta h_{FE1} = \pm 15$ percent of initial value.	Subgroup 2 of table I herein; $\Delta I_{CB02} = 100$ percent of initial value or 50 nA dc, whichever is greater; $\Delta h_{FE1} = \pm 15$ percent of initial value.
14	Required	Required

(1) Thermal impedance see 1.3.

(2) Hermetic seal test shall be performed in either screen 7 or screen 14.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ Vdc. Power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum T_A ambient rated as defined in 1.3.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of Mil-Std-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in Screen 3c shall comply with the thermal Impedance graph in figures 6 and 7 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein: delta requirements only apply to subgroups, B4, and B5. See 4.4.2.2 herein for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.3 herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} = 10 \text{ V dc.}$
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample). $V_{CB} = 10 \text{ V dc; } P_D \geq 100$ percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum, sample size in accordance with table VIa of MIL-PRF-19500, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum. Option 2: 216 hours., sample size = 45, $c = 0$; adjust T_A or P_D to achieve $T_J = +225^\circ\text{C}$ minimum.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1039	Steady-state life: Test condition B, 1,000 hours, $V_{CB} = 10 \text{ V dc}$, power shall be applied to achieve a junction temperature of $T_J = +150^\circ\text{C}$ minimum. A minimum of 75 percent of rated power shall be dissipated. No heat sink or forced-air cooling on devices shall be permitted. $n = 45, c = 0$.
2	1039	HTRB: Test condition A, 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22, c = 0$.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish, see MIL-PRF-19500.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table VII of MIL-PRF-19500, and 4.4.3.1 (JANS), and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein, delta measurements apply to subgroup C6.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C6	1026	1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C5	3131	See 4.5.2, $R_{\square JC}$. See (1.3) and (4.3.3).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following conditions shall apply:

- a. I_M : Collector current..... 10 mA.
- b. V_{CE} : Measurement current (same as V_H)..... 10 V dc.
- c. I_H : Collector heating current..... 0.375 A.
- d. V_H : Collector-emitter heating voltage 10 V dc.
- e. t_H : Heating time..... 1.0 s.
- f. t_{MD} : Measurement delay time..... 30 to 60 μ s.
- g. t_{sw} : Sampling window time 10 μ s maximum.

4.5.3 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, $V_{CB} = 80$ V dc	ΔI_{CB02} (1)	100 percent of initial value or 50 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	$V_{CE} = 5$ V dc; $I_C = 5$ A dc; pulsed see 4.5.1 (see figure 8).	Δh_{FE2} (1)	± 20 percent change from initial reading.

(1) Devices which exceed the table I limits for this test shall not be accepted.

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvent <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temperature cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>4/</u>	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical Measurements <u>4/</u>		Table I, subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T _A = +250°C at t = 24 hrs or T _A = +300°C at t = 2 hrs, n = 11 wires, c = 0				
* Decap internal visual (design verification) <u>4/</u>	2075	n = 4 device, c = 0				
<u>Subgroup 2</u>						
* Thermal impedance	3131	See 4.3.3.	Z _{θJX}			°C/W
Collector to base cutoff current	3036		I _{CBO1}		10	μA dc
2N4150, 2N4150S 2N5237, 2N5237S 2N5238, 2N5238S		V _{CB} = 100 V dc V _{CB} = 150 V dc V _{CB} = 200 V dc				
Breakdown voltage, collector to emitter	3011	Bias condition D, I _C = 0.1 A dc, pulsed (see 4.5.1)	V _{(BR)CEO}			V dc
2N4150, 2N4150S 2N5237, 2N5237S 2N5238, 2N5238S				70 120 170		

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued.						
Emitter to base cutoff current	3061	$V_{BE} = 7 \text{ V dc}$	I_{EBO1}		10	$\mu\text{A dc}$
Collector to emitter cutoff current	3041	Bias condition D $V_{CE} = 60 \text{ V dc}$ $V_{CE} = 110 \text{ V dc}$ $V_{CE} = 160 \text{ V dc}$	I_{CEO1}		10	$\mu\text{A dc}$
Collector to emitter cutoff current	3041	Bias condition A $V_{BE} = 0.5 \text{ V dc}$ $V_{CE} = 60 \text{ V dc}$ $V_{CE} = 110 \text{ V dc}$ $V_{CE} = 160 \text{ V dc}$	I_{CEX1}		10	$\mu\text{A dc}$
Emitter to base cutoff current	3061	Bias condition D, $V_{BE} = 5 \text{ V dc}$	I_{EBO2}		0.1	$\mu\text{A dc}$
Collector to base cutoff current	3036	Bias condition D, $V_{CB} = 80 \text{ V dc}$	I_{CBO2}		0.1	$\mu\text{A dc}$
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$, $I_C = 1 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE1}			
				50	200	
				50	225	
				50	225	
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$, $I_C = 5 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE2}	40	120	
Collector to emitter voltage (saturated)	3071	$I_C = 5 \text{ A dc}$, $I_B = 0.5 \text{ A dc}$, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.6	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 10 \text{ A dc}$, $I_B = 1 \text{ A dc}$, pulsed (see 4.5.1)	$V_{CE(sat)2}$		2.5	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued.						
Base emitter voltage saturation	3066	Test condition A, $I_C = 5$ A dc, $I_B = 0.5$ A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.5	V dc
Base emitter voltage saturation	3066	Test condition A, $I_C = 10$ A dc, $I_B = 1$ A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.5	V dc
Forward-current transfer ratio	3076	$V_{CE} = 5$ V dc, $I_C = 10$ A dc, pulsed (see 4.5.1)	h_{FE3}	10		
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition A, $V_{BE} = -0.5$ V dc	I_{CEX2}		40	μA dc
2N4150, 2N4150S 2N5237, 2N5237S 2N5238, 2N5238S		$V_{CE} = 60$ V dc $V_{CE} = 110$ V dc $V_{CE} = 160$ V dc				
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 5$ V dc, $I_C = 5$ A dc, pulsed (see 4.5.1)	h_{FE4}	20		
<u>Subgroup 4</u>						
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 10$ V dc, $I_C = 0.2$ A dc, $f = 10$ MHz	$ h_{fe} $	1.5	7.5	
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = 5$ V dc, $I_C = 50$ mA dc, $f = 1$ kHz	h_{fe}			
2N4150, 2N4150S 2N5237, 2N5237S 2N5238, 2N5238S				40	160	
				40	160	
				40	250	

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued.						
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}$, $I_E = 0$, $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		350	pF
Pulse response	3251	Test condition A				
Delay time		See figure 9	t_d		50	ns
Rise time		See figure 9	t_r		500	ns
Storage time		See figure 9	t_s		1.5	μs
Fall time		See figure 9	t_f		500	ns
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}$, $t = 1.0 \text{ s}$,				
Test 1		$V_{CE} = 40 \text{ V dc}$, $I_C = 0.22 \text{ A dc}$				
Test 2		$V_{CE} = 70 \text{ V dc}$, $I_C = 90 \text{ mA dc}$				
Test 3						
2N5237, 2N5237S only		$V_{CE} = 120 \text{ V dc}$, $I_C = 15 \text{ mA dc}$				
2N5238, 2N5238S only		$V_{CE} = 170 \text{ V dc}$, $I_C = 3.5 \text{ mA dc}$				
Clamped inductive sweep	3053	$T_C = +100^\circ\text{C}$ minimum, $I_B = 0.5 \text{ A dc}$, $I_C = 5 \text{ A dc}$, (see figure 10)				
Electrical measurements		See 4.5.3 herein.				

1/ For sampling plan, see MIL-PRF-19500.

2/ For resubmission of failed table I, subgroup 1, double the sample size of the failed test or sequence of tests.

3/ Separate samples may be used.

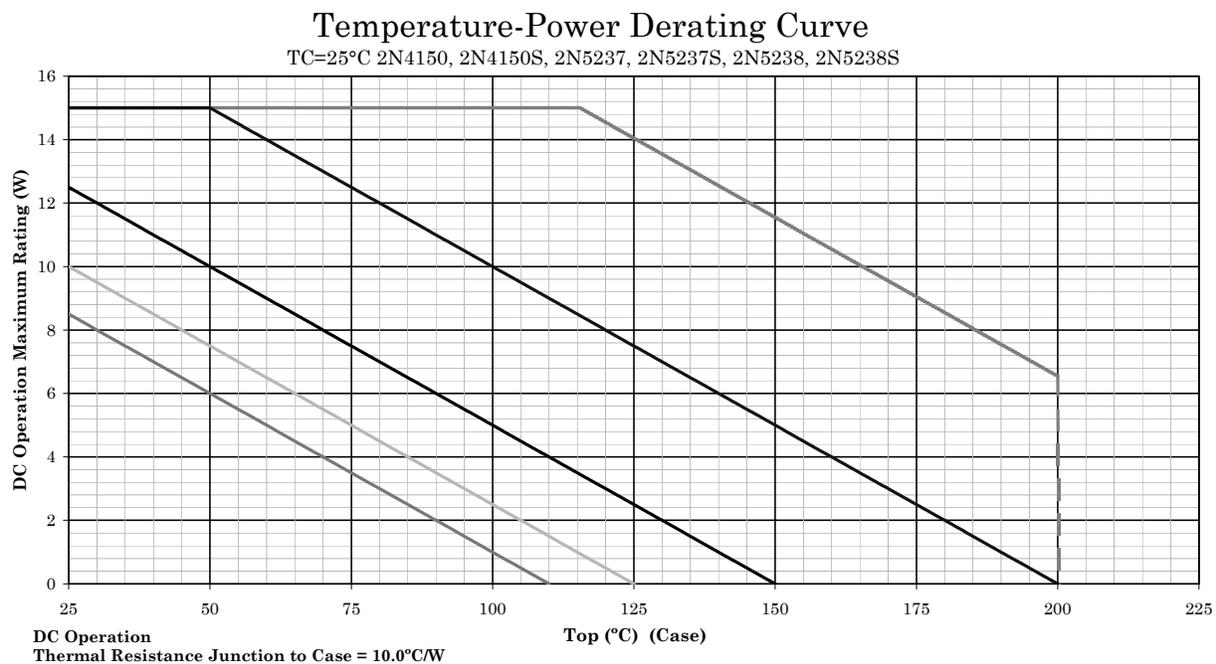
4/ Not required for JANS.

5/ Not required for laser marked devices.

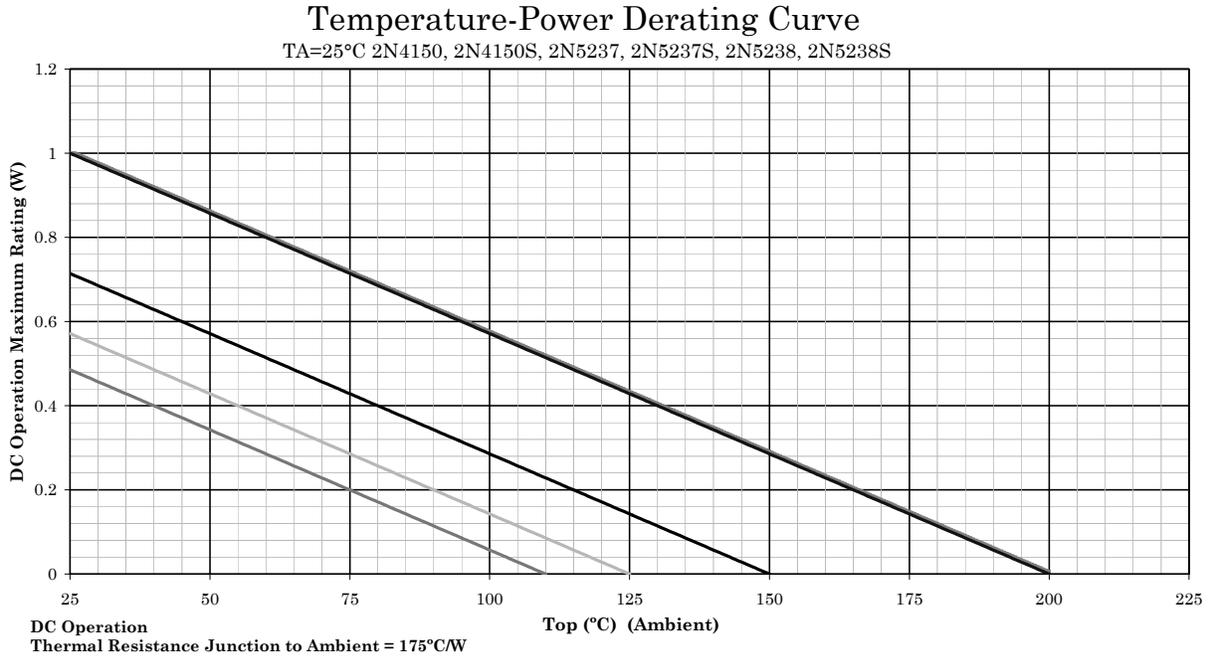
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* TABLE II. Group E inspection (all quality levels) – for qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal			
Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V _{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 herein.	
<u>Subgroup 3</u>			3 devices c = 0
Destructive physical analysis (DPA)	2102		
<u>Subgroup 4</u>			15 devices, c = 0
Thermal impedance, thermal resistance curves		Each supplier shall submit their (typical) maximum design thermal impedance curves. In addition, optimal test conditions and Z _{θJX} limit shall be provided to the qualifying activity in the qualification report	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices c = 0
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V Condition B for devices < 400 V	

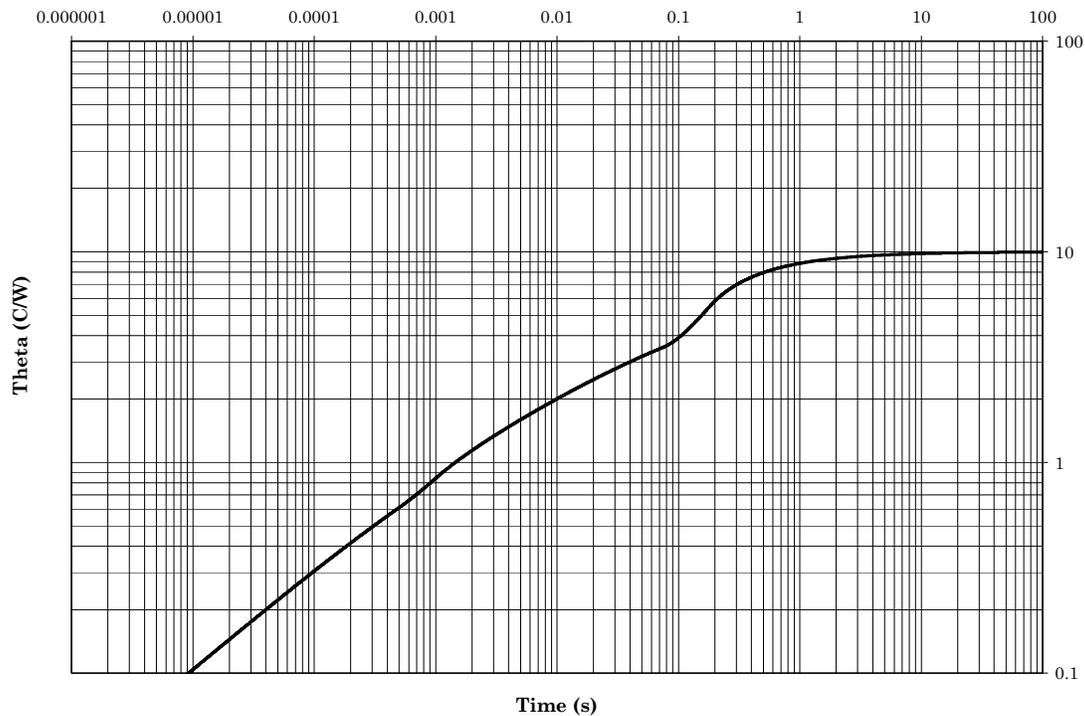


* FIGURE 4. Derating for 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S ($R_{\theta JC}$) (TO-5).



* FIGURE 5. Derating for 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S ($R_{\theta JA}$) (TO-5).

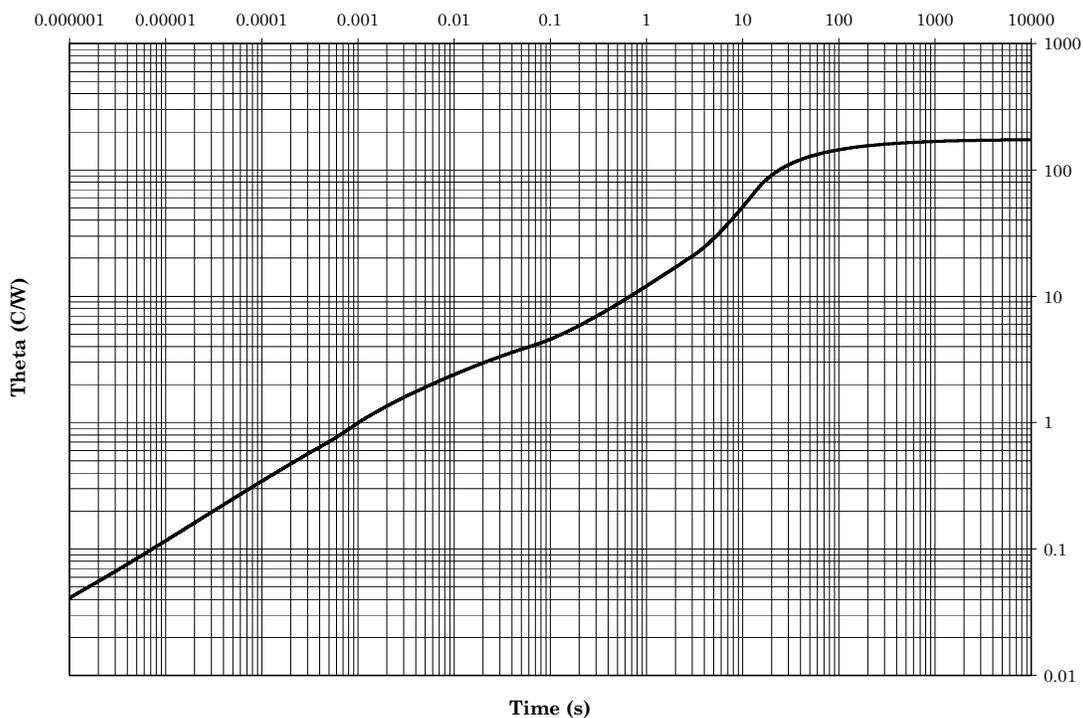
Maximum Thermal Impedance



$T_C = +25^\circ\text{C}$, Thermal Resistance $R_{\theta JC} = 10^\circ\text{C/W}$.

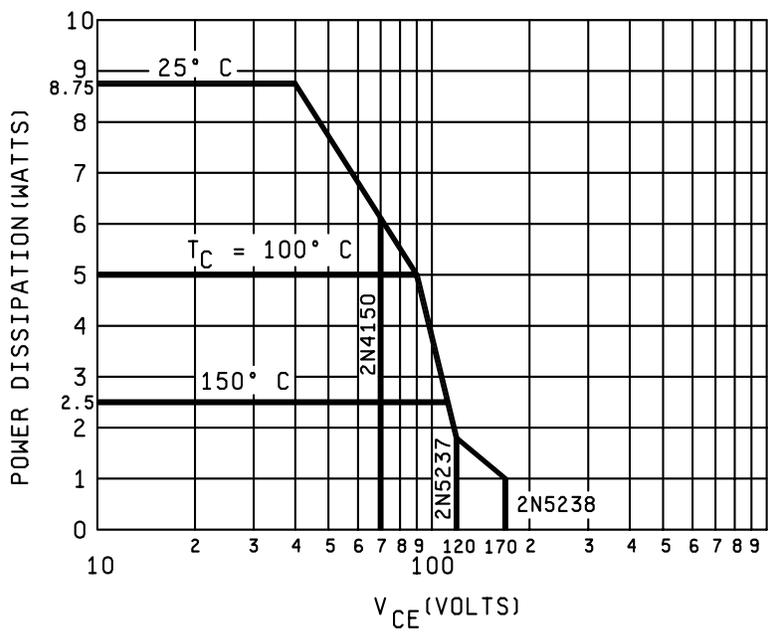
* FIGURE 6. Thermal impedance graph ($R_{\theta JC}$) for all 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S devices (TO-5) kovar.

Maximum Thermal Impedance

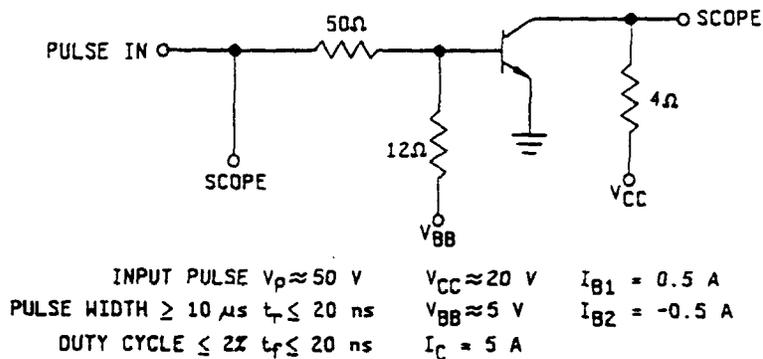


$T_A = +25^\circ\text{C}$, 1W, Thermal Resistance $R_{\theta JA} = 175^\circ\text{C/W}$.

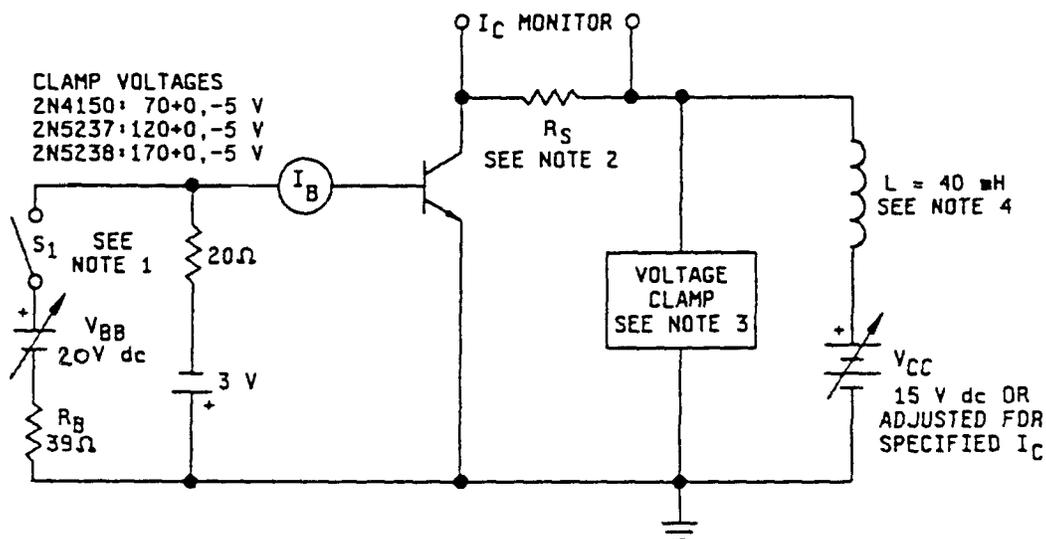
* FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for all 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S devices (TO-5).



* FIGURE 8. Maximum operating conditions - dc forward biased mode.



* FIGURE 9. Speed of response test circuit.



NOTES:

1. An appropriate pulse generator may be substituted.
2. $R_S \leq 1.0 \Omega$ noninductive.
3. Clamp voltage: 2N4150: 70 V dc +0 V dc, -5 V dc; 2N5237: 120 V dc +0 V dc, -5 V dc; 2N5238: 170 V dc +0 V dc, -5 V dc
4. STANCOR C-2691 or equivalent; 2 in series.

* FIGURE 10. Clamped inductive sweep test circuit.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example, JANHCA2N4150) will be identified on the QML.

JANC ordering information		
PIN	Manufacturers	
	43611	34156
2N4150	JANHCA2N4150 JANKCA2N4150	JANHCB2N4150 JANKCB2N4150

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961 - 2791)

Review activities:
 Army - MI, SM
 Air Force - 19, 71, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://www.dodssp.daps.mil>.