

The documentation and process conversion measures necessary to comply with this document shall be completed by 15 May, 2004.

INCH-POUND

MIL-PRF-19500/423E
 15 March 2004
 SUPERSEDING
 MIL-PRF-19500/423D
 3 July 2002

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, SWITCHING,
 TYPES 2N5581 AND 2N5582, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, switching transistors. Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 herein (similar to TO-46).

* 1.3 Maximum ratings.

Types	$P_T = (1)$ $T_A = +25^\circ\text{C}$	$P_T = (2)$ $T_C = +25^\circ\text{C}$	$R_{\theta JA}$ $T_A = +25^\circ\text{C}$ (1) (3)	$R_{\theta JC}$ $T_C = +25^\circ\text{C}$ (2) (4)	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_{STG} and T_J
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>°C</u>
2N5581	0.5	2.0	325	80	75	6	50	800	-65 to
2N5582	0.5	2.0	325	80	75	6	50	800	+200

- (1) For derating see figure 2.
- (2) For derating see figure 3.
- (3) For thermal resistance see figure 4.
- (4) For thermal resistance see figure 5.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://www.dodssp.daps.mil/>.

* 1.4 Primary electrical characteristics at T_A = +25°C.

	h _{FE2}		h _{FE4}		h _{fe} V _{CE} = 20 V dc I _C = 20 mA dc f = 100 MHz	C _{obo} V _{CB} = 10 V dc I _E = 0 100 kHz ≤ f ≤ 1 MHz	Switching		
	V _{CE} = 10 V dc I _C = 1.0 mA dc		V _{CE} = 10 V dc I _C = 150 mA dc (1)				t _{on}	t _{off}	t _{on} + t _{off}
	2N5581	2N5582	2N5581	2N5582		pF	ns	ns	ns
Min	35	75	40	100	2.5				
Max			120	300	5.0	8	35	300	18

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://www.dodssp.daps.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

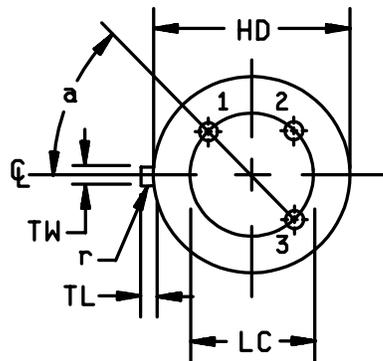
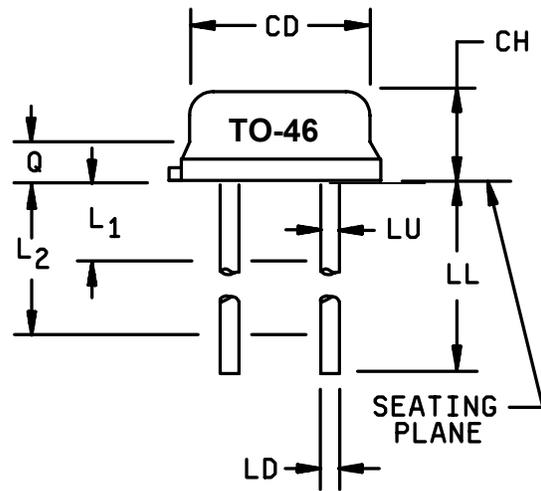
2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L1		.050		1.27	6
L2	.250		6.35		6
Q		.040		1.02	3
TL	.028	.048	0.71	1.22	8
TW	.036	.046	0.91	1.17	4
r		.010		0.25	9
α	45° TP		45° TP		5



NOTES:

1. Dimensions are in inches. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) - .000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
6. Symbol LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Physical dimensions 2N5581, and 2N5582 (TO-46).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I, subgroup 2.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX, and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement
	JANTX and JANTXV level
3c	Thermal impedance (see 4.3.2).
9	Not applicable
10	48 hours minimum
11	I_{CBO2} ; h_{FE4} :
12	See 4.3.1, 80 hours minimum.
13	Subgroups 2 of table I herein; $\Delta I_{CBO2} = 100$ percent of initial value or 5 nA dc, whichever is greater. $\Delta h_{FE4} = \pm 15$ percent.
14	Required

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc, power shall be applied to the device to achieve a junction temperature, $T_J = +135^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum T_A ambient rated as defined in 1.3.

4.3.2 Thermal impedance ($Z_{\theta JX}$ measurements). See figures 4, and 5. The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in 4.3, screen 3c and the subgroup 2 of table I shall comply with the thermal impedance graph in figures 4, and 5 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified as follows for JAN, JANTX, and JANTXV group B testing herein. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each following step and shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

* 4.4.2.1 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during conformance inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$.
2	1039	HTRB: Test condition A, 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

4.4.2.2 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot.
- b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B herein for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

* 4.4.3.1 Group C inspection, (JAN, JANTX, and JANTXV)

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$, see 1.3.
C6		Not applicable

4.4.3.2 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta requirements shall be in accordance with the steps of table 4.5.2 herein as specified in the notes for 4.5.2.

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4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, $V_{CB} = 60 \text{ V dc}$	ΔI_{CB02} (1)	100 percent of initial value or 8 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc};$ $I_C = 150 \text{ mA dc};$ pulsed see 4.5.1	Δh_{FE4} (1)	± 25 percent change from initial reading.	

(1) Devices which exceed the table I limits for this test shall not be accepted.

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		Table I, subgroup 2				
Bond strength <u>3/</u>	2037	Precondition T _A = +250°C at t = 24 hours or T _A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	Z _{θJX}			°C/W
Collector to base cutoff current	3036	Bias condition D; V _{CB} = 75 V dc	I _{CBO1}		10	μA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 6 V dc	I _{EBO1}		10	μA dc
Breakdown voltage collector to emitter	3011	Bias condition D; I _C = 10 mA dc pulsed (see 4.5.1)	V _{(BR)CEO}	50		V dc
Collector to base cutoff current	3036	Bias condition D; V _{CB} = 60 V dc	I _{CBO2}		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 4 V dc	I _{EBO2}		10	nA dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/ 	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 0.1 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE1}	30 50		
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 1.0 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE2}	35 75		
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE3}	40 100		
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE4}	40 100	120 300	
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE5}	20 30		
Collector to emitter voltage (saturated)	3071	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.3	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.0	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 150 \text{ mA dc};$ $I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)1}$	0.6	1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 500 \text{ mA dc};$ $I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.0	V dc
<u>Subgroup 3</u>						
High-temperature operation		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 60 \text{ V dc}$	I_{CB03}		10	$\mu\text{A dc}$
Low-temperature operation		$T_A = -55^\circ\text{C}$				
Forward current transfer ratio 2N5581 2N5582	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE6}	15 35		

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Small-signal short-circuit forward-current transfer ratio 2N5581 2N5582	3206	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ mA dc},$ $f = 1 \text{ kHz}$	h_{fe}	30 50		
Magnitude of small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 20 \text{ V dc}; I_C = 20 \text{ mA dc};$ $f = 100 \text{ MHz}$	$ h_{fe} $	2.5	5.0	
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		8	pF
Input capacitance (output open circuited)	3240	$V_{EB} = 0.5 \text{ V dc}; I_C = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{ibo}		25	pF
Turn-on time		(See figure 6)	t_{on}		35	ns
Turn-off time		(See figure 7)	t_{off}		300	ns
Pulse response		(See figure 8)	$t_{on} + t_{off}$		18	ns
<u>Subgroups 5 and 6</u>						
Not required						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

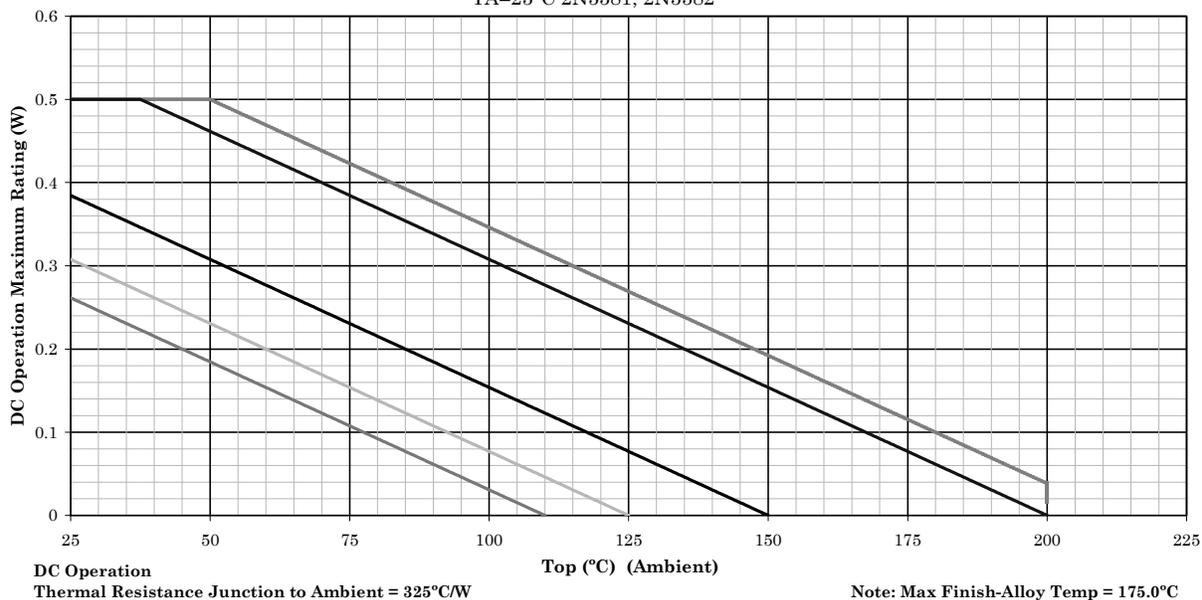
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* TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V _{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and steps 1 and 2 of 4.5.2 herein.	
<u>Subgroup 3</u>			3 devices c = 0
Destructive physical analysis (DPA)	2102		
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance, thermal resistance curves	3131	Each supplier shall submit their (typical) maximum design thermal impedance curves. In addition, the optional test conditions and Z _{θJX} limit shall be provided to the qualifying activity in the qualification report.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices c = 0
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V Condition B for devices < 400 V	

Temperature-Power Derating Curve

TA=25°C 2N5581, 2N5582



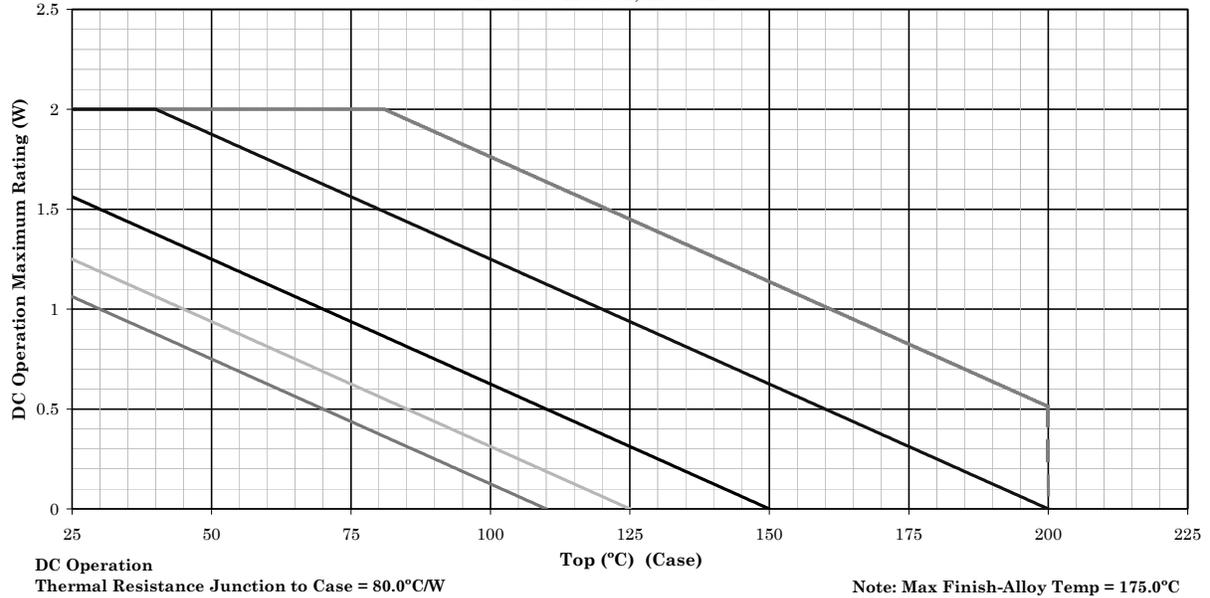
NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

* FIGURE 2. Derating for 2N5581 and 2N5582 ($R_{\theta JA}$) leads .125 inch (TO-46).

Temperature-Power Derating Curve

TC=25°C 2N5581, 2N5582

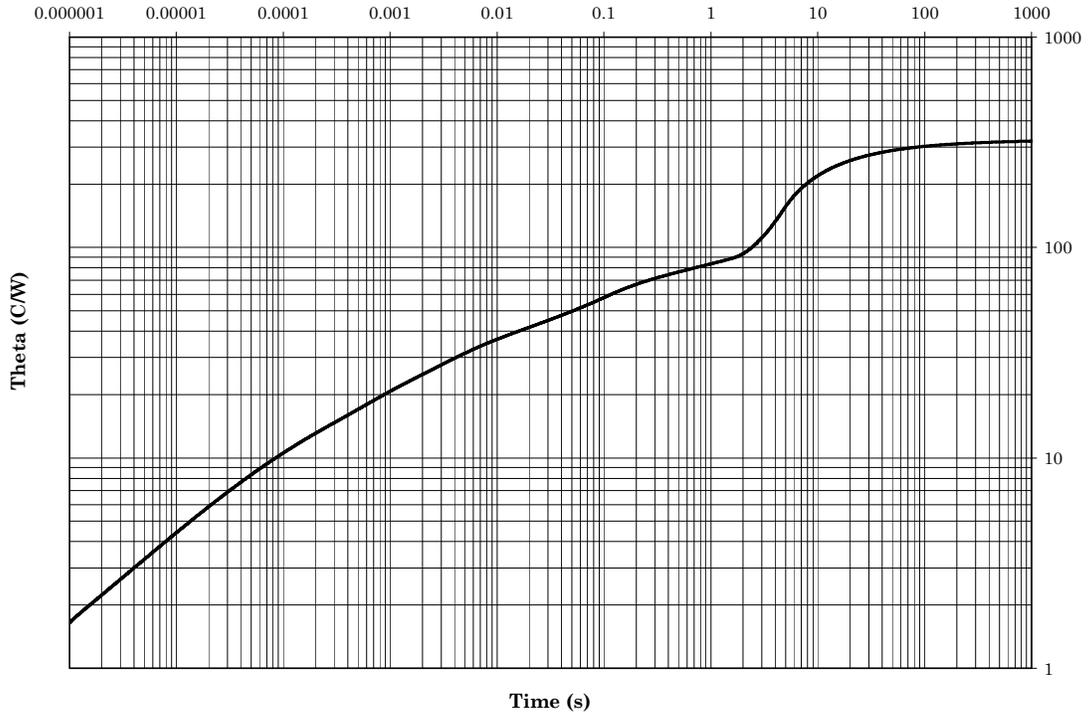


NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

* FIGURE 3. Derating for 2N5581 and 2N5582 ($R_{\theta JC}$) (TO-46).

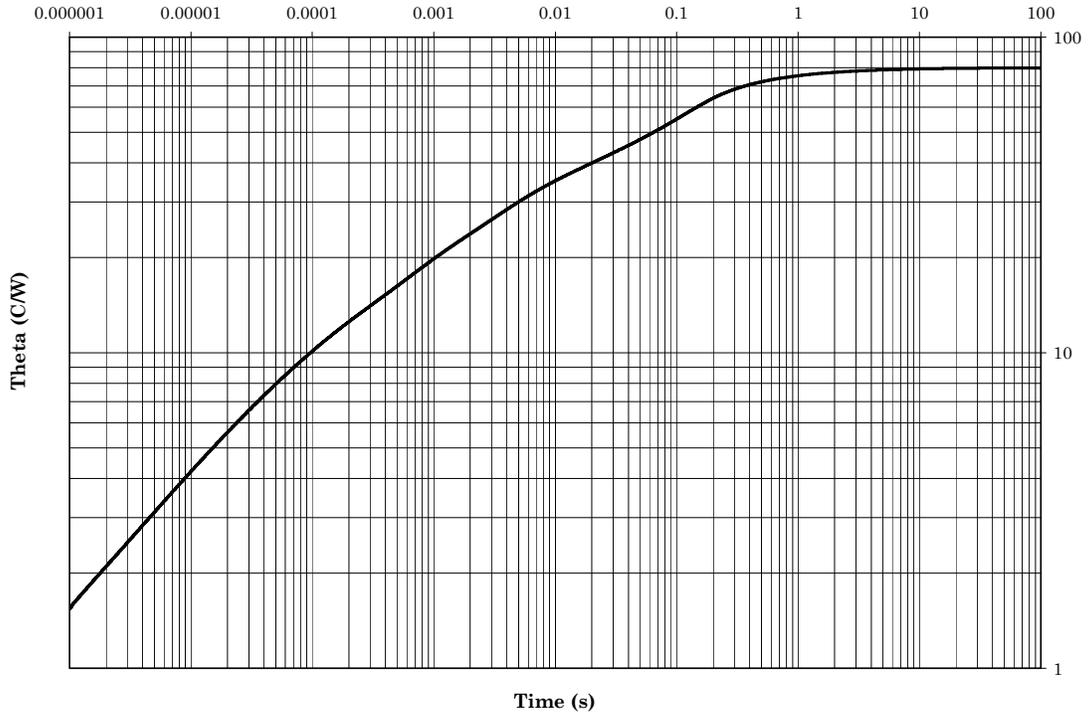
Maximum Thermal Impedance



$T_A = +25^\circ\text{C}$, 500mW, thermal resistance $R_{\theta JA} = 325^\circ\text{C/W}$

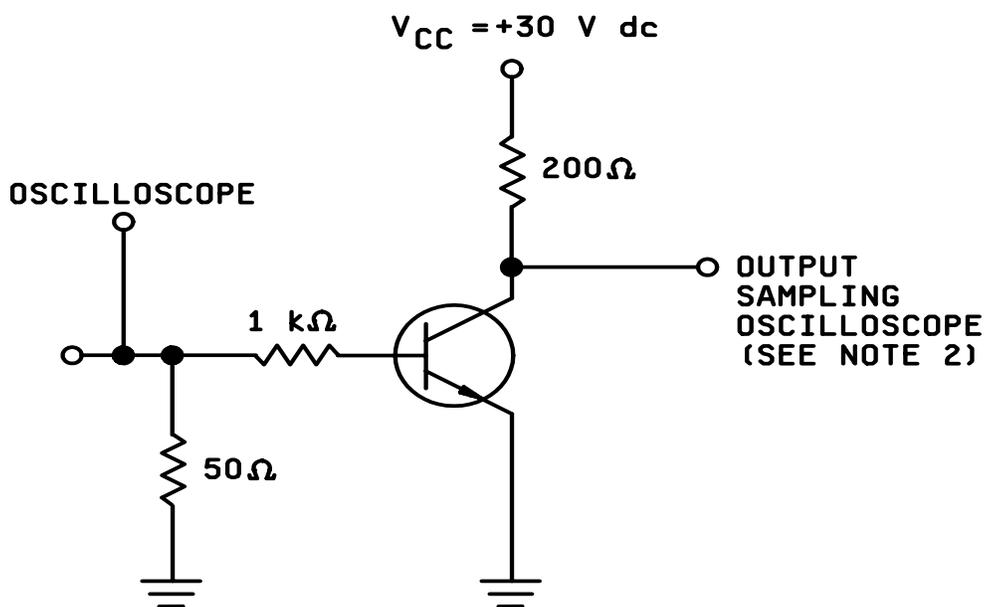
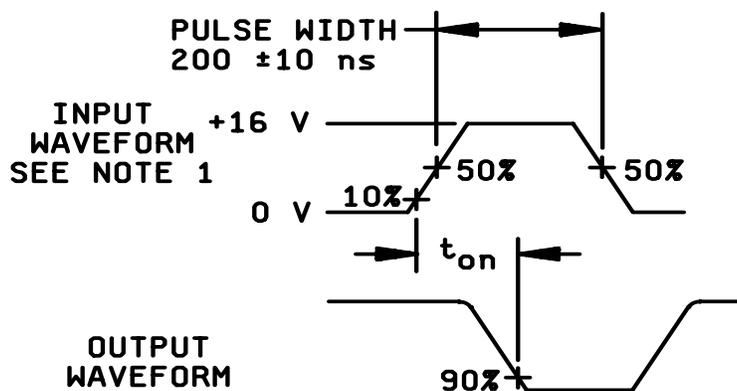
FIGURE 4. Thermal impedance graph ($R_{\theta JA}$) for 2N5581 and 2N5582 (TO-46).

Maximum Thermal Impedance



$T_C = +25^\circ\text{C}$, 2.0 W, thermal resistance $R_{\theta JC} = 80^\circ\text{C/W}$

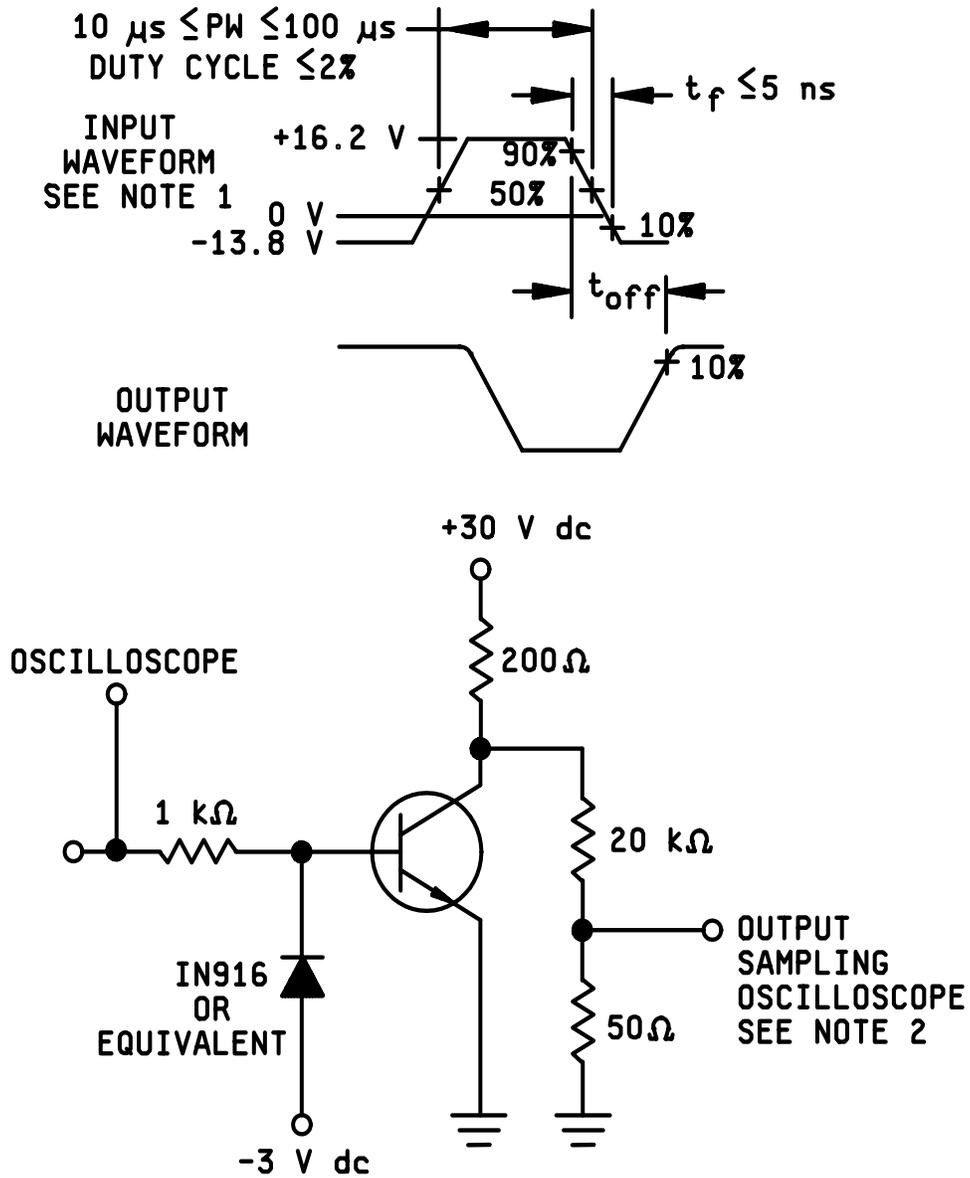
FIGURE 5. Thermal impedance graph ($R_{\theta JC}$) for 2N5581 and 2N5582 (TO-46).



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 2.0 ns;
duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ k Ω ; $C_{in} \leq 12$ pF; rise time ≤ 5.0 ns.

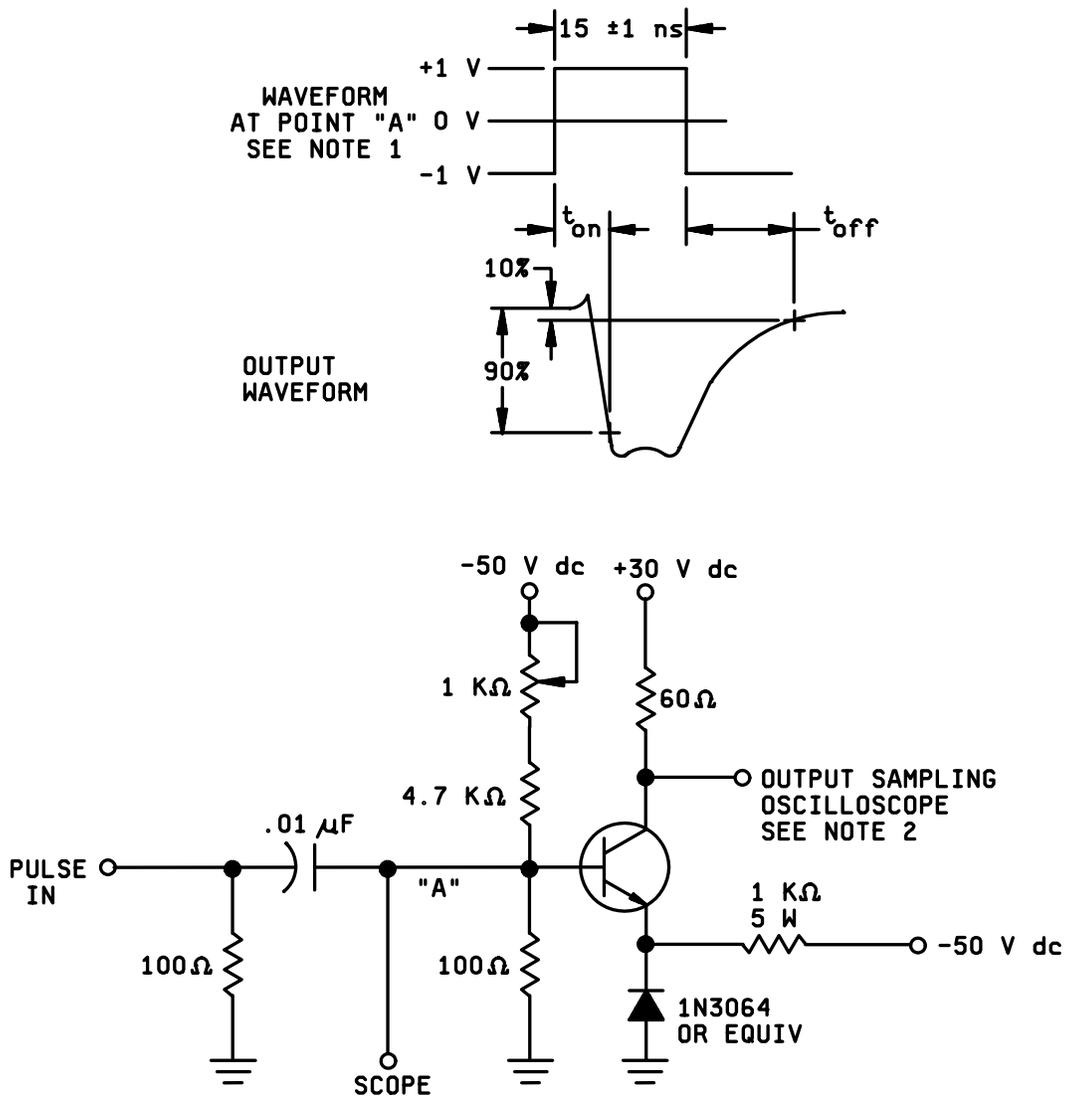
FIGURE 6. Saturated turn-on switching time test circuit.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be $\leq 2.0 \text{ ns}$; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms .
2. Output sampling oscilloscope: $Z_{\text{in}} \geq 100 \text{ k}\Omega$; $C_{\text{in}} \leq 12 \text{ pF}$; rise time $\leq 0.2 \text{ ns}$.

FIGURE 7. Saturated turn-off switching time test circuit.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ k Ω ; $C_{in} \leq 12$ pF; rise time ≤ 0.2 ns.

* FIGURE 8. Nonsaturated turn-on switching time test circuit.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead formation and finish may be specified (see 3.4.1).
- d. Type designation and product assurance level.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML No. 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2796)

Review activities:
Air Force - 2, 19

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://www.dodssp.daps.mil/>