

The documentation and process conversion measures necessary to comply with this revision shall be completed by 11 September 2002.

INCH-POUND

MIL-PRF-19500/496B
AMENDMENT 2
11 June 2002
SUPERSEDING
AMENDMENT 1
25 March 2001

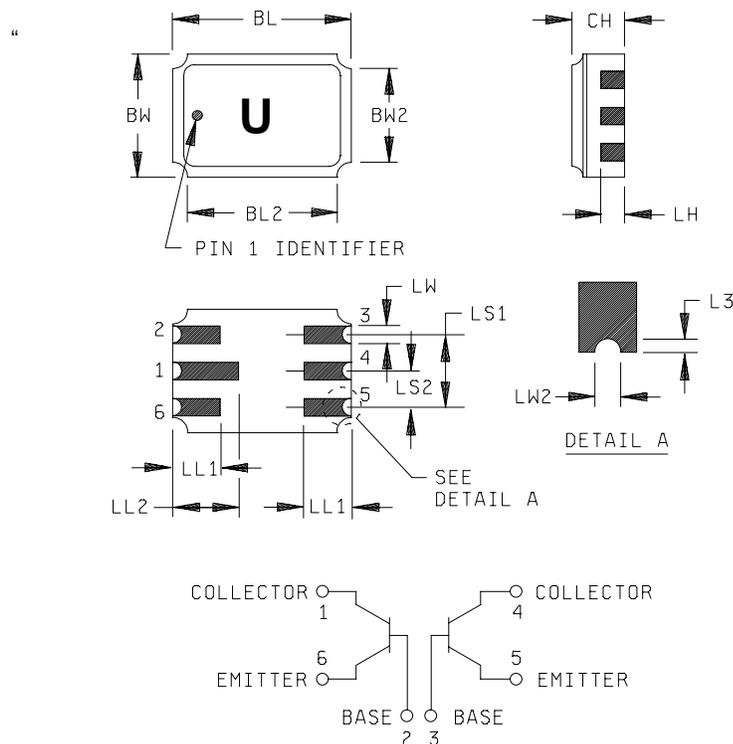
PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, DUAL, PNP, UNITIZED,
SILICON, TYPES 2N5795 2N5796, AND 2N5796U, JAN, JANTX AND JANTXV

This amendment forms a part of MIL-PRF-19500/496B, dated 15 September 1998, and is approved for use by all Departments and Agencies of the Department of Defense.

PAGE 4

* FIGURE 2, delete and substitute:



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“

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL ₂		.250		6.35
BW	.165	.175	4.19	4.45
BW ₂		.175		4.45
CH	.058	.100	1.47	2.54
L ₃	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99
LL ₁	.060	.070	1.52	1.78
LL ₂	.082	.098	2.08	2.49
LS ₁	.095	.105	2.41	2.67
LS ₂	.045	.055	1.14	1.40
LW	.022	.028	0.56	0.71
LW ₂	.006	.022	0.15	0.56

“NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Dimension "CH" controls the overall package thickness.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "LW₂" minimum and "L₃" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW₂" maximum and "L₃" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. Lead 4 = no connection.

FIGURE 2. Physical dimensions, 2N5796U.”

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4.3.1, delete and substitute:

“4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc. Power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum and a minimum $P_D = 75$ percent of P_T maximum rated as defined in 1.3.”

4.4.2, step 1, condition column, delete and substitute:

“Steady-state life: Test condition B, 340 hours, $V_{CB} = 10 - 30$ V dc. Power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0.$ ”

FIGURE 3, delete and substitute:

“

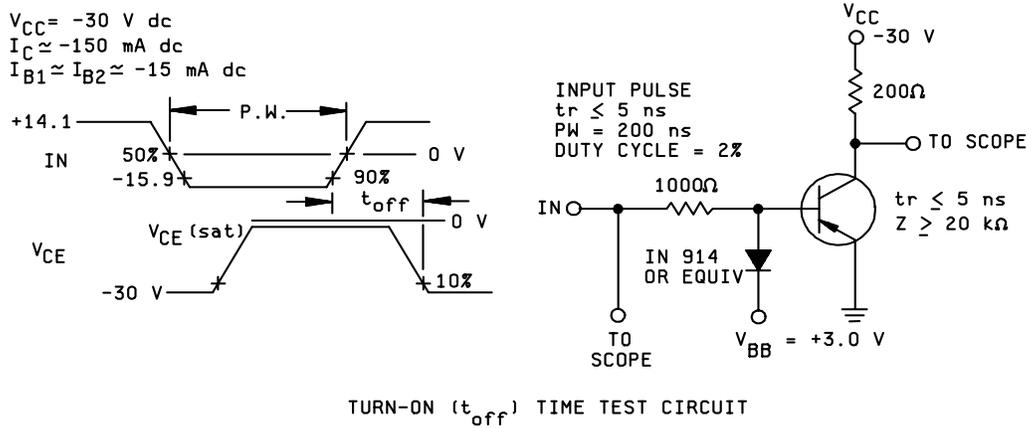
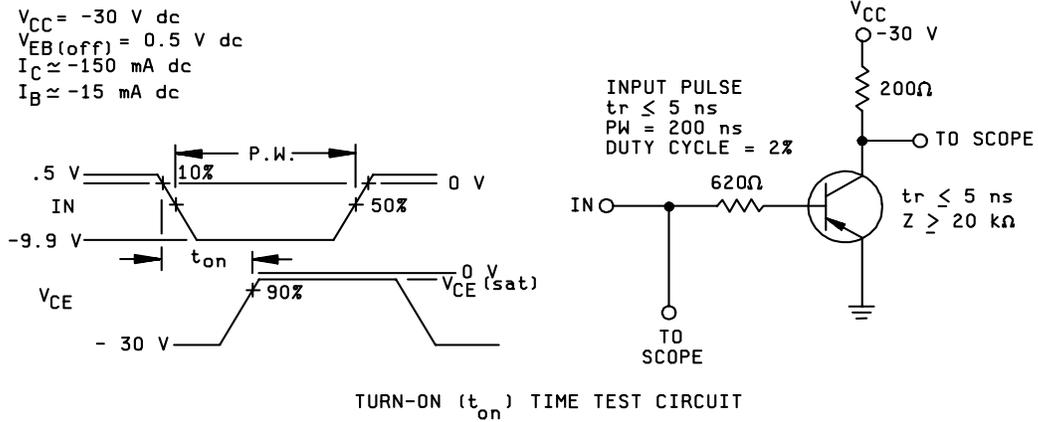


FIGURE 3. Switching time test circuits.”

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The margins of this amendment are marked with an asterisk to indicate where changes from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2639)

Review activities:
Army - AR, MI, SM
Navy - AS, MC, OS
Air Force - 19, 99