-The documentation and process conversion measures necessary to comply with this revision shall be completed by 20 January 1999

INCH-POUND

MIL-PRF-19500/566B
20 October 1998
SUPERSEDING
MIL-S-19500/566A
8 September 1987

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, FIELD EFFECT, N-CHANNEL, SILICON, LOGIC LEVEL, TYPES 2N6902, AND 2N6904 JAN, JANTX, JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for logic level, N-channel, enhancement-mode, MOSFET, power transistor. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1. (TO-204AA for types 2N6902 and 2N6904; (formerly TO-3)).

1.3 Maximum ratings. (Unless otherwise specified, T_A = +25°C).

Type	P_T 1/ T_C = +25°C	P_T T_A = +25°C	V_{DS}	V_{DG}	V_{GS}	I_{D1} 2/ T_C = +25°C	I_{D2} 2/ T_C = +100°C	I_S 2/
	W	W	V dc	V dc	V dc	A dc	A dc	A dc
2N6902	75	4	100	100	±10	12.0	9.6	12.0
2N6904	75	4	200	200	±10	8.0	5.1	8.0

1/ Derate linearly, 0.6 W/°C for T_C > +25°C.

2/ Derate above T_C = +25°C according to the formula $I_D = \sqrt{\frac{P(rated)}{K}}$ where P(rated) = P_T - (T_C -25) (W/°C) watts;

K = Max $r_{DS(on)}$ at T_J = + 150max - T_C°C.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAT, 3990 East Broad Street, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	I_{DM}	Min $V_{(BR)DSS}$ V_{GS} = 0 V I_D = 1 mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA		Max I_{DSS1} V_{GS} = 0 V		T_J and T_{STG}	Max $r_{DS(on)}$ 1/ V_{GS} = 5 V dc		$R_{\theta JC}$ max
					V_{DS} = 80 V	V_{DS} = 160 V		T_J = +25°C at I_{D1}	T_J = +150°C at I_{D2}	
	A (pk)	V dc	V dc Min	V dc Max	µA dc	µA dc	°C	Ω	Ω	°C/W
2N6902	30	100	1.0	2.0	1.0		-55 to +150	0.2	0.52	1.67
2N6904	20	200	1.0	2.0		1.0		0.6	1.17	1.67

1/ Pulsed (see 4.5.1)

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications or specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

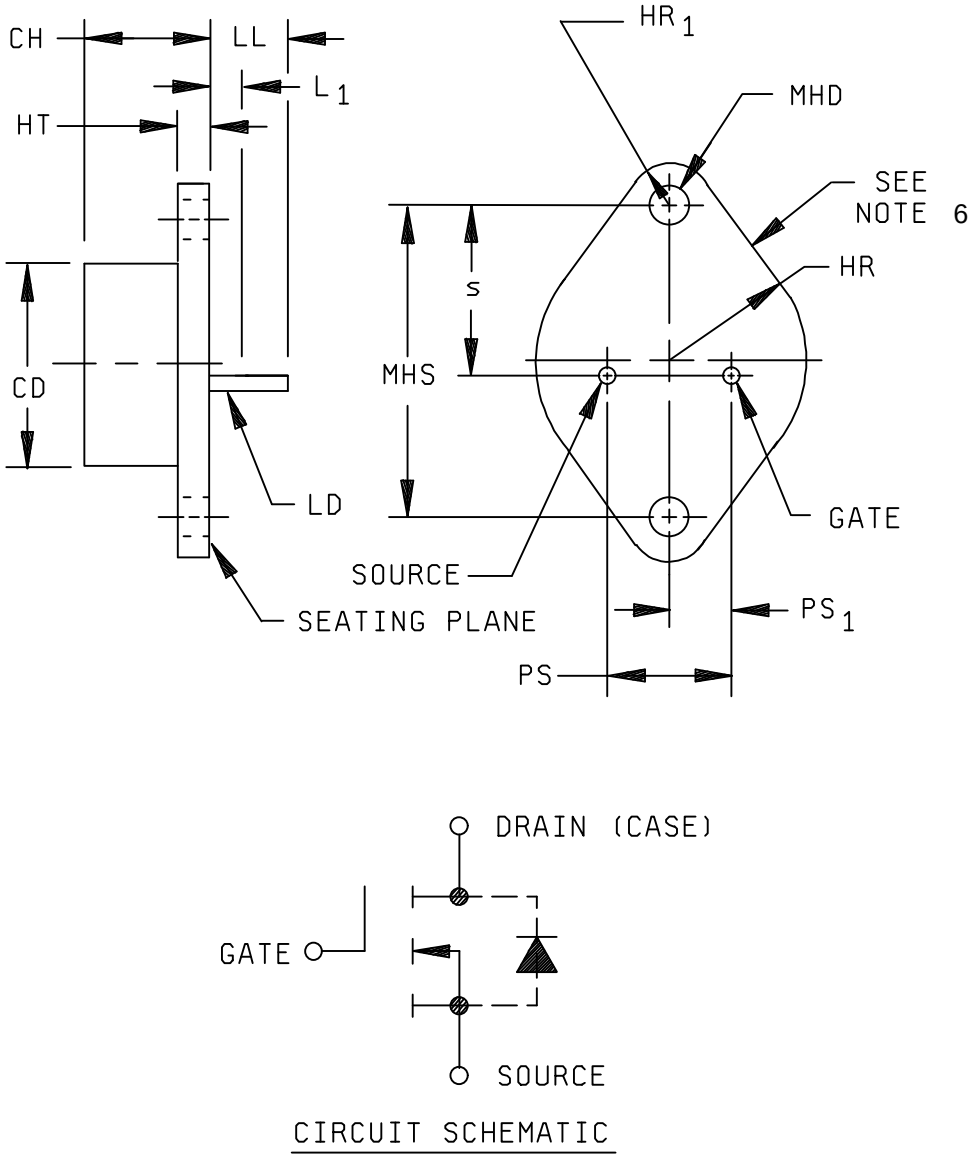

FIGURE 1. Physical dimensions of transistor type TO-204AA.

Dimensions					
Ltr	Inches		Millimeter		Notes
	Min	Max	Min	Max	
CD		.875		22.23	
CH	.250	.360	6.35	9.15	3
HR	.495	.525	12.57	13.3	
HR_1	.131	.188	3.33	4.78	
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.10	
LL	.312	.500	7.92	12.70	
L_1		.050		1.27	
MHD	.151	.161	3.84	4.09	
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	3
PS_1	.205	.225	5.21	5.72	3
s	.655	.675	16.64	17.15	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. These dimensions shall be measured at points .050 inch (1.27 mm) and .055 inch (1.40 mm) below the seating plane. When gauge is not used, measurement will be made at the seating plane.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. Mounting holes shall be deburred on the seating plane side.
6. Drain is electrically connected to the case.

FIGURE 1. Physical dimensions of transistor type TO-204AA - Continued.

3. REQUIREMENTS

3.1 Qualification. Devices furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list before contract award (see 4.2 and 6.3).

3.2 Associated specification. The individual item performance requirements shall be in accordance with MIL-PRF-19500, and as specified herein.

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.3 Interface requirements and physical dimensions. The interface requirements and physical dimensions for the purpose of interchangeability shall be as specified on figures 1 and 2 herein.

3.3.1 Lead material and finish. Lead material shall be Kovar or Alloy 52; a copper core or a plated core is permitted. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein.

3.3.2 Construction. These devices shall be constructed in a manner and using materials which enable the diodes to meet the applicable requirements of MIL-PRF-19500 and this document.

3.3.3 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.4 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static discharge. The following handling practices are recommended (see 3.5).

a. Devices shall be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care shall be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate shall be terminated to source, $R \leq 100$ k, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be subgroups specified in 4.4.2 and 4.4.3.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3)

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with MIL-PRF-19500 (Appendix E, table IV), and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see MIL-PRF-19500, appendix E, table IV	Measurements	
	JANS level	JANTX and JANTXV
3	Test condition F, except T_{low} = - 55°C, 20 cycles.	Test condition F, except T_{low} = - 55°C, 20 cycles.
1/ 2/	MIL-STD-750, method 3470 (see 4.5.4)	MIL-STD-750, method 3470 (see 4.5.4)
1/	MIL-STD-750, method 3161 (see 4.5.3)	MIL-STD-750, method 3161 (see 4.5.3).
9	I_{GSS1}, I_{DSS1}, gate stress test (see 4.5.5) Subgroup 2 of table 1 herein.	Gate stress test (see 4.5.5) Subgroup 2 of table 1 herein.
10	MIL-STD-750, method 1042, test condition B	MIL-STD-750, method 1042, test condition B
11	Subgroup 2 of table I herein. I_{GSS1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ ΔI_{GSS1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±.2 µA dc or ±100 percent of initial value, whichever is greater	Subgroup 2 of table I herein I_{GSS1}, I_{DSS1}, $r_{DS(on)1}$. $V_{GS(th)1}$
12	MIL-STD-750, method 1042, test condition C, (see 4.3.1)	MIL-STD-750, method 1042, test condition A.
13	Subgroups 2 and 3 of table I. ΔI_{GSS1} = ±20 nA dc or ±100 percent of initial value whichever is greater. ΔI_{DSS1} = ± .2 µA dc or ±100 percent of initial value whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value.	Subgroups 2 and 3 of table I. ΔI_{GSS1} = ±20 nA dc or ±100 percent of initial value whichever is greater. ΔI_{DSS1} = ± .2 µA dc or ±100 percent of initial value whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value.

1/ Shall be performed anytime before screen 9.
2/ This test method in no way implies an avalanche energy rating. This is a stress test designed to ensure a rugged product.

4.3.1 Power burn-in. Power burn-in conditions are as follows: T_A = room ambient as defined in the general requirements of MIL-STD-750. $V_{DS} \geq 10$ V minimum; I_D adjusted to meet a junction temperature of +140°C - 0°C + 5°C by controlling V_{GS} voltage to obtain a specific I_D current required to apply appropriate power for the device under stress. Power condition and T_J requirements can be established by ΔV_{SD} measurement technique described in MIL-STD-750, method 3161. For condition C, t = 240 hours.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Alternate flow is allowed for conformance inspection in accordance with figure 2 of MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, appendix E, table V and table I herein. End-point electrical and delta measurements shall be in accordance with the applicable tests of table II herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table VIa (JANS) and table VIb (JANTX, JANTXV, and JANS) of MIL-PRF-19500, and as follows. End-point electrical and delta measurements shall be in accordance with the applicable steps of table II herein.

4.4.2.1 Group B inspection, appendix E, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
B3	1051	Test condition F3, except T_{low} = -55°C
B4	1042	Test condition D; The heating cycle shall be 3 minutes minimum for 2,000 cycles. No forced air cooling on the device shall be permitted.
		V_{DS} = 20 V dc; P_T = 4 W at TA = + 25°C ± 3°C.
B5	1042	120 hours; see 4.3.1; T_A = +200°C . Marking legibility requirements shall not apply
		V_{DS} = 20 V dc; P_T = 4 W at T_A = + 75°C ± 3°C.

4.4.2.2 Group B inspection, appendix E, table VIb (JAN, JANTX and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Conditions
B2	1051	Test condition F3, except T_{low} = -55°C and 25 cycles.
B3	1042	Test condition D; The heating cycle shall be 3 minutes minimum for 2,000 cycles. No forced air cooling on the device shall be permitted.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table VII of MIL-PRF-19500. End-point electrical and delta measurements shall be in accordance with the applicable steps of table II herein.

4.4.3.1 Group C inspection, appendix E, table VII of MIL-PRF-19500.

Subgroup	Method	Conditions
C6	1042	Test condition D; 6,000 cycles minimum. The heating cycle shall be 1 minute minimum.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal impedance. Thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750. $R_{\theta JC}$max = 1.67°C/W.

a. I_M measuring current ..... 10 mA.

b. I_H drain heating current ` ..... 2 A.

c. t_H heating time..... Steady-state (see MIL-STD-750, method 3161 for definition).

d. V_H drain-source heating voltage..... 25 V.

e. t_{MD} measurement time delay ..... 10 to 80 µs.

f. t_{SW} sample window time ..... 10 µs (max).

4.5.3 Thermal response (ΔV_{SD} measurements). The ΔV_{SD} measurements shall be performed with method 3161 of MIL-STD-750. The ΔV_{SD} conditions (I_H and V_H) and maximum limit shall be derived by each vendor. The read and record ΔV_{SD} measurements and conditions for each device in the qualification lot shall be submitted in the qualification report. The chosen ΔV_{SD} shall be considered final after the manufacturer has had the opportunity to test five consecutive lots. The following parameter measurements shall apply:

a. I_M measuring current ..... 10 mA.

b. I_H drain heating current ..... 2 A.minimum

c. t_H heating time ..... 100 ms.

d. V_H drain-source heating voltage..... 25 V minimum.

e. t_{MD} measurement time delay ..... 10 to 80 µs.

f. t_{SW} sample window time ..... 10 µs (max).

4.5.4 Unclamped inductive switching.

a. Peak current, I_D..... 3.0 A.

b. Peak gate voltage, V_{GS}..... 10 V.

c. Gate to source resistor, R_{GS}

d. Initial case temperature ..... +25°C +10°C, -5°C.

e. Inductance ..... 100 µH ±10 percent.

f. Number of pulses to be applied ..... 1 pulse minimum.

4.5.5 Gate stress test.

a. V_{GS} = 15 V minimum.

b. t = 250 µs minimum.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Breakdown voltage drain to source	3407	V_{GS} = 0 V dc; I_D = 1 mA dc, Bias condition C	$V_{(BR)DSS}$			V dc
2N6902				100		
2N6904				200		
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = 1.0 mA dc	$V_{GS(th)1}$	1.0	2.0	V dc
Gate current	3411	V_{GS} = +10 and -10 V dc; bias condition C, V_{DS} = 0	I_{GSS1}		± 100	nA dc
Drain current	3413	Bias condition C V_{GS} = 0 V dc;	I_{DSS1}			µA dc
2N6902		V_{DS} = 80 V dc			1.0	
2N6904		V_{DS} = 160 V dc			1.0	
Static drain to source on-state resistance	3421	Bias condition A V_{GS} = 5 V dc, pulsed (see 4.5.1),	$r_{DS(on)1}$			µA dc
2N6902		I_{D2} = 9.6 A dc			0.2	
2N6904		I_{D2} = 5.1 A dc			0.6	
Drain to source “on-state” voltage	3405	Bias condition A V_{GS} = 5 V dc, pulsed (see 4.5.1),	$V_{DS(on)}$			V dc
2N6902		I_D = 12.0 A dc			3.3	
2N6904		I_D = 8.0 A dc			5.5	
Forward voltage (source-drain diode)	4011	Pulsed (see 4.5.1) V_{GS} = 0 V	V_{SD}	0.8	1.6	V dc
2N6902		I_S = 12.0 A dc				
2N6904		I_S = 8.0 A dc				
Forward transconductance	3475	I_D = Rated I_{D2} (see 1.3) Pulsed (see 4.5.1)	gFS			S
2N6902				3	12	
2N6904				3	12	

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J$ =125°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = 1.0 mA dc	$V_{GS(th)2}$	0.5		V dc
Gate current	3411	Bias condition C; V_{GS} = +10 and -10 V dc V_{DS} = 0 V dc	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C; V_{GS} = 0 V dc	I_{DSS2}		50	µA dc
2N6902		V_{DS} = 80 V dc				
2N6904		V_{DS} = 100 V dc				
Static drain to source on-state resistance	3421	V_{GS} = 5 V dc pulsed (see 4.5.1)	$r_{DS(on)2}$			Ω
2N6902		I_{D2} = 9.6 A dc			0.32	
2N6904		I_{D2} = 5.1 A dc			1.11	
Low temperature operation:		$T_C = T_J$ = - 55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = 1.0 mA dc	$V_{GS(th)3}$		3.0	V dc
Subgroup 4						
Switching time	3472	I_D = rated I_{D2} (see 1.3) V_{GS} = 5 V dc Gate drive impedance = 7.5 Ω				
Turn-on delay time			$t_{d(on)}$			ns
2N6902		V_{DD} = 50 V dc			50	
2N6904		V_{DD} = 100 V dc			45	
Rise time			t_r			ns
2N6902		V_{DD} = 50 V dc			150	
2N6904		V_{DD} = 100 V dc			150	
Turn-off delay time			$t_{d(off)}$			ns
2N6902		V_{DD} = 50 V dc			130	
2N6904		V_{DD} = 100 V dc			135	
Fall time			t_f			ns
2N6902		V_{DD} = 50 V dc			150	
2N6904		V_{DD} = 100 V dc			105	

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area	3474	See figure 2, V_{DS} = 80 percent of rated V_{DS} and $V_{DS} \leq 200$ V max				
High voltage test		t_p = 1 s				
2N6902 2N6904						
Electrical measurements		See table II, steps, 1, 2, 3, 4, 5 6 and 7				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition A or B				
On-state gate charge			$Q_g(on)$			nC
2N6902 2N6904				9 7	19 17	
Gate to source charge			Q_{gs}			nC
2N6902 2N6904				1.1 1.4	5.0 5.0	
Gate to source charge			Q_{gd}			nC
2N6902 2N6904				5 3	16 14	
Reverse recovery time		di/dt = 100 A/µs $V_{DD} \leq 30$ V dc, I_F = 4 A	t_{rr}			ns
2N6902 2N6904					375 625	

1/ For sample plan, see MIL-PRF-19500.

TABLE II. Groups B and C electrical measurements. 1/ 2/ 3/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Breakdown voltage drain to source	3407	V_{GS} = 0, I_D = 1 mA dc Bias condition C;	$V_{(BR)DSS}$			V dc
	2N6902 2N6904				100 200		
2.	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D =1 mA dc	$V_{GS(th)1}$	1.0	2.0	V dc
3.	Gate current	3411	V_{GS} = +10 and -10 V dc Bias condition C; V_{DS} = 0,	I_{GSS1}		± 100	nA dc
4.	Drain current	3413	V_{GS} = 0 Bias condition C;	I_{DSS1}		50	µA dc
	2N6902 2N6904		V_{DS} =80 V dc V_{DS} =160 V dc				
5.	Static drain to source on-state resistance	3421	V_{GS} = 10 V dc condition A, pulsed (see 4.5.1).	$r_{DS(on)1}$			Ω
	2N6902 2N6904		I_{D2} = 9.6 A dc I_{D2} = 5.1 A dc			0.2 0.6	
6.	Static drain to source on-state resistance	3405	V_{GS} = 5 V dc condition B, pulsed (see 4.5.1).	$V_{DS(on)}$			V
	2N6902 2N6904		I_D = 12.0 A dc I_D = 8.0 A dc			3.3 5.5	
7.	Forward voltage (source-drain diode)	4011	Pulsed (see 4.5.1) V_{GS} = 0	V_{SD}	0.8	1.6	V
	2N6902 2N6904		I_S = 12.0 A dc I_S = 8.0 A dc				
8.	Thermal response		See 4.5.3	ΔV_{SD}			

1/ The electrical measurements for appendix E, table VIa (JANS) of MIL-PRF-19500 are as follows:

a. Subgroup 3, table I, steps 1, 2, 3, 4, 5, 6, and 7.

b. Subgroup 4, table I, steps 1, 2, 3, 4, 5, 6, 7, and 8.

c. Subgroup 5, table I, steps 1, 2, 3, 4, 5, 6, and 7.

TABLE II. Groups A, B, and C electrical measurements - Continued. 1/ 2/ 3/

2/ The electrical measurements for appendix E, table VIb (JANTX and JANTXV) of MIL-PRF-19500 are as follows:

a. Subgroup 2, table I, steps 1, 2, 3, 4, 5, 6, and 7.

b. Subgroup 3, table I, steps 1, 2, 3, 4, 5, 6, 7, and 8.

c. Subgroup 6, table I, steps 1, 2, 3, 4, 5, 6, and 7.

3/ The electrical measurements for appendix E, table VII of MIL-PRF-19500 are as follows:

a. Subgroup 2, table I, steps 1, 2, 3, 4, 5, 6, and 7.

b. Subgroup 3, table I, steps 1, 2, 3, 4, 5, 6, and 7.

c. Subgroup 6, table I, steps 1, 2, 3, 4, 5, 6, 7, and 8.

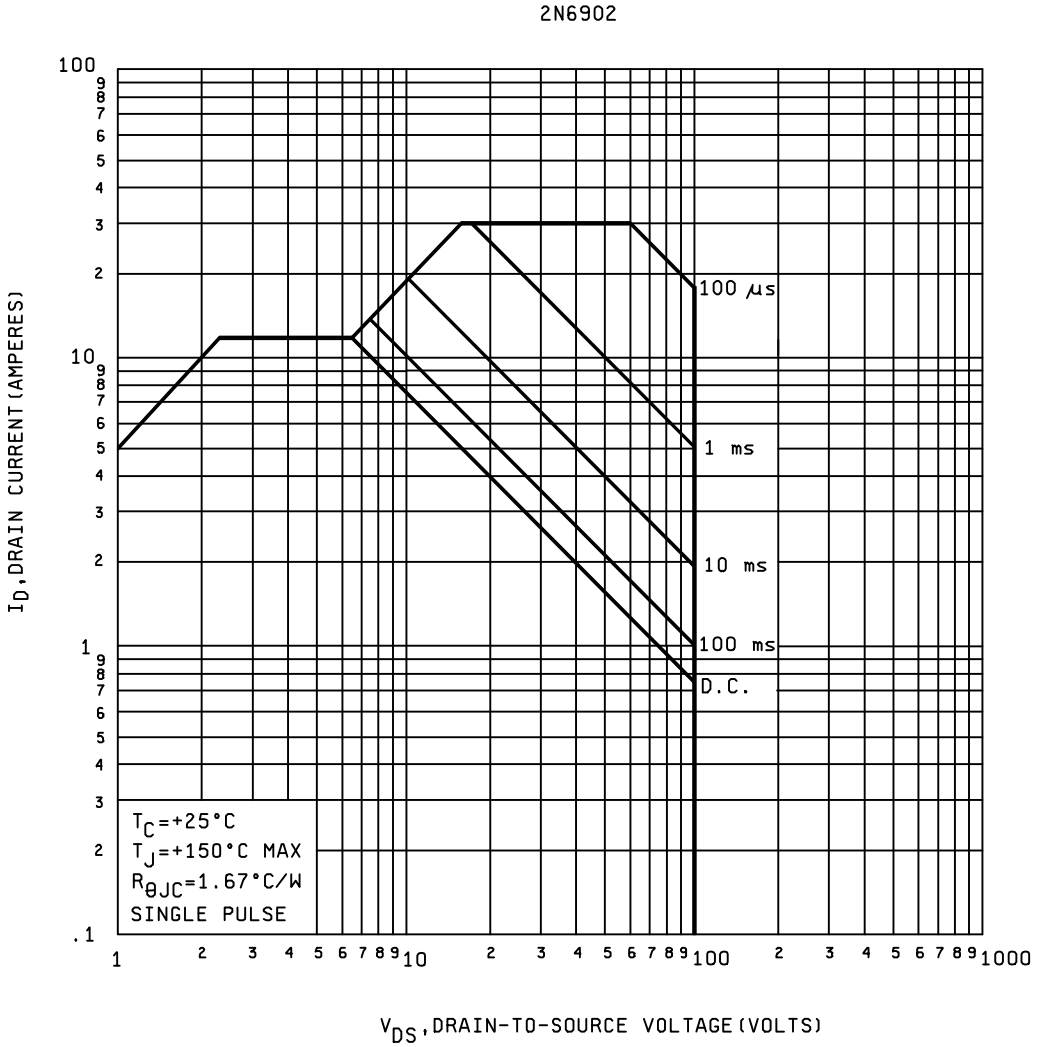

FIGURE 2. Safe operating area graph.

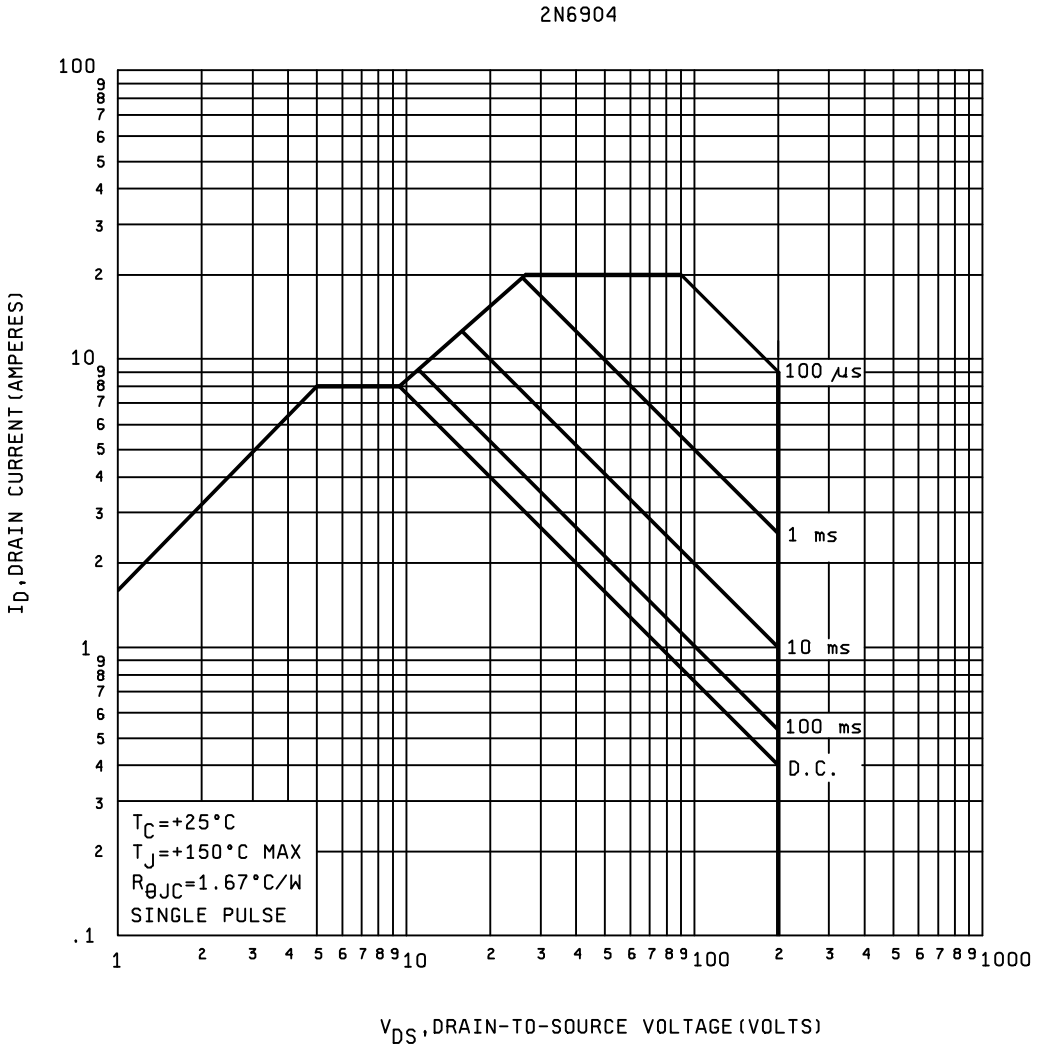

FIGURE 2. Maximum safe operating area graph - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of material is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Department or Defense Agency, or within the Military Departments' System Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

5.2 Marking. Unless otherwise specified (see 6.2), marking shall be in accordance with MIL-PRF-19500.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. See MIL- PRF-19500.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Products List QPL No.19500 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from: Commander, Defense Supply Center Columbus, ATTN: DSCC-VQE, 3990 East Broad Street, Columbus, OH 43216-5000.

6.4 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:
Army - CR
Navy -EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI, SM
Air Force - 11, 13, 19, 85, 99
Navy - AS, CG, MC, OS

Preparing activity:
DLA - CC

(Project 5961-2037)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.

2. The submitter of this form must complete blocks 4, 5, 6, and 7.

3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	**1. DOCUMENT NUMBER** MIL-PRF-19500/566B	**2. DOCUMENT DATE (YYMMDD)** 981020

3. DOCUMENT TITLE
SEMICONDUCTOR DEVICE, FIELD EFFECT TRANSISTORS, N-CHANNEL, SILICON, LOGIC - LEVEL TYPES 2N6902 AND 2N6904 JAN, JANTX, JANTXV AND JANS

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) Commercial: DSN: FAX: EMAIL:	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. Point of contact: Alan Barone	b. TELEPHONE (Include Area Code) Commercial: (614)692-0510 DSN: 850-0510 FAX: (614)692-6939 EMAIL: alan_barone@dscc.dla.mil
c. ADDRESS: Defense Supply Center Columbus, ATTN: DSCC-VAT, 3990 East Broad Street, Columbus, OH 43216-5000	**IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT:** Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 DSN 289-2340