The documentation and process conversion measures necessary to comply with this revision shall be completed by 2 December 2003.

INCH-POUND

MIL-PRF-19500/595E
2 September 2003
SUPERSEDING
MIL-PRF-19500/595D
13 August 2002

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT,
TRANSISTOR, P-CHANNEL, SILICON,
TYPES 2N7236, 2N7237, 2N7236U, AND 2N7237U,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an P-channel, enhancement-mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500, and two levels of product assurance for each unencapsulated device type die, with avalanche energy ratings (E_{AS} and E_{AR}) and maximum avalanche current (I_{AR}).

1.2 Physical dimensions. See figure 1 (TO-254AA), figure 2 (TO-267AB) for surface mount devices, and figure 3 for JANHC and JANKC (die) dimensions.

* 1.3 Maximum ratings (T_C = +25°C, unless otherwise specified).

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = -1.0 mA dc	P_T (1) T_C = +25°C	P_T T_A = +25°C	V_{GS}	I_{D1} (2) (3) T_C = +25°C	I_{D2} (2) T_C = +100°C	I_S	I_{DM} (4)	T_{op} and T_{STG}	$R_{\theta JC}$ max
	V dc	W	W	V dc	A dc	A dc	A dc	A(pk)	°C	°C/W
2N7236, 2N7236U	-100	125	4.0	±20	-18	-11	-18	-72	-55 to +150	1.0
2N7237, 2N7237U	-200	125	4.0	±20	-11	-7	-11	-44	-55 to +150	1.0

See footnotes next page.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5961

* 1.3 Maximum ratings - continued.

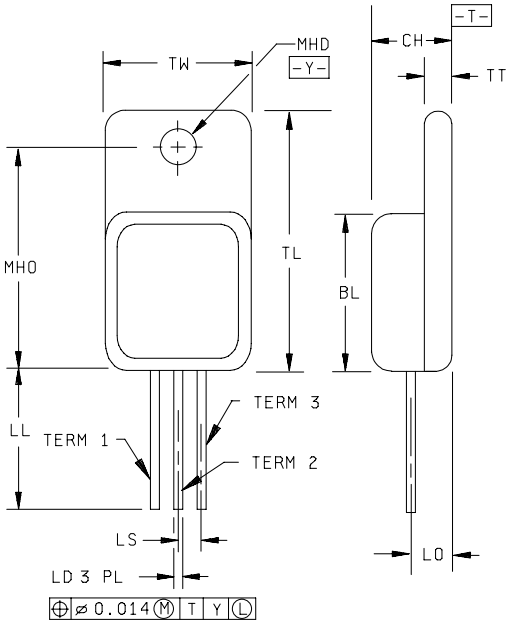
Type	I_{AR}	E_{AS}	E_{AR}	$r_{DS(on)}$ max (5) V_{GS} = -10 V dc $I_D = I_{D2}$	
				T_J = +25°C	T_J = +150°C
	A	mj	mj	ohm	ohm
2N7236, 2N7236U	-18	500	12.5	0.20	0.400
2N7237, 2N7237U	-11	500	12.5	0.51	1.122

(1) Derate linearly 1.0 W/°C for T_C > +25°C;
(2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter: $I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$
(3) See figure 4, maximum drain current graphs.
(4) I_{DM} = 4 X I_{D1} as calculated in footnote (2).
(5) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. T_C = +25°C (unless otherwise specified).

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = -1.0 mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ I_D = -0.25 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(on)1}$ (1) $I_D = I_{D2}$ V_{GS} = 10 V
	V dc	V dc		µA dc	Ohms
		Min	Max		
2N7236, 2N7236U	-100	-2.0	-4.0	25	0.20
2N7237, 2N7237U	-200	-2.0	-4.0	25	0.51

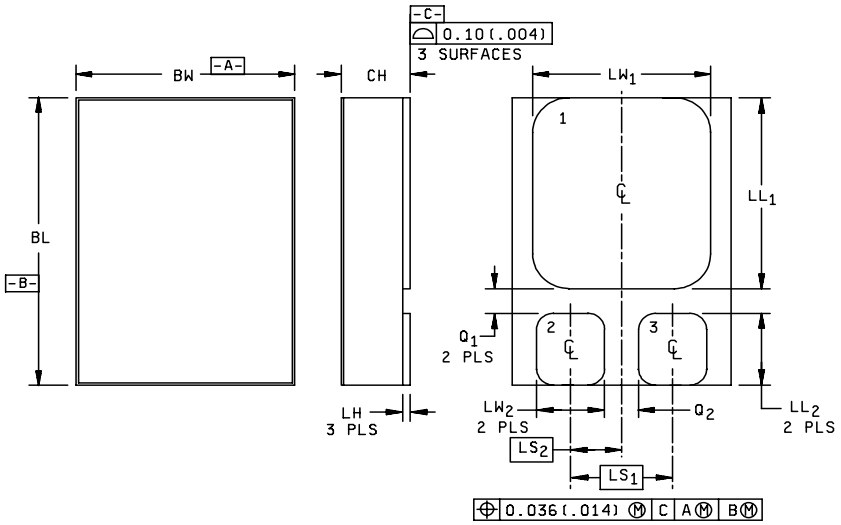
(1) Pulsed (see 4.5.1).



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.750	12.95	14.48	
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	3, 4
TT	.040	.050	1.02	1.27	3, 4
TW	.535	.545	13.59	13.84	
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Glass meniscus included in dimension TL and TW.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

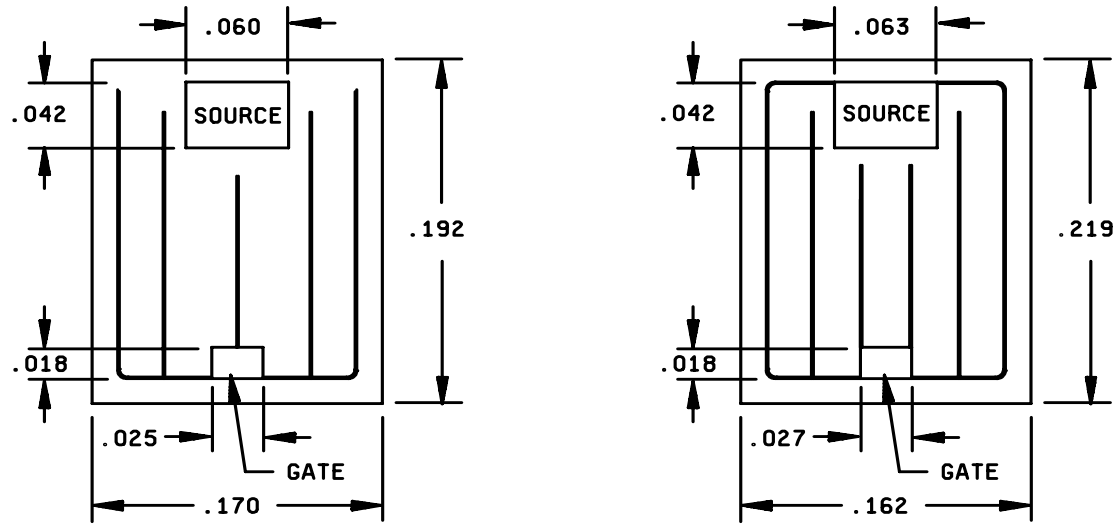
* FIGURE 1. Physical dimensions for TO-254AA (2N7236 and 2N7237).



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL_1	.410	.420	10.41	10.67
LL_2	.152	.162	3.86	4.11
LS_1	.210 BSC		5.33 BSC	
LS_2	.105 BSC		2.67 BSC	
LW_1	.370	.380	9.40	9.65
LW_2	.135	.145	3.43	3.68
Q_1	.030		0.76	
Q_2	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. Dimensioning and tolerancing shall be in accordance with ASME Y14.5M.

* FIGURE 2. Dimensions and configuration of surface mount package outline (TO-267AB), 2N7236U and 2N7237U).



A version

Inches	mm
.018	0.46
.025	0.64
.027	0.69
.042	1.07
.060	1.52
.063	1.60
.162	4.11
.170	4.32
.192	4.88
.219	5.56

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Unless otherwise specified, tolerance is .005 inch (0.13 mm).
4. Physical characteristics of the die thickness = .0187 inch (0.47 mm).
5. Back metal: Cr - Ni - Ag.
6. Top metal: Al.
7. Back contact: Drain.
8. See 6.5 for ordering information.

* FIGURE 3. Physical dimensions JANHC and JANKC die.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 (TO-254AA), 2 (TO-267AB, surface mount), and 3 (die) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

* 3.4.1 Lead formation material and finish. Lead material shall be Kovar or Alloy 52; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation material or finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table IV of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source. $R \leq 100$ k, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

* 3.7 Electrical test requirements. The electrical test requirements shall be table I, as specified herein.

* 3.8 Marking. Marking shall be in accordance with MIL-PRF-19500, except at the option of the manufacturer, the country of origin and/or the manufacturers identification may be omitted from the body of the transistor.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for qualification inspection in accordance with of MIL-PRF-19500.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the associated specification that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV level
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2)
(3)	Method 3470 of MIL-STD-750. (see 4.3.3)	Method 3470 of MIL-STD-750. (see 4.3.3)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
9	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, subgroup 2 of table I herein	Subgroup 2 of table I herein
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = +20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A or T_A = +175°C and t = 48 hours
13	Subgroup 2 and 3 of table I herein. ΔI_{GSSF1} = +20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(th)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein. ΔI_{GSSF1} = +20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(th)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1} and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime before screen 9.

* 4.3.1 Screening (JANHC and JANKC). Screening of die shall be in accordance with MIL-PRF-19500, (appendix H), as a minimum die shall be 100 percent probed in accordance with table I, subgroup 2, except test current shall not exceed 20 A.

* 4.3.2 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

* 4.3.3 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_D)..... I_{AR}(max).

b. Peak gate voltage (V_{GS}) ..... -10 V.

c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200\ \Omega$.

d. Initial case temperature..... +25°C +10°C, -5°C.

e. Inductance..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V for 2N7236, 2N7236U, -50 V for 2N7237, 2N7237U.

* 4.3.4 Thermal impedance ($Z_{\theta JC}$ measurements). The $Z_{\theta JC}$ measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit (not to exceed the table I, subgroup 2 limit or figure 5 thermal impedance curve) for $Z_{\theta JC}$ in screening (table IV of MIL-PRF-19500) shall be derived by each vendor by means of statistical process control. When the process has exhibited control and capability, the capability data shall be used to establish the fixed screening limit. In addition to screening, once a fixed limit has been established, monitor all future sealing lots using a random five piece sample from each lot to be plotted on the applicable X bar R chart. If a lot exhibits an out of control condition, the entire lot shall be removed from the line and held for engineering evaluation and disposition. This procedure may be used in lieu of an in-line monitor. The following parameter measurements shall apply:

a. Measuring current (I_M) ..... 10 mA.

b. Drain heating current (I_H)..... 3.3 A minimum (2.5 A minimum for surface mount devices).

c. Heating time (t_H) ..... 100 ms minimum (25 ms minimum for surface mount devices).

d. Drain-source heating voltage (V_H)..... 25 V minimum (20 V minimum for surface mount devices).

e. Measurement time delay (t_{MD})..... 30 to 60 μs maximum.

f. Sample window time (t_{SW}) ..... 10 μs maximum.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G.
B3	2037	Test condition A. All internal wires for each device shall be pulled separately. If group B3 is to be continued to C6, strength test may be performed after C6.
B4	1042	Test condition D, 2,000 cycles. The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the "on" cycle.
B5	1042	A separate sample may be pulled for each test. Accelerated steady-state reverse bias; test condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours, read and record $V_{BR(DSS)}$ (pre and post) at I_D = -1 mA dc. Read and record I_{DSS} (pre and post) in accordance with table I, subgroup 2 herein. $V_{BR(DSS)}$ delta cannot exceed 10 percent.
B5	2037	Bond strength; test condition A.
B6	3161	See 4.5.2.

4.4.2.2 Group B inspection, table VIb (JAN, JANTX and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G.
B3	1042	Test condition D, 2,000 cycles. The heating cycle shall be 1 minute minimum.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

Subgroup	Method	Conditions
C2	2036	Test condition A; weight = 10 pounds, t = 10 s (not applicable for surface mount devices).
C5	3161	See 4.5.2
C6	1042	Test condition D, 6,000 cycles. The heating cycle shall be 1 minute minimum.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. $R_{\theta JC(max)}$ = 1.0°C/W for TO-254AA case style devices and surface mount devices. The following parameter measurements shall apply:

a. Measuring current (I_M) ..... 10 mA.

b. Drain heating current (I_H) ..... 3.3 A minimum (2.5 A minimum for surface mount devices).

c. Heating time (t_H) ..... Steady-state (see method 3161 of MIL-STD-750 for definition).

d. Drain-source heating voltage (V_H) ..... 25 V minimum (20 V minimum for surface mount devices).

e. Measurement time delay (t_{MD}) ..... 30 to 60 µs maximum.

f. Sample window time (t_{SW}) ..... 10 µs maximum.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.4	$Z_{\theta JC}$		1.30	°C/W
Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0V, I_D = 1 mA dc	$V_{(BR)DSS}$			
2N7236, 2N7236U				-100		V dc
2N7237, 2N7237U				-200		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -.25 mA	$V_{GS(th)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	Bias condition C, V_{GS} = ±20 V dc, V_{DS} = 0 V dc	I_{GSS1}		±100	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V dc, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		-25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D2} (see 1.3)	$r_{DS(on)1}$			
2N7236, 2N7236U					0.20	Ω
2N7237, 2N7237U					0.51	Ω
Static drain to source on-state resistance	3421	V_{GS} = -10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D1} (see 1.3)	$r_{DS(on)2}$			
2N7236, 2N7236U					0.22	Ω
2N7237, 2N7237U					0.52	Ω
Forward voltage (source drain diode)	4011	V_{GS} = 0 V dc, I_D = rated I_{D1}, pulsed (see 4.5.1)	V_{SD}			
2N7236, 2N7236U					-5.0	V
2N7237, 2N7237U					-5.0	V

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate reverse current	3411	Bias condition C $V_{GS} = \pm 20$ V dc, $V_{DS} = 0$ V dc,	I_{GSS2}		±200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, V_{DS} = 100 percent of rated V_{DS}	I_{DSS2}		-1.0	mA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, V_{DS} = 80 percent of rated V_{DS}	I_{DSS3}		-0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -0.25$ mA	$V_{GS(th)2}$	-1.0		V dc
Static drain to source on-state resistance	3421	$V_{GS} = -10$ V dc, pulsed (see 4.5.1), I_D = rated I_{D2} (see 1.3)	$r_{DS(on)3}$			
2N7236, 2N7236U					0.34	Ω
2N7237, 2N7237U					1.10	Ω
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -0.25$ mA	$V_{GS(th)3}$		-5.0	V dc
Subgroup 4						
Switching time test	3472	I_D = rated I_{D2} (see 1.3), $V_{GS} = -10$ V dc, gate drive impedance = 9.1 Ω, V_{DD} = 50 percent of $V_{BR(DSS)}$				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		85	ns
Turn-off delay time			$t_{d(off)}$		85	ns
Fall time			t_f		65	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 6; t_p = 10 ms, V_{DS} = 80 percent of rated $V_{BR(DSS)}$, V_{DS} = 200 V maximum				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7236, 2N7236U					60	nC
2N7237, 2N7237U					60	nC
Gate to source charge			Q_{gs}			
2N7236, 2N7236U					13	nC
2N7237, 2N7237U					15	nC
Gate to drain charge			Q_{gd}			
2N7236, 2N7236U					35.2	nC
2N7237, 2N7237U					38	nC
Reverse recovery time	3473	$d_i/d_t \leq 100$ A/µs, $V_{DD} \leq 30$ V, $I_D = I_{D1}$, (see 1.3)	t_{rr}			
2N7236, 2N7236U					280	ns
2N7237, 2N7237U					440	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test is required for the following end-point measurement only (not intended for screen 9, 11, or 13): JANS, table VIa of MIL-PRF-19500, group B, subgroups 3 and 4; JAN, JANTX, and JANTXV, table VIb of MIL-PRF-19500, group B, subgroups 2 and 3; and table VII of MIL-PRF-19500, group C, subgroup 6, and table IX of MIL-PRF-19500, group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

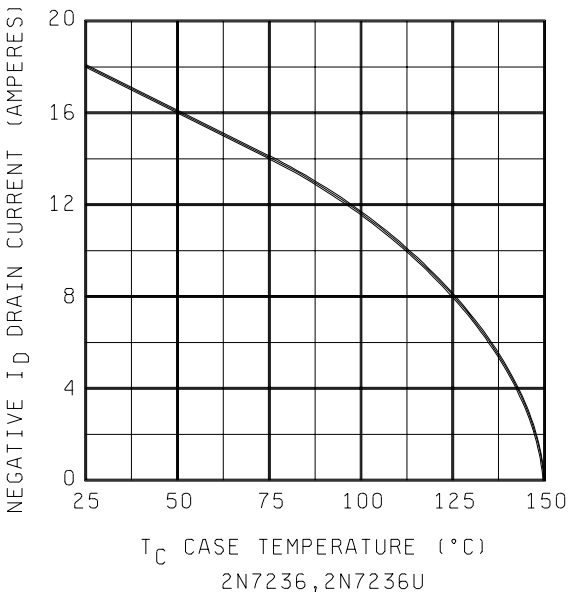
Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 1			22 devices c = 0
Temperature cycling	1051	500 cycles, test condition G	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 3			3 devices c = 0
DPA	2102		
Subgroup 4			sample size N/A
Thermal resistance, thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
Subgroup 5			
Not applicable			
Subgroup 6			3 devices
ESD	1020		
Subgroup 7			45 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		
Soldering heat	2031	1 cycle	

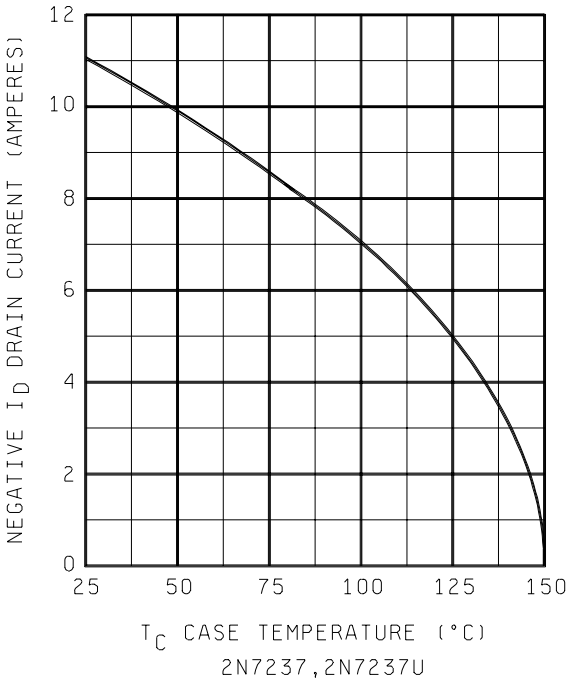
See footnotes at end of table.

* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only- Continued.

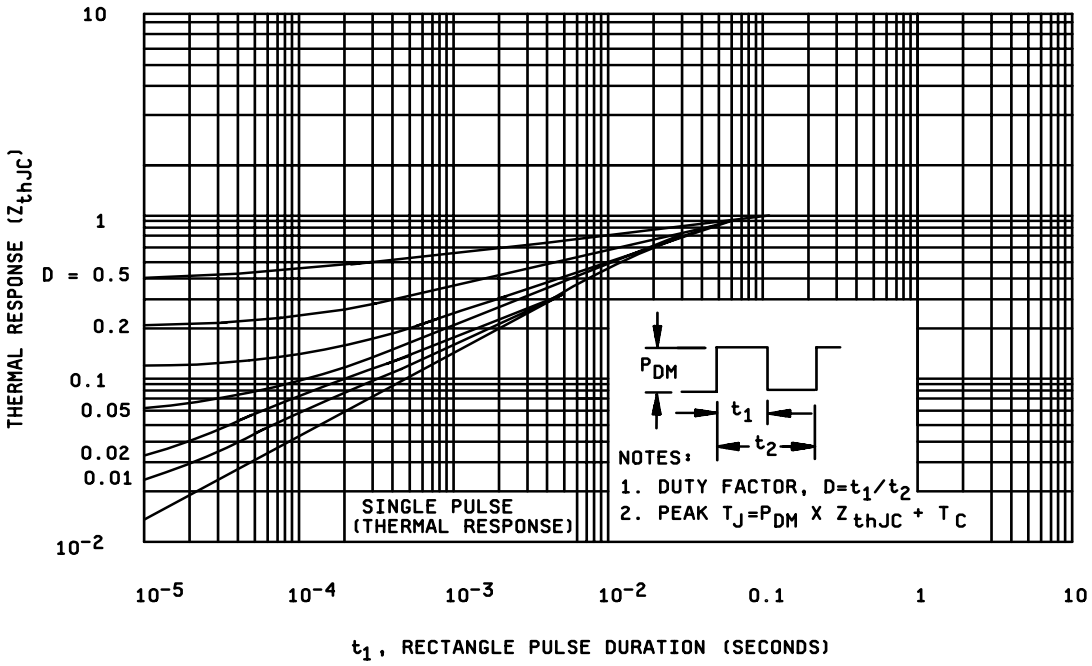
Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 8			
Repetitive avalanche energy	3469	Peak current $I_{AR} = I_D$; Peak gate voltage V_{GS} = -10 V; Gate to source resistor, R_{GS} 25 ≤ R_{GS} ≤ 200 ohms; temperature = T_J = +150°C +0, -10°C. Inductance = $\left[\frac{2E_{AR}}{(I_{D1})^2}\right]\left[\frac{V_{BR}-V_{DD}}{V_{BR}}\right]$ mH minimum Number of pulses to be applied = 3.6 X 10^8; Supply voltage (V_{DD}) = -25 V for 2N7236 and 2N7236U, (V_{DD}) = -50 V for 2N7237 and 2N7237U, time in avalanche = 2 µs min., 20 µs max., frequency = 500 Hz minimum.	5 devices c = 0
Electrical measurements		See table I, subgroup 2	

1/ A separate sample for each test may be pulled.

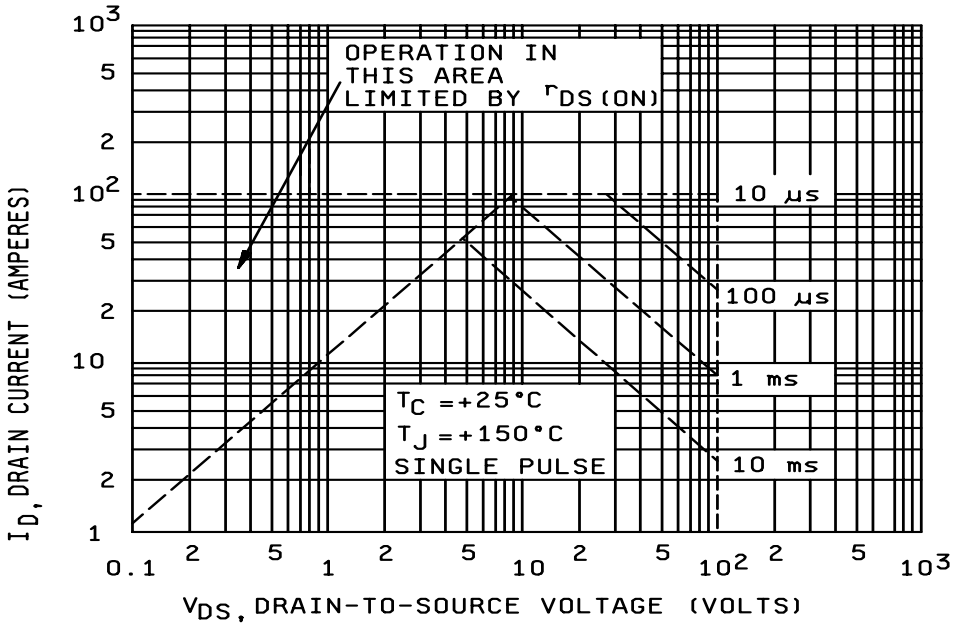




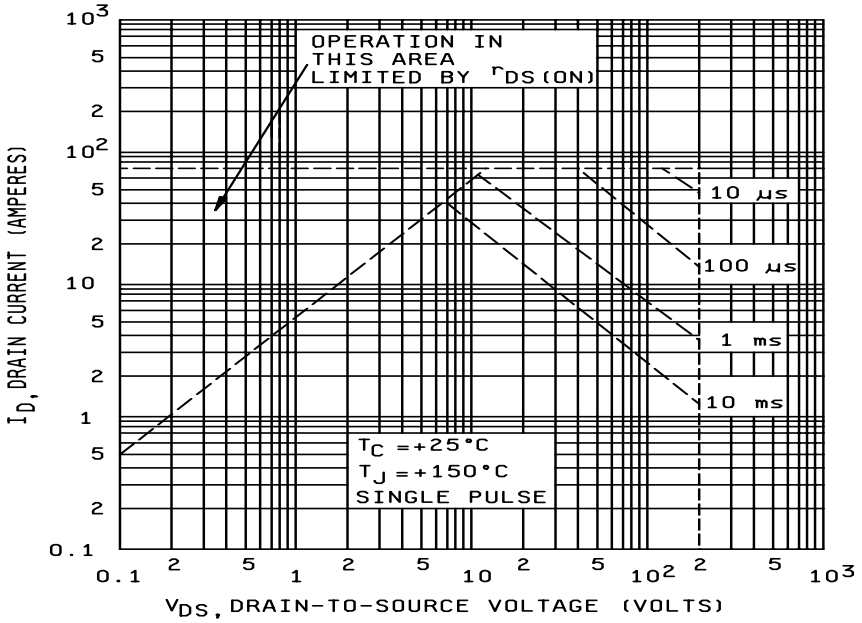
* FIGURE 4. Maximum drain current vs case temperature graphs.



* FIGURE 5. Thermal response curves.



2N7236, 2N7236U



2N7237, 2N7237U

* FIGURE 6. Safe operating area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of material is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Department or Defense Agency, or within the Military Departments' System Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification.

b. Issue of DODISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced (see 2.2.1).

c. Packaging requirements (see 5.1).

d. Lead finish (see 3.4.1).

e. Type designation and product assurance level and for die acquisition, specify the JANHC or JANKC letter version (see figure 3 and 6.5).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable as a substitute for the military PIN.

Military PIN	Manufacturer's CAGE	Manufacturer's and user's PIN
2N7236	59993	IRFM9140
2N7237	59993	IRFM9240
2N7236U	59993	IRFM9140
2N7237U	59993	IRFM9240

6.5 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example JANHCA2N7236) will be identified on the QML.

JANC ordering information		
Military PIN	Manufacturer	
	59993	59993
2N7236	JANHCA2N7236	JANKCA2N7236
2N7237	JANHCA2N7219	JANKCA2N7219

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - MI, SM
Navy - AS, MC
Air Force - 19, 99

Preparing activity:
DLA - CC

(Project 5961-2767)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.

2. The submitter of this form must complete blocks 4, 5, 6, and 7.

3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-PRF-19500/595E	2. DOCUMENT DATE 2 September 2003

3. **DOCUMENT TITLE**
SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT, TRANSISTOR, P-CHANNEL, SILICON, TYPES 2N7236, 2N7237, 2N7236U, AND 2N7237U, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) COMMERCIAL DSN FAX EMAIL	7. DATE SUBMITTED

8. PREPARING ACTIVITY

a. Point of Contact Alan Barone	b. TELEPHONE Commercial 614-692-0510	DSN 850-0510	FAX 614-692-6939	EMAIL alan.barone@dla.mil
c. ADDRESS Defense Supply Center Columbus ATTN: DSCC-VAC P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Standardization Program Office (DLSC-LM) 8725 John J. Kingman, Suite 2533 Fort Belvoir, VA 22060-6221 Telephone (703) 767-6888 DSN 427-6888			